Si4720/21

BROADCAST FM RADIO TRANSCEIVER FOR PORTABLE APPLICATIONS

Features

- Integrated FM antenna support
- Excellent real-world performance
- Only two external components required
- Worldwide FM band support (76 to 108 MHz)
- RDS/RBDS processor (Si4721)
- Programmable pre/de-emphasis (50/75 µs)
- Frequency synthesizer with integrated VCO
- Adjustable seek parameters
- Adjustable mono/stereo blend
- Adjustable soft mute
- Programmable transmit output voltage control
- Audio dynamic range control
- Advanced modulation control
- Analog/digital audio interface
- Audio silence detector
- Programmable reference clock input
- 2-wire and 3-wire control interface
- Integrated LDO regulator
- 2.7 to 5.5 V supply voltage
- 3 x 3 x 0.55 mm 20-pin Pb-free QFN package

Ordering Information:
See page 35.

Applications

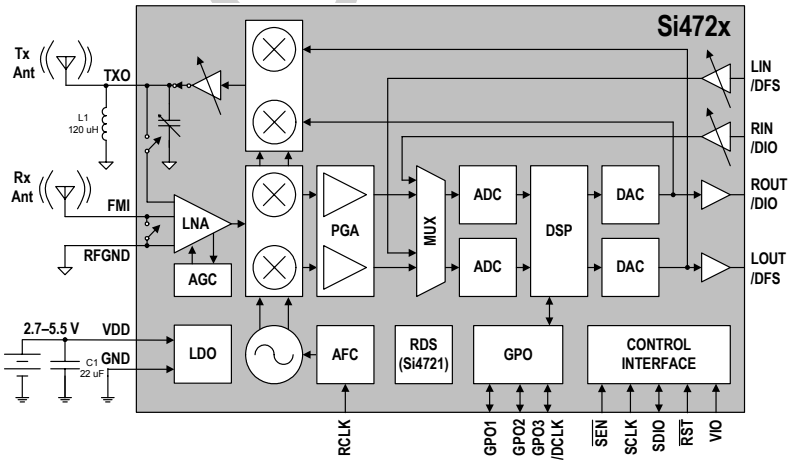
- Cellular handsets/hands-free
- MP3 players
- Portable media players
- Wireless speakers/microphone
- Satellite digital audio radios
- Personal computers/notebooks

Description

The Si4720/21 integrates the complete tuner and transmit functions for FM broadcast reception and standards-compliant, unlicensed FM broadcast stereo transmission.

Users must comply with local regulations on radio frequency (RF) transmission.

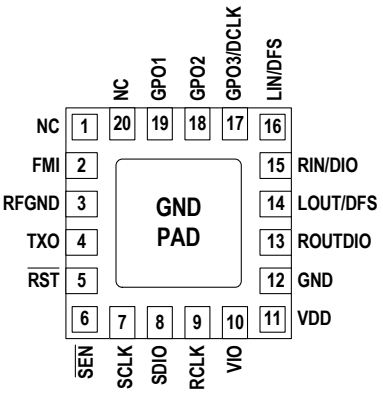
Functional Block Diagram



Pin Assignments

Si4720/21

(Top View)



Patents pending

1. To ensure proper operation and FM transceiver performance, follow the guidelines in “AN286: Si4720/21 Headphone and Antenna Interface.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place the Si4720/21 as close as possible to the antenna jack, and keep the FMI trace as short as possible.

TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		2.7	—	5.5	V
Interface Supply Voltage	VIO		1.5	—	3.6	V
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_D	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (VIO + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	Vpk

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4720/21 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, DIN, DOUT, GPO1, GPO2/IRQ, and GPO3.
4. At RF input pin, FMI.

Table 3. DC Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Receiver to Line Output						
RX Supply Current[2]	I_{RX}		—	16.6	—	mA
RX Supply Current[2,3]	I_{RX}	RSSI < 18, LNA gain = MAX	—	17.9	—	mA
RX RDS Supply Current[2]	I_{RXRDS}	(Si4721 only)	—	18	—	mA
RX Interface Supply Current[2]	I_{IO}		—	400	—	µA
FM Receiver to Digital Audio Output[4]						
RX Supply Current[2]	I_{RX}		—	16.3	—	mA
RX Supply Current[2,3]	I_{RX}	RSSI < 18, LNA gain = MAX	—	17.6	—	mA
RX Digital Supply Current[2]	I_{RXRDS}	(Si4721 only)	—	17.7	—	mA
RX Interface Supply Current[2]	I_{IO}	C_L = 20 pF	—	500	—	µA
FM Transmitter from Line Input						
TX Supply Current	I_{TX}		—	17	—	mA
TX Supply Current (RDS Enabled)	$I_{TX\ RDS}$	(Si4721 only)	—	18	—	mA
TX Interface Supply Current	I_{IO}		—	400	—	µA
FM Transmitter from Digital Audio Input						
TX Supply Current	I_{TX}		—	14	—	mA
TX Supply Current (RDS Enabled)	I_{TXRDS}	(Si4721 only)	—	15	—	mA
TX Interface Supply Current	I_{IO}		—	TBD	—	µA
Supplies and Interface						
Powerdown Current[5]	I_{PDA}	Powerdown mode	—	10	20	µA
Interface Powerdown Current[5]	I_{IO}	SCLK, RCLK inactive Powerdown mode	—	1	10	µA

Notes:

1. Test conditions: V_{RF} = 115 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, unless otherwise specified.
   Production test conditions: VDD = 5 V, VIO = 3.3 V, TA = 25 °C, F_{RF} = 98 MHz.
   Characterization test conditions: VDD = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, TA = –20 to 85 °C, F_{RF} = 76–108 MHz.
2. Si4720/21 operating in receive mode.
3. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
4. Using digital audio interface.
5. Specifications are guaranteed by characterization only.
6. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, DIN, GPO1, GPO2/IRQ, and GPO3.
7. For output pins SDIO, GPO1, GPO2/IRQ, and GPO3.

Table 3. DC Characteristics[1] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, F_{RF} = 76–108 MHz, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage[6]	V_{IH}		0.7 x VIO	—	VIO + 0.3	V
Low Level Input Voltage[6]	V_{IL}		–0.3	—	0.3 x VIO	V
High Level Input Current[6]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[6]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[7]	V_{OH}	I_{OUT} = 500 µA	0.8 x VIO	—	—	V
Low Level Output Voltage[7]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x VIO	V

Notes:

1. Test conditions: V_{RF} = 115 dBµV, stereo, ∆f = 68.25 kHz, ∆fpilot = 6.75 kHz, REFCLK = 32.768 kHz, unless otherwise specified.
   Production test conditions: VDD = 5 V, VIO = 3.3 V, TA = 25 °C, F_{RF} = 98 MHz.
   Characterization test conditions: VDD = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, TA = –20 to 85 °C, F_{RF} = 76–108 MHz.
2. Si4720/21 operating in receive mode.
3. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
4. Using digital audio interface.
5. Specifications are guaranteed by characterization only.
6. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, DIN, GPO1, GPO2/IRQ, and GPO3.
7. For output pins SDIO, GPO1, GPO2/IRQ, and GPO3.

Table 4. Reset Timing Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GPO1, GPO2/IRQ Input to $\overline{RST}$↑ Setup	t_{SRST}		100	—	—	µs
GPO1, GPO2/IRQ Input to $\overline{RST}$↑ Hold	t_{HRST}		30	—	—	ns

Note: The bus mode is selected by sampling the state of the GPO1 and GPO2/IRQ pins on the rising edge of RST. The GPO1 pin includes a 1 MΩ internal pull-up resistor that is connected while RST is low, and the GPO2/IRQ pin includes an internal 1 MΩ pull-down resistor that is connected while the RST pin in low. Therefore, it is only necessary for the system controller to actively drive pins if a mode other than the default 2-wire mode is required, as shown in Table 3. After bus mode selection is complete, the device is placed in powerdown mode. The minimum setup time for GPO1 and GPO2 before RST = 1 is 30 ns when actively driven by the system controller and 100 µs if the internal 1 MΩ resistor is allowed to set the default GPO1 (high) and GPO2 (low).

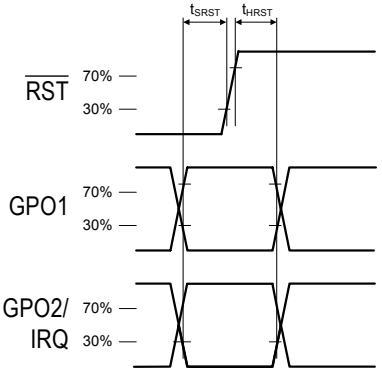


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK↓ Hold[2,3]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		20 + 01.C_b	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		20 + 01.C_b	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When VIO = 0 V, SCLK and SDIO are low-impedance. 2-wire control interface is I^2C compatible.
2. The Si4720/21 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the 0 ns $t_{HD:DAT}$ specification.
3. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

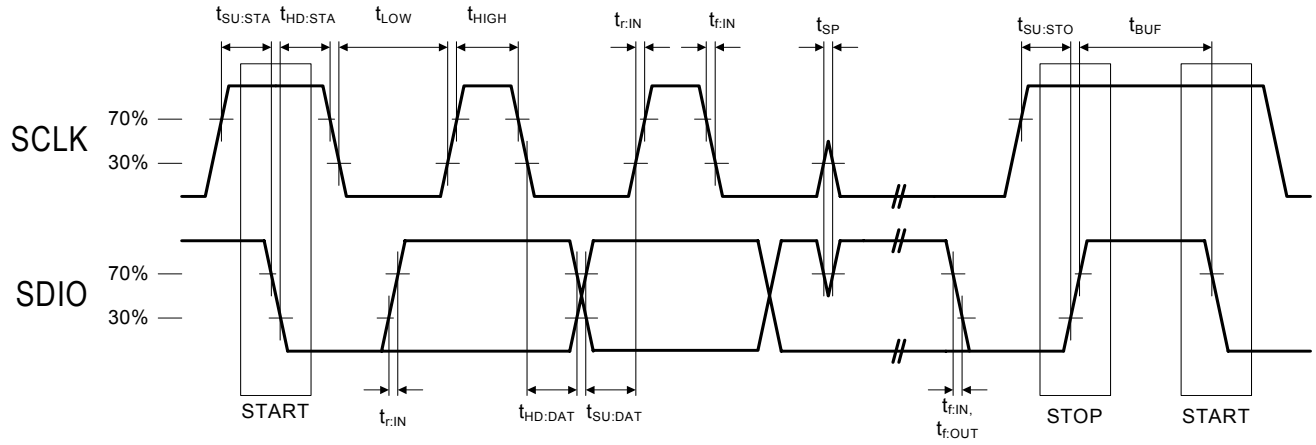


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

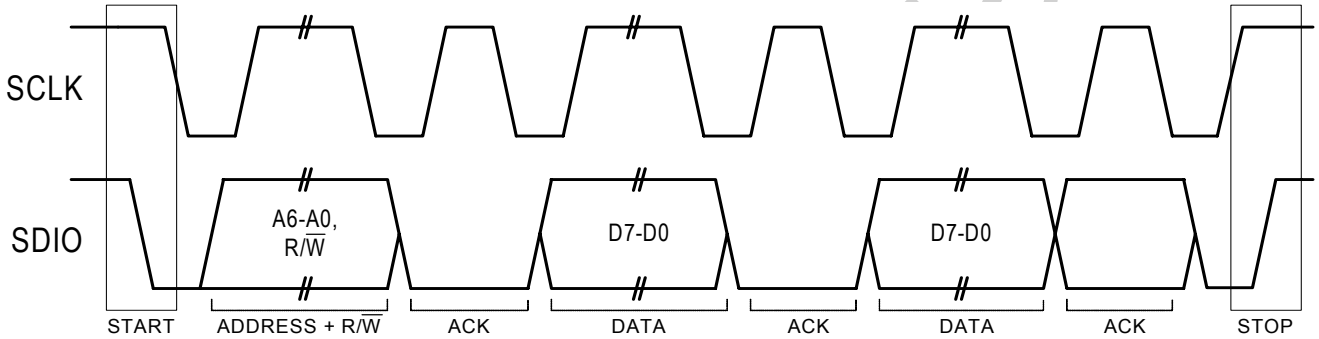


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R t_F				10	ns

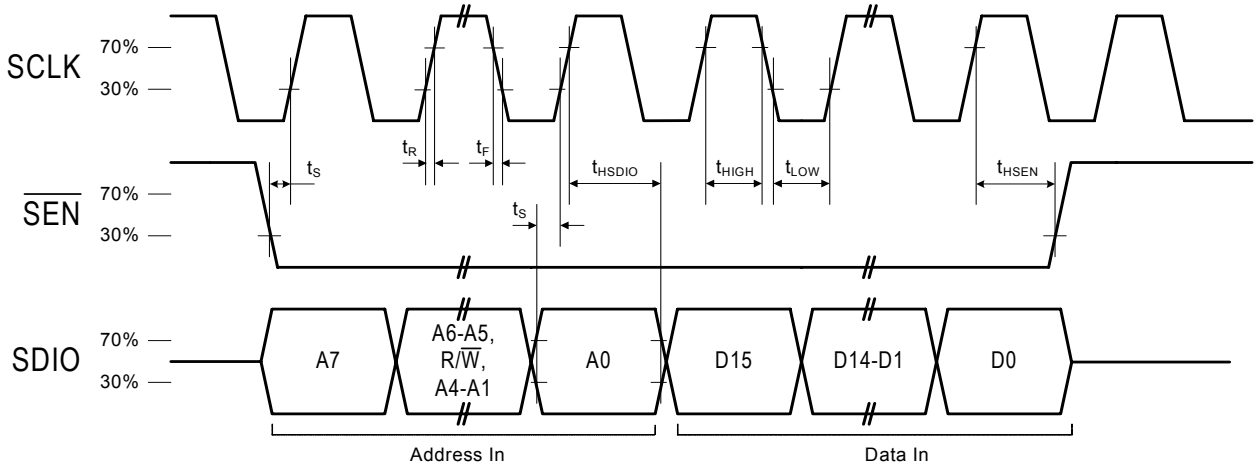


Figure 4. 3-Wire Control Interface Write Timing Parameters

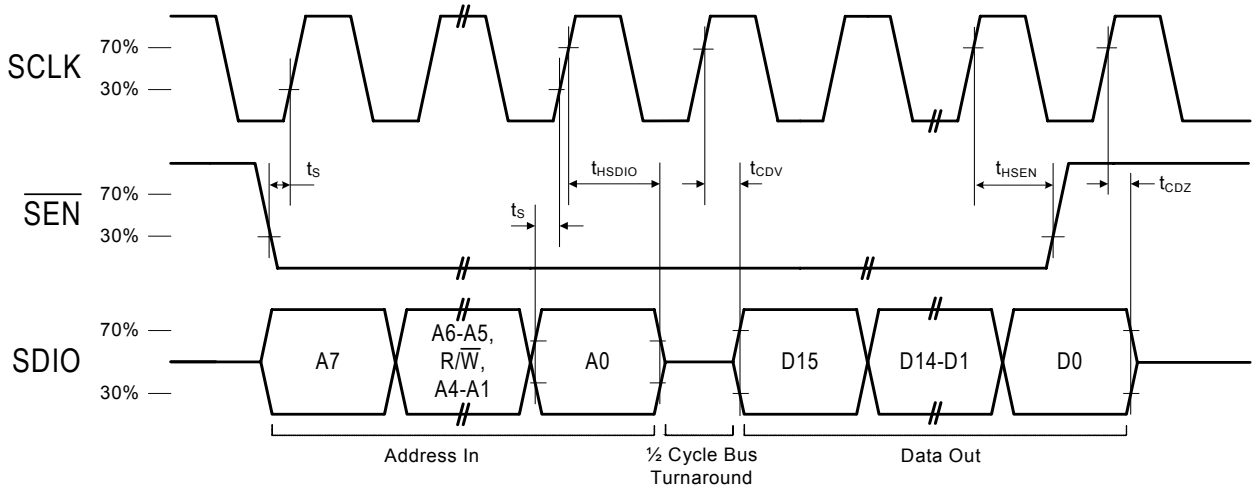


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R t_F				10	ns

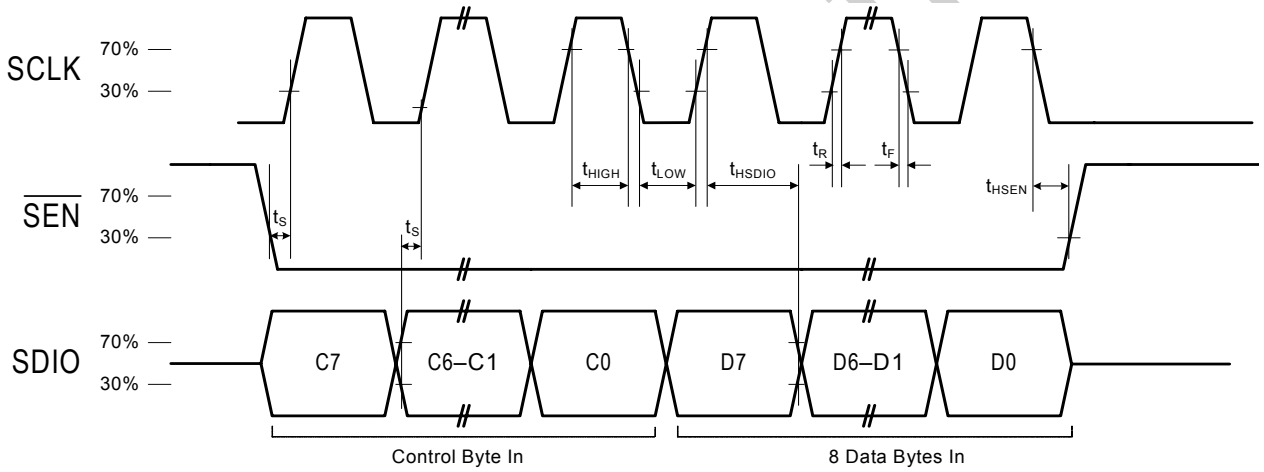


Figure 6. SPI Control Interface Write Timing Parameters

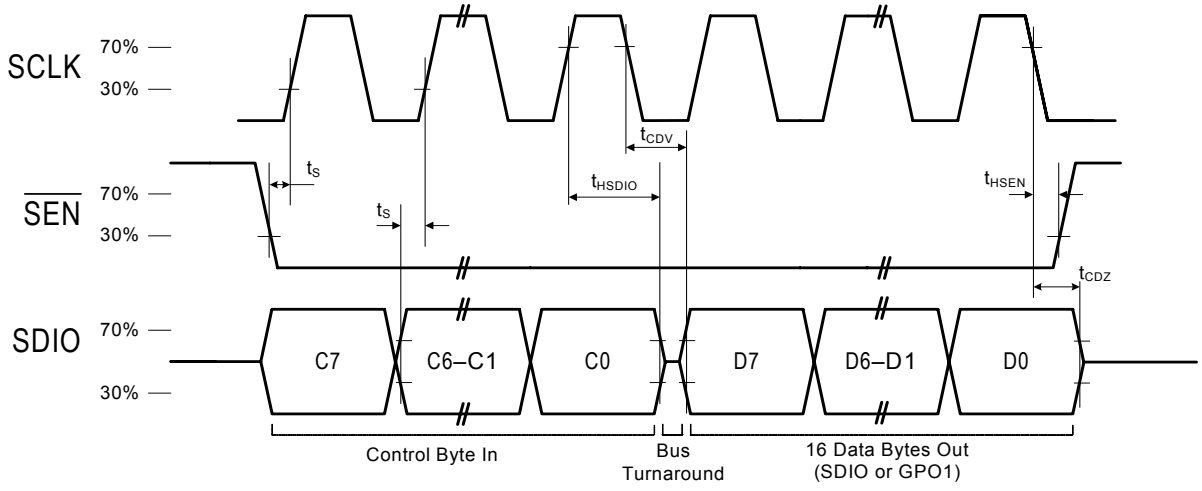


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	—	ns
DCLK pulse width high	t_{DCH}		10	—	—	ns
DCLK pulse width low	t_{DCL}		10	—	—	ns
DFS set-up time to DCLK rising edge	$t_{SU:DFS}$		5	—	—	ns
DFS hold time from DCLK rising edge	$t_{HD:DFS}$		5	—	—	ns
DIN set-up time from DCLK rising edge	$t_{SU:DIN}$		5	—	—	ns
DIN hold time from DCLK rising edge	$t_{HD:DIN}$		5	—	—	ns
DCLK, DFS, DIN, Rise/Fall time	t_R t_F		—	—	10	ns

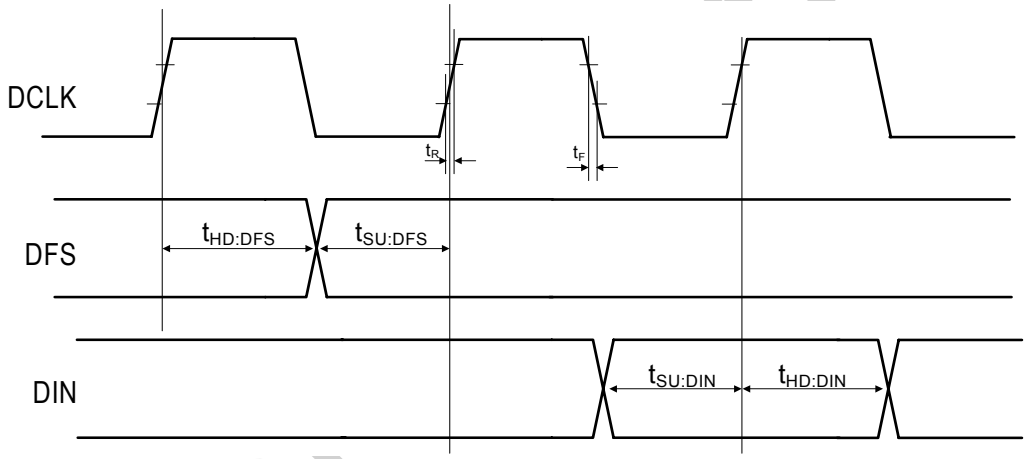


Figure 8. Digital Audio Interface Timing Parameters, I²S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity[3,4,5]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
RDS Sensitivity		∆f = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
RDS Sensitivity in Performance Mode		∆f = 2 kHz, RDS BLER < 5% RDSPRF = 1	—	12	—	µVEMF
LNA Input Resistance[6,10]			3	4	5	kΩ
LNA Input Capacitance[6,10]			4	5	6	pF
Input IP3[7,10]			105	108	—	dBµV EMF
AM Suppression[3,4,6,10]		m = 0.3	40	55	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[10]		In-band	35	—	—	dB
RCLK Frequency Tolerance			–200	—	200	ppm
Audio Output Voltage[3,4,6]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[3,6,8]			—	—	1	dB
Audio Band Limits[3,6,10]		±1.5 dB	30	—	15k	Hz
Audio Stereo Separation[3,6,8]			25	—	—	dB
Mono/Stereo Switching Level[8]			—	34	—	dBµVEMF
Audio Mono S/N[3,4,5,6]			58	63	—	dB
Audio Stereo S/N[5]			—	58	—	dB
Audio THD[3,6,8]			—	0.1	0.5	%
De-emphasis Time Constant			70	75	80	µs
			45	50	54	µs
Audio Common Mode Voltage[9]			0.7	0.8	0.9	V
Audio Common Mode Voltage[9]		High-Z mode	—	0.5 x VIO	—	V

Notes:

1. Additional testing information is available in Application Note AN234. Volume = maximum for all tests. Tested at RF = 100 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN286: Si4720/21 Antenna Interface.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. ∆f = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
7. $|f_2 – f_1| > 1$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4720/21-GM" on page 34.
8. ∆f = 75 kHz.
9. At L_{OUT} and R_{OUT} pins.
10. Guaranteed by characterization.

Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Output Load Resistance[9,10]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[9,10]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time		RCLK tolerance = 200 ppm	—	—	60	ms/channel
Powerup Time		From powerdown	—	—	110	ms
RSSI Offset		Input levels of 8 and 60 dBµV EMF	–3		3	dB
0 dB Full Scale Output Voltage		At LOUT/ROUT	—	0.35	—	V_{RMS}

Notes:

1. Additional testing information is available in Application Note AN234. Volume = maximum for all tests. Tested at RF = 100 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN286: Si4720/21 Antenna Interface.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz, A-weighted.
6. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
7. $|f_2 - f_1| > 1$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4720/21-GM" on page 34.
8. Δf = 75 kHz.
9. At L_{OUT} and R_{OUT} pins.
10. Guaranteed by characterization.

Table 10. FM Transmitter Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, T_{RF} = 76 to 108 MHz, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Frequency Range[2]	f_{RF}		76	—	108	MHz
Transmit Frequency Stability[2,3]			–3.5	—	3.5	kHz
Maximum Transmit Voltage	V_{RF}	V_{RF} = 115 dBµV	113	115	117	dBuV
Minimum Transmit Voltage	V_{RF}	V_{RF} = 88 dBµV	79	83	87	dBuV
Transmit Voltage Step[2]		V_{RF} = 102–115 dBµV	—	1	2	dB
Transmit Voltage Stability[2]		V_{RF} = 115 dBµV	–1	—	1	dB
Transmit Channel Edge Power		> ±100 kHz	—	—	–20	dBc
Transmit Adjacent Channel Power		> ±200 kHz	—	–30	–26	dBc
Transmit Alternate Channel Power		> ±400 kHz	—	–30	–26	dBc
Transmit Emissions		In-band (76–108 MHz)	—	—	–30	dBc
Output Capacitance Max[2]	C_{tune}		—	53	—	pF
Output Capacitance Min[2]	C_{tune}		—	5	—	pF
Pre-emphasis Time Constant[2]		TX_PREMPHASIS = 75 µs	70	75	80	µs
		TX_PREMPHASIS = 50 µs	45	50	54	µs
Audio SNR[2]		Δf = 22.5 kHz, Mono	58	63	—	dB
Audio SNR		Δf = 22.5 kHz, Δfpilot = 6.75 kHz, Stereo	53	58	—	dB
Audio THD[2]		Δf = 75 kHz, Mono	—	0.1	0.5	%
Audio THD		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	—	0.1	0.5	%
Audio Stereo Separation		left channel only	30	35	—	dB
Sub Carrier Rejection Ratio	SCR		40	50	—	dB
Powerup Settling Time[2]			—	110	—	ms
Input Signal Level[2]	V_{AI}		—	—	0.636	V_{PK}

Notes:

1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN306: Si4720/21 Short Monopole Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 9 on page 16.
   Test conditions: V_{RF} = 115 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, unless otherwise specified
   Production test conditions: VDD = 5 V, VIO = 3.3 V, TA = 25 °C, F_{RF} = 98 MHz
   Characterization test conditions: VDD = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, TA = –20 to 85 °C, F_{RF} = 76–108 MHz
   All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
   Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
   Parameters are tested in production unless otherwise specified.
2. Guaranteed by characterization only.
3. No measurable ΔfRF/ΔVDD at ΔVDD of 500 mVpk-pk at 100 Hz to 10 kHz.

Table 10. FM Transmitter Characteristics[1] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C, T_{RF} = 76 to 108 MHz, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Pass Frequency Response[2]		Mono, –3 dB	5	—	30	Hz
Low Pass Frequency Response[2]		Mono, –3 dB	15 K	—	15.5 K	Hz
Audio Imbalance		Mono	–1	—	1	dB
Pilot Modulation Rate Accuracy[2]		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	—	6.75	—	kHz
Audio Modulation Rate Accuracy[2]		Δf = 68.25 kHz, Δfpilot = 6.75 kHz, Stereo	—	68.25	—	kHz
Input Resistance[2]			50	60	—	kΩ
Input Capacitance[2]			—	10	—	pF

Notes:

1. FM transmitter performance specifications are subject to adherence to Silicon Laboratories guidelines in "AN306: Si4720/21 Short Monopole Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested with test schematic (L = 120 nH, Q ≥ 30) shown in Figure 9 on page 16.
   Test conditions: V_{RF} = 115 dBµV, stereo, Δf = 68.25 kHz, Δfpilot = 6.75 kHz, REFCLK = 32.768 kHz, unless otherwise specified
   Production test conditions: VDD = 5 V, VIO = 3.3 V, TA = 25 °C, F_{RF} = 98 MHz
   Characterization test conditions: VDD = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, TA = –20 to 85 °C, F_{RF} = 76–108 MHz
   All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions.
   Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
   Parameters are tested in production unless otherwise specified.
2. Guaranteed by characterization only.
3. No measurable ΔfRF/ΔVDD at ΔVDD of 500 mVpk-pk at 100 Hz to 10 kHz.

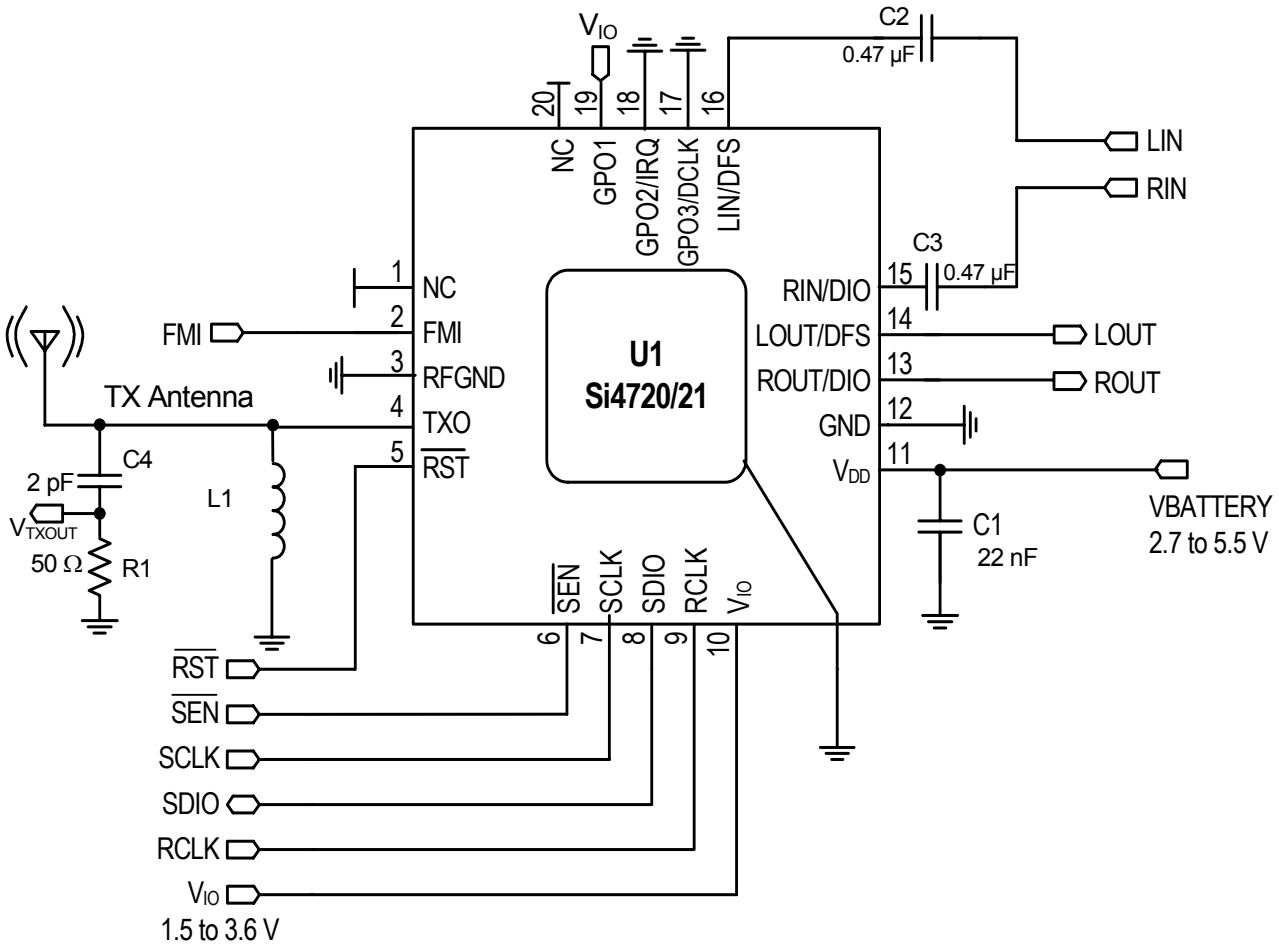
Table 11. Reference Clock Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Supported Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RCLK Frequency Range*			31.130	32.768	40,000	kHz
Frequency Tolerance			–20		+20	ppm

***Note:** The RCLK frequency divided by an integer number (the prescaler value) must fall in the range of 31,130 to 34,406 Hz. Therefore, the range of RCLK is not continuous below frequencies of 311.3 kHz.

2. Test Schematic

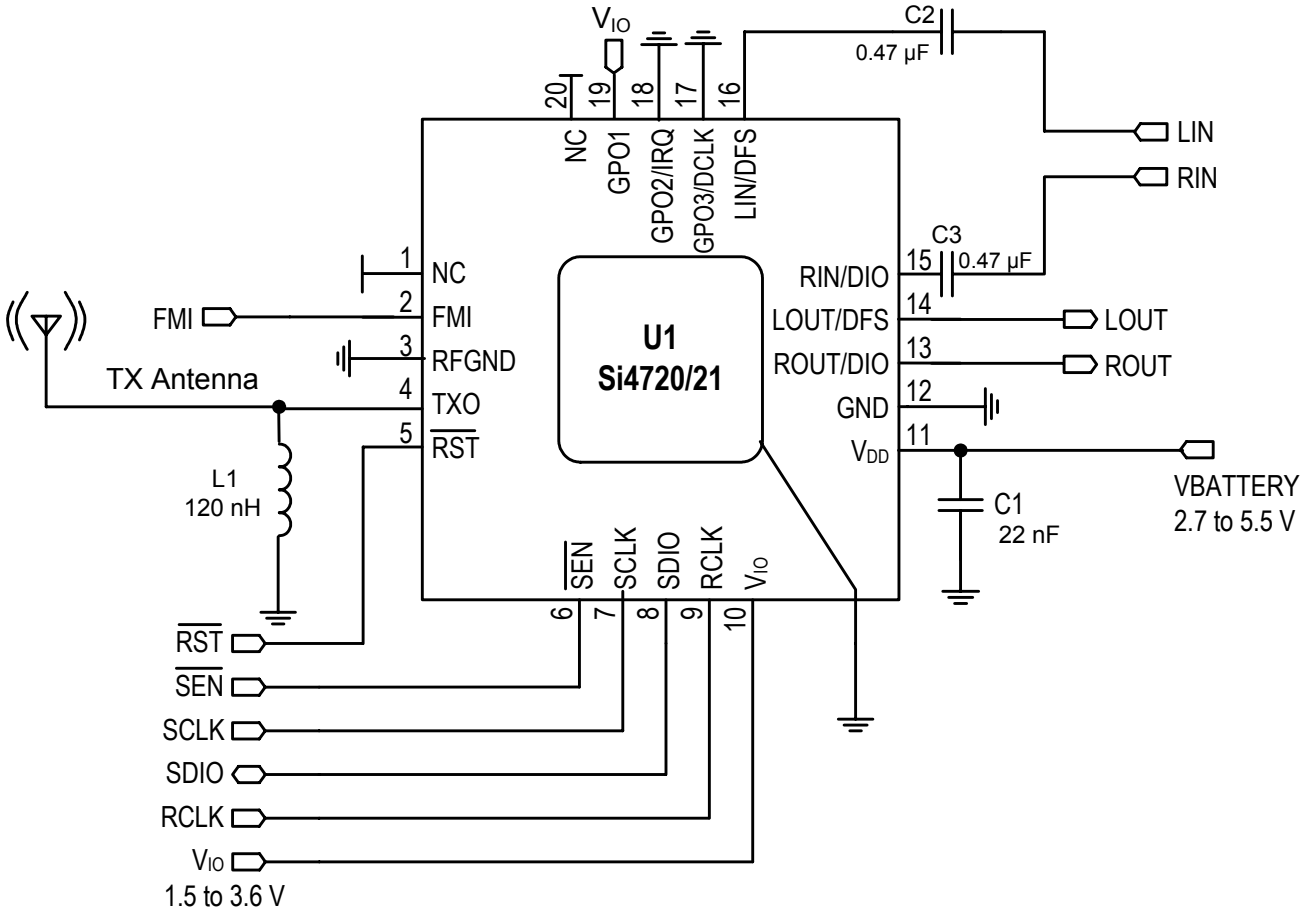


Notes:

1. Si4720/21 is shown configured in I^2C compatible bus mode.
2. GPO2/IRQ can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN231: Antenna Interface" and "AN306: Si471x Short Monopole Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.

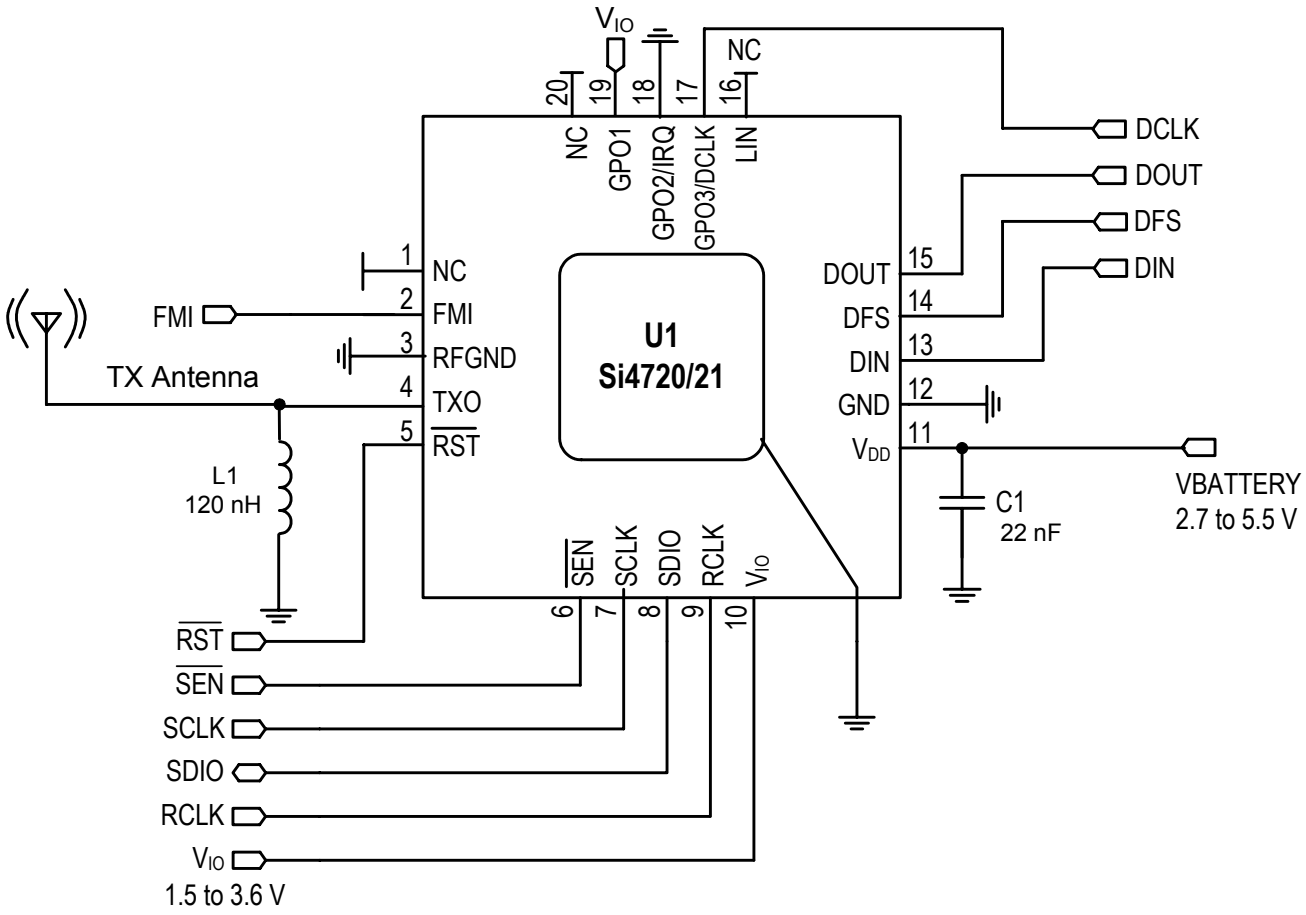
Figure 9. Test Schematic

3. Typical Application Schematic



Notes:
1. Si4720/21 is shown configured in I^2C compatible bus mode.
2. GPO2/IRQ can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN231: Antenna Interface" and "AN306: Si471x Short Monopole Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. LIN, RIN line inputs must be ac-coupled.

Figure 10. Analog Audio Inputs (LIN, RIN)



Notes:
1. Si4720/21 is shown configured in I^2C compatible bus mode.
2. GPO2/IRQ can be configured for interrupts with the powerup command.
3. To ensure proper operation and FM transmitter performance, follow the guidelines in "AN231: Antenna Interface" and "AN306: Si471x Short Monopole Antenna Interface." Silicon Laboratories will evaluate schematics and layouts for qualified customers.

Figure 11. Digital Audio Inputs (DIN, DOUT, DFS, DCLK)

4. Bill of Materials

Table 12. Si4720/21 Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF (Analog Audio Input Mode)	Murata
L1	120 nH inductor, Qmin = 30	Murata
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

Table 13. Si4720/21 Test Circuit Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2, C3	AC Coupling Capacitor, 0.47 µF	Murata
C4	2 pF, ±.05 pF, 06035JZR0AB	AVX
L1	120 nH inductor, Qmin = 30	Murata
R1	49.9 Ω, 5%	Murata
U1	Si4720/21 FM Radio Transceiver	Silicon Laboratories

5. Functional Description

5.1. Overview

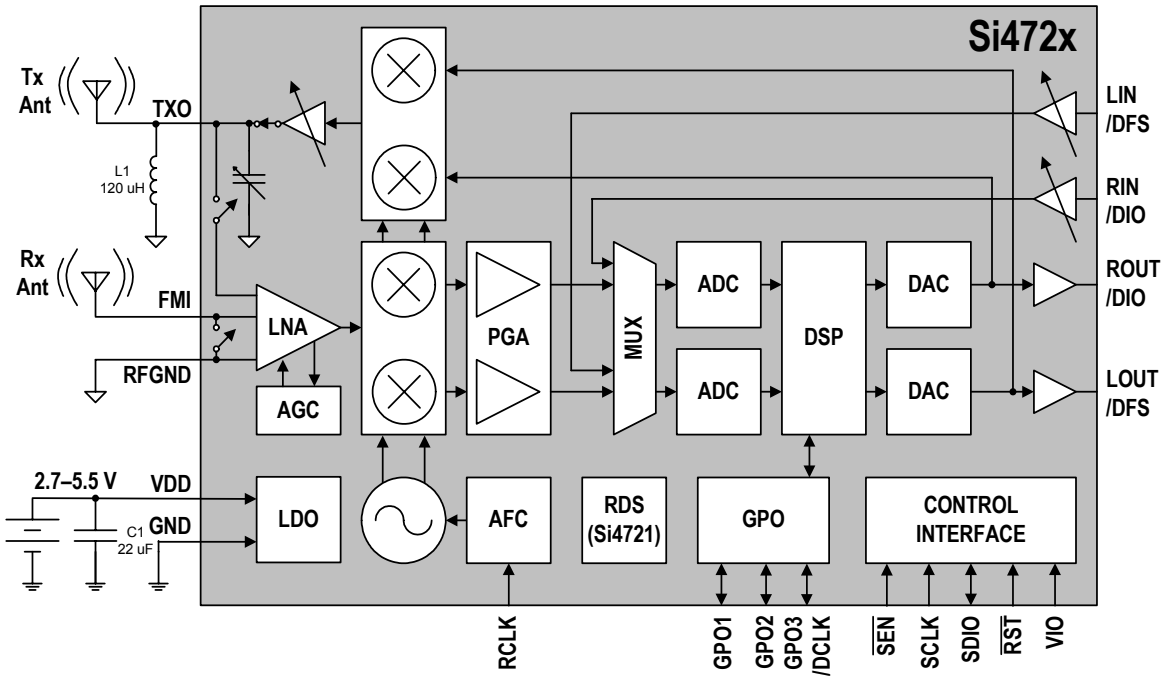


Figure 12. Functional Block Diagram

The Si4720/21 is the first single chip FM radio transceiver. The proven and patented digital architecture of the Si4720/21 combines the functionality of the Si470x FM radio receiver with the Si471x FM transmitter, offering full FM receive and transmit capabilities in a single, ultra-small 3x3x0.55 mm QFN package. The device leverages Silicon Lab's highly successful and proven FM technology, and offers unmatched integration and performance allowing FM receive and transmit to be added to any portable device by using a single chip. As with the Si470x and Si471x products, the Si4720/21 offers industry leading size, performance, low power consumption, and ease of use.

The Si4720/21 is layout compatible with Silicon Laboratories' Si4710/11 FM Transmitter and Si4730/31 AM/FM Receiver. The Si4720/21 is the first FM radio transceiver integrated circuit to support a small loop antenna, which can be integrated into the enclosure or PCB of a portable device. This feature enables applications that also include Bluetooth functionality to perform FM radio reception without cables. For portable navigation devices, the Si4720/21's antenna architecture permits integration of the traffic messaging antenna into the enclosure of the portable device, and eliminates the need for external antenna cables.

The Si4720/21's digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external inductor and bypass capacitor, and a PCB space of approximately 15 mm^2. The Si4720/21 is layout compatible with Silicon Laboratories' Si470x FM radio receivers, Si473x AM/FM radio receivers, and the Si471x FM radio transmitter solutions, allowing a single PCB layout to accommodate a variety of music features. High yield manufacturability, unmatched performance, easy design-in, and software programmability are key advantages of the Si4720/21.

The Si4720/21 includes line inputs to the on-chip analog-to-digital converters (ADC), line outputs from the on-chip digital-to-analog converters (DAC), digital audio mixers, a programmable reference clock input, and a configurable digital audio interface. The chip supports I^2C-compliant 2-wire, and an additional Si4700/01 backwards compatible 3-wire control interface standards.

The Si4720/21 performs much of the FM modulation and demodulation digitally to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The on-board DSP provides unmatched pilot rejection, selectivity, and optimum sound quality.

The Si4721 is the industry's first single-chip integrated FM radio transceiver including both receive and transmit support for the European Radio Data System (RDS) and the U.S. Radio Broadcast Data System (RBDS). RDS allows digital information sent from the broadcaster to be displayed, such as station ID, song name and music category. In Europe, alternate frequency (AF) information is also provided to automatically change stations in areas where broadcasters use multiple frequencies. In transmit mode, digital information such as artist name, song title, music category, and branded messaging can be transmitted and displayed on any RDS/RBDS receiver.

The Si4720/21 FM receive functionality is based on the proven Si4700/01 FM tuner. FMI is the FM input to the receiver's low-noise amplifier and RFGND is the RF return.

The transmit output (TXO) connects directly to the transmit antenna with only one external inductor to provide harmonic filtering. The output is programmable over a 20 dB voltage range in 1 dB steps. The TXO output pin can also be configured for loop antenna support. Users are responsible for complying with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4720/21 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

The Si4720/21 includes a low-noise stereo line input (LIN/RIN) with programmable attenuation. To ensure optimal audio performance, the Si4720/21 has a transmit line input property that allows the user to specify the peak amplitude of the analog input required to reach maximum deviation level. The deviation levels of the audio, pilot, and RDS/RBDS signals can be independently programmed to customize FM transmitter designs. The Si4720/21 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. In addition, the device provides an overmodulation indicator to allow the user to dynamically set the maximum deviation level. The Si4720/21 has a programmable audio dynamic range control that can be used to reduce the dynamic range of the audio input signal and increase the volume at the receiver. These features can dramatically improve the end user's listening experience.

The Si4720/21 is reset by applying a logic low on the RST pin. This causes all register values to be reset to their default values. The digital input/output interface supply (VIO) provides voltage to the RST, SEN, SDIO, RCLK, DIN, DFS, and DCLK pins and can be connected to the audio baseband processor's supply voltage to save power and remove the need for voltage level translators. RCLK is not required for register operation.

The Si4720/21 reference clock is programmable, supporting many RCLK inputs as shown in Table 10.

5.2. FM Receiver

The Si4720/21 FM receiver is based on the proven Si4700/01 FM radio receiver. The receiver uses a digital low-IF architecture allowing the elimination of external components and factory adjustments. The receive (RX) section integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled. Refer to Section "6. Commands and Properties (Subject to Change)" on page 30 for additional programming and configuration information. An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the use of digital signal processing (DSP) to perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

The digital audio interface and line input/output signals enable direct digital FM recording with the digital output DOUT. Also, digital audio signals such as ring tones and music can be digitally mixed into the FM received signal.

5.3. FM Transmitter

The Si4720/21 transmitter uses a digital architecture. The transmitter (TX) integrates a stereo 16-bit audio ADC to convert analog audio signals to high fidelity digital signals. Alternatively, digital audio signals can be applied to the Si4720/21 directly to reduce power consumption by eliminating the need to convert audio baseband signals to analog and back again to digital. Digital signal processing is used to perform the stereo MPX encoding and FM modulation to a low digital IF. Transmit baseband filters suppress out-of-channel noise and images from the digital low-IF signal. A quadrature single-sideband mixer up-converts the digital IF signal to RF, and internal RF filters suppress

noise and harmonics to support the harmonic emission requirements of cellular phones, GPS, WLAN, and other wireless standards.

The TXO output has up to 20 dB of output level control, programmable in approximately 1 dB steps. This large output range enables a variety of antennas to be used for transmit, such as a monopole stub antenna or a loop antenna. The 1 dB step size provides fine adjustment of the output voltage.

The TXO output requires only one external 120 nH inductor. The inductor is used to resonate the antenna and is automatically calibrated within the integrated circuit to provide the optimum output level and frequency response for supported transmit frequencies. Users are responsible for adjusting their system's radiated power levels to comply with local regulations on RF transmission (FCC, ETSI, ARIB, etc.).

5.4. Digital Audio Interface

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^{2}S and left-justified modes.

5.4.1. Audio Data Formats

In I^{2}S format, the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. Depending on word size, DCLK frequency, and sample rate, there may be unused DCLK cycles that follow the LSB of each word, before the next DFS transition and MSB of the next word.

In addition to I^{2}S format, the digital audio interface supports a variety of other PCM audio formats that can be configured by setting the DIGITAL_INPUT_FORMAT property of the device. Figures 13–15 show examples of some supported digital audio formats. The user can configure DFS to act as a "frame" for the left and right samples (similar to I^{2}S format) or simply a pulse that signals the start of a stereo sample. Other options allow data to be captured on either the rising or falling edge of DCLK, the polarity of DFS to be inverted, the left/right word positions to be reversed, or word size to be configured for 8, 16, 20, or 24 bits.

5.4.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor. The sampling rate is selected using the DIGITAL_INPUT_SAMPLE_RATE property.

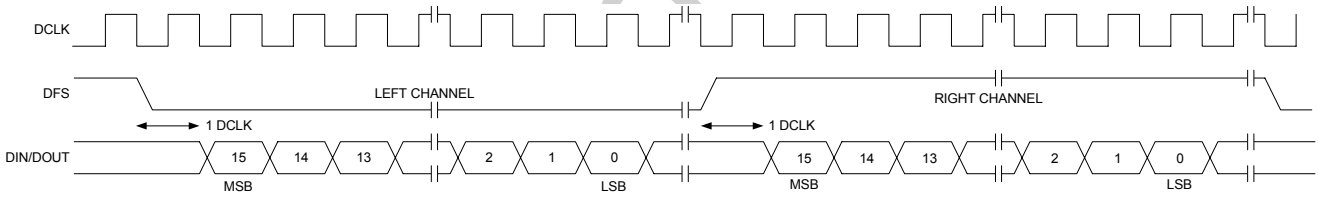


Figure 13. I^{2}S Audio (16-bit stereo)

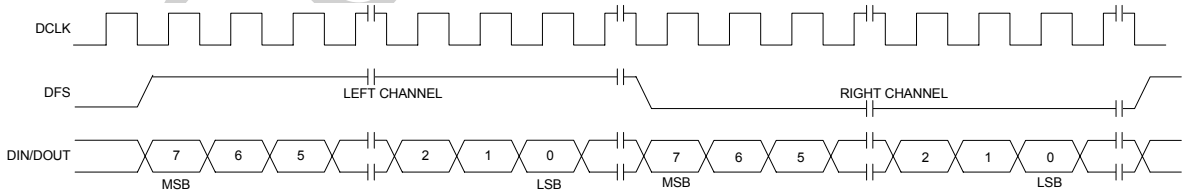


Figure 14. Left-Justified Audio Example (8-bit stereo, inverted DFS, late DFS)

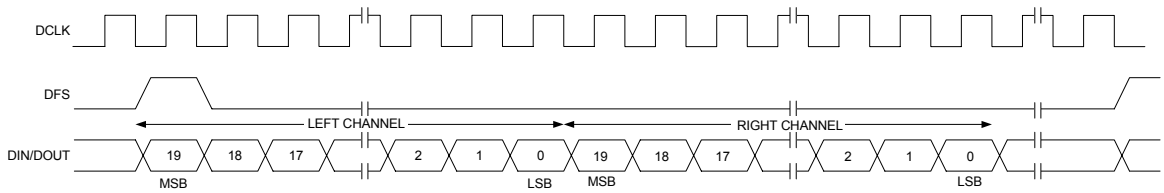


Figure 15. Left-Justified Audio Example (20-bit stereo, DFS pulse, late DFS)

5.5. Line Input

The Si4720/21 provides left and right channel line inputs (LIN and RIN). The inputs are high-impedance and low-capacitance, suited to receiving line level signals from external audio baseband processors. Both line inputs are low-noise inputs with programmable attenuation. Passive and active anti-aliasing filters are incorporated to prevent high frequencies from aliasing into the audio band and degrading performance.

To ensure optimal audio performance, the Si4720/21 has a TX_LINE_INPUT_LEVEL property that allows the user to specify the peak amplitude of the analog input (LILEVEL[9:0]) required to reach the maximum deviation level programmed in the audio deviation property, TX_AUDIO_DEVIATION. A corresponding line input attenuation code, LIATTEN[1:0], is also selected by the expected peak amplitude level. Table 14 shows the line attenuation codes.

Table 14. Line Attenuation Codes

LIATTEN[1:0]	Peak Input Voltage [mV]	RIN/LIN Input Resistance [kΩ]
00	190	396
01	301	100
10	416	74
11	636	60

The line attenuation code is chosen by picking the lowest Peak Input Voltage in Table 14 that is just above the expected peak input voltage coming from the audio baseband processor. For example, if the expected peak input voltage from the audio baseband processor is 400 mV, the user chooses LIATTEN[1:0] = 10 since the Peak Input Voltage of 416 mV associated with LIATTEN[1:0] = 10 is just greater than the expected peak input voltage of 400 mV. The user also enters 400 mV into the LILEVEL[9:0] to associate this input level to the maximum frequency deviation level programmed into the audio deviation property. Note that selecting a particular value of LIATTEN[1:0] changes the input resistance of the LIN and RIN pins. This feature is used for cases where the expected peak input level exceeds the maximum input level of the LIN and RIN pins.

The maximum analog input level is 636 mVpK. If the analog input level from the audio baseband processor exceeds this voltage, series resistors must be inserted in front of the LIN and RIN pins to attenuate the voltage such that it is within the allowable operating range. For example, if the audio baseband's expected peak amplitude is 900 mV and the VIO supply voltage is 1.8 V, the designer can use 30 kΩ series resistors in front of the LIN and RIN pins and select LIATTEN[1:0] = 11. The resulting expected peak input voltage at the LIN/RIN pins is 600 mV, since this is just a voltage divider between the LIN/RIN input resistance (see Table 14, 60 kΩ for this example) and the external resistor. Note that the Peak Input Voltage corresponding to the chosen LIATTEN[1:0] code still needs to satisfy the condition of being just greater than the attenuated voltage. In this example, a line attenuation code of LIATTEN[1:0] = 11 has a Peak Input Voltage of 636 mV, which is just greater than the expected peak attenuated voltage of 600 mV. Also, the expected peak attenuated voltage is entered into the LILEVEL[9:0] parameter. Again, in this example, 600 mV is entered into LILVEVEL[9:0]. This example shows one possible solution, but many other solutions exist. The optimal solution is to apply the largest possible voltage to the LIN and RIN pins for signal-to-noise considerations; however, practical resistor values may limit the choices.

Note that the TX_LINE_INPUT_LEVEL parameter will affect the high-pass filter characteristics of the ac-coupling capacitors and the resistance of the audio inputs.

The Si4720/21 has a programmable low audio level and high audio level indicators that allows the user to selectively enable and disable the carrier based on the presence of audio content. The TX_ASQ_LEVEL_LOW and TX_ASQ_LEVEL_HIGH parameters set the low level and high level thresholds in dBFS, respectively. The time required for the audio level to be below the low threshold is set with the TX_ASQ_DURATION_LOW parameter, and similarly, the time required for the audio level to be above the high threshold is set with the TX_ASQ_DURATION_HIGH parameter.

5.6. Stereo Audio Processing

The multiplexed (MPX) standard was developed in 1961 and is used worldwide for FM transmission. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 16.

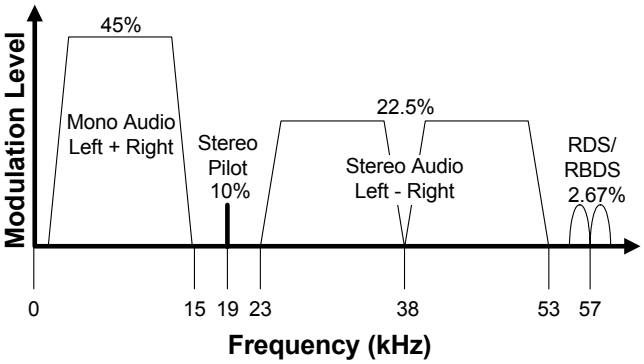


Figure 16. MPX Signal Spectrum

5.6.1. Stereo Decoder

The Si4720/21's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM radio receiver. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

5.6.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. The signal level range over which the stereo to mono blending occurs can be adjusted by setting the stereo blend adjust properties. Stereo/mono status can be monitored with the RSQ STATUS command and mono operation can be forced with the STEREO BLEND OVERWRITE property.

5.6.3. Stereo Encoder

Figure 16 shows an example modulation level breakdown for the various components of a typical MPX signal.

The total modulation level for the MPX signal shown in Figure 16, assuming no correlation, is equal to the arithmetic sum of each of the subchannel levels resulting in 102.67 percent modulation or a peak frequency deviation of 77.0025 kHz (an instantaneous frequency deviation of 75 kHz corresponds to 100 percent modulation). Frequency deviation is related to the amplitude of the MPX signal by a gain constant, K_{VCO}, as given by the following equation:

$$\Delta f = K_{VCO} A_m$$

where Δf is the frequency deviation; K_{VCO} is the voltage-to-frequency gain constant, and A_m is the amplitude of the MPX message signal. For a fixed K_{VCO}, the amplitude of all the subchannel signals within the MPX message signal must be scaled to give the appropriate total frequency deviation.

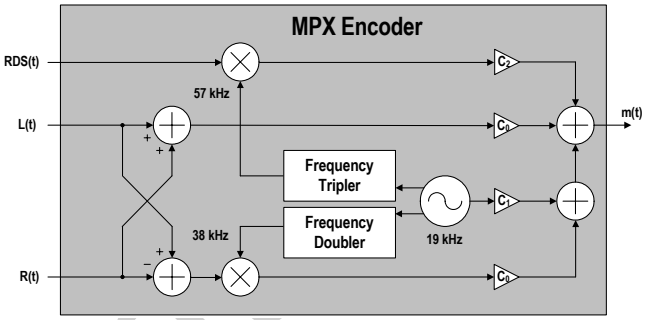


Figure 17. MPX Encoder

Figure 17 shows a conceptual block diagram of an MPX encoder used to generate the MPX signal. L(t) and R(t) denote the time domain waveforms from the left and right audio channels, and RDS(t) denotes the time domain waveform of the RDS/RBDS signal. The MPX message signal can be expressed as follows:

$$m(t) = C_0[L(t) + R(t)] + C_1 \cos(2\pi 19\ \text{kHz}) + C_0[L(t) - R(t)] \cos(2\pi 38\ \text{kHz}) + C_2 RDS(t) \cos(2\pi 57\ \text{kHz})$$

where C_0, C_1, and C_2 are gains used to scale the amplitudes of the audio signals (L(t) ± R(t)), the 19 kHz pilot tone, and the RDS subcarrier respectively, to generate the appropriate modulation level. To achieve the modulation levels of Figure 17 with K_{VCO} = 75 kHz/V, C_0 would be set to 0.45; C_1 would be set to 0.1, and C_2 would be set to 0.0267 giving a peak audio frequency deviation of 0.9 x 75 kHz = 67.5 kHz, a peak pilot frequency deviation of 0.1 x 75 kHz = 7.5 kHz, and a peak RDS frequency deviation of 0.0267 x 75 kHz = 2.0025 kHz for a total peak frequency deviation of 77.0025 kHz.

In the Si4720/21, the peak audio, pilot, and RDS frequency deviations can be programmed directly with the Transmit Audio, Pilot, and RDS Deviation commands with an accuracy of 10 Hz. For the example in Figure 17, the Transmit Audio Deviation is programmed with the value 6750, the Transmit Pilot Deviation with 750, and the Transmit RDS Deviation

with 200, generating peak audio frequency deviations of 67.5 kHz, peak pilot deviations of 7.5 kHz, and peak RDS deviations of 2.0 kHz for a total peak frequency deviation of 77 kHz. The total peak transmit frequency deviation of the Si4720/21 can range from 0 to 100 kHz and is equal to the arithmetic sum of the Transmit Audio, Pilot, and RDS deviations. Users must comply with local regulations on radio frequency transmissions.

Each of the individual deviations (transmit audio, pilot, and RDS) can be independently programmed; however, the total peak frequency deviation cannot exceed 100 kHz.

The Si4720/21 provides an overmodulation indicator to allow the user to dynamically set the maximum deviation level. If the instantaneous frequency exceeds the deviation level specified by the TX_AUDIO_DEVIATION property, the SQINT interrupt bit (and optional interrupt) will be set.

5.7. Audio Dynamic Range Control

The audio dynamic range control can be used to reduce the dynamic range of the audio signal. Audio dynamic range reduction increases the transmit volume by decreasing the peak amplitudes of audio signals and increasing the root mean square content of the audio signal. In other words, it amplifies signals below the threshold by a fixed gain and compresses audio signals above the threshold by the ratio of Threshold/(Gain + Threshold). Figure 18 shows an example transfer function of an audio dynamic range controller with the threshold set at –40 dBFS and a Gain = 20 dB relative to an uncompressed transfer function.

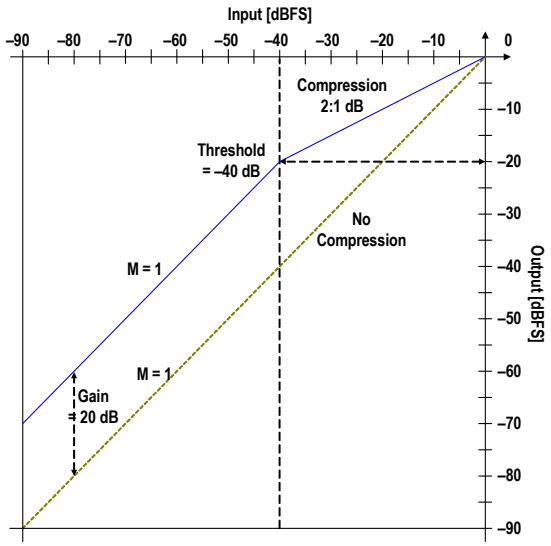


Figure 18. Audio Dynamic Range Transfer Function

For input signals below the threshold of –40 dBFS, the output signal is amplified or gained up by 20 dB relative to an uncompressed signal. Audio inputs above the threshold are compressed by a 2 to 1 dB ratio, meaning that every 2 dB increase in audio input level above the threshold results in an audio output increase of 1 dB. In this example, the input dynamic range of 90 dB is reduced to an output dynamic range of 70 dB.

The Si4720/21 includes digital audio dynamic range control with programmable gain, threshold, attack rate, and release rate. The total dynamic range reduction is set by the gain value and the audio output compression above the threshold is equal to Threshold/(Gain + Threshold) in dB. The gain specified cannot be larger than the absolute value of the threshold. This feature can also be disabled if audio compression is not desired.

Figure 19 shows the time domain characteristics of the audio dynamic range controller. The attack rate sets the speed with which the audio dynamic range controller responds to changes in the input level, and the release rate sets the speed with which the audio dynamic range controller returns to no compression once the audio input level drops below the threshold.

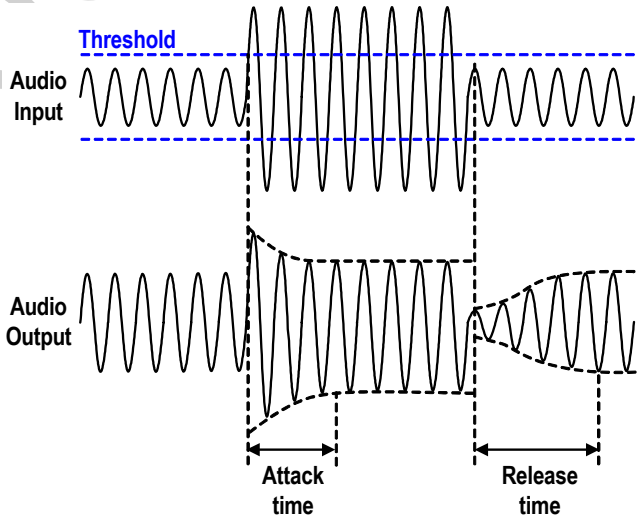


Figure 19. Time Domain Characteristics of the Audio Dynamic Range Controller

5.8. Pre-emphasis and De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter that attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The pre-emphasis time constant is programmable to 50 or 75 µs and is set by using the TX_PREEMPHASIS property.

5.9. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted or placed in high impedance (High-Z). Volume is adjusted digitally with the VOLUME property. The output volume ranges from 0 to –60 dBFS and can be programmed in 1 dB increments.

5.10. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The softmute attack and decay rate are adjustable, and the attenuation levels are adjustable using the SOFTMUTE ATTENUATION property. Soft mute can be disabled.

5.11. RDS/RBDS Processor (Si4721 Only)

The Si4721 implements an RDS/RBDS* processor for symbol encoding/decoding, block synchronization, and error correction. Digital data can be transmitted/received with the Si4721 RDS/RBDS encoding/decoding feature.

The Si4721 device provides an interrupt when RDS is synchronized and RDS group data has been received by the device. The interrupt is set regardless of RDS block error levels in the data group. The device provides interrupts every 1.1875 ms. If the device loses RDS synchronization, RDS data decode and data capture are not possible, and interrupts will not be set until RDS synchronization is reestablished, and an RDS data group has been received.

The Si4721 reports RDS decoder synchronization status, and detailed bit errors in the information word for each RDS block with the RX RDS STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors, or that the block checkword contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

RDS transmission is supported with three different modes. The first mode is the simplest mode and requires no additional user support except for pre-loading the desired RDS PI and PTY codes and up to 12 8-byte PS character strings. The Si4721 will transmit the PI code and rotate through the transmission of the PS character strings with no further control required from outside the device. The second mode allows for more complicated transmissions. The PI and PTY codes are written to the device as in mode 1. The remaining blocks (B, C, and D) are written to a 252 byte buffer. This buffer can hold 42 sets of BCD blocks. The Si4721 creates RDS groups by creating block A from the PI code, concatenating blocks BCD from the buffer, and rotating through the buffer. The BCD buffer is circular; so, the pattern is repeated until the buffer is changed. Finally, the third mode allows the outside controller to burst data into the BCD buffer, which emulates a FIFO. The data does not repeat, but, when the buffer is nearly empty, the Si4721 signals the outside device to initiate another data burst. This mode permits the outside device to use any RDS functionality (including open data applications) that it wants.

5.12. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to upconvert the low intermediate frequency to RF. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during transmission.

The tuning frequency can be directly programmed with commands. For example, to tune to 98.1 MHz, the user writes the TX_TUNE_FREQ command with an argument = 9810.

The Si4720/21 supports channel spacing of 50, 100, or 200 kHz.

5.13. Seek

Seek tuning searches up or down for a channel with an RSSI greater than or equal to the seek threshold. In addition, an optional SNR and/or impulse noise detector may be used to qualify valid stations. Using the extra seek qualifiers can reduce false stops and, in combination with lowering the RSSI seek threshold, increase the number of identified stations. The SNR and impulse noise detectors are disabled by default. Refer to AN284 for additional information.

Two seek modes are available. The device will either wrap or stop at the band limits. If the seek operation is unable to find a channel, the device will indicate failure and return to the channel selected before the seek

operation began. The seek operation may be aborted at any time.

5.14. Reference Clock

The Si4720/21 reference clock is programmable, supporting RCLK frequencies from 31.130 kHz to 40 MHz. The RCLK frequency divided by an integer number (the prescaler value) must fall in the range of 31,130 to 34,406 Hz. Therefore, the range of RCLK is not continuous below frequencies of 311.3 kHz. The default RCLK frequency is 32.768 kHz. Please refer to "AN305: Si471x FM Transmitter Programming Guide" for using other RCLK frequencies.

5.15. Control Interface

A serial port slave interface is provided; this allows an external controller to send commands to the Si4720/21 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, SPI mode, or 3-wire mode. The Si4720/21 selects the bus mode by sampling the state of the GPO1 and GPO2/IRQ pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor that is connected while RST is low, and the GPO2/IRQ pin includes an internal pull-down resistor that is connected while RST is low. Therefore, it is only necessary for the user to actively drive pins that differ from these states.

Table 15. Bus Mode Select on Rising Edge of RST

Bus Mode	GPO1	GPO2/IRQ
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of RST, the pins, GPO1 and GPO2/IRQ, are used as general-purpose output (O) pins as described in Section "5.16. GPO Outputs". In any bus mode, commands may only be sent after VIO and VDD supplies are applied.

5.15.1. 2-Wire Control Interface Mode

2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a seven bit device address followed by a read/write bit (read = 1, write = 0). The Si4720/21 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4720/21 responds to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the seven-bit device address is 0010001. When SEN = 1, the address is 1100011.

For write operations, the user then sends an eight bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4720/21 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to eight data bytes in a single two-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4720/21 has acknowledged the control byte, it drives an eight-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction ends. The user may read up to 16 data bytes in a single two-wire transaction. These bytes contain the response data from the Si4720/21.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5 "2-Wire Control Interface Characteristics[1]", Figure 2 "2-Wire Control Interface Read and Write Timing Parameters", and Figure 3 "2-Wire Control Interface Read and Write Timing Diagram".

5.15.2. SPI Control Interface Mode

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. For reads, the user can choose to receive data from the device on either SDIO or GPO1. A transaction begins when the user drives SEN low. The user then pulses SCLK eight times while driving an 8-bit control byte (MSB first) serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of these values:

0x48 = write eight command/argument bytes (user drives write data on SDIO)

0x80 = read status byte (device drives read data on SDIO)

0xA0 = read status byte (device drives read data on GPO1)

0xC0 = read 16 response bytes (device drives read data on SDIO)

0xE0 = read 16 response bytes (device drives read data on GPO1)

When writing a command, after the control byte has been written, the user must drive exactly eight data bytes (a command byte and seven argument bytes) on

SDIO. The data will be captured by the device on the rising edges of SCLK. After all eight data bytes have been written, the user raises SEN after the last falling edge of SCLK to end the transaction.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high). In SPI mode, this is done by sending control byte 0x80 or 0xA0, followed by reading a single byte on SDIO or GPO1. The Si4720/21 changes the state of SDIO or GPO1 after the falling edges of SCLK. Data should be captured by the user on the rising edges of SCLK. After the status byte has been read, the user raises SEN after the last falling edge of SCLK to end the transaction.

When reading a response, the user must read exactly 16 data bytes after sending the control byte. It is recommended that the user keep SEN low until all bytes have transferred. However, it will not disrupt the protocol if SEN temporarily goes high at any time, as long as the user does not change the state of SCLK while SEN is high. After 16 bytes have been read, the user raises SEN after the last falling edge of SCLK to end the transaction.

At the end of any SPI transaction, the user must drive SEN high after the final falling edge of SCLK. At any time during a transaction, if SEN is sampled high by the device on a rising edge of SCLK, the transaction will be aborted. When SEN is high, SCLK may toggle without affecting the device.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

5.15.3. 3-Wire Control Interface Mode

3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a three-bit device address (A7:A5 = 101), a read/write bit (read = 1, write = 0), and a five-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turnaround. Next, the Si4720/21 drives the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1-0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA9-0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9, Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

5.16. GPO Outputs

The Si4720/21 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-Z. The GPO pins are multiplexed with the bus mode pins or DCLK depending on the application schematic of the transmitter. GPO2/IRQ can be configured to provide interrupts.

5.17. Audio Output Summation

The audio outputs LOUT and ROUT may be capacitively summed with another device. Setting the audio high-Z enable property maintains a dc bias of 0.5 x VIO on the LOUT and ROUT pins to prevent the ESD diodes from clamping to the VIO or GND rail in response to the output swing of the other device. The bias point is set with a 160 kΩ resistor to VIO and GND. In powerup the LOUT and ROUT pins are set to the common mode voltage specified in Table 9, “FM Receiver Characteristics[1,2],” on page 12, regardless of the state of AHIZEN.

5.18. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset and place it in powerdown mode.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry and keep the bus active. For more information concerning Reset, Powerup, Powerdown, and Initialization, refer to “AN305: Si471x FM Transmitter Programming Guide”.

5.19. Programming with Commands

To ease development time and offer maximum customization, the Si4720/21 provides a simple yet powerful software interface to program the transmitter. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control actions, such as powering up the device, shutting down the device, or tuning to a station. Arguments are specific to a given command and are used to modify the command. For example, after the TX_TUNE_FREQ command, arguments are required to set the tune frequency. A complete list of commands is available in Table 16, "Si4720/21 Command Summary," on page 30.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are TX_PREEMPHASIS and GPO_CONFIGURE. A complete list of properties is available in Table 17, "Si4720/21 Property Summary," on page 31.

Responses provide the user information and are echoed after a command and associated arguments are issued. At a minimum, all commands provide a one-byte status update indicating interrupt and clear-to-send status information.

For a detailed description of using the commands and properties of the Si4720/21, see "AN305: Si471x FM Transmitter Programming Guide".

6. Commands and Properties (Subject to Change)

Table 16. Si4720/21 Command Summary

Cmd	Name	Description
0x00	NOP	No operation command.
0x01	POWER_UP	Power up device and mode selection. Modes include FM transmit and analog/digital audio interface configuration.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Power down device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x14	GET_INT_STATUS	Read interrupt status bits.
0x15	PATCH_RESERVED	Reserved command used for patch file downloads.
0x16	PATCH_RESERVED	Reserved command used for patch file downloads.
0x20	RX_TUNE_FREQ	Tunes to a given receive frequency.
0x21	RX_SEEK_START	Seeks to the next station.
0x22	RX_TUNE_STATUS	Queries the status of a seek or tune.
0x23	RX_RSQ_STATUS	Queries the status and the receive signal quality of the current channel.
0x24	RX_RDS_STATUS	**Si4721 Only.** Returns RDS information for the current channel including block data and error rates.
0x30	TX_TUNE_FREQ	Tunes to given transmit frequency.
0x31	TX_TUNE_POWER	Sets the output power level and tunes the antenna capacitor
0x33	TX_TUNE_STATUS	Queries the status of a previously sent TX Tune Freq, TX Tune Power, or TX Tune Measure command.
0x34	TX_ASQ_STATUS	Query the TX status and input audio signal metrics.
0x35	TX_RDS_BUFF	**Si4721 Only**. Queries the status of the RDS Group Buffer and loads new data into buffer.
0x36	TX_RDS_PS	**Si4721 Only**. Set up default PS strings.

Table 17. Si4720/21 Property Summary

Prop	Name	Description	Default
0x0001	GPO_IEN	Enables interrupt sources.	0x0000
0x0002	GPO_CONFIG	Set Operation for GPO1, GPO2/IRQ, and GPO3.	0x0000
0x0101	DIGITAL_INPUT_FORMAT	Configures the digital input format.	0x0000
0x0102	DIGITAL_OUTPUT_FORMAT	Configures the digital output format.	0x0000
0x0103	DIGITAL_INPUT_SAMPLE_RATE	Configures the digital input sample rate in 10 Hz steps. Default is 44.1 kHz	0x113A
0x0104	DIGITAL_OUTPUT_SAMPLE _RATE	Configures the digital output sample rate in 100 Hz steps. Default is 44.1 kHz.	0x113A
0x0201	RCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0201	REF_CLK_FREQ	Sets frequency of reference clock in Hz.	0x8000
0x0202	RCLK_PRESCALE	Sets the prescaler value for RCLK input. Range is 1 to 4095.	0x0001
0x0202	REF_CLK_PRESCALER	Sets the prescaler value for reference clocks above 65.536 kHz.	0x0000
0x1030	VARACTOR_OVERWRITE	Manually sets the capacitance in the capacitor bank.	0x0000
0x1100	DE-EMPHASIS	Sets de-emphasis level.	0x0000
0x1107	RX_ANTENNA_TYPE	Antenna selection.	0x0000
0x1200	RSQ_INTERRUPT_SOURCE	Configures interrupts related to signal quality metrics.	0x0000
0x1201	SNR_HIGH_THRESHOLD	Sets the high SNR threshold level. A SNR level higher than this threshold will trigger an interrupt if set by the Set Interrupt property (0x1206).	0x0000
0x1202	SNR_LOW_THRESHOLD	Sets the low SNR threshold level. A SNR level lower than this threshold will trigger an interrupt if set by the Set Interrupt property (0x1206).	0x0000
0x1203	RSSI_HIGH_THRESHOLD	Sets the high RSSI threshold level. A RSSI level higher than this threshold will trigger an interrupt if set by the Set Interrupt property (0x1206).	0x0000
0x1204	RSSI_LOW_THRESHOLD	Sets the low RSSI threshold level. A RSSI level lower than this threshold will trigger an interrupt if set by the Set Interrupt property (0x1206).	0x0000
0x1205	IMPULSE_HIGH_THRESHOLD	Sets the high impulse count threshold. An impulse count higher than this threshold will trigger an interrupt if set by the Set Interrupt property (0x1206).	0x0000
0x1206	IMPULSE_LOW_THRESHOLD	Sets the low impulse count threshold. An impulse count lower than this threshold will trigger an interrupt if set by the Set Interrupt property (0x1206).	0x0000
0x1300	SOFT_MUTE_RATE	Sets the soft mute attack and decay rate.	0x0000

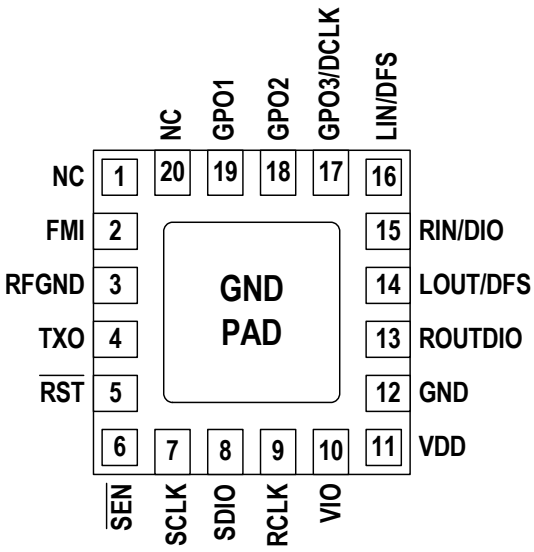
Table 17. Si4720/21 Property Summary (Continued)

Prop	Name	Description	Default
0x1302	SOFT_MUTE_ATTENUATION	Sets the soft mute attenuation.	0x0000
0x1400	SEEK_BAND_BOTTOM	Sets the bottom of the FM band for seek in 100 kHz steps.	0x036B
0x1401	SEEK_BAND_TOP	Sets the top of the FM band for seek in 100 kHz steps.	0x0438
0x1402	SEEK_FREQ_SPACING	Sets the seek channel spacing in kHz.	0x00C8
0x1403	SEEK_SNR_THRESHOLD	Sets the minimum seek SNR threshold level.	0x0000
0x1404	SEEK_RSSI_THRESHOLD	Sets the minimum seek impulse threshold level in dB.	0x000A
0x1405	SEEK_IMPULSE_THRESHOLD	Sets the maximum seek impulse threshold level.	0x0000
0x1500	RX_RDS_CONFIGURE	**Si4721 Only.** Configures interrupts related to RDS. Interrupts are disabled by default.	0x0000
0x2100	TX_COMPONENT_ENABLE	Enable transmit multiplex signal components. Default has pilot and L-R enabled.	0x0003
0x2101	TX_AUDIO_DEVIATION	Configures audio frequency deviation level. Units are in 10 Hz increments. Default is 6750 (67.5 kHz).	0x1AA9
0x2102	TX_PILOT_DEVIATION	Configures pilot tone frequency deviation level. Units are in 10 Hz increments. Default is 750 (7.5 kHz)	0x02A3
0x2103	TX_RDS_DEVIATION	**Si4721 Only.** Configures the RDS/RBDS frequency deviation level. Units are in 10 Hz increments.	0x0000
0x2104	TX_LINE_INPUT_LEVEL	Configures maximum analog line input level to the LIN/RIN pins to reach the maximum deviation level programmed into the audio deviation property TX Audio Deviation. Default is 636 mVpk.	0x027C
0x2105	TX_LINE_INPUT_MUTE	Sets line input mute. L and R inputs may be independently muted.	0x0000
0x2106	TX_PREEMPHASIS	Configures pre-emphasis time constant. Default is 0 (75 µS).	0x0000
0x2107	TX_PILOT_FREQUENCY	Configures the frequency of the stereo pilot. Default is 19000 Hz.	0x4A38
0x2200	TX_ACCOMP_ENABLE	Enables audio dynamic range control. Default is 0 (disabled).	0x0000
0x2201	TX_ACCOMP_THRESHOLD	Sets the threshold level for audio dynamic range control. Default is –40 dB.	0xFFD8
0x2202	TX_ACCOMP_ATTACK_TIME	Sets the attack time for audio dynamic range control. Default is 0 (0.5 msec).	0x0000
0x2203	TX_ACCOMP_RELEASE_TIME	Sets the release time for audio dynamic range control. Default is 4 (1000 msec).	0x0004

Table 17. Si4720/21 Property Summary (Continued)

Prop	Name	Description	Default
0x2204	TX_ACCOMP_GAIN	Sets the gain for audio dynamic range control. Default is 15 dB.	0x000F
0x2300	TX_ASQ_ENABLE	Configures measurements related to signal quality metrics.	0x0000
0x2301	TX_ASQ_LEVEL_LOW	Configures low audio input level detection threshold. This threshold can be used to detect silence on the incoming audio.	0x0000
0x2302	TX_ASQ_DURATION_LOW	Configures the duration which the input audio level must be below the low threshold in order to detect a low audio condition.	0x0000
0x2303	TX_ASQ_LEVEL_HIGH	Configures high audio input level detection threshold. This threshold can be used to detect activity on the incoming audio.	0x0000
0x2304	TX_ASQ_DURATION_HIGH	Configures the duration which the input audio level must be above the high threshold in order to detect a high audio condition.	0x0000
0x2C00	TX_RDS_CONFIG	**Si4721 Only.** Set up RDS for transmit.	0x0000
0x2C01	TX_RDS_PI	**Si4721 Only.** Sets transmit RDS program identifier.	0x0000
0x2C02	TX_RDS_PS_MIX	**Si4721 Only.** Configures mix of RDS PS Group with RDS Group Buffer.	0x0000
0x2C03	TX_RDS_PS_MISC	**Si4721 Only.** Miscellaneous bits to transmit along with RDS_PS Groups.	0x0000
0x2C04	TX_RDS_PS_REPEAT_COUNT	**Si4721 Only.** Number of times to repeat transmission of a PS message before transmitting the next PS message.	0x0000
0x2C05	TX_RDS_PS_MESSAGE_COUNT	**Si4721 Only.** Number of PS messages in use.	0x0001
0x2C06	TX_RDS_PS_AF	**Si4721 Only.** RDS Program Service Alternate Frequency. This provides the ability to inform the receiver of a single alternate frequency using AF Method A coding and is transmitted along with the RDS_PS Groups.	0xE0E0
0x4000	RX_VOLUME	Sets the device volume.	0x0000
0x4001	MUTE	Sets mute.	0x0000
0xXXXX	STEREO_BLEND_THRESHOLD	Configures stereo blend parameters.	0x0000
0xXXXX	STEREO_BLEND_MONO_ THRESHOLD	Configures stereo blend parameters.	0x000

7. Pin Descriptions: Si4720/21-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM RF input.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	TXO	FM transmit output connection to transmit antenna.
5	RST	Device reset (active low) input.
6	SEN	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference oscillator input.
10	VIO	I/O supply voltage.
11	VDD	Supply voltage. May be connected directly to battery.
13	ROUT/DIO	Right audio line output—digital input/output data.
14	LOUT/DFS	Left audio line output—digital frame synchronization.
15	RIN/DIO	Right audio line input—digital input/output data.
16	LIN/DFS	Left audio line input—digital frame synchronization.
17	GPO3/DCLK	General purpose output—digital bit synchronous clock.
18	GPO2	General purpose output.
19	GPO1	General purpose output.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.

8. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4720-A-GM	Portable Broadcast Radio Transceiver	QFN Pb-free	–20 to 85 C
Si4721-A-GM	Portable Broadcast Radio Tuner FM Stereo + RDS/RBDS	QFN Pb-free	–20 to 85 C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

9. Package Outline: Si4720/21-GM

Figure 20 illustrates the package details for the Si4720/21. Table 18 lists the values for the dimensions shown in the illustration.

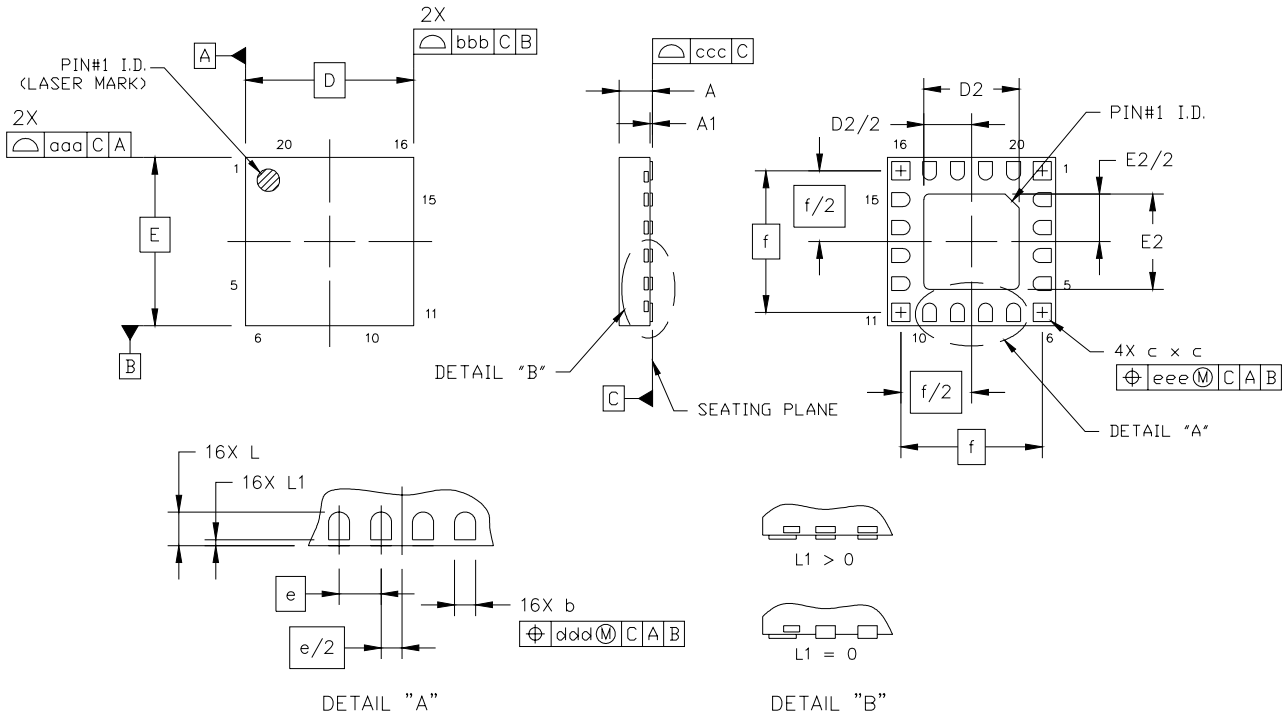


Figure 20. 20-Pin Quad Flat No-Lead (QFN)

Table 18. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

10. PCB Land Pattern: Si4720/21-GM

Figure 21 illustrates the PCB land pattern details for the Si4720/21-GM. Table 19 lists the values for the dimensions shown in the illustration.

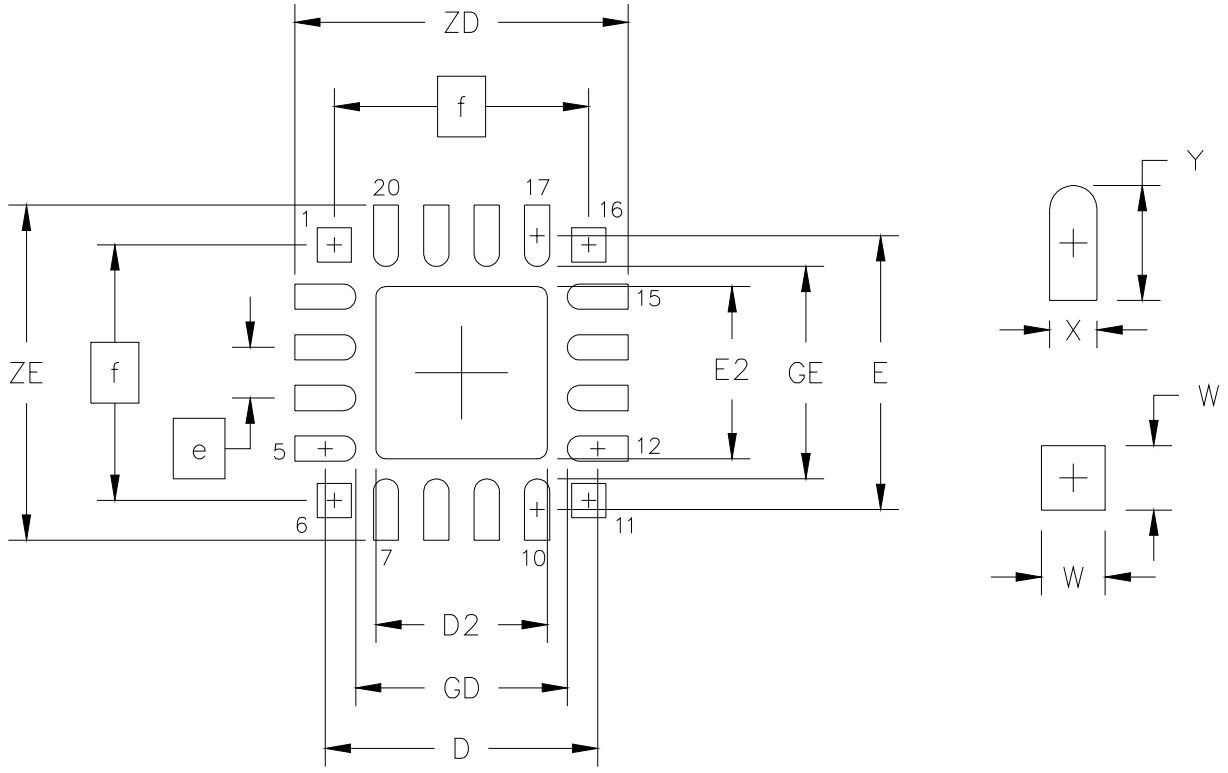


Figure 21. PCB Land Pattern

Table 19. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

Note: Solder Mask Design

1. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

Additional Reference Resources

- “AN231: Si4700/01 Headphone and Antenna Interface”
- “AN234: Si4700/01 FM Tuner Evaluation Board Test Procedure”
- “AN284: Si4700/01 Firmware 15 Seek Adjustability and Settings”
- “AN305: Si471x FM Transmitter Programming Guide”
- “AN306: Si4720/21 Short Monopole Antenna Interface”
- “Si471x-EVB” Rev 0.3 User’s Guide
- “AN308: Si4720/21 FM Transmitter Evaluation Board Test Procedure”
- “AN309: Si4720/21 Evaluation Board Quick-Start Guide”
- Si4720/21 Customer Support Site: www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, send mysilabs user name and request for access to fminfo@silabs.com.

Document Change List

Revision 0.2 to Revision 0.3

- Changed package from 4 x 4 0.55 mm 24-pin QFN to 3 x 3 0.55 mm 20-pin QFN.
  - Updated “9. Package Outline: Si4720/21-GM” and added “10. PCB Land Pattern: Si4720/21-GM”.
  - Updated block diagram to reflect new package.
  - Updated application schematics.
  - Removed application schematics 5 through 7.
  - Updated Table 12 on page 23 to reflect new pin diagram.
- Updated Table 9, “FM Receiver Characteristics[1,2],” on page 12.
  - Changed RSSI Offset test condition.
  - Added Line Output parameters.
- Updated Table 10, “FM Transmitter Characteristics[1],” on page 14.
  - Updated test conditions.
  - Removed Pilot Modulation Rate parameter.
  - Added Modulation Rate Accuracy
  - Added Line Input parameters.
- Removed Analog Audio Characteristics Table from “1. Electrical Specifications”.
- Updated Pin Diagram and Pin Descriptions in “7. Pin Descriptions: Si4720/21-GM”.
- Added "5.6. Stereo Audio Processing" on page 24.
  - Added "5.6.1. Stereo Decoder" on page 24.
  - Added "5.6.3. Stereo Encoder" on page 24.
  - Added "5.6.2. Stereo-Mono Blending" on page 24.
- Added "5.7. Audio Dynamic Range Control" on page 25.
- Added "5.8. Pre-emphasis and De-emphasis" on page 26.
- Added "5.9. Stereo DAC" on page 26.
- Changed 2-wire control interface address from 001000b to 1100011b in "4.16.1. 2-wire Control Interface" on page 30.
- Changed 3-wire control interface address from 0110b to 1010b in "4.16.2. 3-Wire Control Interface" on page 30.
- Added "5.1. Si4720/21 Commands" on page 36.
- Added "5.2. Si4720/21 Properties" on page 52.
- Changed Command Summary section to "6. 3-Wire Command Format" on page 71.
- Removed Command Descriptions.

Revision 0.3 to Revision 0.31

- Corrected “ Command 01h. Power Up / Switch Modes”.
  - Updated modes of operation.
- Fixed typo error in Table 19.
  - “Vacator” changed to “Varactor”.
- Updated “Table 3. DC Characteristics1”.

Revision 0.31 to Revision 0.4

- Updated Figure 12, “Functional Block Diagram,” on page 20.
- Updated Table 10, “FM Transmitter Characteristics[1],” on page 14.
- Added “2. Test Schematic”.
- Added Table 13, “Si4720/21 Test Circuit Bill of Materials,” on page 19.
- Updated “5. Functional Description” to include revised transmit specifications.
- Updated “6. Commands and Properties (Subject to Change)”.
- Removed “Detailed Commands and Properties” Section, this will be included in the programming guide.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: FMinfo@silabs.com
Internet: www.silabs.com