High Voltage Pulser Circuits

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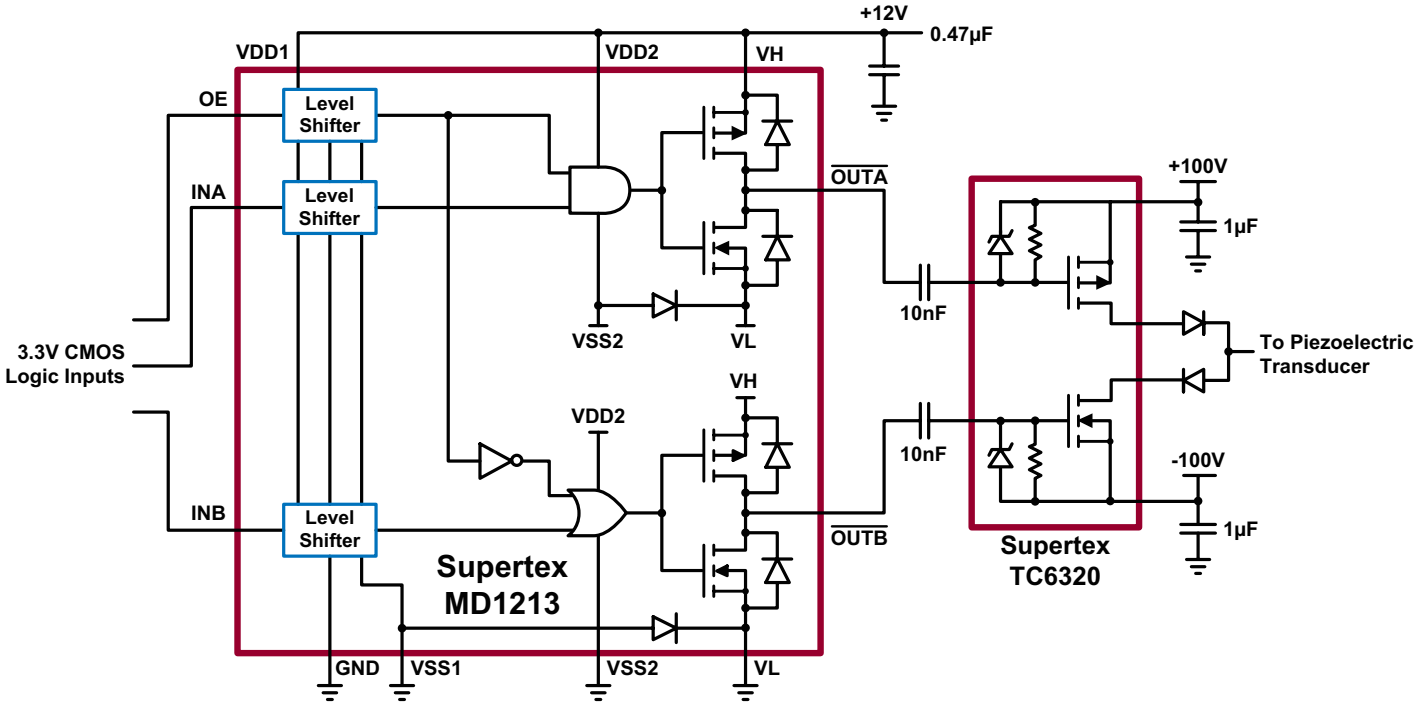
Introduction

The high voltage pulser circuit shown in Figure 1 utilizes Supertex's complementary P- and N-channel transistors (TC6320) driven by an MD1213 to achieve excellent performance and efficiency with minimal components. The output voltage swings are -100 to +100V. Rise and fall times are less than 15ns while sourcing and sinking over ±2.0 amps respectively. The output is conveniently controlled by input logic signals with 1.2 to 5.0V over any CMOS logic circuit. The MD1213 only needs a single V_{DD} supply voltage of 5.0 to 12V, and does not need any logic supply voltage.

High voltage, high speed, and high current pulses at low duty cycles are usually required in applications such as medical ultrasound imaging, B-scan ultrasound, material flaw detection in NDT ultrasound, sonar transmitters and signal generation in test instruments.

Figure 1: ±100V Bipolar Pulser Using the MD1213 and TC6320



Circuit Description

The high voltage pulser in Figure 1 consists of 3 basic stages; the input signal interface, the high current buffer and level translation, and the high voltage and current output drivers. The first stage has been designed and integrated into the MD1213. Low input capacitance and fast switching speed are the most important considerations in the MD1213 input stage. The logic inputs operate at more than 20kΩ with less than 5.0pF input impendence, and an internal speed of 100MHz. The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. The MD1213 input logic is fully compatible and will work with1.8, 2.0, 2.5, 3.3 or 5.0V CMOS logic IC, FPGA, CPLD and CPU families. Second, when OE is low, the outputs are disabled, with the A output high and the B output low. This assists in properly pre-charging the AC coupling capacitors that may be used in series in the gate drive circuit of a pair of external P- and N-channel FETs.

The output stage of the MD1213 has separate power connections enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0 and 1.8V, and the control logic may be powered

by +5.0 to 12V. Typically, the MD1213 output has about a 6ns rise and fall time with a 1000pF load. The output stage is capable of peak currents of up to ±2.0A, depending on the supply voltages used and load capacitance present. Such high currents are required to adequately drive the input capacitances, including Miller effect of the output MOSFETs, to accomplish fast switching speeds.

The Supertex TC6320TG consists of a high voltage, low threshold, P-channel and N-channel MOSFET in an 8-Lead SO package. Both MOSFETs have integrated gate-source resistors and gate-source Zener diode clamps which are desired for high voltage pulser applications. The TC6320TG offers 200V breakdown voltage and 2.0A output peak current and low input capacitance. The 2.0A output current capability will minimize the high voltage pulser output rise and fall times. The low input capacitance will minimize propagation delay times and also make the rise and fall times faster.

The TC6320 P- and N-channel FETs have integrated gate-source resistors and gate-source Zener diode clamps that are desired for high voltage pulser applications to save board space and improve performance. Output voltage swings can switch from -100 to +100V. Input capacitance is increased due to the Miller effect, $C_{IN} = C_{ISS} + C_{RSS}$ (GFS* RL). Low C_{RSS} & C_{ISS} capacitance, high output current, low on-resistance and high breakdown voltage are required parameters for the output transistors. The Supertex TC6320 is ideally suited for the high voltage pulser. Also, complementary P- and N-channel DMOS transistors array TC7320 or discreet TN5325/TP5322, TN0104/TP0102, TP0620/TN0620 or TP2640/TN2640, may be used for their low threshold voltages, low input capacitances and high output current capabilities. These are essential features to generate high voltage pulses with high speeds and currents. All these high voltage MOSFETs are cost-effective, and in 8-Lead SO, 32-Lead LQFP, SOT-89 or SOT-23 etc. packages, which have low package inductance, they have excellent thermal performance and save board space.

During power up and power down conditions, it is possible for transient voltages greater than 20V to appear across the gate-to-source on the output transistors. Maximum gate-to-source voltage, V_{GS}, is rated at ±20V. The built-in 15 - 18V Zener diodes are connected across the gate and source of the output transistors to protect against such transient voltages. These diodes will not have Zener current during normal operation. But even if the high voltage V_{PP} and V_{NN} can be ramped slowly, the Zener diodes can't be omitted, because these diodes also serve as the gate DC voltage restoring functions.

V_{PP} and V_{NN} voltages can be varied without additional changes within the circuitry. For example, V_{NN} can be 0V and V_{PP} +200V for positive unipolar pulses. Or V_{NN} can be –200V and V_{PP} 0V for a negative unipolar pulser. See Figure 2 and Figure 4.

For a single supply to MD1213, connect VDD1, VDD2, and VH pins to a V_{DD} of +5.0, +10 or +12V and connect VSS1, VSS2 and VL, to ground.

For all the unipolar cases, if V_{DD} is 200V, the high voltage supply bypass capacitors need to have a working voltage higher than 200V. And the high voltage side gate coupling capacitor(s) need to have a similar working voltage as well. In the case of a positive unipolar and single driver supply, the OUTB to N-FET gate can be DC coupled without a coupling capacitor. See Figure 5.

A bipolar return-to-zero high voltage pulser circuitry powered by +10 and ±100V is shown in Figure 6.

Note the outputs of the two drain MOSFETs may or may not be connected. The output condition in each application will determine the connections. When one uses the pulser alone as shown, then connecting the two drains is fine and even delivers some speed advantages. But if the circuit is only part of multi-level pulser and it is not the highest voltage one, then the drains must not be connected. In these cases the diodes need to direct the voltage and current separately when positive or negative pulses are generated.

PCB Layout Design Considerations

For proper operation of the MD1213, low inductance (ESL) bypass capacitors should be used on the various supply pins. The GND input pin should be connected to the digital ground. The INA, INB, and OE pins should be connected to their logic source with a swing of GND to logic level high which is 1.2 to 5.0V. Good trace practices should be followed corresponding to the desired operating speed.

The internal circuitry of the MD1213 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. The VSS1, VSS2, and VL pins should have low inductance feed-through connections directly to a ground plane. The power connections VDD1 and VDD2 should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads. A common capacitor and voltage source may be used for these two pins, which should always have

the same DC voltage applied. For applications sensitive to jitter and noise, a separate decoupling ferrite bead may be used for VDD1 from VDD2. The supplied voltages of VH and VL determine the output logic levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistor in series with the output signal to obtain better waveform integrity at the load terminals. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. Pay particular attention to the parasitic coupling from the driver output to the input signal terminals. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.2V, even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that the circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry.

Figure 2: +200V Unipolar Pulser Using the MD1213 and TC6320

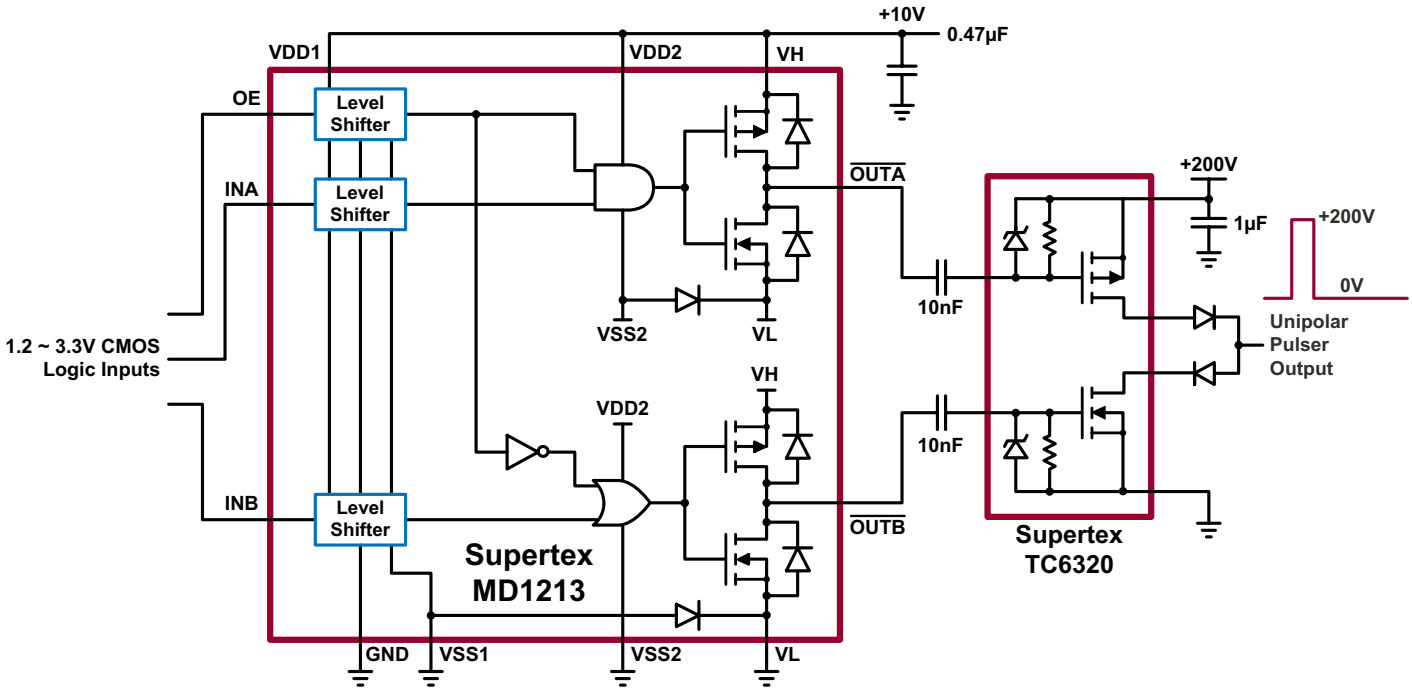


Figure 3: +200V Unipolar Pulser with MD1213 Power Supply

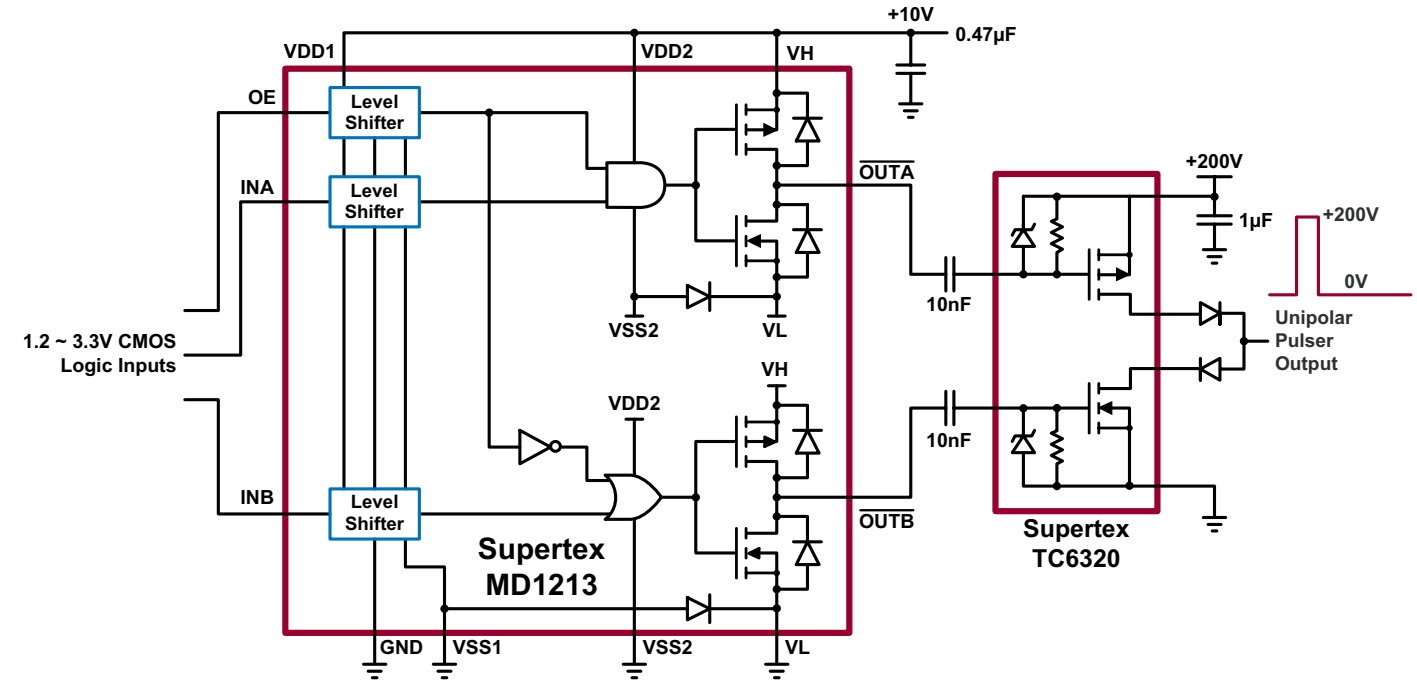


Figure 4: -200V Unipolar Pulser Using the MD1213, TC6320

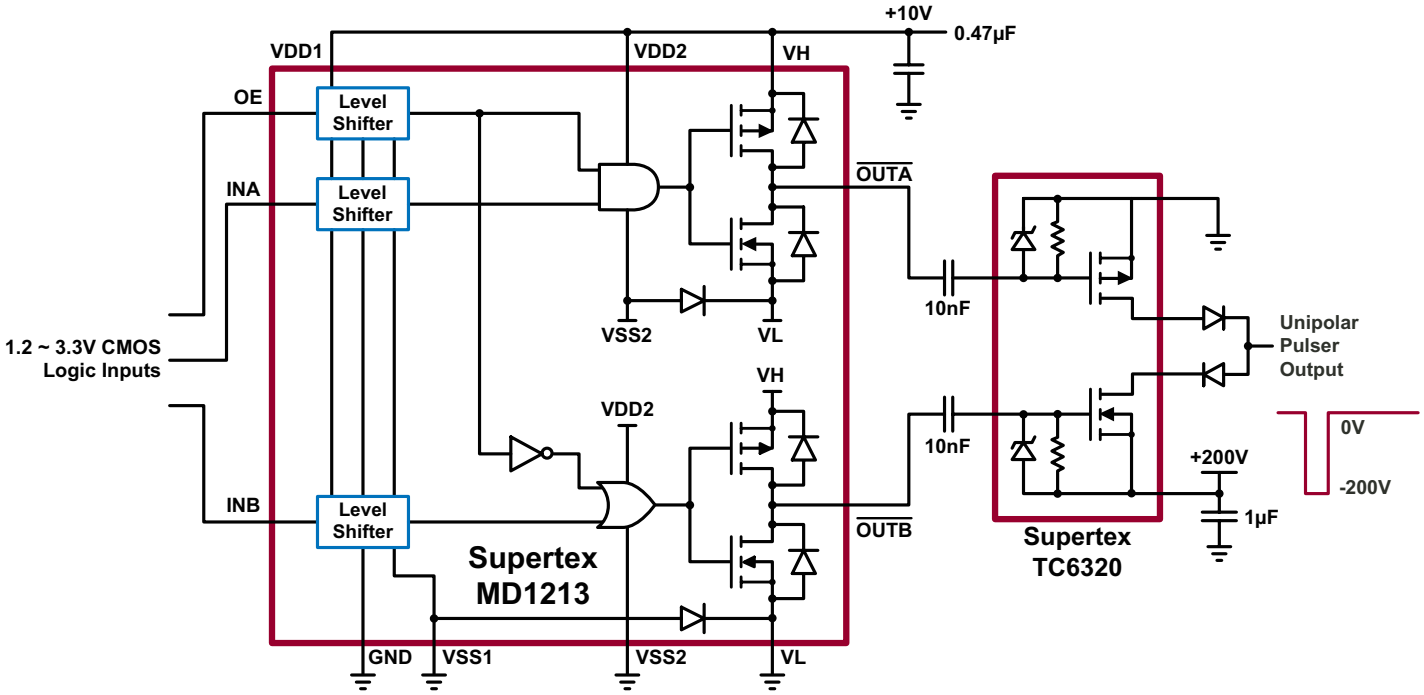


Figure 5: +200V Unipolar Pulser Using the MD1213, TP2640, and the TN2640

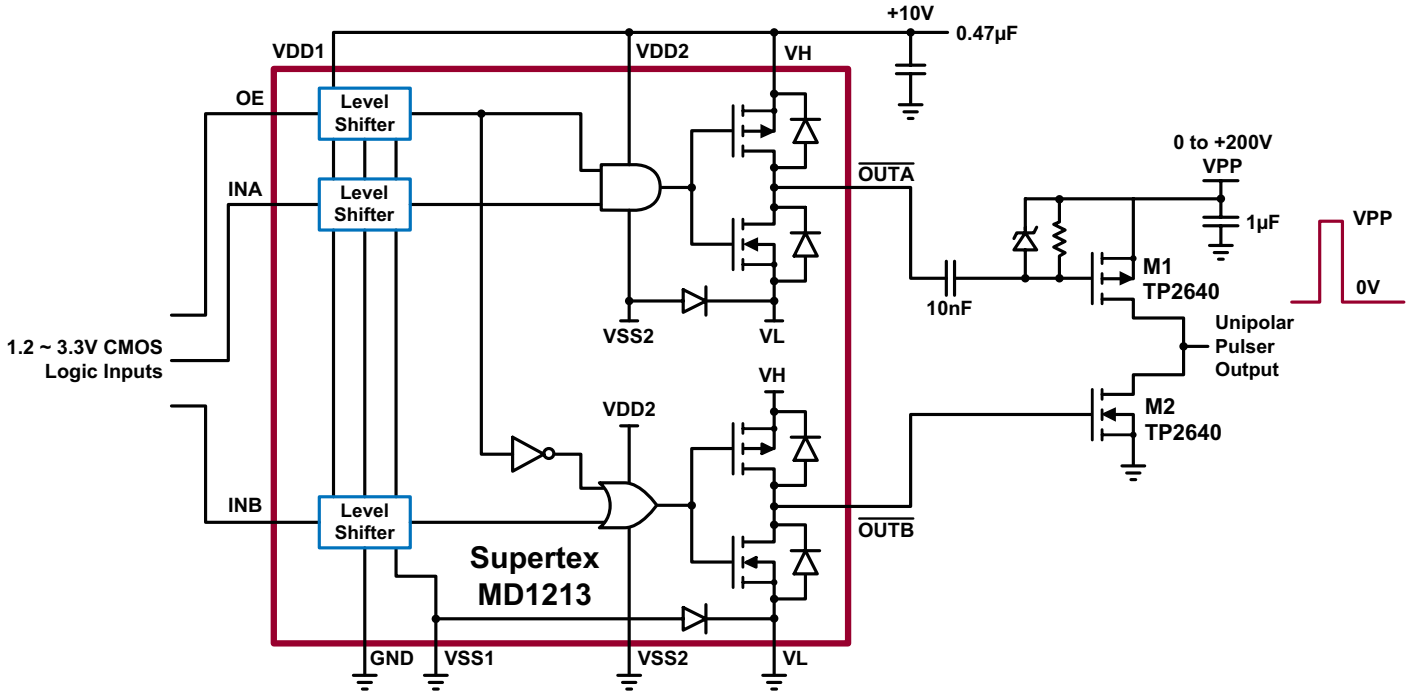


Figure 6: ±100V Bipolar 3-Level Pulser Using the MD1213, and the TC6320

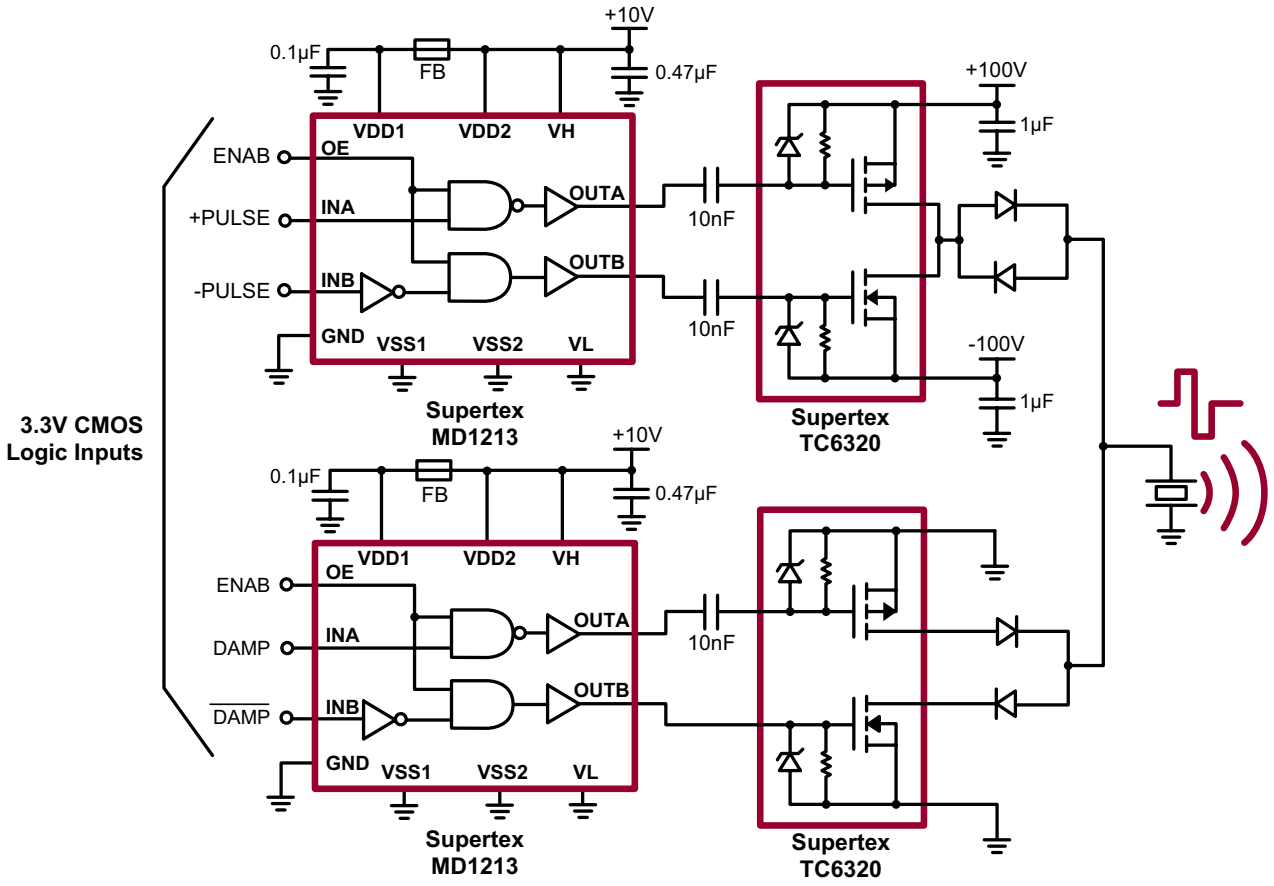
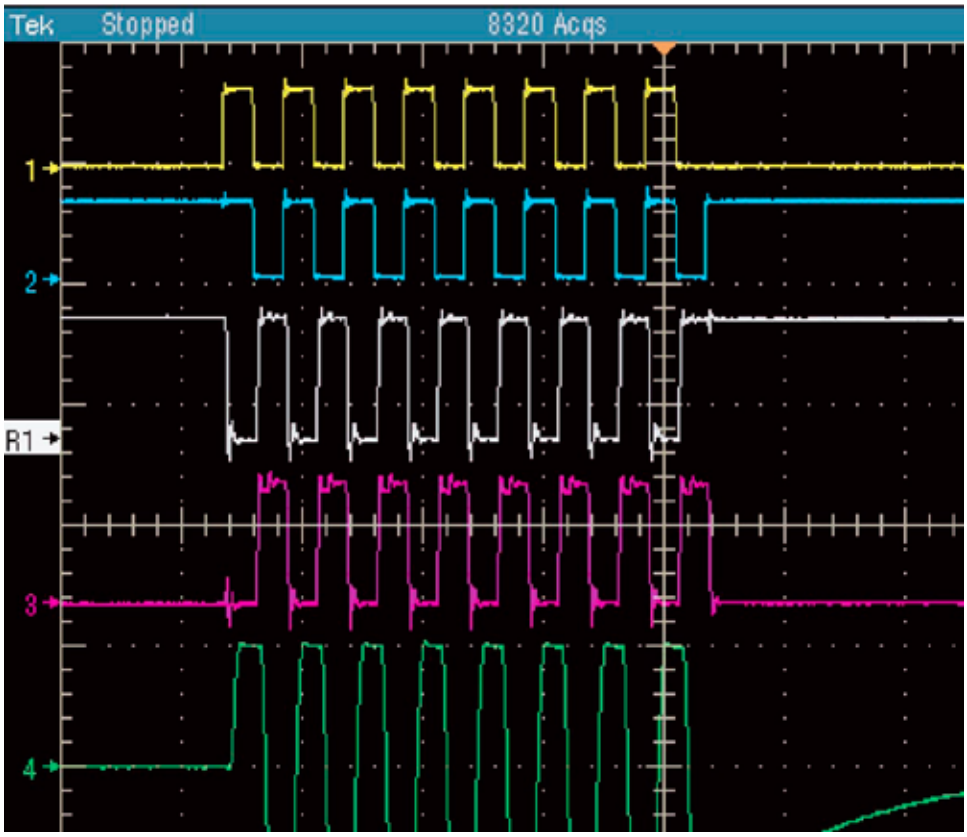


Figure 7: MD1213DB1 Waveform



CH1:	**INA**	**5.0V/div**
CH2:	**INB**	**5.0V/div**
CH3:	**UOA**	**10.0V/div**
REF1:	**OUB**	**10.0V/div**
CH4:	**HVOUT**	**100.0V/div**

Recorded by TEK TDS5104B 2.5GS/sec
P6243 1GHz Probes
1K//120pF load, at 200ns/div Horizontal.

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