KIWA7/A8

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:0.4

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.		
Title: **Cover Sheet**		
Size: B	Document Number: **KIWAX_LA-5082P**	Rev: 0.4
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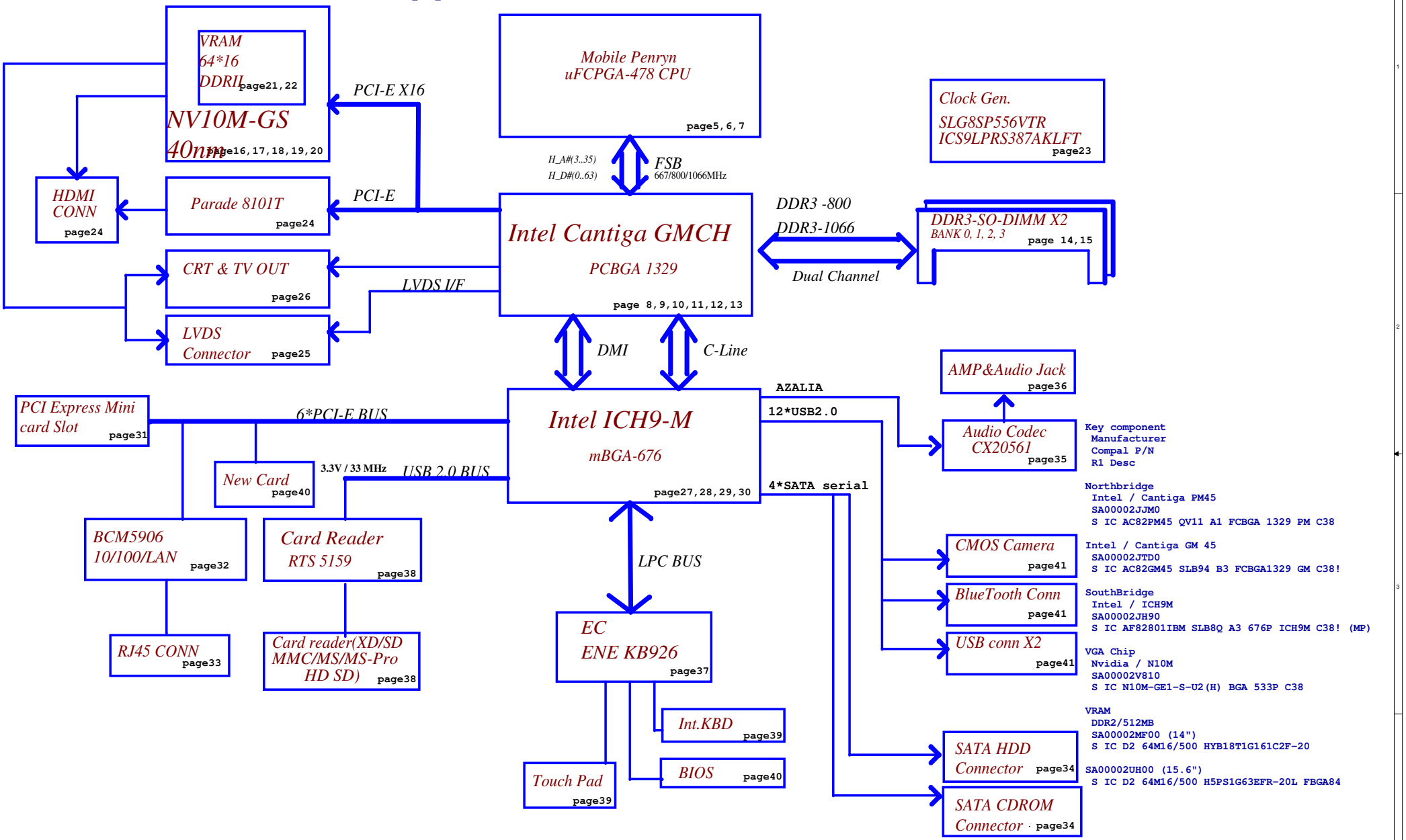
Compal confidential
File Name :

ZZZ
15W_PCB_LA5082P

POWER Board

CAP SENSE LEDs Board

USB board



Key component
Manufacturer
Compal P/N
R1 Desc

Northbridge
Intel / Cantiga PM45
SA00002JJM0
S IC AC82PM45 QV11 A1 FCBGA 1329 PM C38

Intel / Cantiga GM 45
SA00002JTD0
S IC AC82GM45 SLB94 B3 FCBGA1329 GM C38!

SouthBridge
Intel / ICH9M
SA00002JH90
S IC AF82801IBM SLB8Q A3 676P ICH9M C38! (MP)

VGA Chip
Nvidia / N10M
SA00002V810
S IC N10M-GE1-S-U2(H) BGA 533P C38

VRAM
DDR2/512MB
SA00002MF00 (14")
S IC D2 64M16/500 HYB18T1G161C2F-20

SA00002UH00 (15.6")
S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	V	X	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

Compal Electronics, Inc.	
Title	MB Notes List
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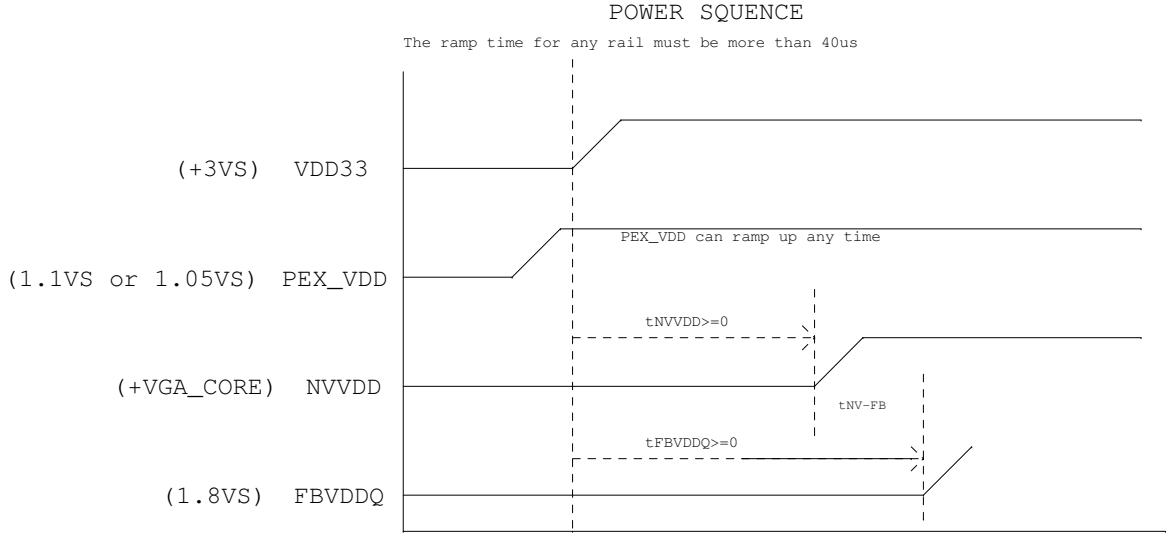
VGA and DDR2 Voltage Rails (N10M)

power plane / State				+3VS +VGA_CORE +1.1VS (for 55nm) +1.05VS (for 40nm) +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SQUENCE



Compal Electronics, Inc.

Title: VGA Notes List

Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

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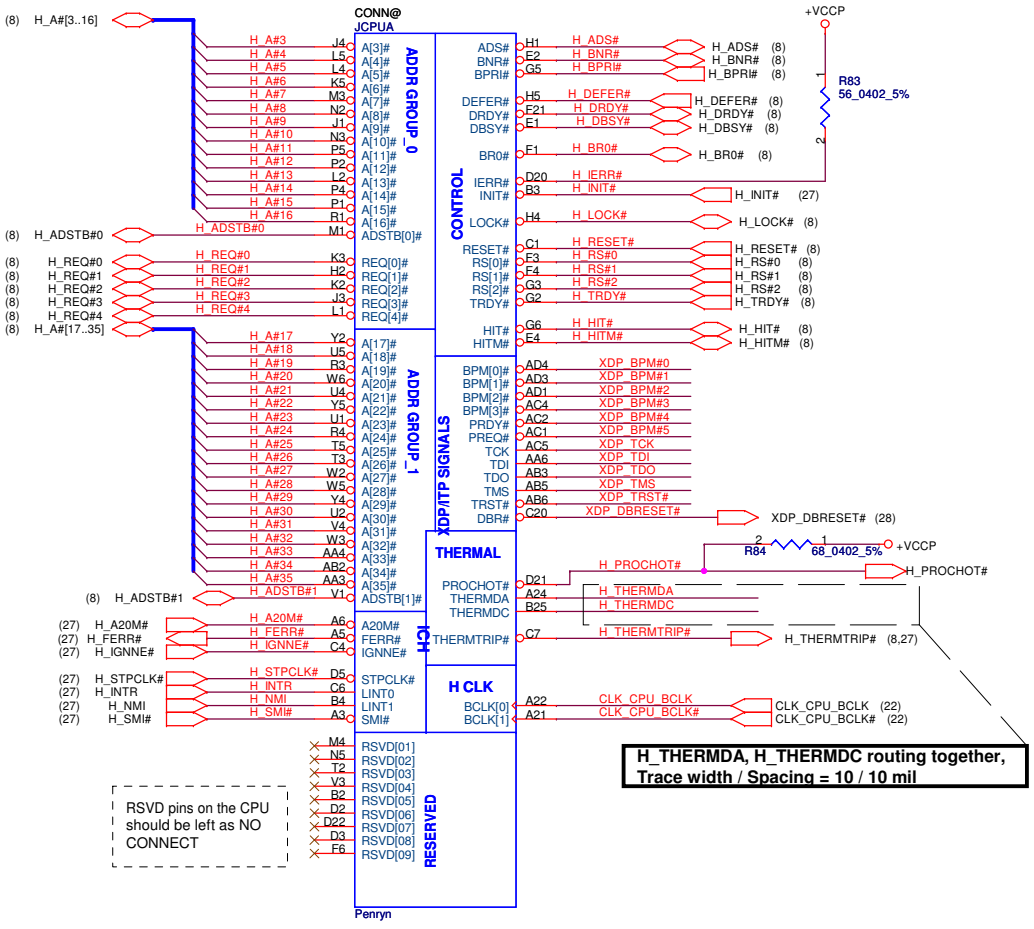
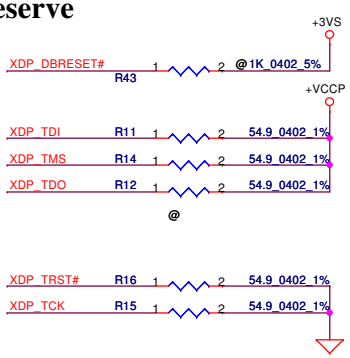
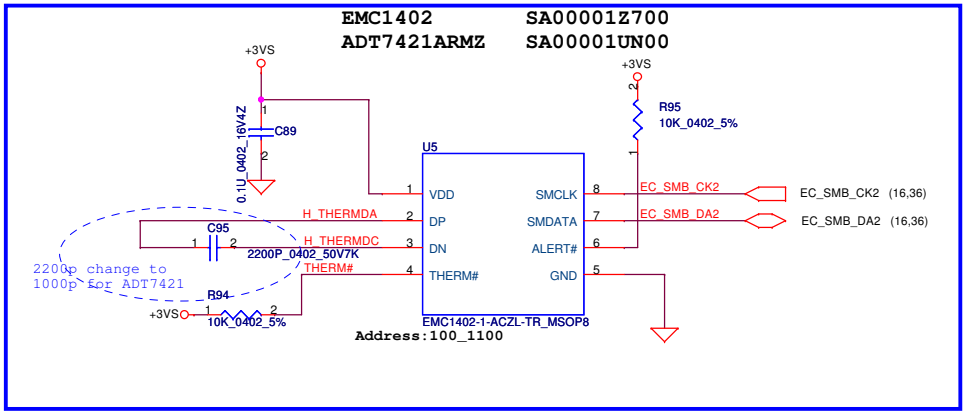
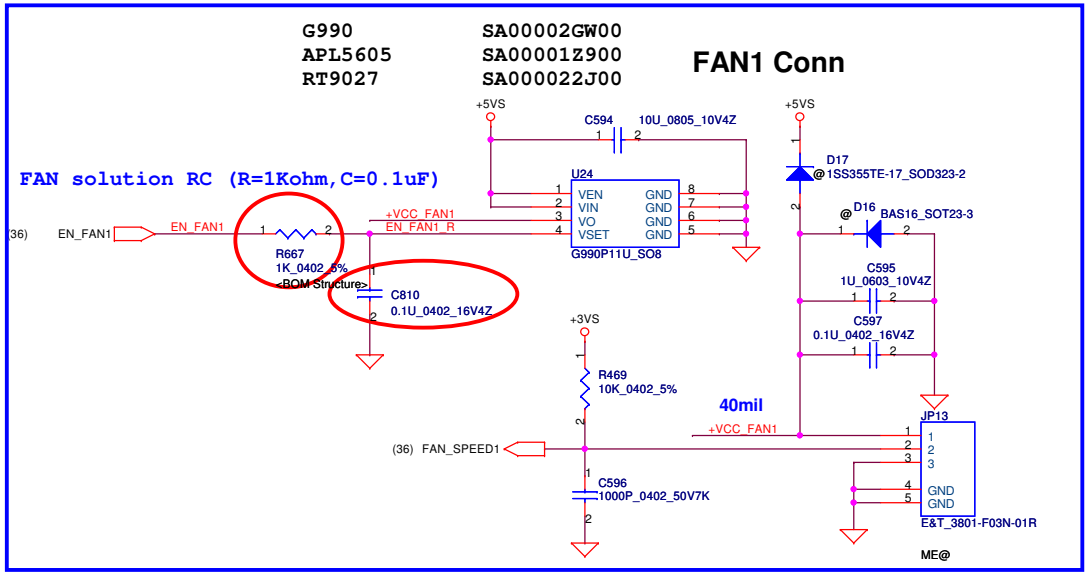


XDP Reserve







Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Penryn (1/3)			
Size: B	Document Number: KIWAX_LA-5082P		Rev: 0.4
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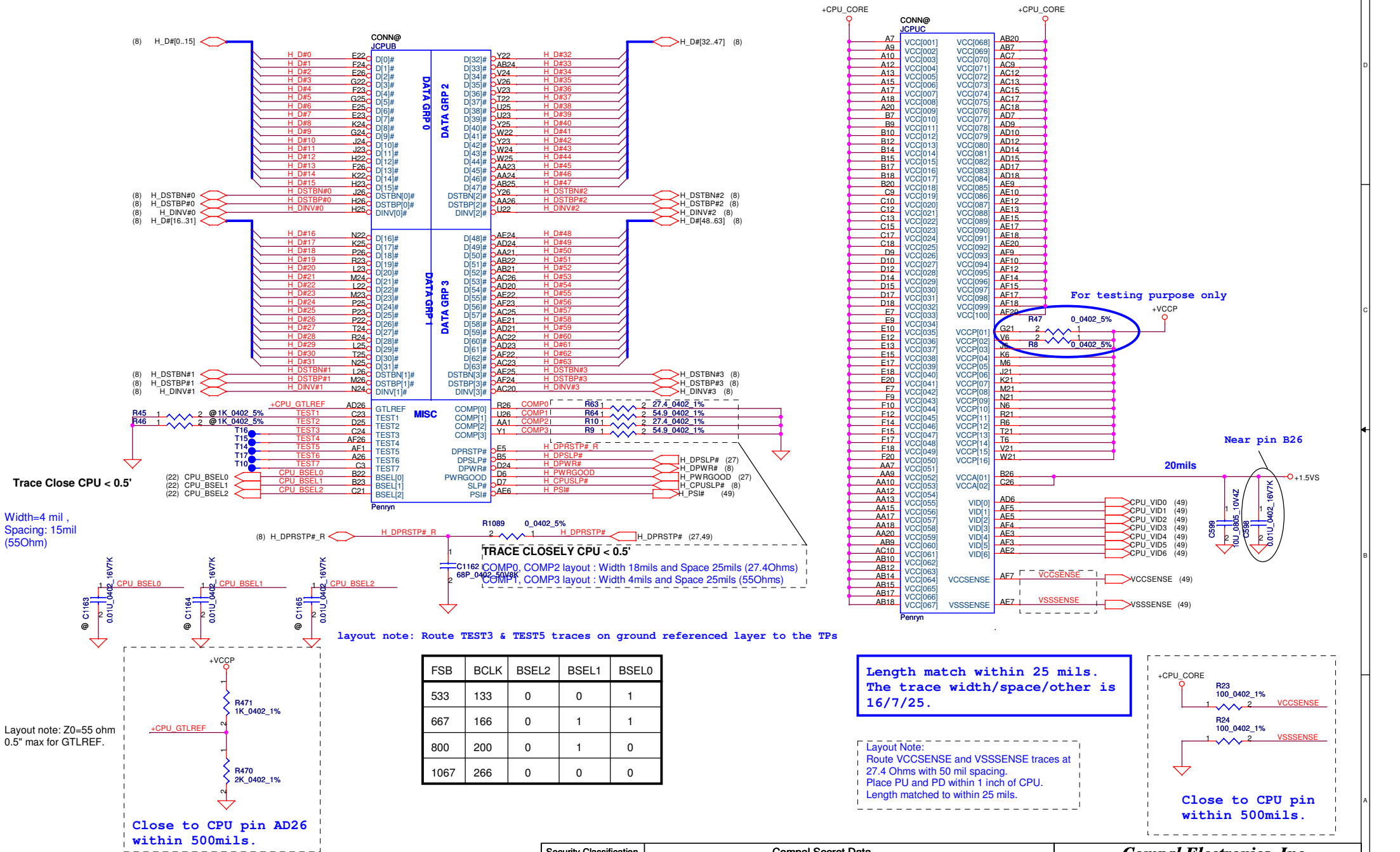
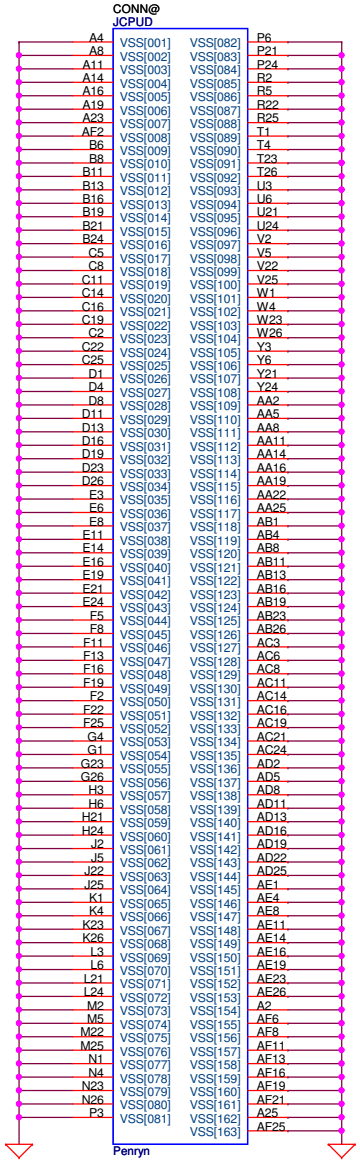
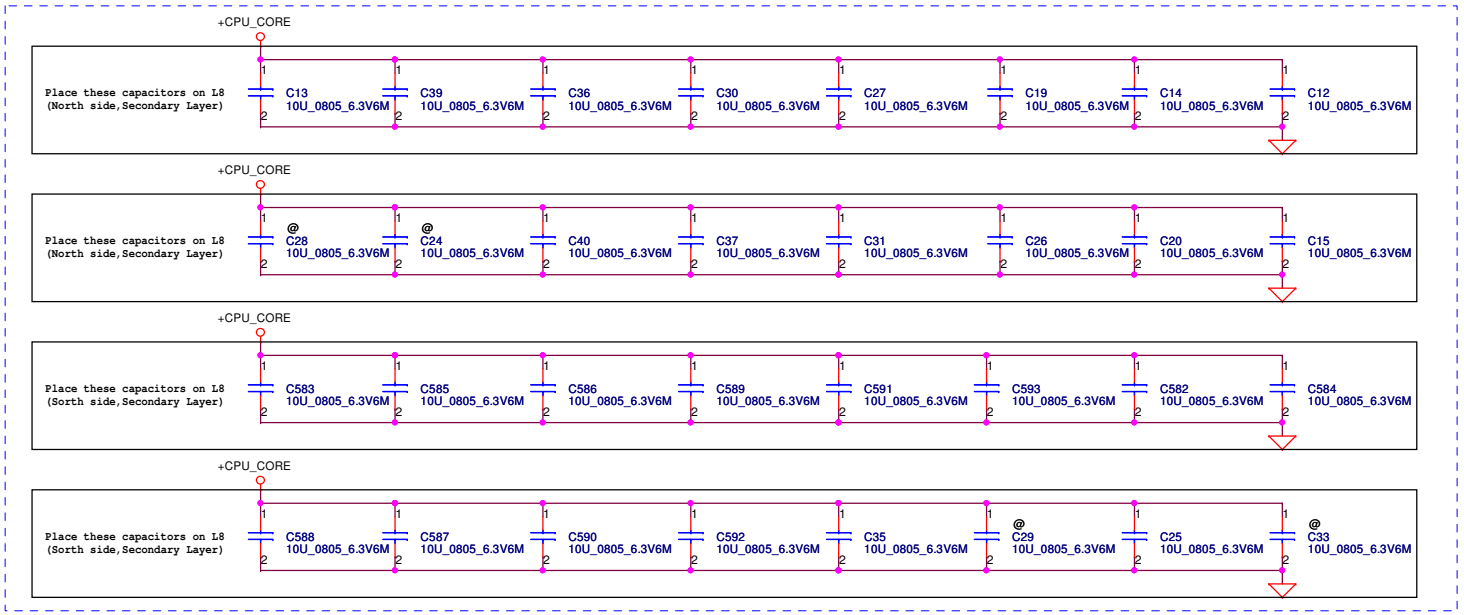


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

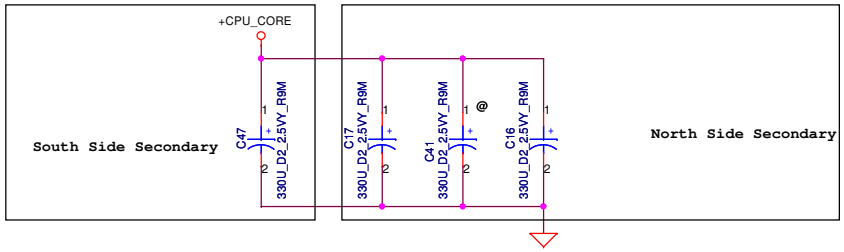
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Penryn (2/3)			
Size: B	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 6 of 53		

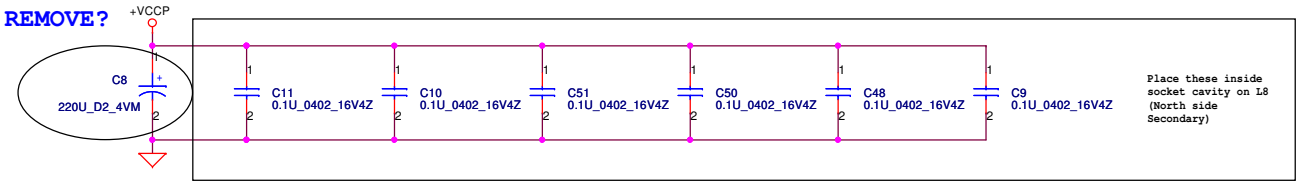




Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Penryn (3/3)**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

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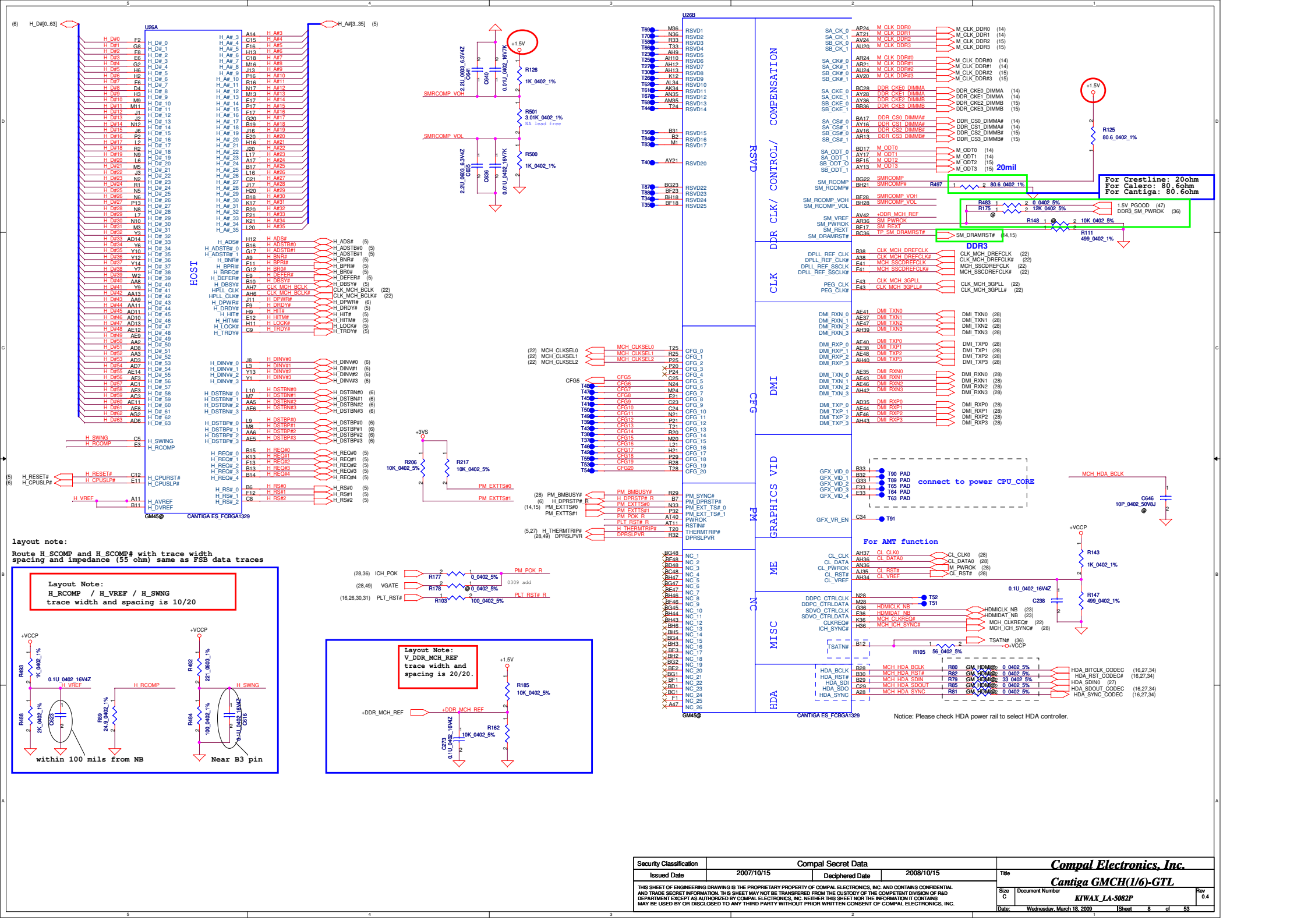

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Title	Compal Electronics, Inc.		
	Cantiga GMCH(1/6)-GTL		
Size C	Document Number KIWAX_LA-5082P		Rev 0.4
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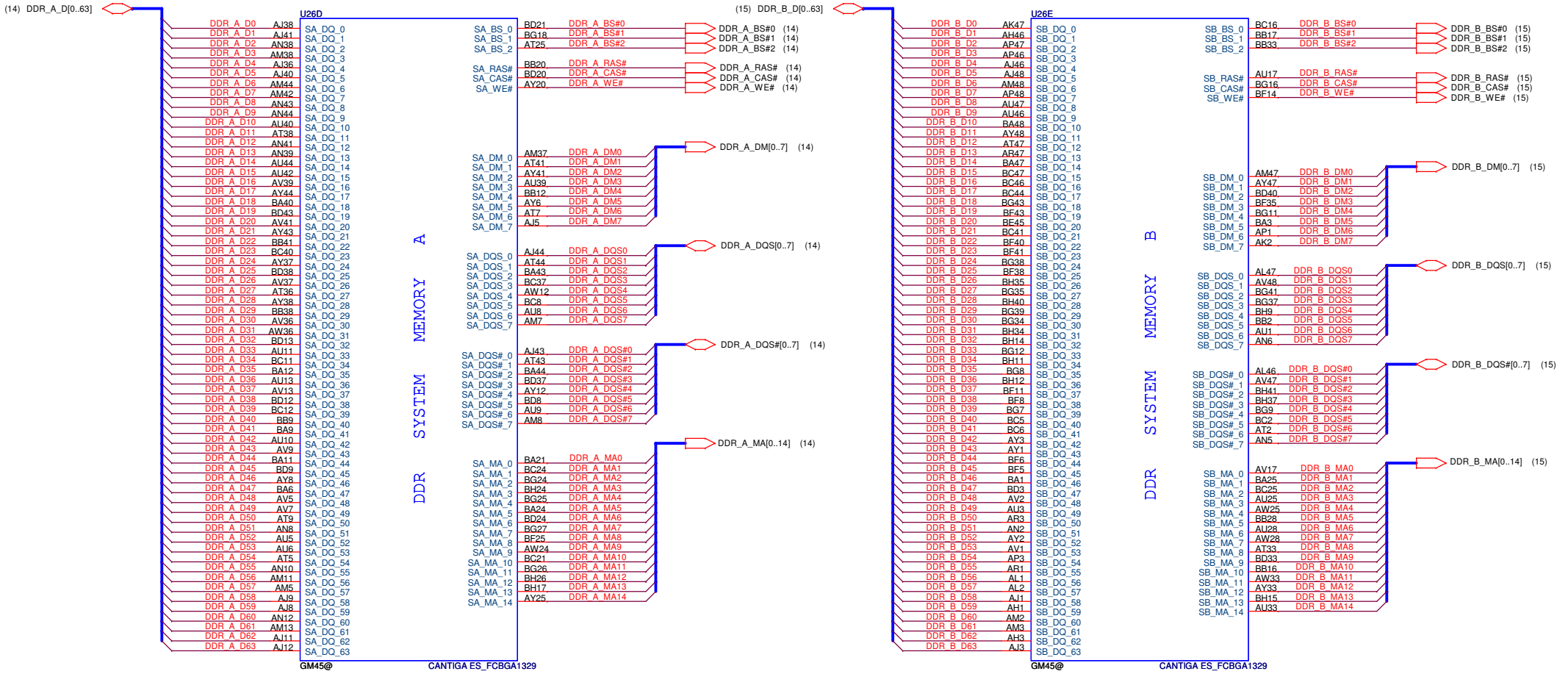


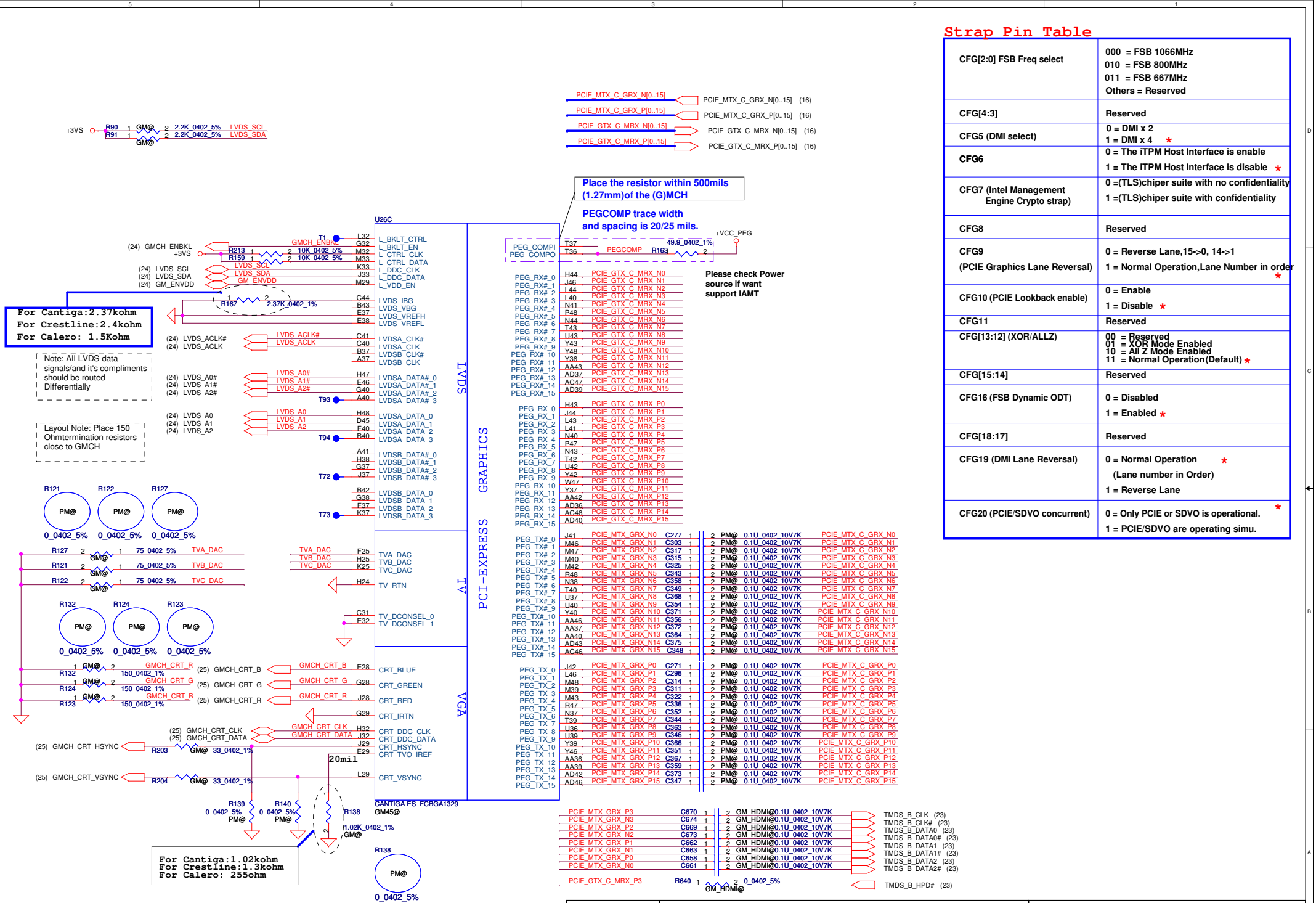
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 Sheet 9 of 53



Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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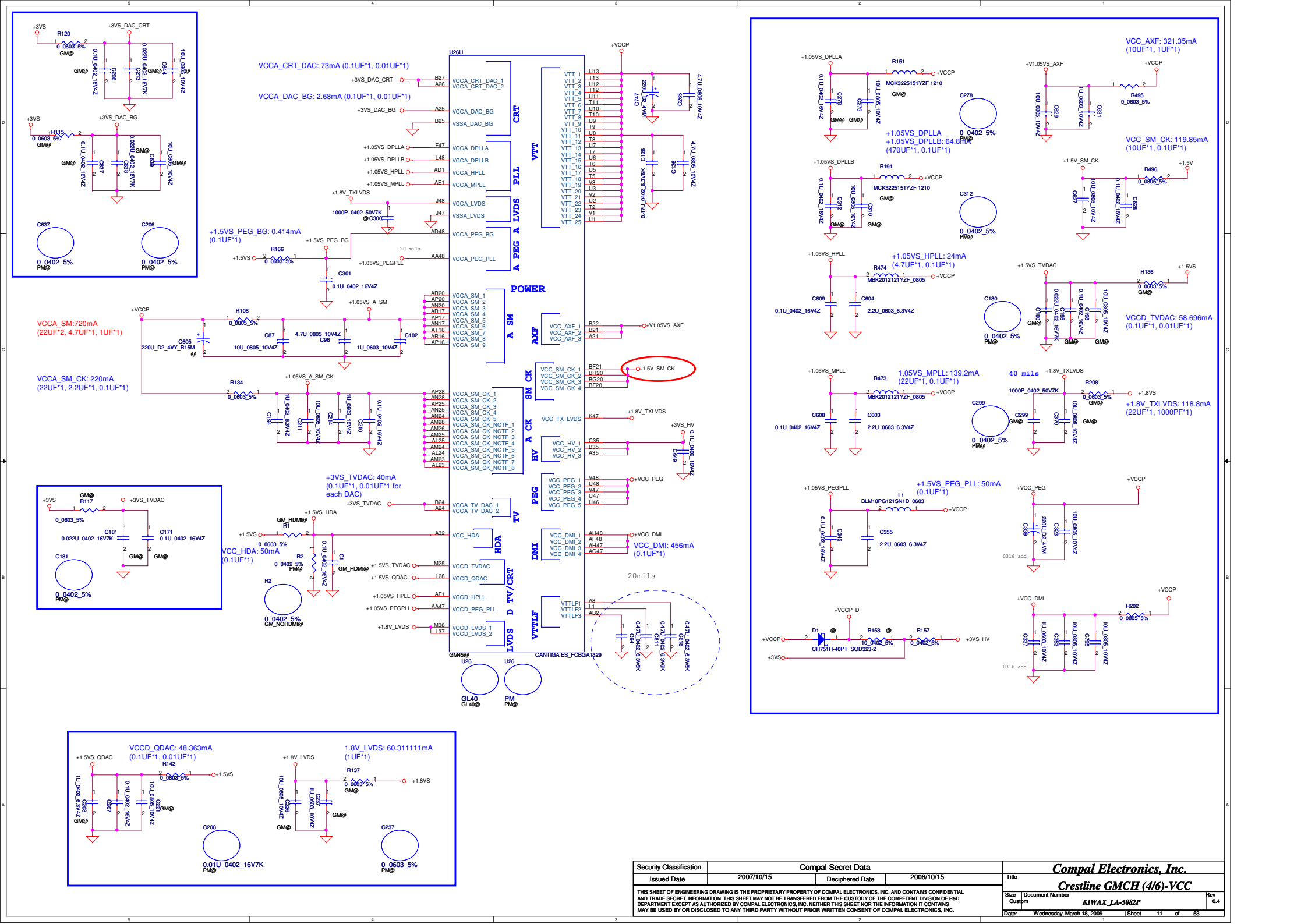
Title: **Cantiga GMCH (3/6)-VGA/LVDS/TV**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 | Sheet 10 of 53



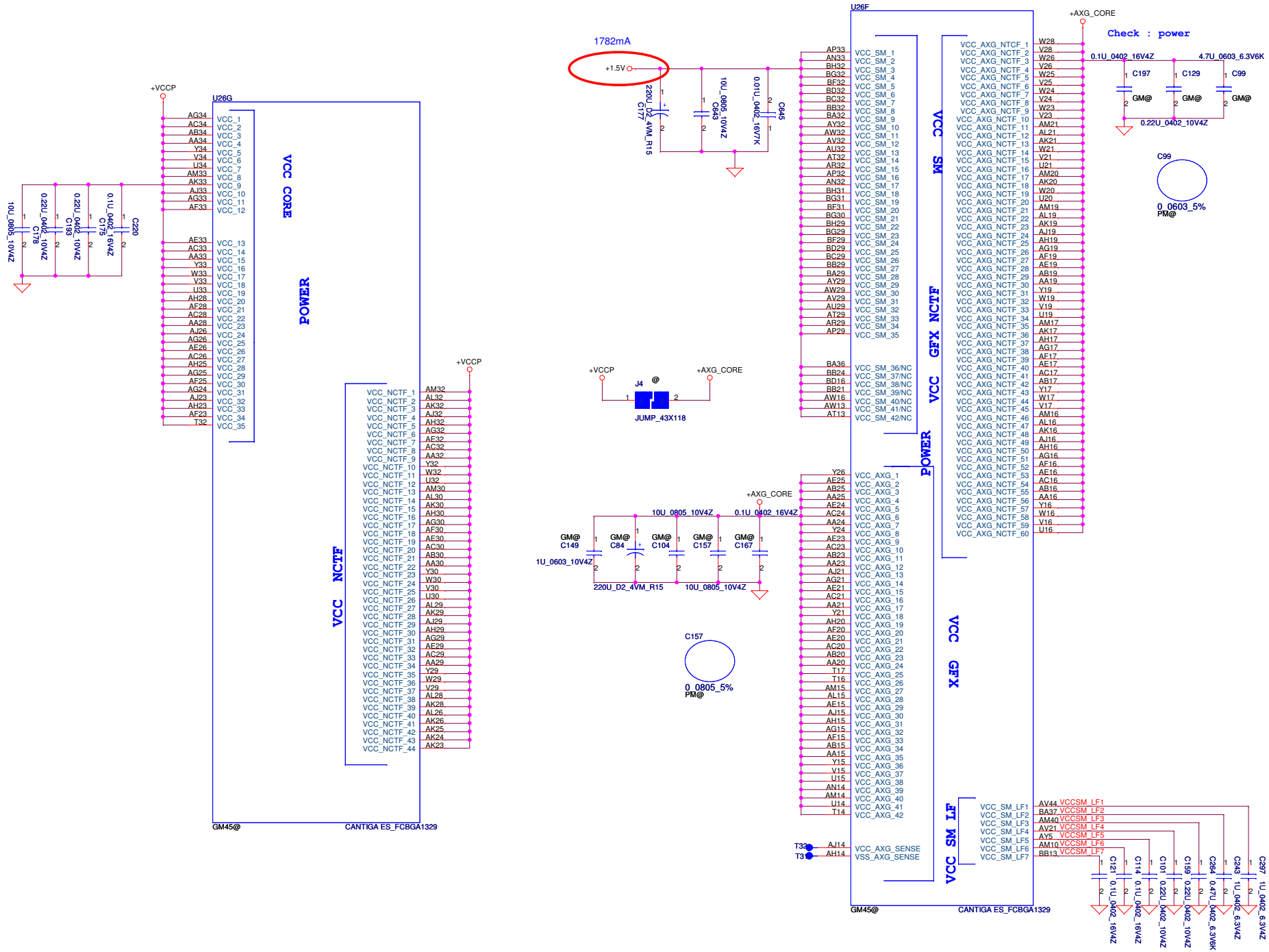
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (4/6)-VCC**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 | Sheet 11 of 53



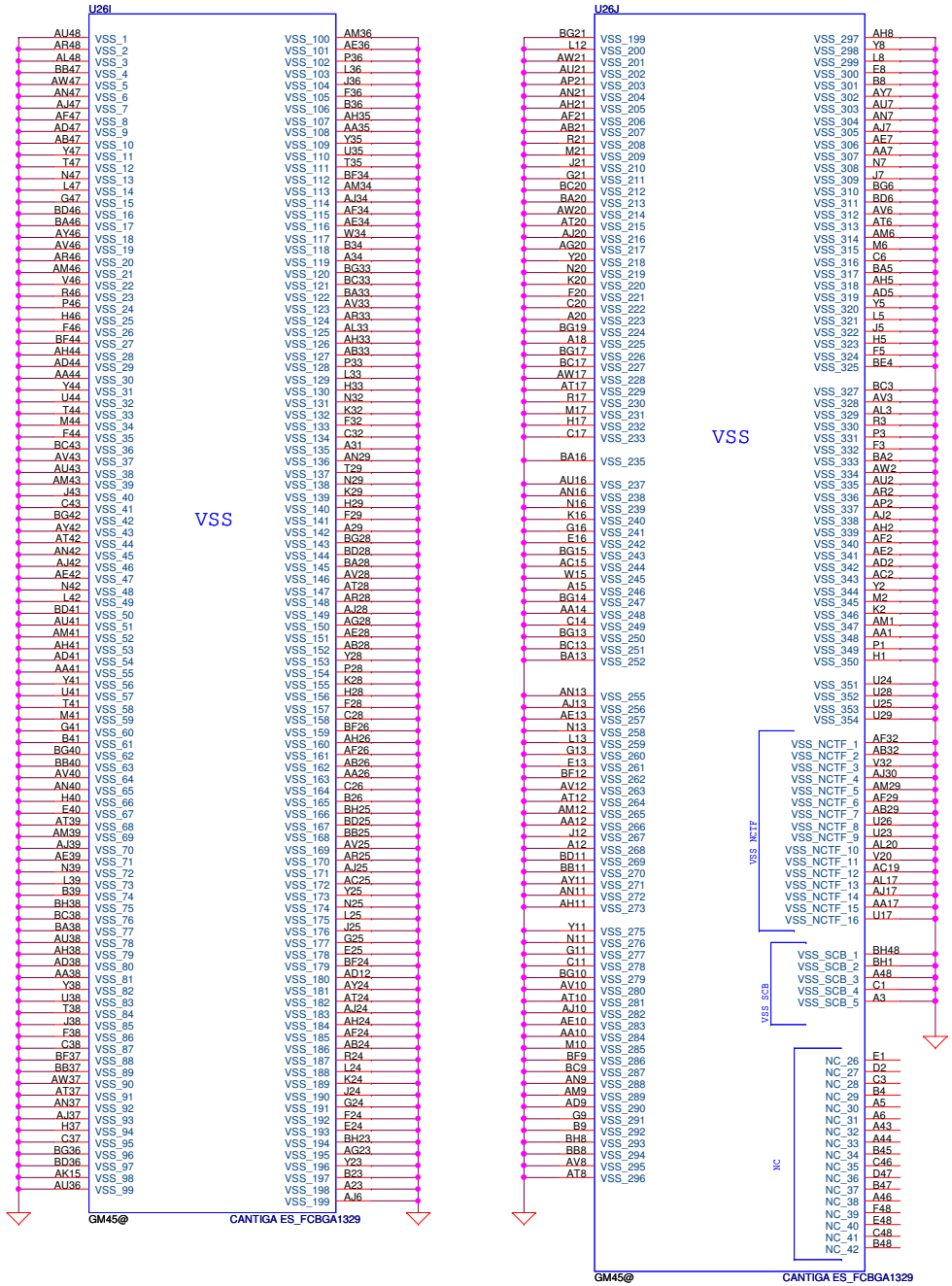
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 | Sheet 12 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
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(9) DDR_A_DQS#[0..7]
(9) DDR_A_D[0..63]
(9) DDR_A_DM[0..7]
(9) DDR_A_DQS[0..7]
(9) DDR_A_MA[0..14]

+1.5V
R625 100_0402_1%
+V_DDR3_DIMM_REF
R626 100_0402_1%
C755 0.1U_0402_16V4Z

Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C761 10U_0805_6.3V6M
C760 10U_0805_6.3V6M
C767 10U_0805_6.3V6M
C763 10U_0805_6.3V6M
C764 10U_0805_6.3V6M
C765 10U_0805_6.3V6M
C766 10U_0805_6.3V6M
C750 0.1U_0402_16V4Z
C752 0.1U_0402_16V4Z
C749 0.1U_0402_16V4Z
C753 0.1U_0402_16V4Z
C787 470U_D2_2.5VM_R15 @

<BOM Structure> <BOM Structure> <BOM Structure> <BOM Structure>

Layout Note:
Place near JP4.203 & JP4.204

+0.75VS
1U_0603_10V4Z C778
1U_0603_10V4Z C779
1U_0603_10V4Z C776
1U_0603_10V4Z C777
10U_0805_6.3V6M C762

+1.5V
+V_DDR3_DIMM_REF
JP17

		1	VREF_DQ	VSS1	2	
		3	VSS2	DQ4	4	DDR_A_D4
DDR_A_D0		5	DQ0	DQ5	6	DDR_A_D5
DDR_A_D1		7	DQ1	VSS3	8	
		9	VSS4	DQS#0	10	DDR_A_DQS#0
DDR_A_DM0		11	DM0	DQS0	12	DDR_A_DQS0
		13	VSS5	VSS6	14	
DDR_A_D2		15	DQ2	DQ6	16	DDR_A_D6
DDR_A_D3		17	DQ3	DQ7	18	DDR_A_D7
		19	VSS7	VSS8	20	
DDR_A_D8		21	DQ8	DQ12	22	DDR_A_D12
DDR_A_D9		23	DQ9	DQ13	24	DDR_A_D13
		25	VSS9	VSS10	26	
DDR_A_DQS#1		27	DQS#1	DM1	28	DDR_A_DM1
DDR_A_DQS1		29	DQS1	RESET#	30	SM_DRAMRST#
		31	VSS11	VSS12	32	
DDR_A_D10		33	DQ10	DQ14	34	DDR_A_D14
DDR_A_D11		35	DQ11	DQ15	36	DDR_A_D15
		37	VSS13	VSS14	38	
DDR_A_D16		39	DQ16	DQ20	40	DDR_A_D20
DDR_A_D17		41	DQ17	DQ21	42	DDR_A_D21
		43	VSS15	VSS16	44	
DDR_A_DQS#2		45	DQS#2	DM2	46	DDR_A_DM2
DDR_A_DQS2		47	DQS2	VSS17	48	
		49	VSS18	DQ22	50	DDR_A_D22
DDR_A_D18		51	DQ18	DQ23	52	DDR_A_D23
DDR_A_D19		53	DQ19	VSS19	54	
		55	VSS20	DQ28	56	DDR_A_D28
DDR_A_D24		57	DQ24	DQ29	58	DDR_A_D29
DDR_A_D25		59	DQ25	VSS21	60	
		61	VSS22	DQS#3	62	DDR_A_DQS#3
DDR_A_DM3		63	DM3	DQS3	64	DDR_A_DQS3
		65	VSS23	VSS24	66	
DDR_A_D26		67	DQ26	DQ30	68	DDR_A_D30
DDR_A_D27		69	DQ27	DQ31	70	DDR_A_D31
		71	VSS25	VSS26	72	
(8) DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	73	CKE0	CKE1	74	DDR_CKE1_DIMMA
		75	VDD1	VDD2	76	
(9) DDR_A_BS#2		77	NC1	A15	78	
DDR_A_BS2		79	BA2	A14	80	DDR_A_MA14
		81	VDD3	VDD4	82	
DDR_A_MA12		83	A12/BC#	A11	84	DDR_A_MA11
DDR_A_MA9		85	A9	A7	86	DDR_A_MA7
		87	VDD5	VDD6	88	
DDR_A_MA8		89	A8	A6	90	DDR_A_MA6
DDR_A_MA5		91	A5	A4	92	DDR_A_MA4
		93	VDD7	VDD8	94	
DDR_A_MA3		95	A3	A2	96	DDR_A_MA2
DDR_A_MA1		97	A1	A0	98	DDR_A_MA0
		99	VDD9	VDD10	100	
(8) M_CLK_DDR0	M_CLK_DDR0	101	CK0	CK1	102	M_CLK_DDR1
(8) M_CLK_DDR#0	M_CLK_DDR#0	103	CK0#	CK1#	104	M_CLK_DDR#1
		105	VDD11	VDD12	106	
DDR_A_MA10		107	A10/AP	BA1	108	DDR_A_BS1
(9) DDR_A_BS#0	DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS#
		111	VDD13	VDD14	112	
DDR_A_WE#		113	WE#	S0#	114	DDR_CS0_DIMMA#
(9) DDR_A_CAS#	DDR_A_CAS#	115	CAS#	ODT0	116	M_ODT0
		117	VDD15	VDD16	118	
DDR_A_MA13		119	A13	ODT1	120	M_ODT1
(8) DDR_CS1_DIMMA#	DDR_CS1_DIMMA#	121	S1#	NC2	122	
		123	VDD17	VDD18	124	
		125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA
		127	VSS27	VSS28	128	
DDR_A_D32		129	DQ32	DQ36	130	DDR_A_D36
DDR_A_D33		131	DQ33	DQ37	132	DDR_A_D37
		133	VSS29	VSS30	134	
DDR_A_DQS#4		135	DQS#4	DM4	136	DDR_A_DM4
DDR_A_DQS4		137	DQS4	VSS31	138	
		139	VSS32	DQ38	140	DDR_A_D38
DDR_A_D34		141	DQ34	DQ39	142	DDR_A_D39
DDR_A_D35		143	DQ35	VSS33	144	
		145	VSS34	DQ44	146	DDR_A_D44
DDR_A_D40		147	DQ40	DQ45	148	DDR_A_D45
DDR_A_D41		149	DQ41	VSS35	150	
		151	VSS36	DQS#5	152	DDR_A_DQS#5
DDR_A_DM5		153	DM5	DQS5	154	DDR_A_DQS5
		155	VSS37	VSS38	156	
DDR_A_D42		157	DQ42	DQ46	158	DDR_A_D46
DDR_A_D43		159	DQ43	DQ47	160	DDR_A_D47
		161	VSS39	VSS40	162	
DDR_A_D48		163	DQ48	DQ52	164	DDR_A_D52
DDR_A_D49		165	DQ49	DQ53	166	DDR_A_D53
		167	VSS41	VSS42	168	
DDR_A_DQS#6		169	DQS#6	DM6	170	DDR_A_DM6
DDR_A_DQS6		171	DQS6	VSS43	172	
		173	VSS44	DQ54	174	DDR_A_D54
DDR_A_D50		175	DQ50	DQ55	176	DDR_A_D55
DDR_A_D51		177	DQ51	VSS45	178	
		179	VSS46	DQ60	180	DDR_A_D60
DDR_A_D56		181	DQ56	DQ61	182	DDR_A_D61
DDR_A_D57		183	DQ57	VSS47	184	
		185	VSS48	DQS#7	186	DDR_A_DQS#7
DDR_A_DM7		187	DM7	DQS7	188	DDR_A_DQS7
		189	VSS49	VSS50	190	
DDR_A_D58		191	DQ58	DQ62	192	DDR_A_D62
DDR_A_D59		193	DQ59	DQ63	194	DDR_A_D63
		195	VSS51	VSS52	196	
		197	SA0	EVENT#	198	PM_EXTTS#0
		199	VDDSPD	SDA	200	CLK_SMBDATA
		201	SA1	SCL	202	CLK_SMBCLK
		203	VTT1	VTT2	204	+0.75VS
		205	G1	G2	206	

FOX_AS0A626-U2RN-7F
ME@

SM_DRAMRST# (8,15)
DDR_CKE1_DIMMA (8)
M_CLK_DDR1 (8)
M_CLK_DDR#1 (8)
DDR_A_BS#1 (9)
DDR_A_RAS# (9)
DDR_CS0_DIMMA# (8)
M_ODT0 (8)
M_ODT1 (8)
PM_EXTTS#0 (8,15)
CLK_SMBDATA (15,22)
CLK_SMBCLK (15,22)

+V_DDR3_DIMM_REF
R623 0_0402_5%
C785 2.2U_0603_6.3V4Z
C751 0.1U_0402_16V4Z

+3VS
R627 10K_0402_5%
C784 2.2U_0603_6.3V4Z
C754 0.1U_0402_16V4Z
R628 10K_0402_5%

DDR3 SO-DIMM A REVERSE

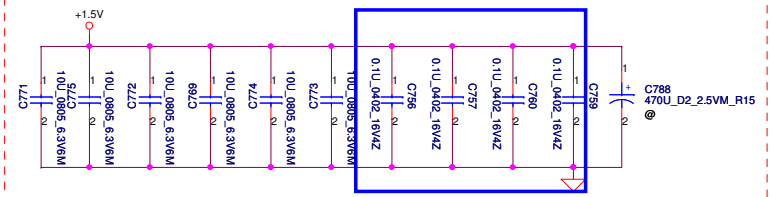
Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT1			
Size: Custom	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 14 of 53		

(9) DDR_B_DQS#[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_DM[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_MA[0..14]

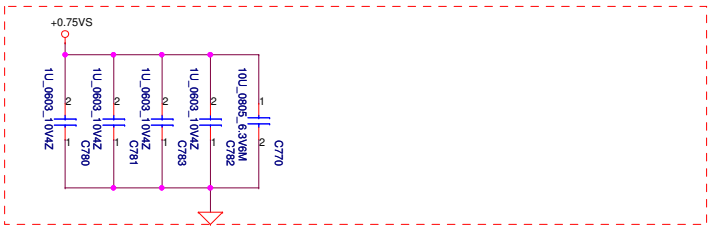
Layout Note:
Place near JP5

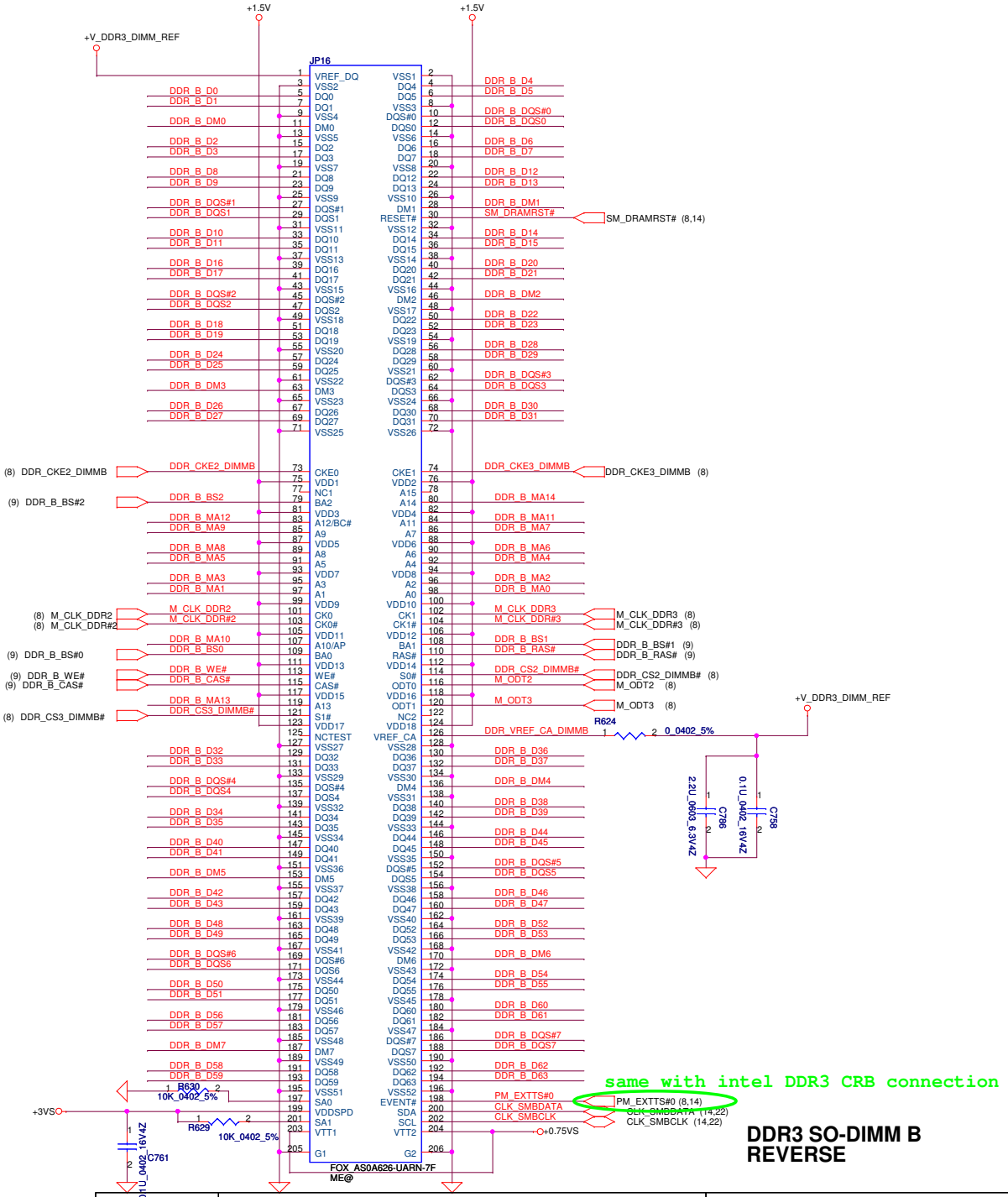
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



<BOM Structure> <BOM Structure> <BOM Structure> <BOM Structure>

Layout Note:
Place near JP5.203 & JP5.204





same with intel DDR3 CRB connection

DDR3 SO-DIMM B
REVERSE

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT2			
Size	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 15 of 53		

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10,12
1	1	1.20V	0
0	1	1.09V	8

	Device ID
NB9M-GS	0x06E9
N10M-GE1-S (55nm)	0x6EC

For N10M 40NM

U59A

Part 1 of 5

NB9M-GS_BGA533

PM@

CRT OUT

EMI

If External Spread Spectrum not stuff than stuff resistor

External Spread Spectrum

Security Classification	Compal Secret Data
Issued Date	2007/10/15
Deciphered Date	2008/10/15

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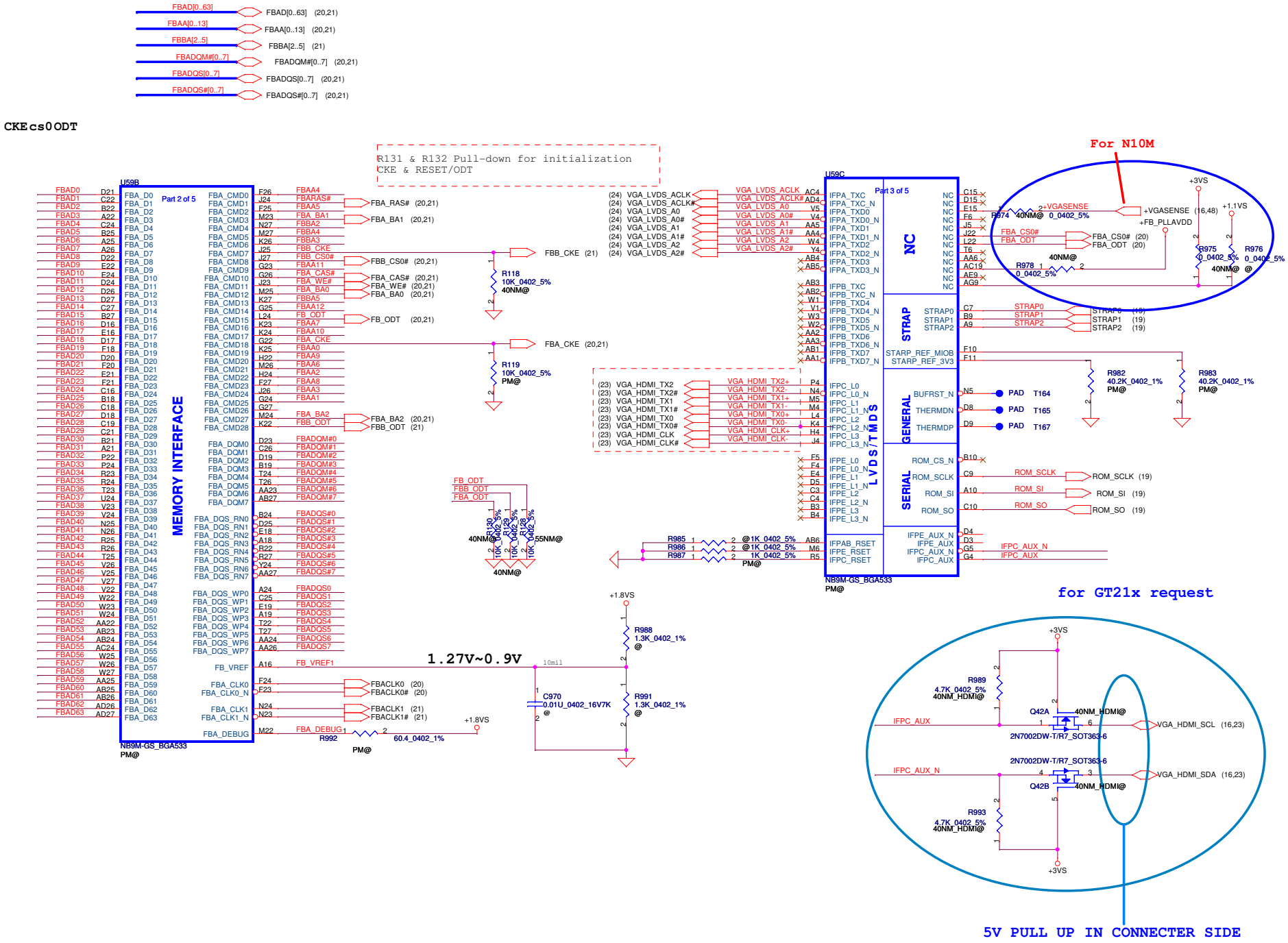
Compal Electronics, Inc.

Title: N10M PCIE,LVDS,GPIO,CLK

Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 16 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: N10M Memory			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 17 of 53		

FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS

+VGA_CORE
13.56A
NEAR BALL
0.1U_0402_16V4Z
0.47U_0402_6.3V6K
220U_D2_4VM
C977 C978 C979 C980 C981 C982 C983
C990 C991 C992 C993 C994 C995
PM@

4.7U 6.3V K X5R 0603
C1001 C1002 PM@
NEAR BGA

+3VS
NEAR BGA
80mA
C1011 C1012 C1013 PM@
1U_0603_10V4Z
NEAR BALL

U59D
Part 4 of 5
POWER
VDD
VDD33
FBVDDQ
PEX_IOVDDQ
PEX_IOVDD
PEX_PLLVDD
VID_PLLVDD
SP_PLLVDD
PLLVDD
FB_PLLAVDD
FB_DLLAVDD
DACA_VDD
DACB_VDD
DACC_VDD
IFPA_IOVDD
IFPB_IOVDD
IFPC_IOVDD
IFPE_IOVDD
IFPAB_PLLVDD
IFPC_PLLVDD
IFPE_PLLVDD
FB_CAL_PD_VDDQ
NB9M-GS_BGA533
PM@

PLACE NEAR BGA
+1.8VS
0.022U_0402_16V7K
0.1U_0402_16V4Z
4.7U 6.3V K X5R 0603
C971 C972 C973 C974 C975 C976
PM@

PLACE BELOW GPU
FBAVDDQ=2.24A
4700P_0402_25V7K
0.022U_0402_16V7K
1U_0603_10V4Z
C984 C985 C986 C987 C988 C989
C996 C997 C998 C999 C1000

0.1U_0402_16V4Z
0.47U_0402_6.3V6K
1U_0402_6.3V4Z
C1003 C1004 C1005 C1006 C1007
NEAR BALL

PEX_IOVDDQ=1.6A
PEX_IOVDD=500mA
PEX_PLLVDD=100mA
10U_0805_10V4Z
C1008 C1009 C1010

+PEX_PLLVDD
+1.1VS_PLL
12~16mil
MBK1608121YZF_0603
L27
C1014 C1015 C1016 C1017 C1018
NEAR BALL
PLLVDD=65mA
SP_PLLVDD=25mA
VID_PLLVDD=50mA

+IFPA_IOVDD
+IFPB_IOVDD
+IFPC_IOVDD
+IFPAB_PLLVDD
+IFPC_PLLVDD
10K_0402_5%
R994 R997
12~16mil
L28 L31
4700P_0402_25V7K
470P_0402_50V7K
C1019 C1020 C1021 C1025 C1026 C1027
110mA
NEAR BGA
NEAR BALL

+FB_PLLAVDD
+FB_DLLAVDD
+DACA_VDD
+DACB_VDD
+DACC_VDD
R995 R996
10K_0402_5%
R998 30.1_0402_1%

+PEX_PLLVDD
L32
C1028 C1029 C1030 C1031
0.01U_0402_16V7K
NEAR BALL
NEAR BGA

+FB_PLLAVDD
+FB_DLLAVDD
L30 L34
C1022 C1023 C1024 C1032 C1033 C1034
0.01U_0402_16V7K
4.7U 6.3V K X5R 0603

IFPC_PLLVDD: please add option to support
both 1.8V (for G9X) and 3.3V(for GT21X)
L35 L37 L40
55NM_HDMI@
40NM_HDMI@
PM_HDMI@
C1035 C1036 C1042 C1043 C1044
PM_HDMI@
C1036
0 0402 5%
PM_NOHDMI@
C1044
NEAR BGA
NEAR BALL

260mA NEAR BGA
L36
MBK1608121YZF_0603
55NM@
L39
40NM@
C1037 C1038
NEAR BALL
IFPAB_PLLVDD: please add option to support
both 1.8V(for G9X) and 1.05V(for GT21X)

R996
37.4_0402_1%
40NM@

+DACA_VDD
110mA
L38
C1039 C1040 C1041
470P_0402_50V7K

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

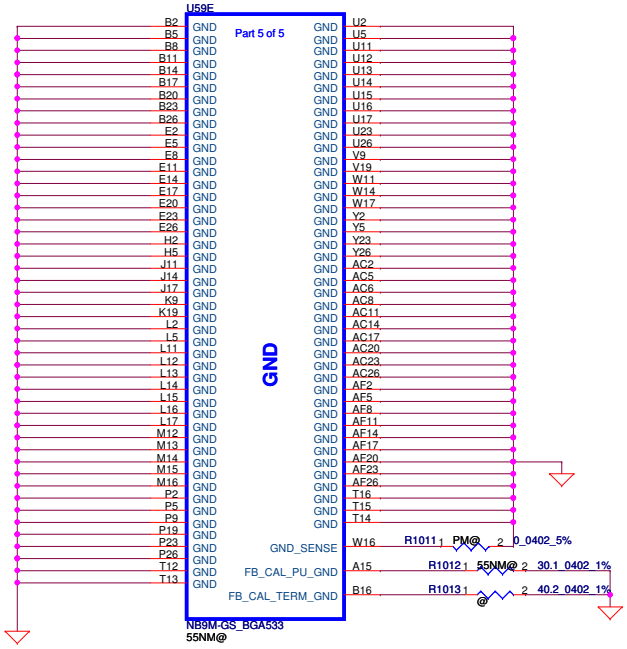
Compal Electronics, Inc.

Title: NB10M Power

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 18 of 53

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available

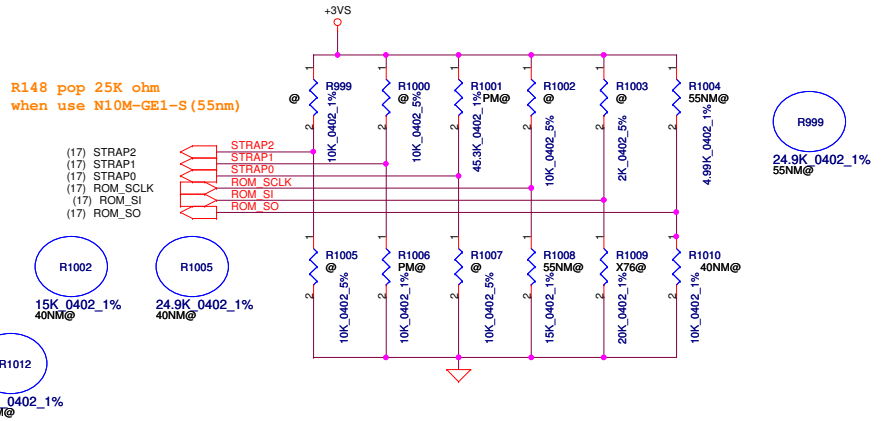


Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)

U59
NB10M-GS-S
40NM@

R148 pop 25K ohm
when use N10M-GE1-S(55nm)



GB1 Family GPU Strap Options X76

GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K	PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 5K	PD 10K	PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K	PU 45K

GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 10K	PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

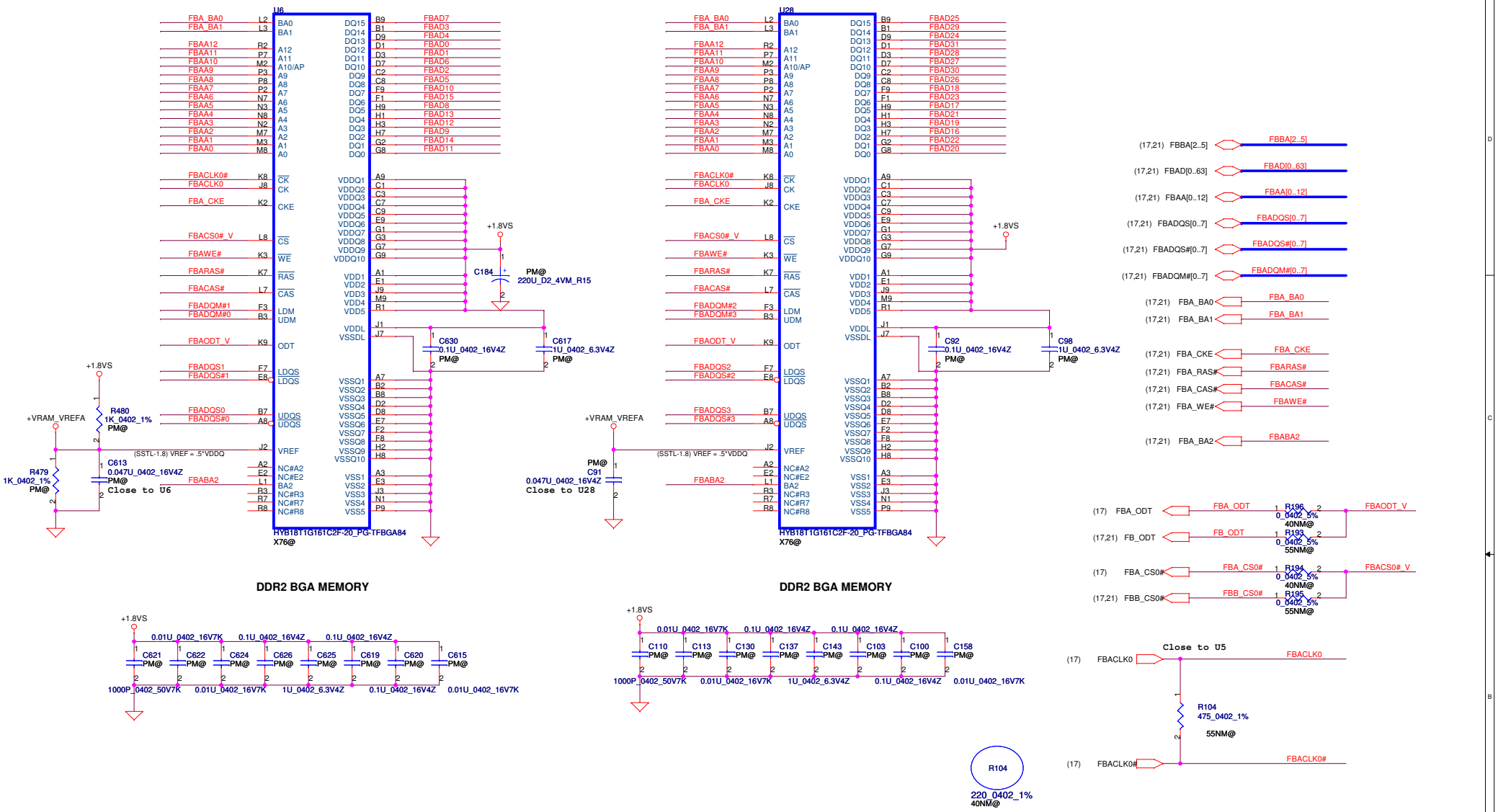
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10M GND & STRAP

Size	Document Number	Rev
B	KIWA5/6 LA-5081P	0.4

Date: Thursday, March 19, 2009 Sheet 19 of 53



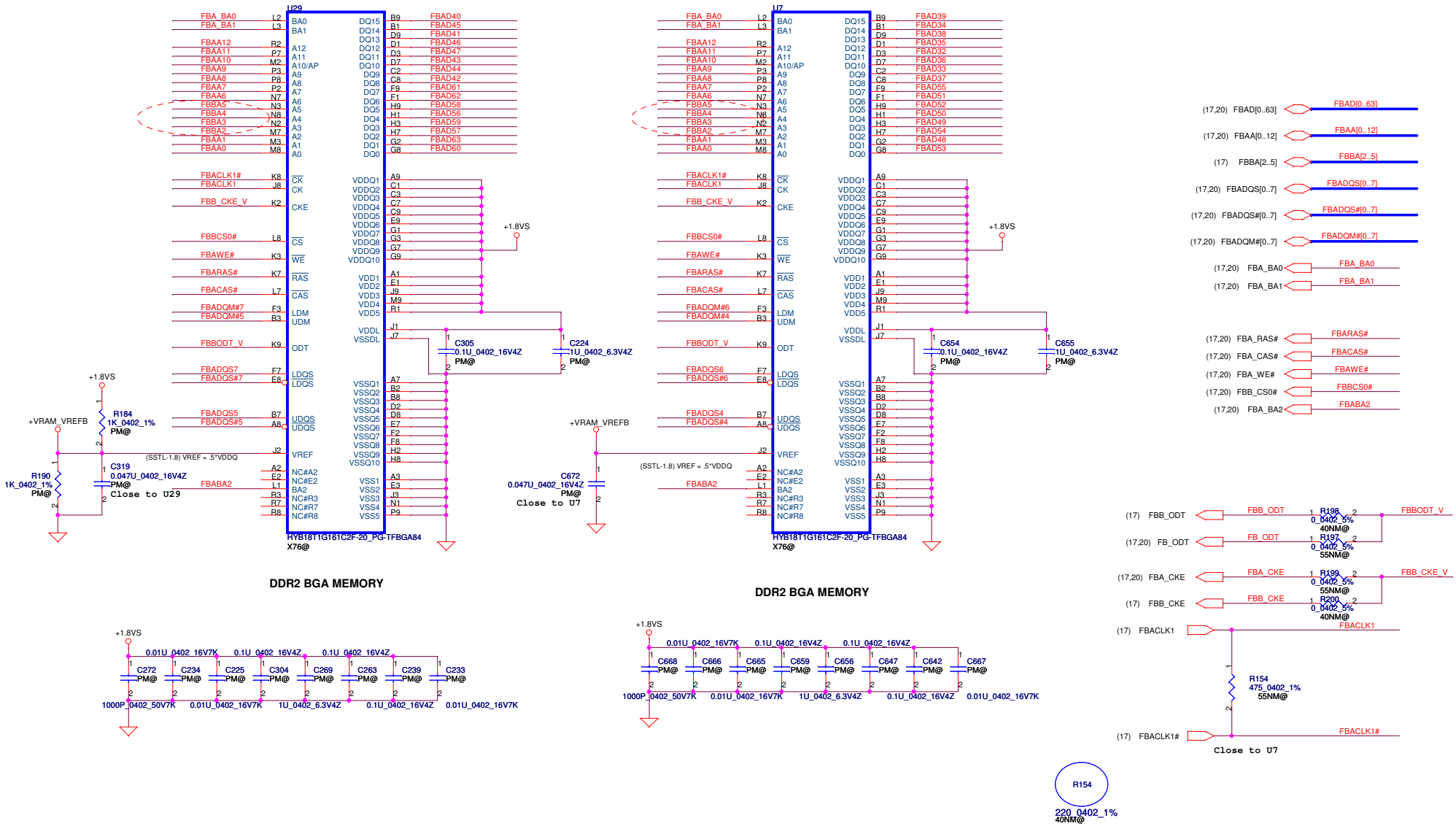
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 20 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDRB**

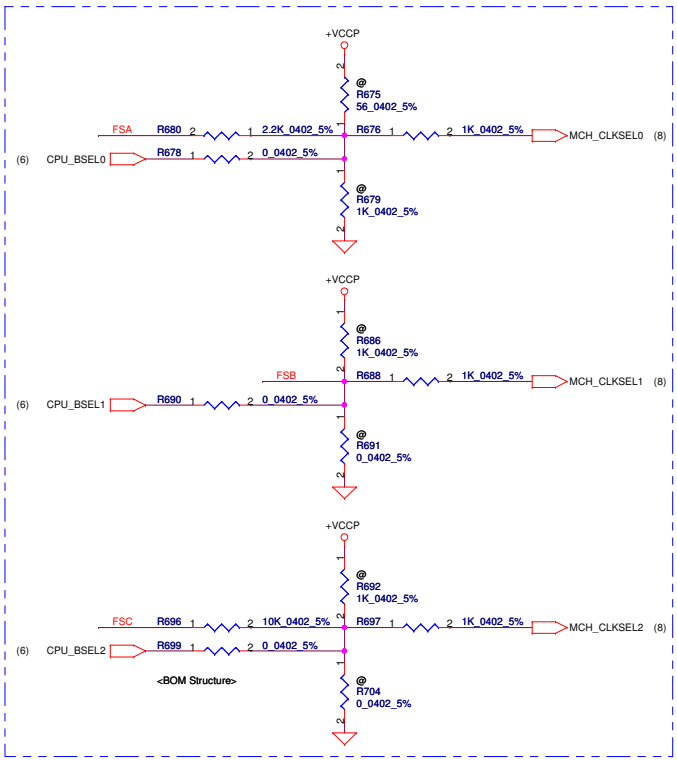
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

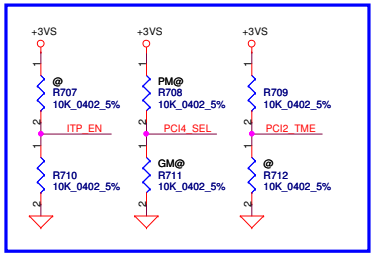
Date: Wednesday, March 18, 2009 | Sheet 21 of 53

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

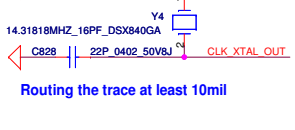
SA000020H00 (ICS : ICS9LPRS387AKLFT)



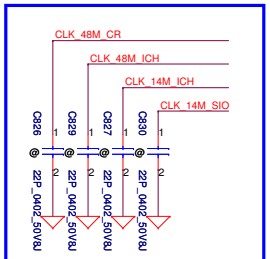


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

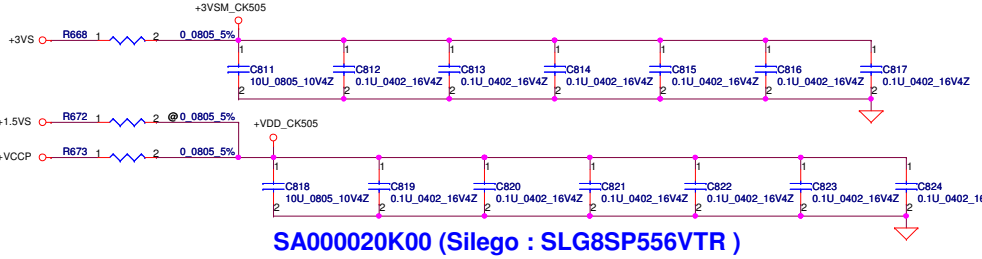
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

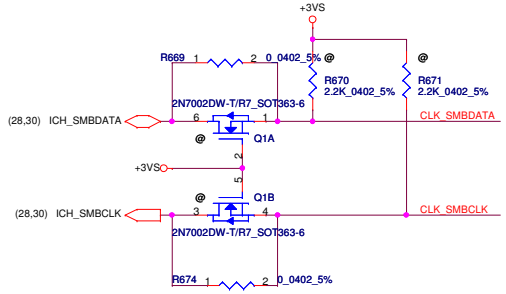


Routing the trace at least 10mil



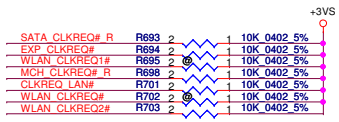
place CAPs near Resistors of U10
For 3G RF noise .





SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: Clock Generator CK505

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 22 of 53

10/30 update PS8171 co-lay circuit

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

For 8171

PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PIO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	ASQ1
PIN12	GND	APD
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD

Reserved for CH7318C

1.2k for CH7318C

TMDS pull down (500ohm) resistors for ATI M92-S2 XT

NEAR CONNECTOR

place those component near JP?
for NV request
0515

U31 PS8101TQFN48G_QFN48_7X7 GM_HDMI@

U31 ASM1442T 1442T@

JHDMI1 SUYIN_100042MR019S153ZL ME@

KIWB3/B4_LA4551P

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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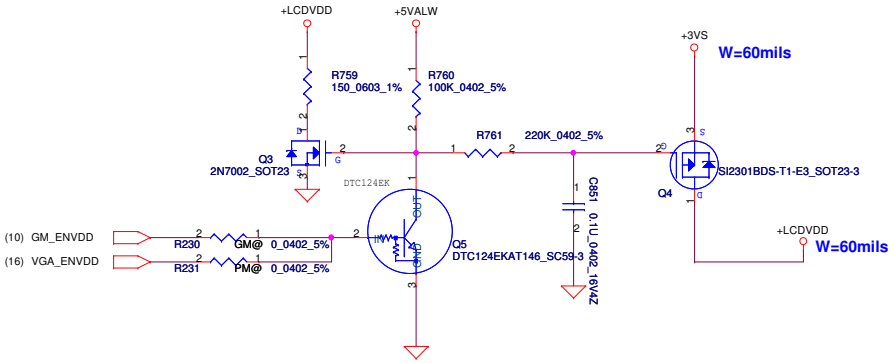
Compal Electronics, Inc.

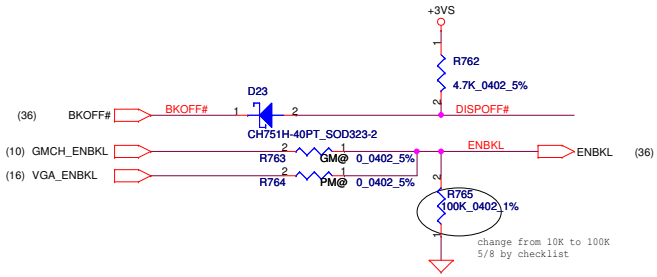
Title: **Level Shiftter_PS8101T**

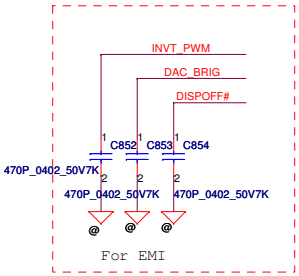
Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 Sheet 23 of 53

LCD POWER CIRCUIT

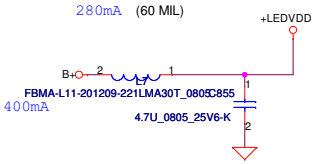


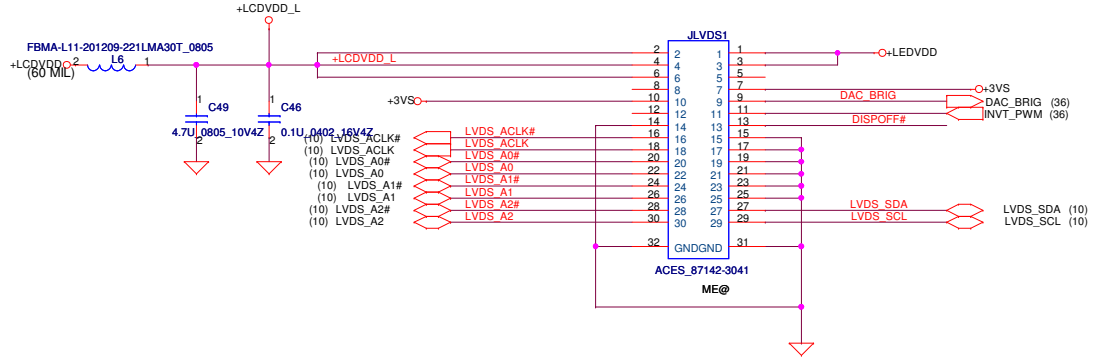


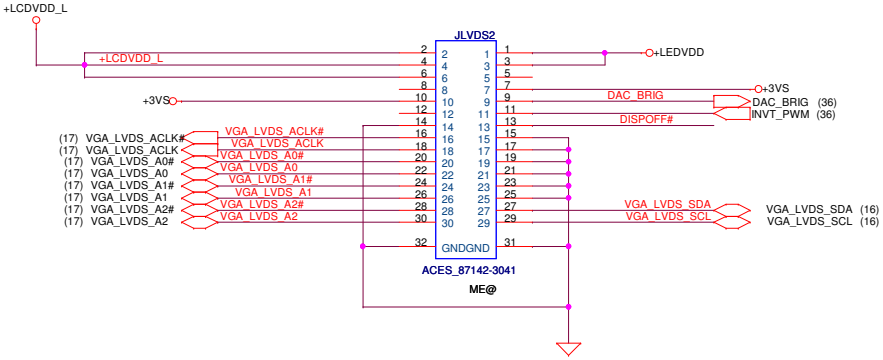


LCD/PANEL BD. Conn. FOR UMA

LCD/PANEL BD. Conn. FOR DIS



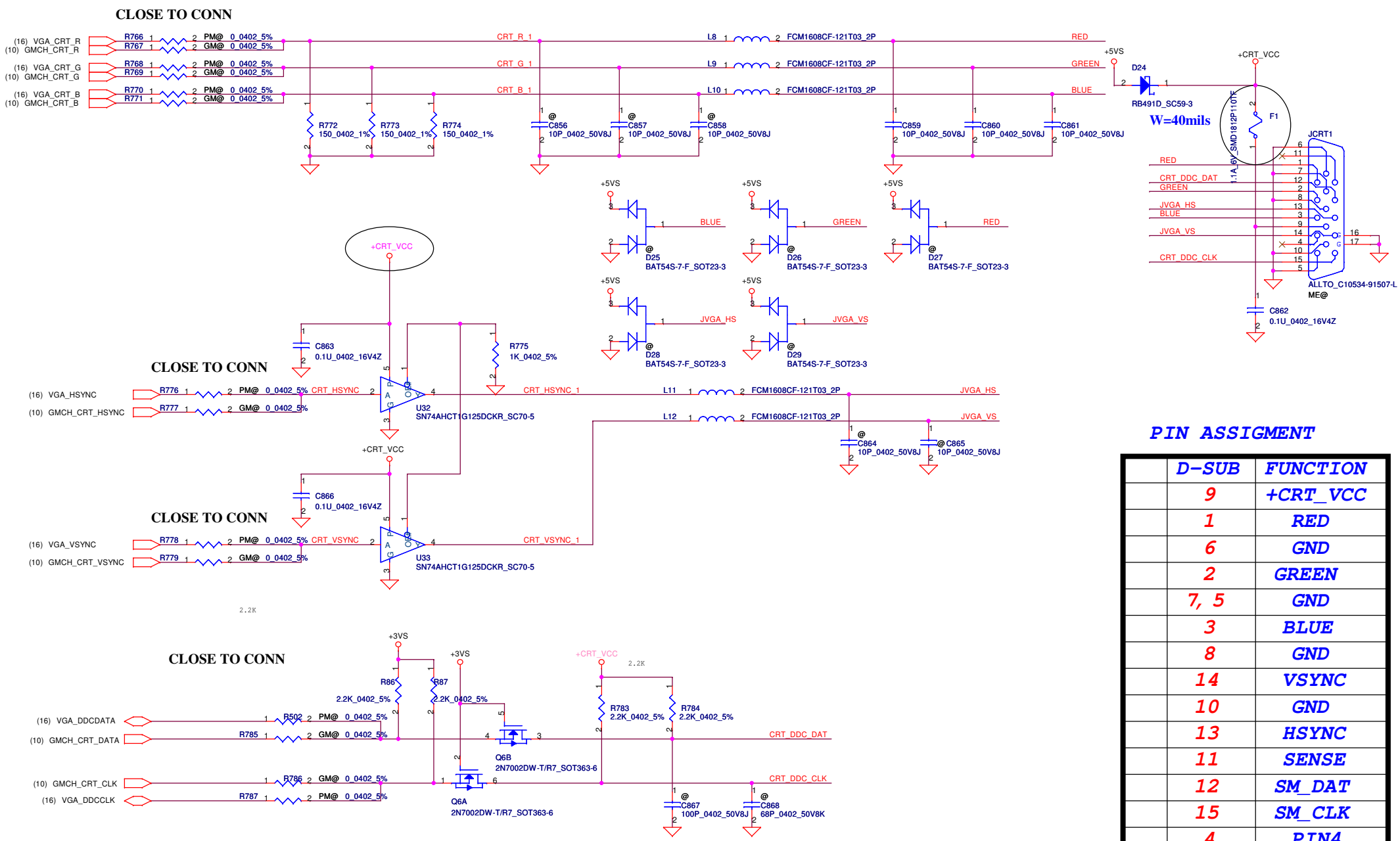




Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	LVDS & DVI Connector		
Size B	Document Number KIWA5/6 LA-5081P		Rev 0.4
Date: Wednesday, March 18, 2009	Sheet 24 of 53		

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

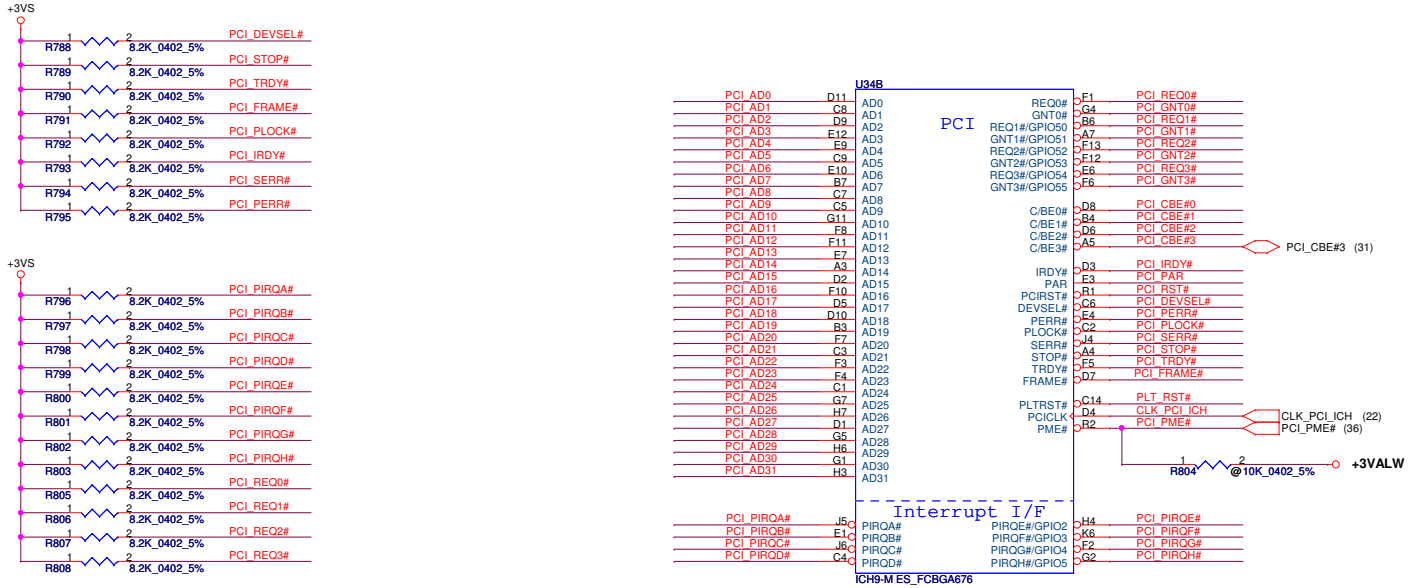
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 25 of 53

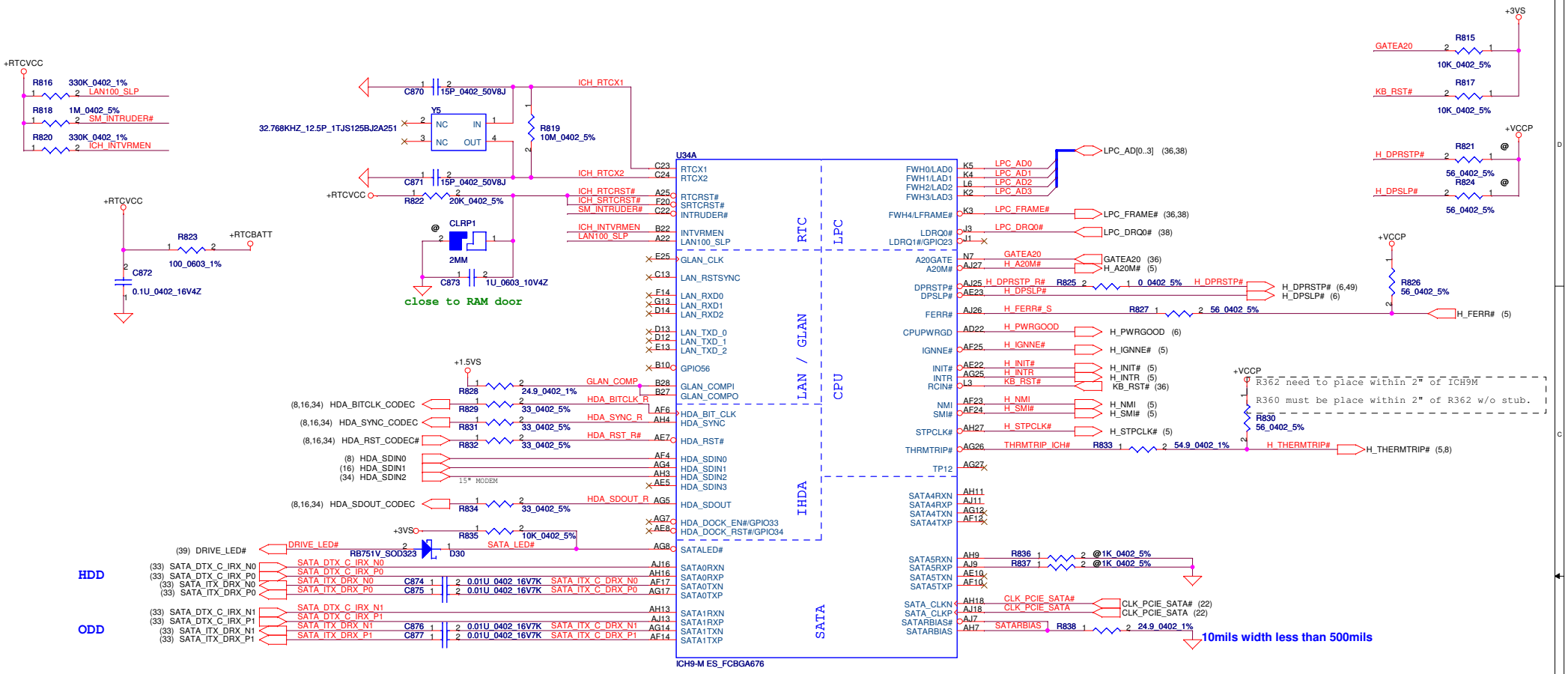


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	ICH9M(1/4)-PCI		
Size	Document Number		Rev
	KIWA5/6 LA-5081P		0.4
Date:	Wednesday, March 18, 2009	Sheet	26 of 53



SATA PORT LIST

PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

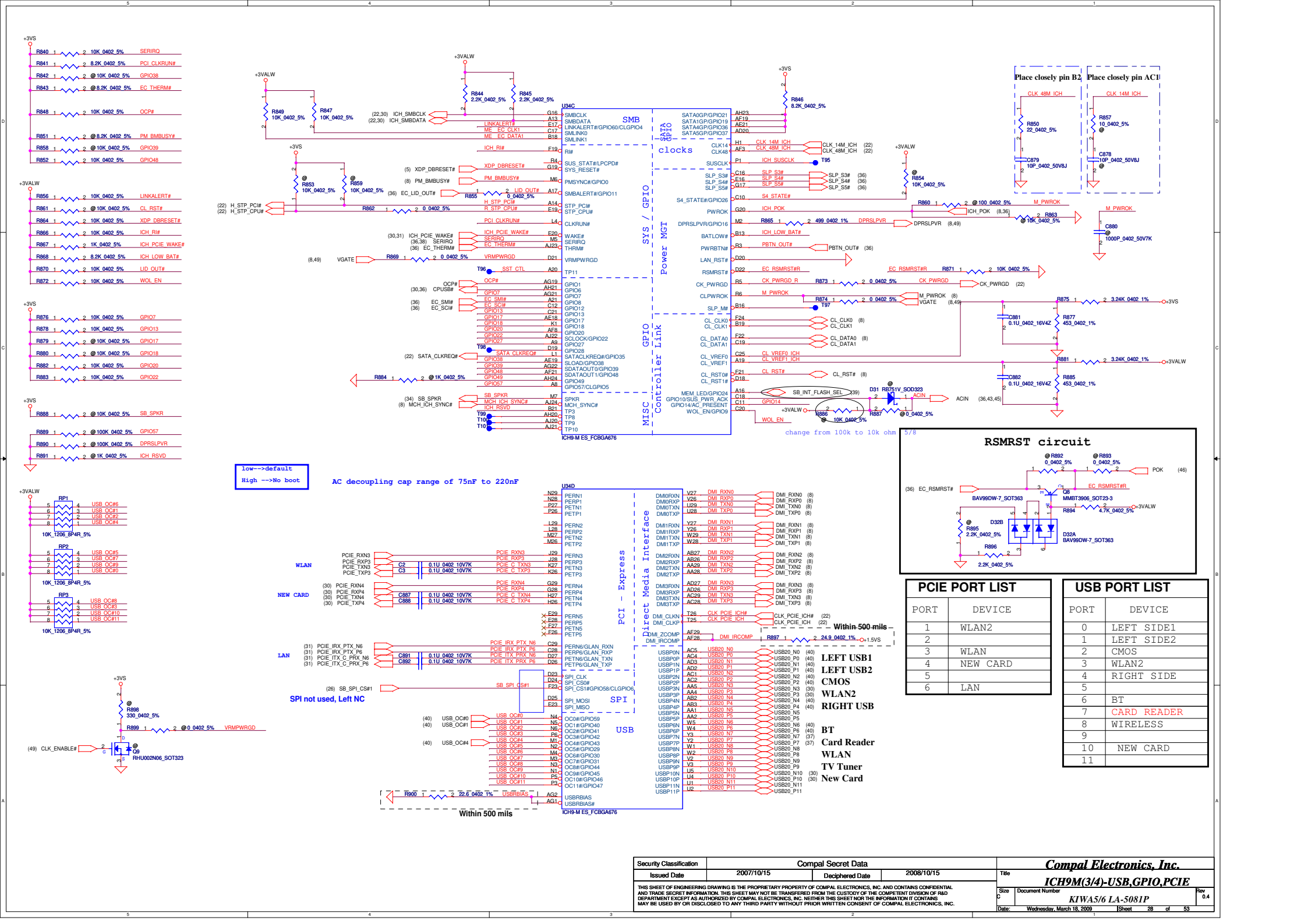
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 27 of 53



PCIE PORT LIST

PORT	DEVICE
1	WLAN2
2	
3	WLAN
4	NEW CARD
5	
6	LAN

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE1
1	LEFT SIDE2
2	CMOS
3	WLAN2
4	RIGHT SIDE
5	
6	BT
7	CARD READER
8	WIRELESS
9	
10	NEW CARD
11	

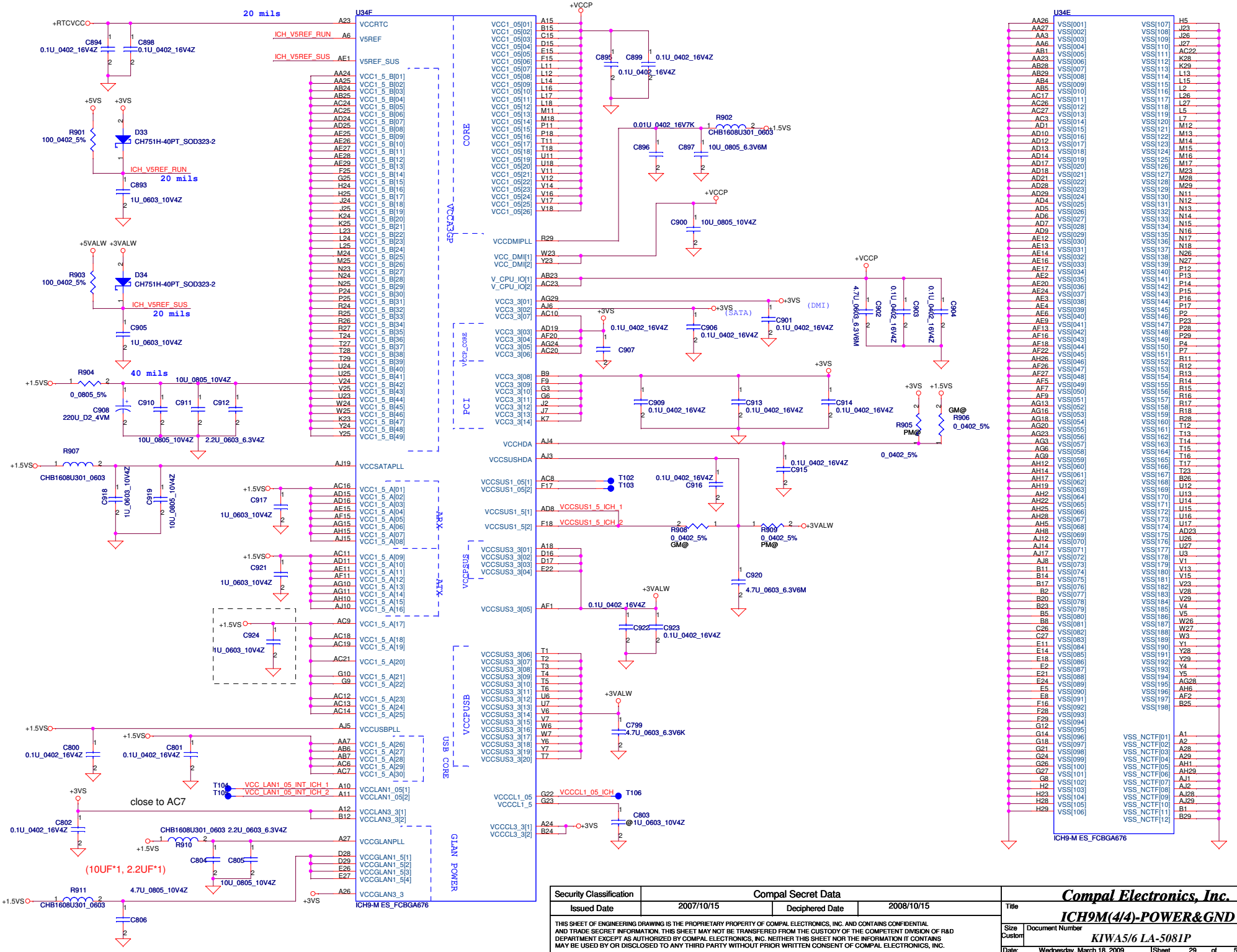
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

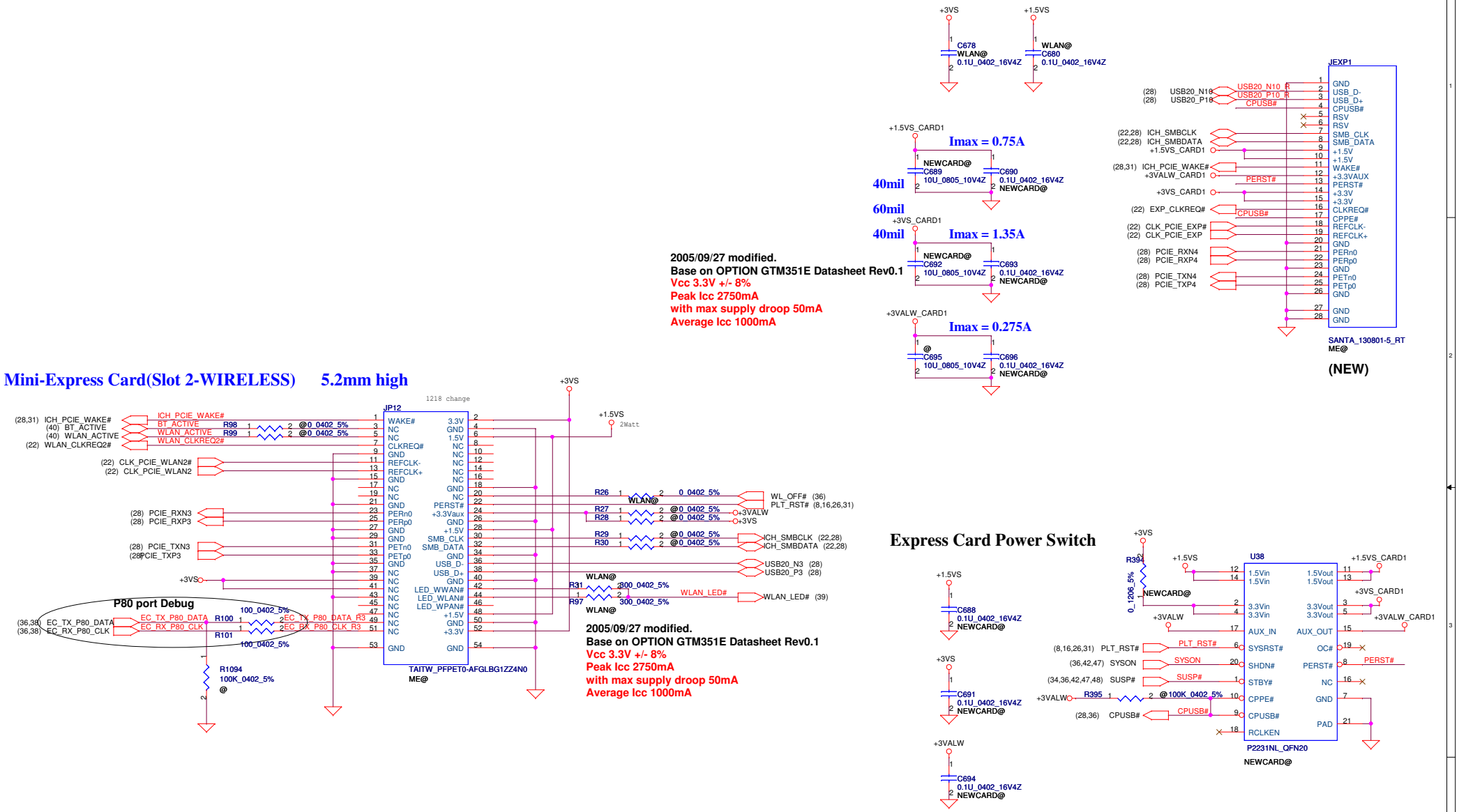
Size	Document Number	Rev
C	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 28 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	ICH9M(4/4)-POWER&GND		
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 29 of 53		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	Mini-Card/3G/TV /BT		
Size	Document Number	KIWAX_LA-5082P	Rev 0.4
Date: Wednesday, March 18, 2009	Sheet 30 of 53		

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : Filter place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

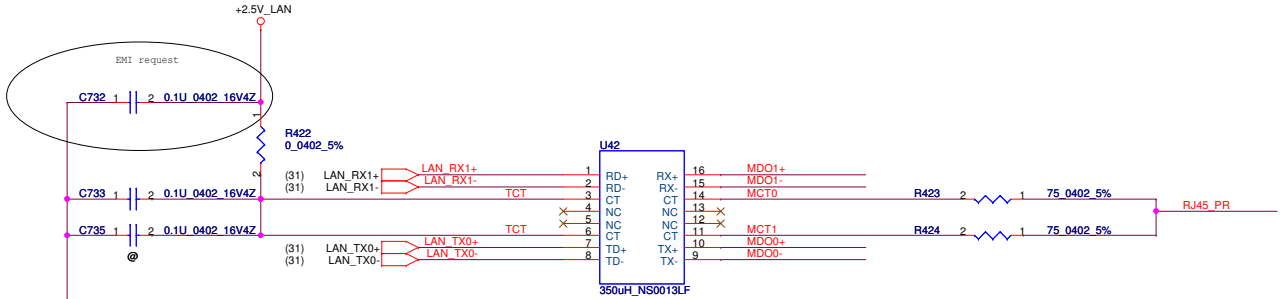
Compal Electronics, Inc.

Title: BCM5787MKML

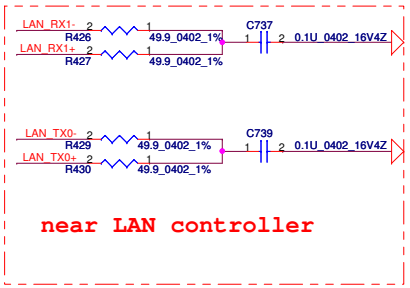
Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

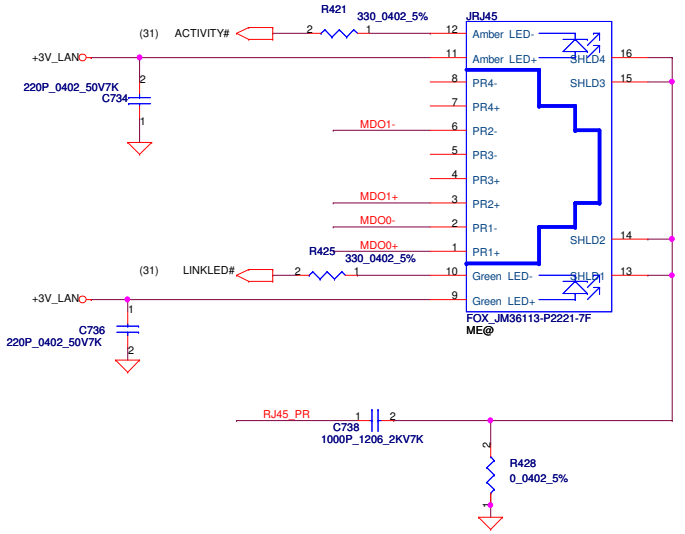
Date: Wednesday, March 18, 2009 | Sheet 31 of 53

RJ45 CONN



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF





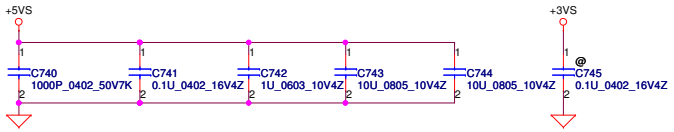
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

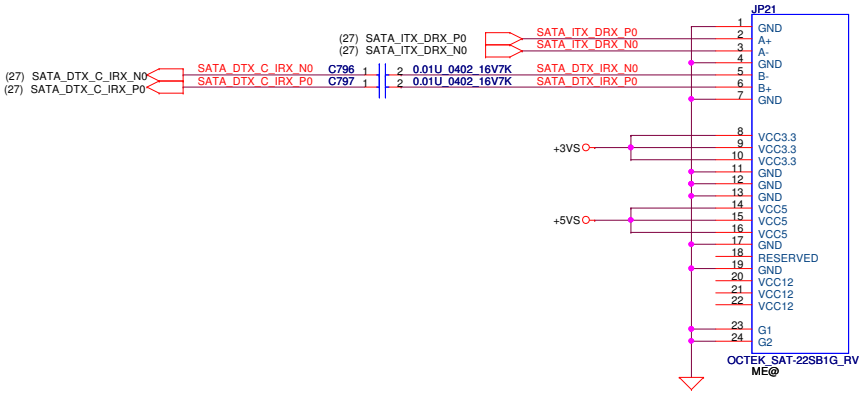
Title: LAN CONTROLLER

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

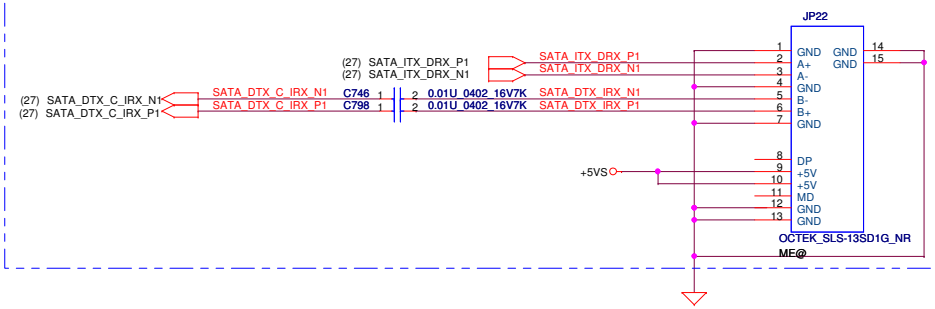
Date: Wednesday, March 18, 2009 | Sheet 32 of 53



SATA HDD Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 33 of 53		

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CX20548
AMOM DAA

11/20 update
PC_BEEP dB control

0216_Change value.

CODEC POWER

(3.33V)
250mW

W=40Mil

2.2kohm for MICL + MICR
4.7kohm for MICL or MICR

external MIC
Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

11/20 update

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

DIGITAL ANALOG

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

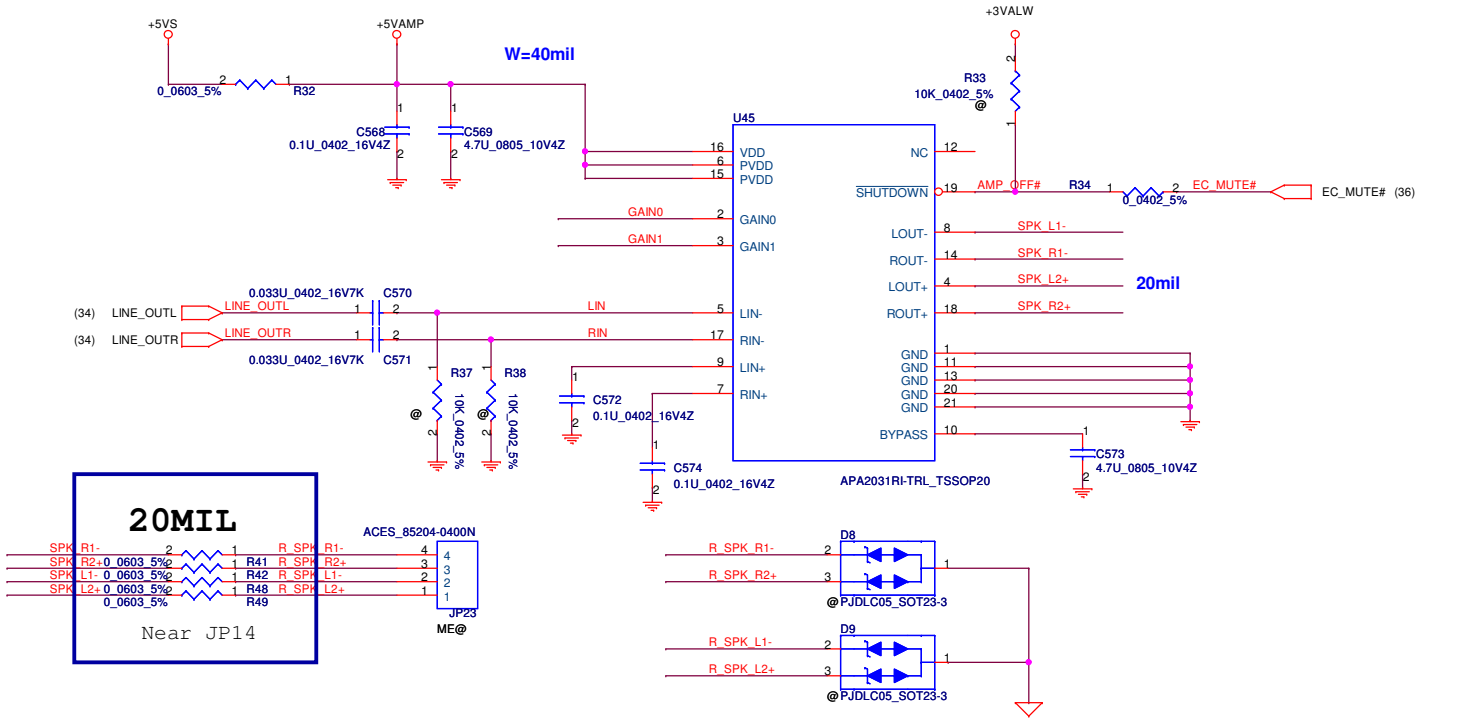
Compal Electronics, Inc.

Title: CX20561-AMOM Codec

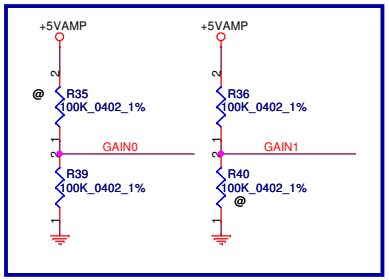
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 34 of 53

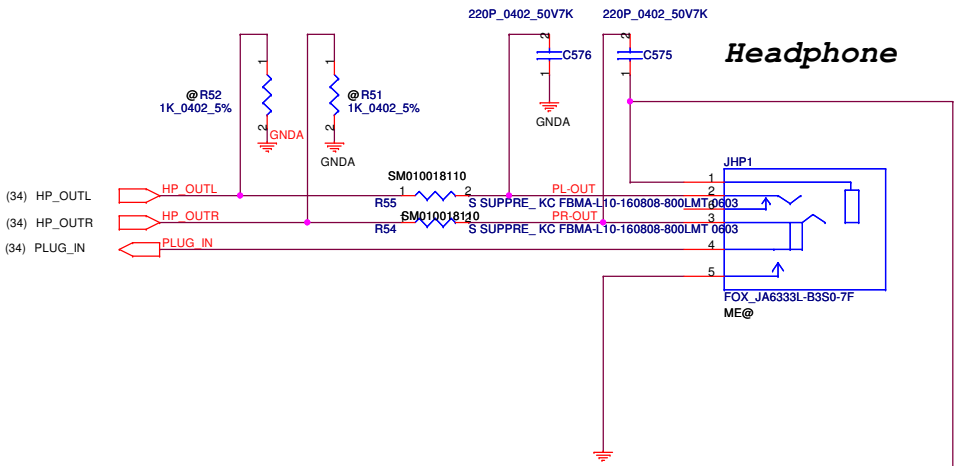
Speaker Connector



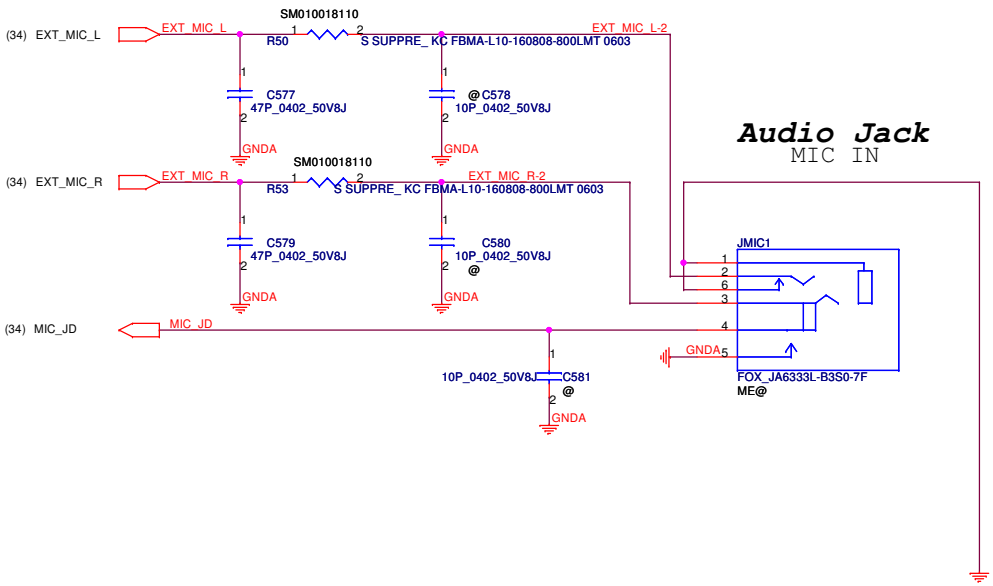
GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Headphone

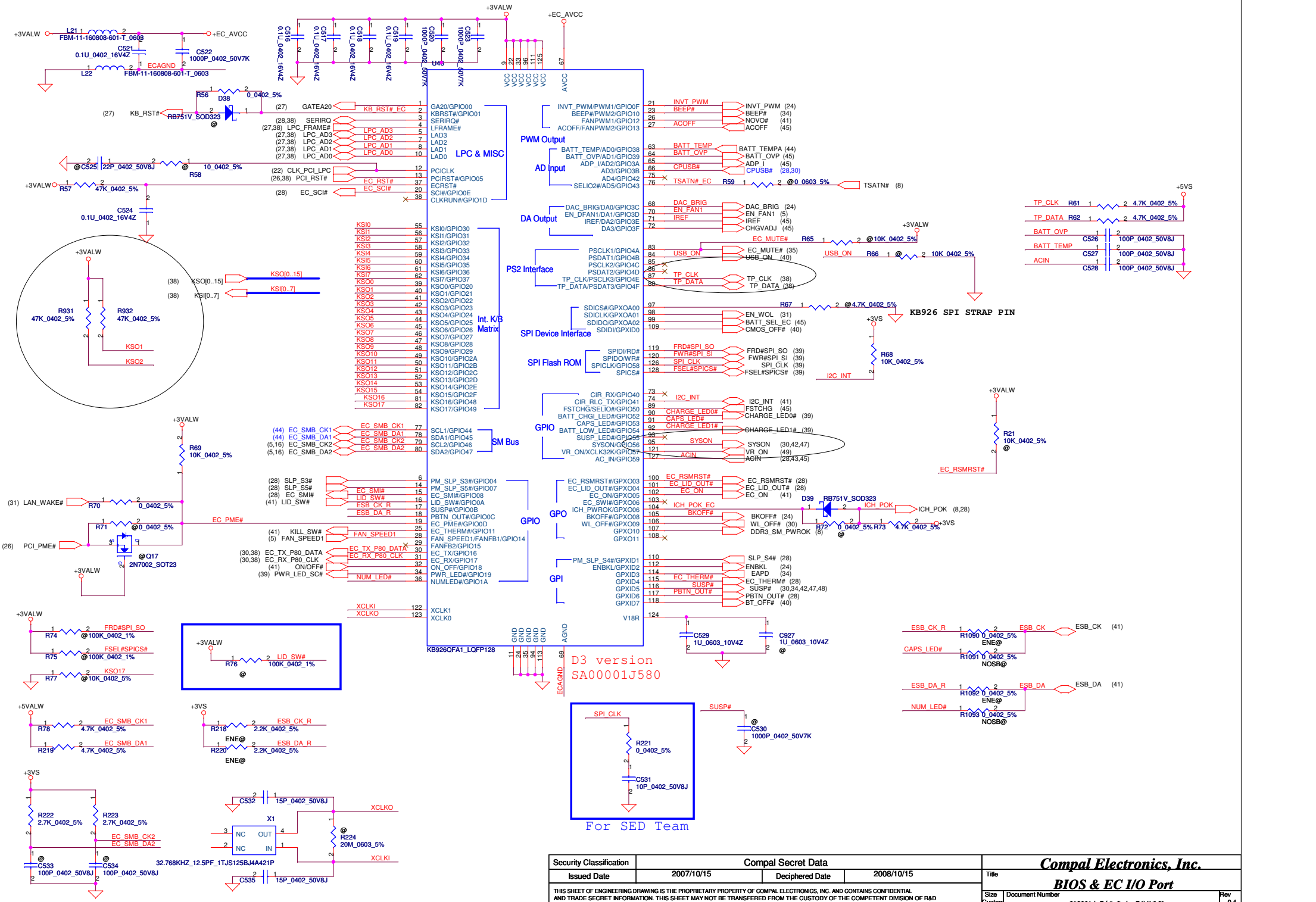


Audio Jack



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.			
Title	AMP,Audio speaker CONN		
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 35 of 53		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

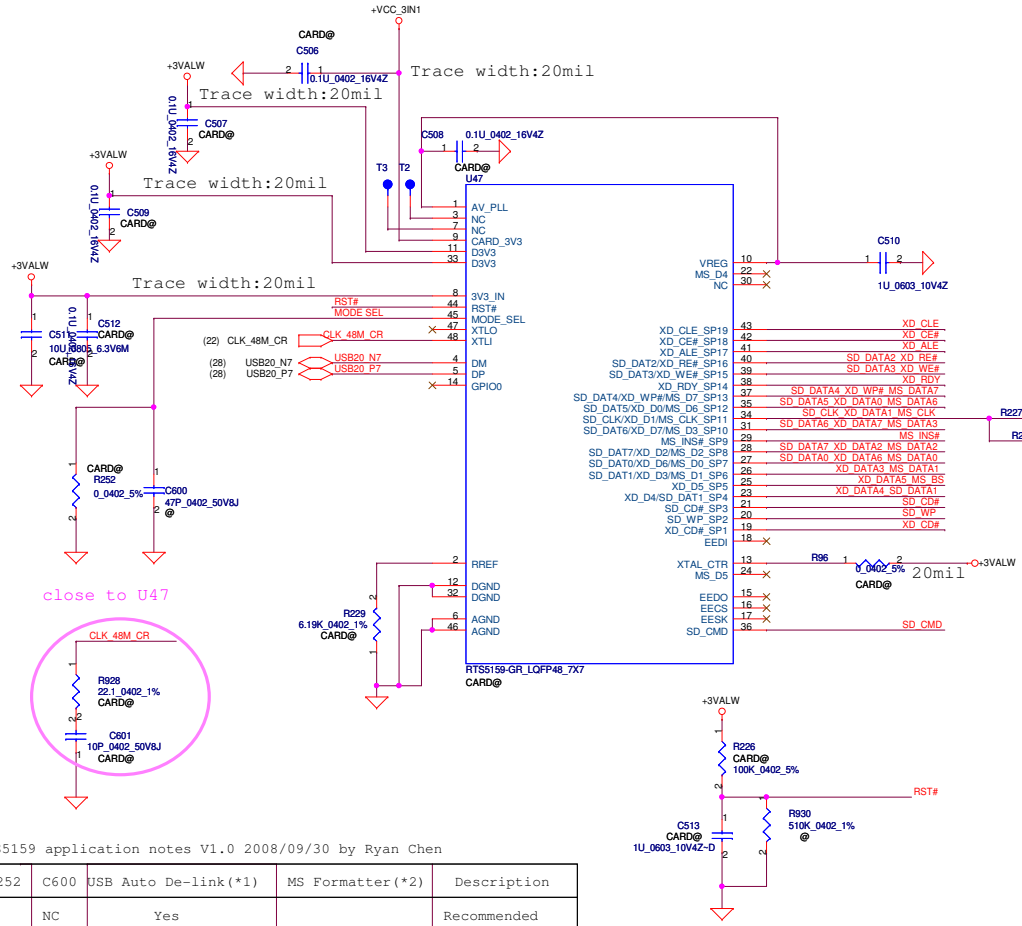
Compal Electronics, Inc.

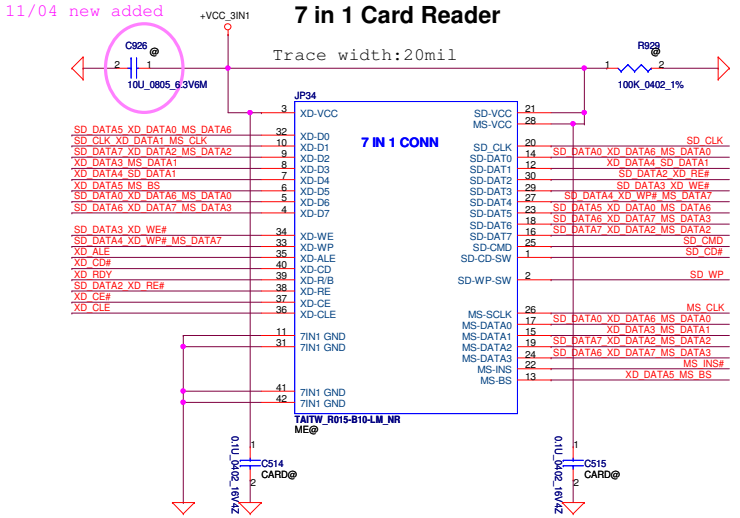
Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 36 of 53

Card reader(XD/SD/MMC/MS/MS-Pro HD SD)





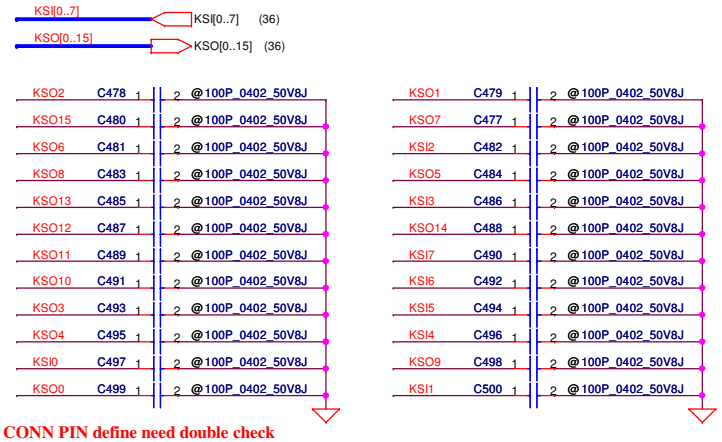
RTS5159 application notes V1.0 2008/09/30 by Ryan Chen

R252	C600	USB Auto De-link(*1)	MS Formatter(*2)	Description
0	NC	Yes		Recommended
NC	47pF	Yes	Yes	
NC	NC			Compatible with RTS5158E
NC	680pF	Yes		LED ON (*3)
10K	180pF			LED ON (*3)
10K	680pF		Yes	

Security Classification	Compal Secret Data		
Issued Date	2008/06/10	Deciphered Date	2008/12/31

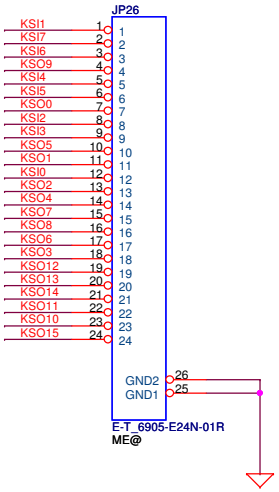
Compal Electronics, Inc.			
Title: USB_CR board			
Size: Custom	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 37 of 53		

INT_KBD Conn.

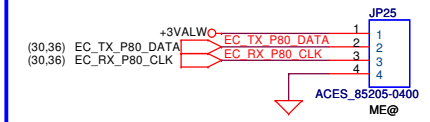


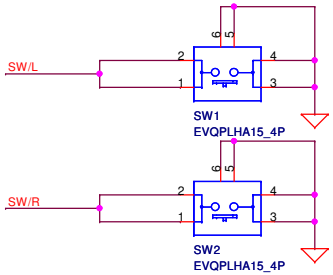
CONN PIN define need double check

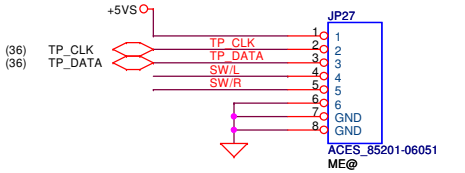
Source:SP01000IE00
2nd source:SP01000IF00
30 pin

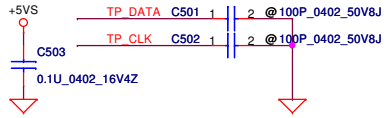


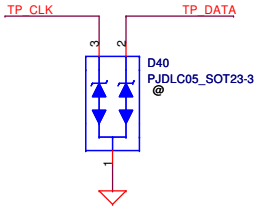
EC DEBUG PORT



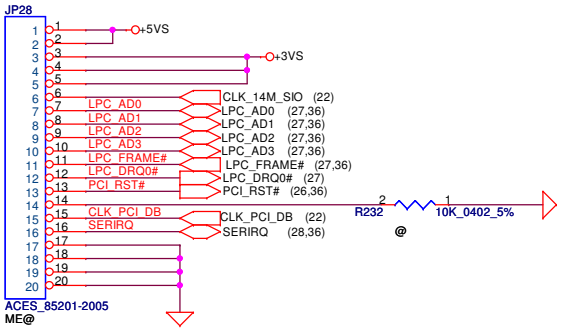








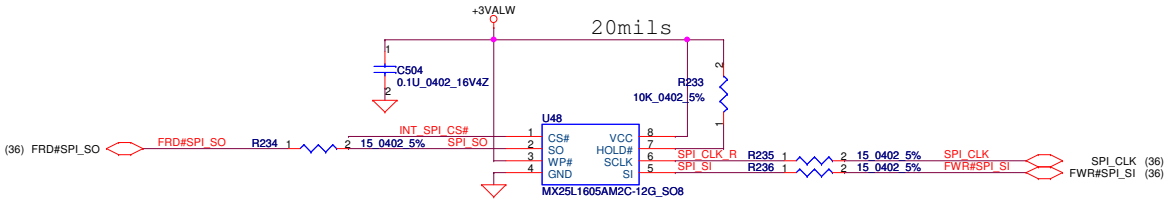
FOR LPC SIO DEBUG PORT

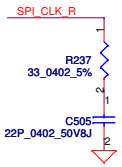


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 38 of 53		

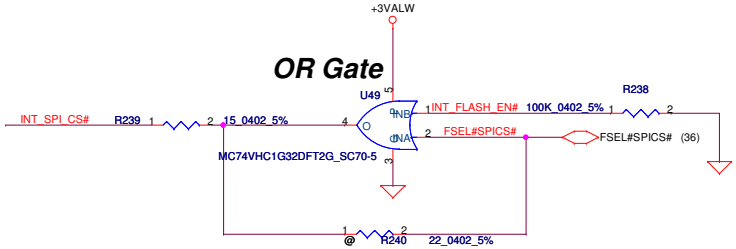
FOR EC 16M SPI ROM

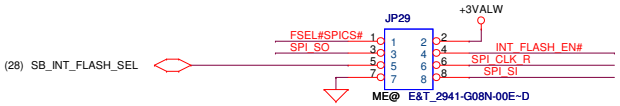




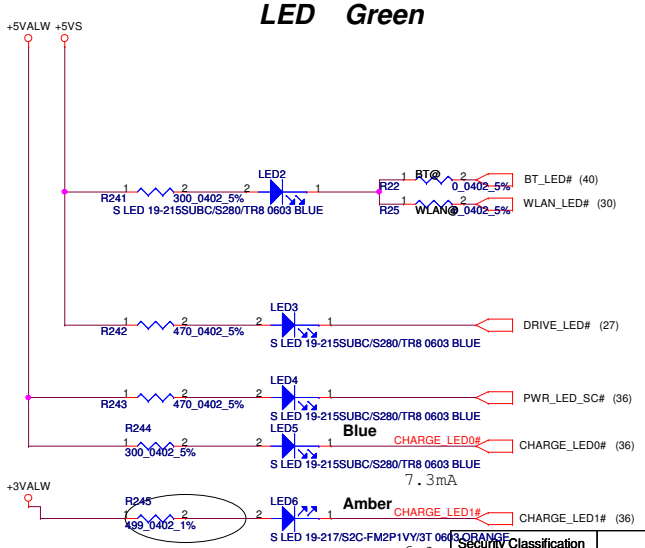
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

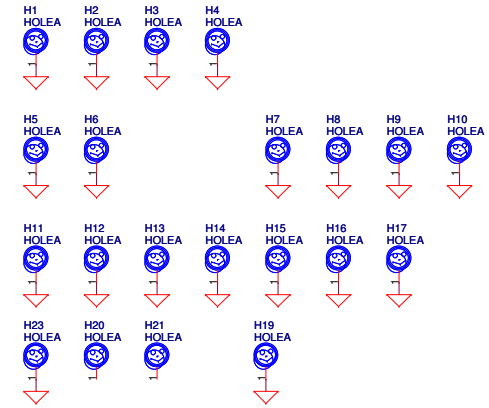
OR Gate





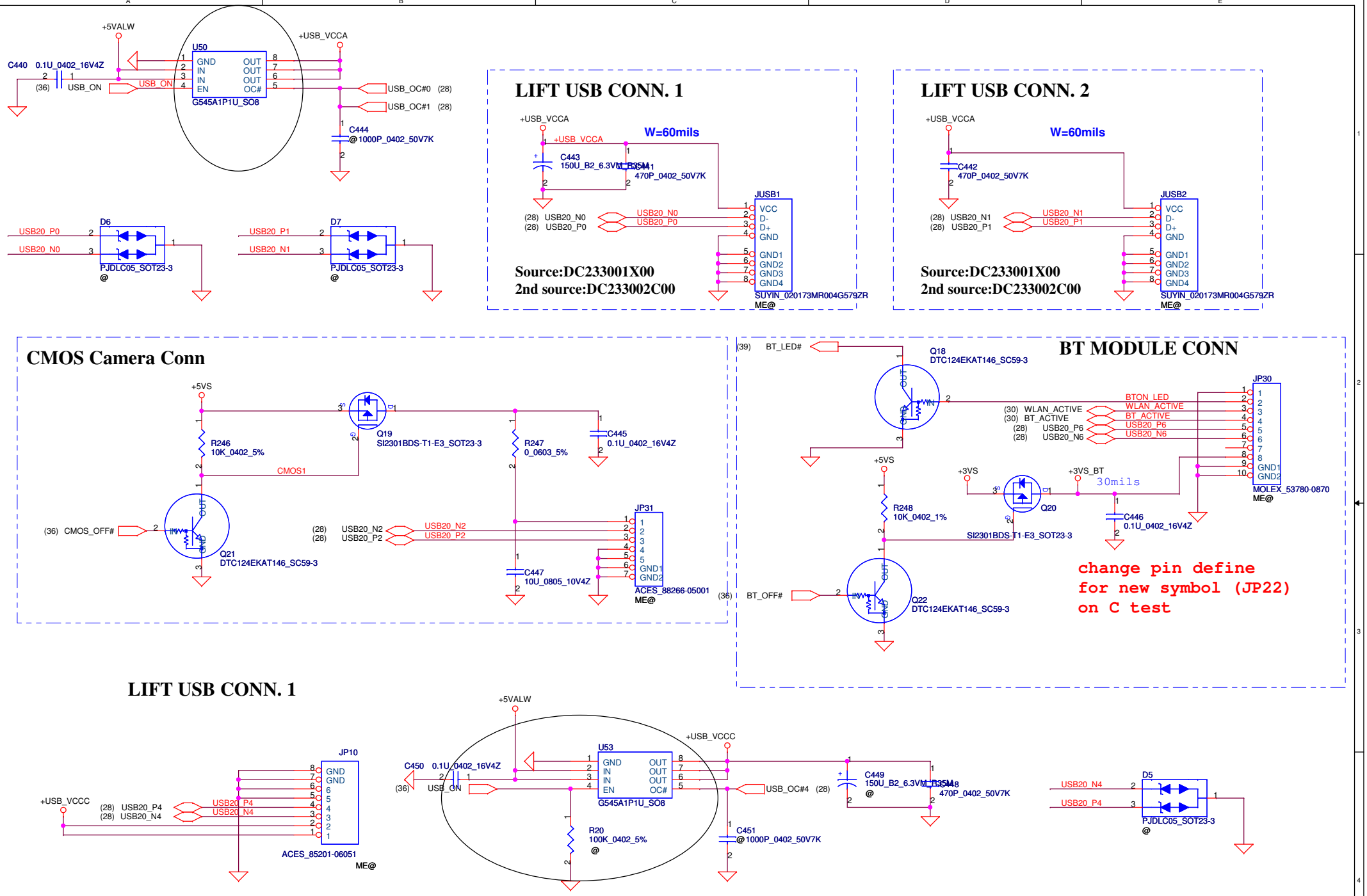
LED Green





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	LED/EC SPI ROM		
Size B	Document Number KIWA5/6 LA-5081P		Rev 0.4
Date: Wednesday, March 18, 2009	Sheet 39 of 53		



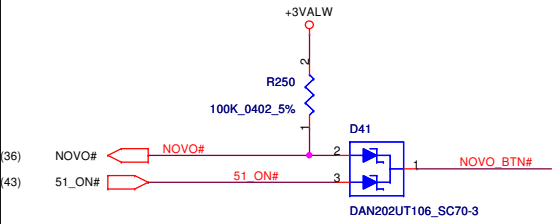
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

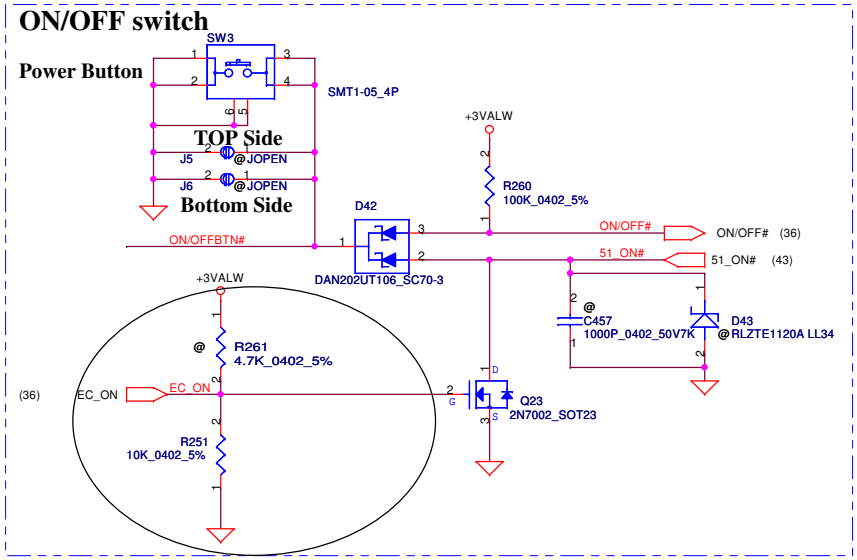
Compal Electronics, Inc.

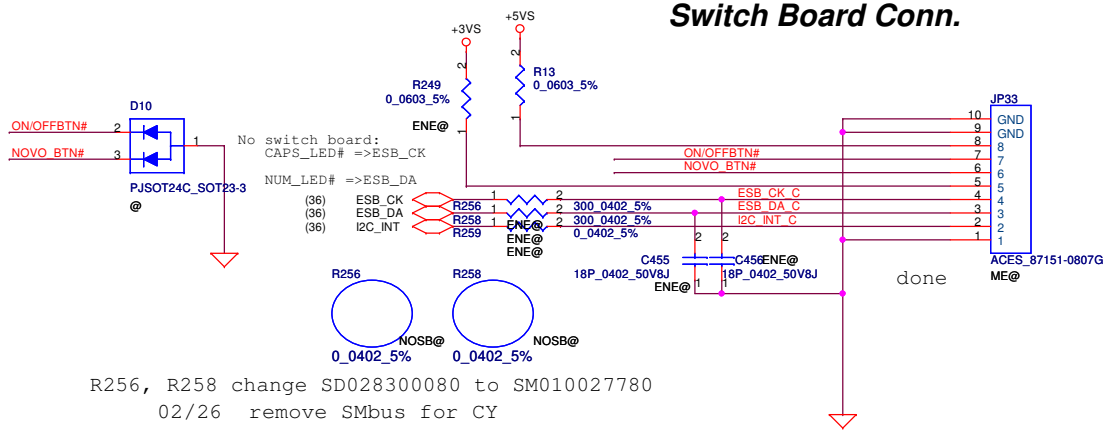
Title: Power OK, Reset and RTC Circuit, TP

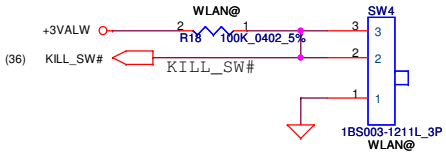
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

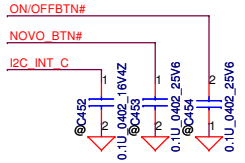
Date: Wednesday, March 18, 2009 | Sheet 40 of 53

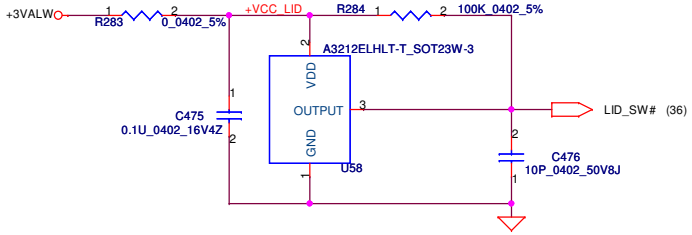








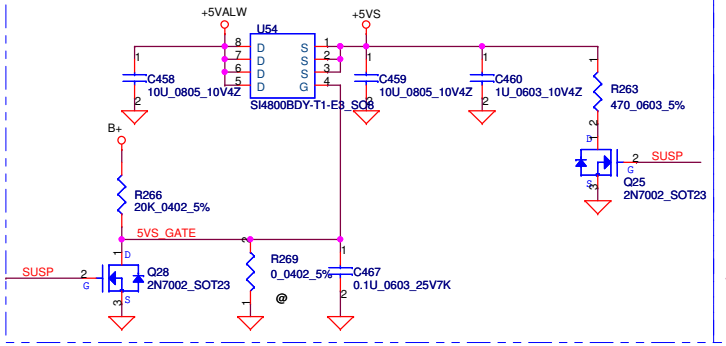




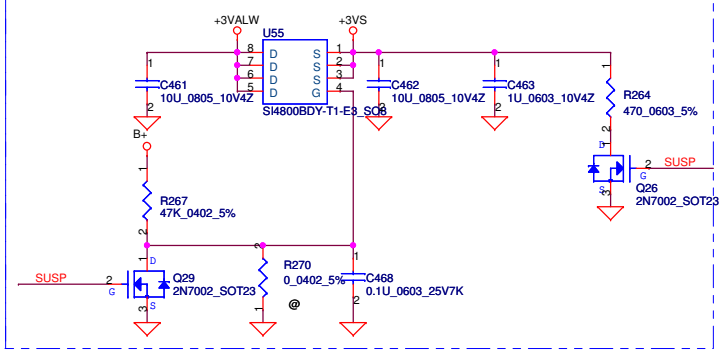
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

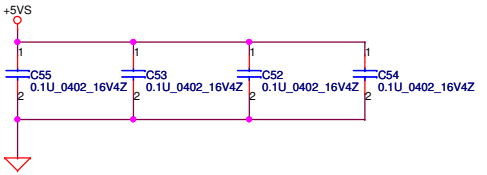
Compal Electronics, Inc.			
Title: Audio Jack & SW connector			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 41 of 53		

+5VALW TO +5VS

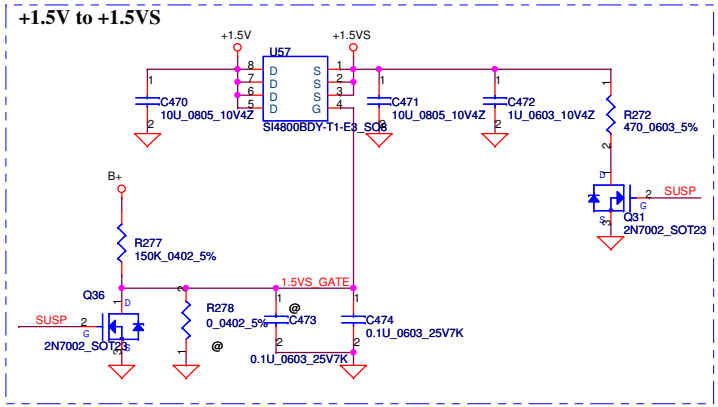


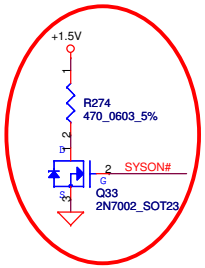
+3VALW TO +3VS

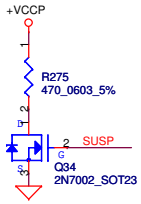


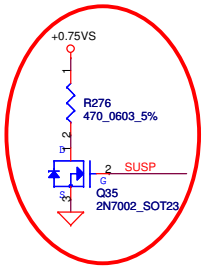


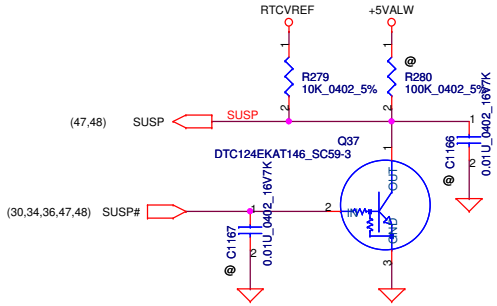
+1.5V to +1.5VS

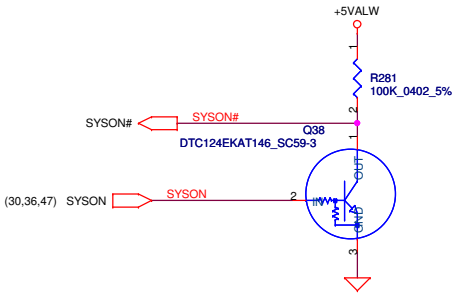












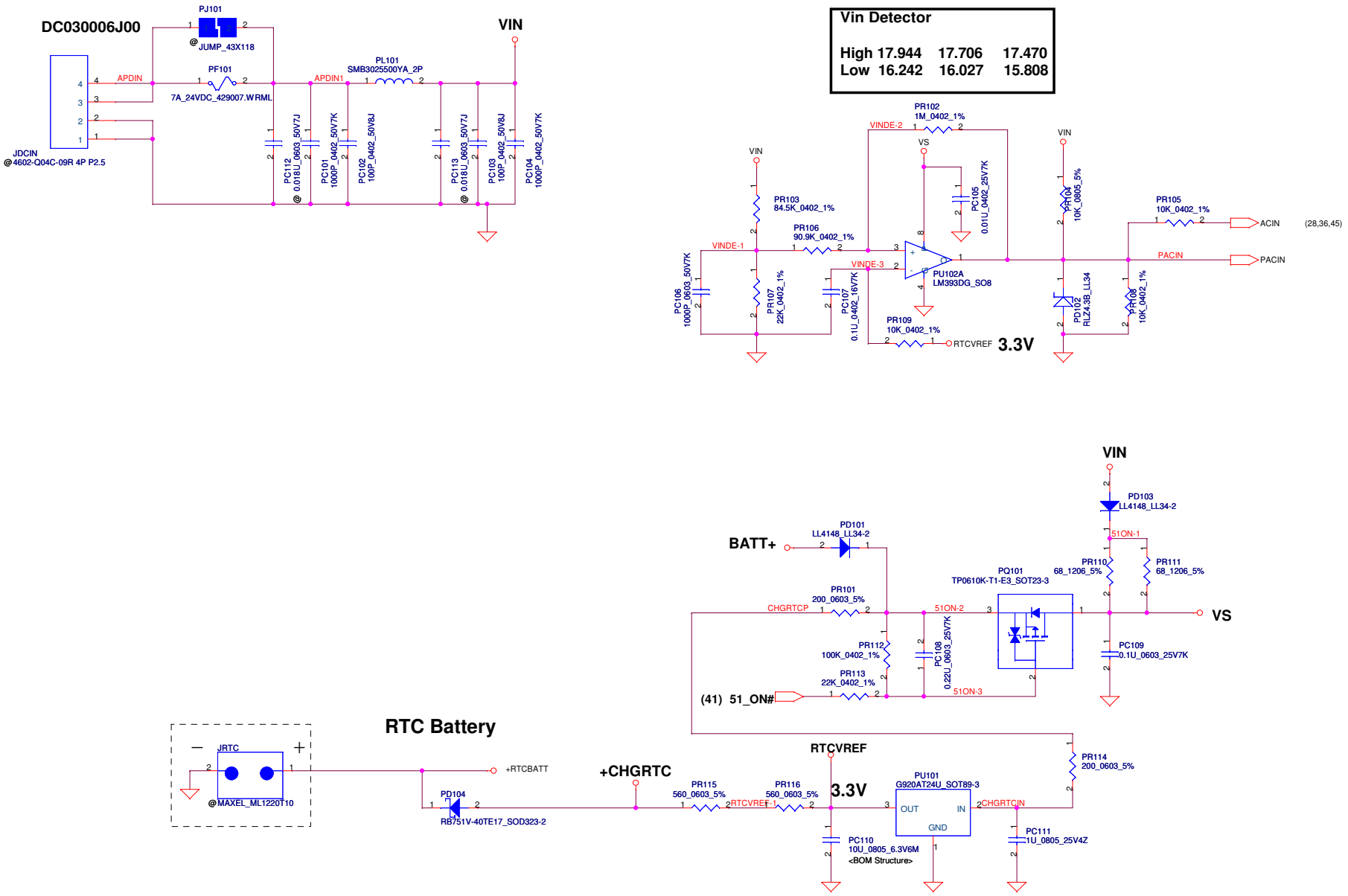
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 42 of 53



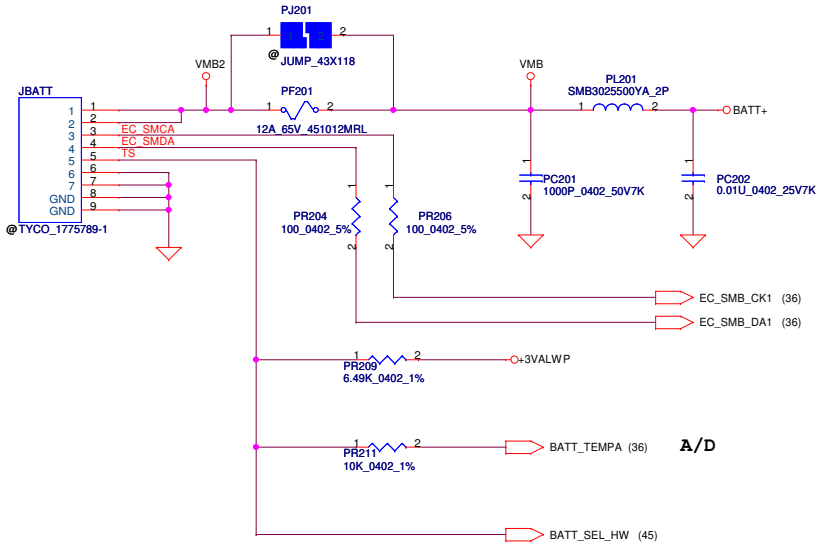
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.4

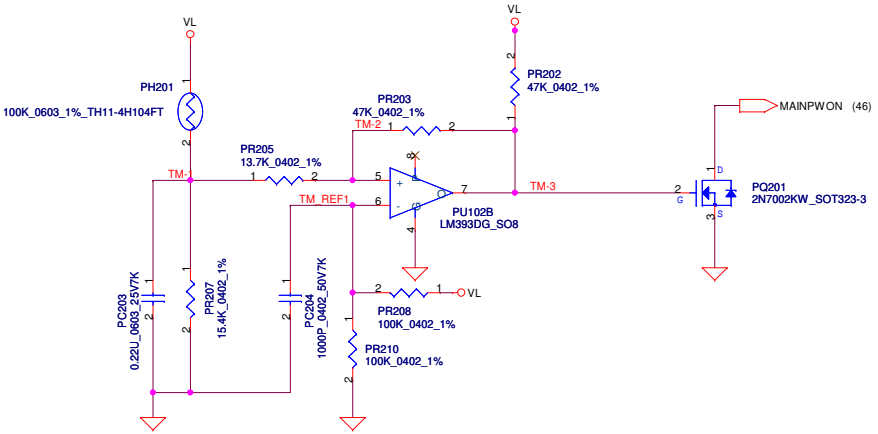
Date: Wednesday, March 18, 2009 | Sheet 43 of 53



PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C



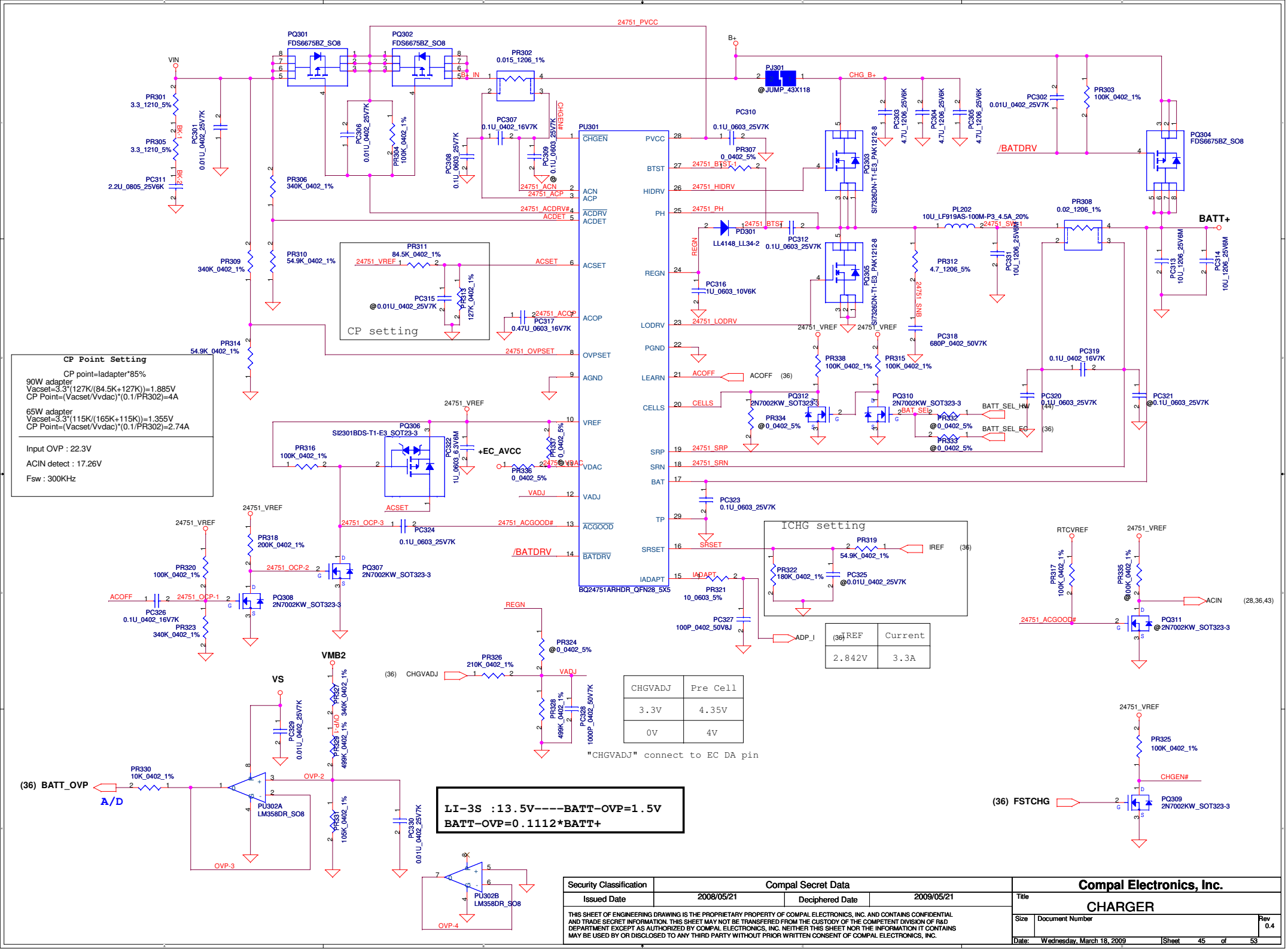
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 44 of 53



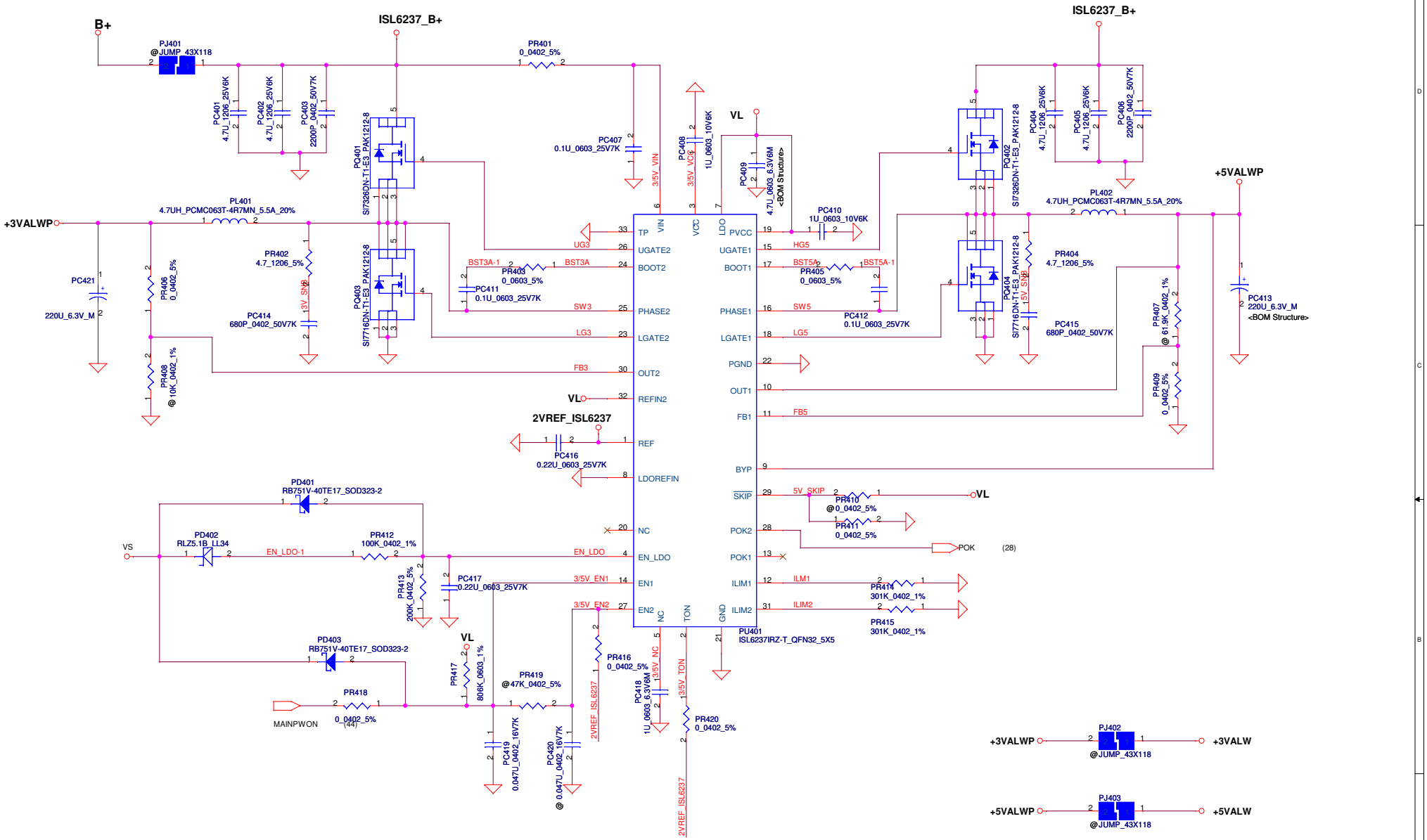
Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 45 of 53



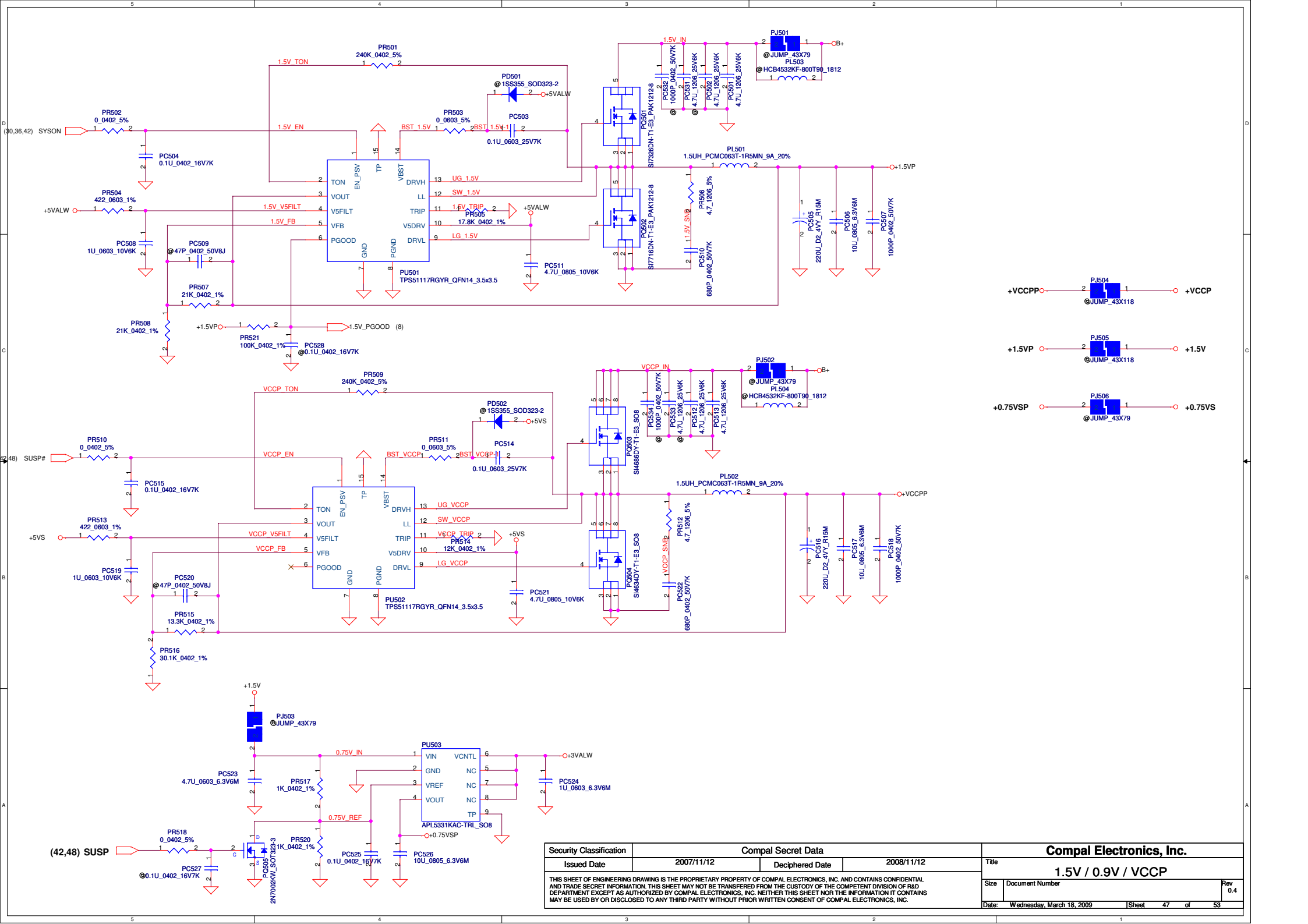
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.4

Date: Wednesday, March 18, 2009 | Sheet 46 of 53



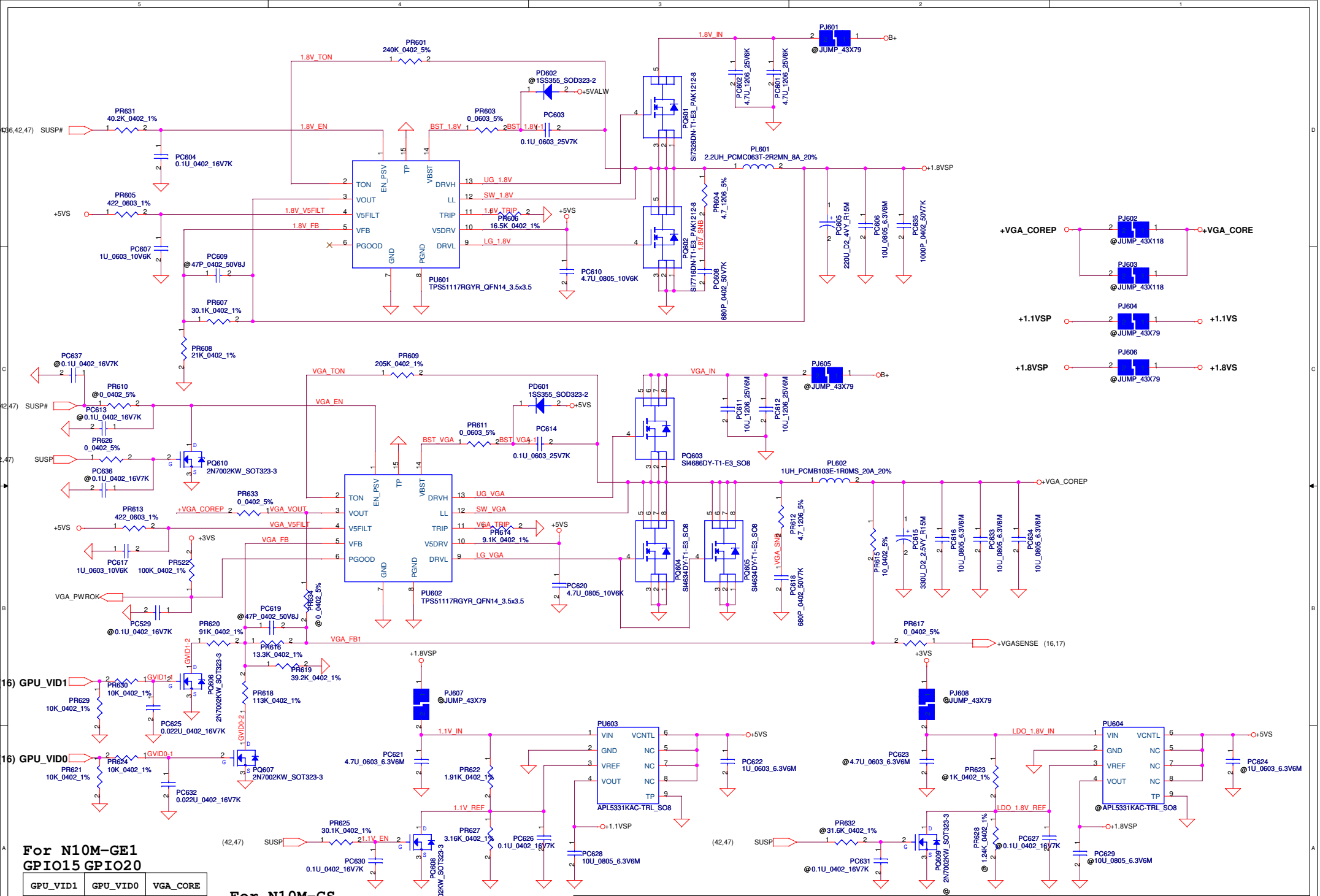
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.5V / 0.9V / VCCP

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 47 of 53



For N10M-GE1
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS

PR616=>9.09K
PR622=>2.21K
PR629,PR630,PC625,PQ606,PR620=>un-pop
PR621,PR624,PC632,PQ607,PR618=>un-pop

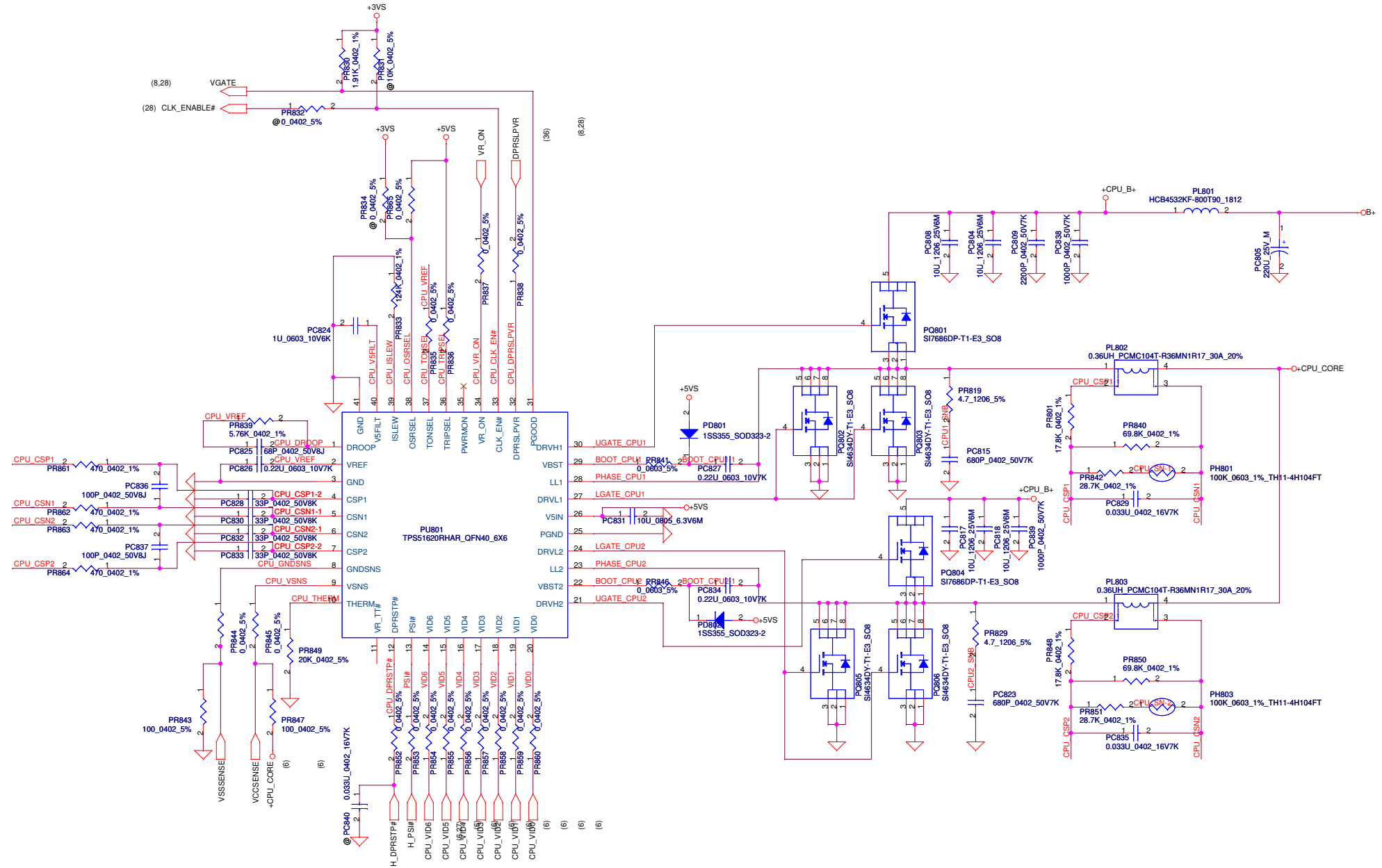
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: VGA_CORE/1.8V/1.1VS

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 48 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.4

Date: Wednesday, March 18, 2009 | Sheet 49 of 53

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)		
3							
4							
5							
6							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: KIWAX_LA-5082P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 50 of 53

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	39	Remove D11, and add R22, R25	
	12/10	36	change PWR_LED_SC# from U46.38 to U46.34	

Compal Electronics, Inc.		
Title: HW PIR		
Size: B	Document Number: KIWAX_LA-5082P	Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 51 of 53	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	39	modify H19 hold size, and change the H5、H6 and H19 hold type.	
		42	add 4 CAPs C52, C53, C54 and C55 for EMI.	
		35	change C572 and C574 footprint from 0603 to 0402.	
		34	add R44 for BEEP# test	
2	1/16	30	Remove one Mini-PCIE function! (Connector Side) Remove component is JP18, R363, R364, R367, R369, R371, R373, R375, R377, R378, R379, R380 and R383 Remove 3G function! Remove component is JP14, D12, R6, C6, C7, R7 and D13	
		28	Remove one Mini-PCIE function!(SB side) Remove component is C884 and C885	

Compal Electronics, Inc.

Title: **HW PIR**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 Sheet 52 of 53

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/16	06	add R1089, C1162 and H_DPRSTP#_R	
			add C1163, C1164,and C1165 for EMC request.	
		08	change H_DPRSTP# to H_DPRSTP#_R	
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU	
			R999 change to 24.9K	
		23	add R1095 pull high	
		35	swap HP_OUTL and HP_OUTR	
		36	add R1090, R1091, R1092, R1093	
			CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R	
		41	add R256, R258 Bom configuration	
			Remove CY SMBus	
		42	add C1166, C1167 for EMC request.	
2	3/16	28	change PCIE Port1 to Port3	
		30	change PCIE Port1 to Port3	

Compal Electronics, Inc.		
Title: HW PIR		
Size: B	Document Number: KIWAX_LA-5082P	Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 53 of 53	