

## Stereo 20W (4Ω) Class-T Digital Audio Amplifier using Digital Power Processing™ Technology TA2020-020

September, 2000

### General Description

The TA2020-020 is a 20W continuous average two-channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

### Applications

- DVD Players
- Mini/Micro Component Systems
- Automotive Audio
- Computer / PC Multimedia
- Cable Set-Top Products
- Televisions
- Battery Powered Systems

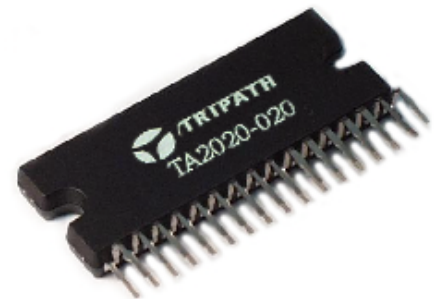
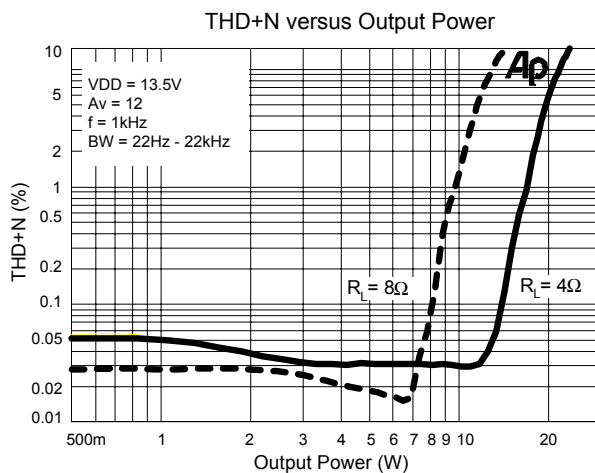
### Benefits

- Fully integrated solution with FETs
- Easier to design-in than Class-D
- Reduced system cost with no heat sink
- Dramatically improves efficiency versus Class-AB
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD, DVD, and internet audio

### Features

- Class-T architecture
- Single Supply Operation
- "Audiophile" Quality Sound
  - 0.03% THD+N @ 10W 4Ω
  - 0.1% THD+N @ 12W 4Ω
  - 0.18% IHF-IM @ 1W 4Ω
- High Power
  - 13W @ 8Ω, 10% THD+N
  - 23W @ 4Ω, 10% THD+N
  - 38W EIAJ\* VDD=14.4V @ 4Ω
- \*saturated square wave output
- High Efficiency
  - 88% @ 12W 8Ω
  - 81% @ 20W 4Ω
- Dynamic Range = 103 dB
- Up to 2X25Wrms @ 4Ω, VDD=14.6V
- Mute and Sleep inputs
- Turn-on & turn-off pop suppression
- Over-current protection
- Over-temperature protection
- Bridged outputs
- 32-pin SSIP package

### Typical Performance



## Absolute Maximum Ratings (Note 1)

| SYMBOL             | PARAMETER                            | Value        | UNITS |
|--------------------|--------------------------------------|--------------|-------|
| V <sub>DD</sub>    | Supply Voltage                       | 16           | V     |
| T <sub>STORE</sub> | Storage Temperature Range            | -40° to 150° | C     |
| T <sub>A</sub>     | Operating Free-air Temperature Range | -40° to 85°  | C     |
| T <sub>J</sub>     | Junction Temperature                 | 150°         | C     |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

## Operating Conditions (Note 2)

| SYMBOL          | PARAMETER                              | MIN. | TYP. | MAX. | UNITS |
|-----------------|----------------------------------------|------|------|------|-------|
| V <sub>DD</sub> | Supply Voltage                         | 8.5  | 13.5 | 14.6 | V     |
| V <sub>IH</sub> | High-level Input Voltage (MUTE, SLEEP) | 3.5  |      |      | V     |
| V <sub>IL</sub> | Low-level Input Voltage (MUTE, SLEEP)  |      |      | 1    | V     |

Note 2: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

## Thermal Characteristics

| SYMBOL          | PARAMETER                              | Value | UNITS |
|-----------------|----------------------------------------|-------|-------|
| θ <sub>JC</sub> | Junction-to-case Thermal Resistance    | 3.5°  | C/W   |
| θ <sub>JA</sub> | Junction-to-ambient Thermal Resistance | 15°   | C/W   |

## Electrical Characteristics (Note 1, 2)

See Test/Application Circuit. Unless otherwise specified,  $V_{DD} = 13.5V$ ,  $f = 1kHz$ , Measurement Bandwidth = 22kHz,  $R_L = 4\Omega$ ,  $T_A = 25^\circ C$ .

| SYMBOL         | PARAMETER                                        | CONDITIONS                                                                                                                 | MIN. | TYP.                | MAX. | UNITS            |
|----------------|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|------|---------------------|------|------------------|
| $P_O$          | Output Power<br>(Continuous Average/Channel)     | THD+N = 0.1% $R_L = 4\Omega$<br>THD+N = 0.1% $R_L = 8\Omega$<br>THD+N = 10% $R_L = 4\Omega$<br>THD+N = 10% $R_L = 8\Omega$ |      | 13<br>8<br>22<br>12 |      | W<br>W<br>W<br>W |
| $I_{DD,MUTE}$  | Mute Supply Current                              | MUTE = $V_{IH}$                                                                                                            |      | 5.5                 | 7    | mA               |
| $I_{DD,SLEEP}$ | Sleep Supply Current                             | SLEEP = $V_{IH}$                                                                                                           |      | 0.25                | 2    | mA               |
| $I_q$          | Quiescent Current                                | $V_{IN} = 0V$                                                                                                              |      | 60                  |      | mA               |
| THD + N        | Total Harmonic Distortion Plus Noise             | $P_O = 10W/Channel$                                                                                                        |      | 0.03                |      | %                |
| IHF-IM         | IHF Intermodulation Distortion                   | 19kHz, 20kHz, 1:1 (IHF)                                                                                                    |      | 0.18                |      | %                |
| SNR            | Signal-to-Noise Ratio                            | A-Weighted, $P_{OUT} = 1W$ , $R_L = 8\Omega$                                                                               |      | 89                  |      | dB               |
| CS             | Channel Separation                               | 0dB = 1W, $R_L = 4\Omega$ , $f = kHz$                                                                                      | 74   | 80                  |      | dB               |
| PSRR           | Power Supply Rejection Ratio                     | Vripple = 100mV                                                                                                            | 60   | 80                  |      | dB               |
| $\eta$         | Power Efficiency                                 | $P_{OUT} = 12W/Channel$ , $R_L = 8\Omega$                                                                                  |      | 88                  |      | %                |
| $V_{OFFSET}$   | Output Offset Voltage                            | No Load, MUTE = Logic low                                                                                                  |      | 50                  | 150  | mV               |
| $V_{OH}$       | High-level output voltage<br>(FAULT & OVERLOADB) |                                                                                                                            | 3.5  |                     |      | V                |
| $V_{OL}$       | Low-level output voltage<br>(FAULT & OVERLOADB)  |                                                                                                                            |      |                     | 1    | V                |
| $e_{OUT}$      | Output Noise Voltage                             | A-Weighted, input AC grounded                                                                                              |      | 100                 |      | $\mu V$          |

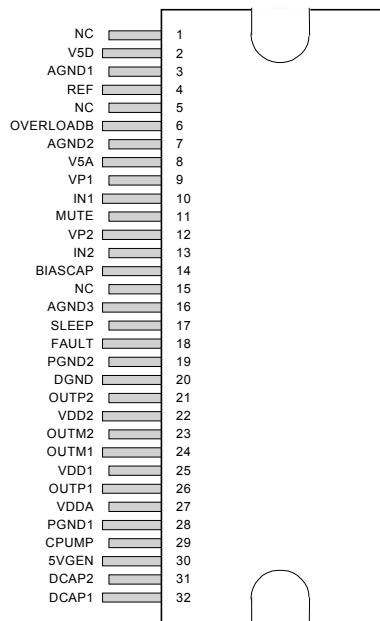
### Notes:

- 1) Minimum and maximum limits are guaranteed but may not be 100% tested.
- 2) For operation in ambient temperatures greater than  $25^\circ C$ , the device must be derated based on the maximum junction temperature and the thermal resistance determined by the mounting technique.

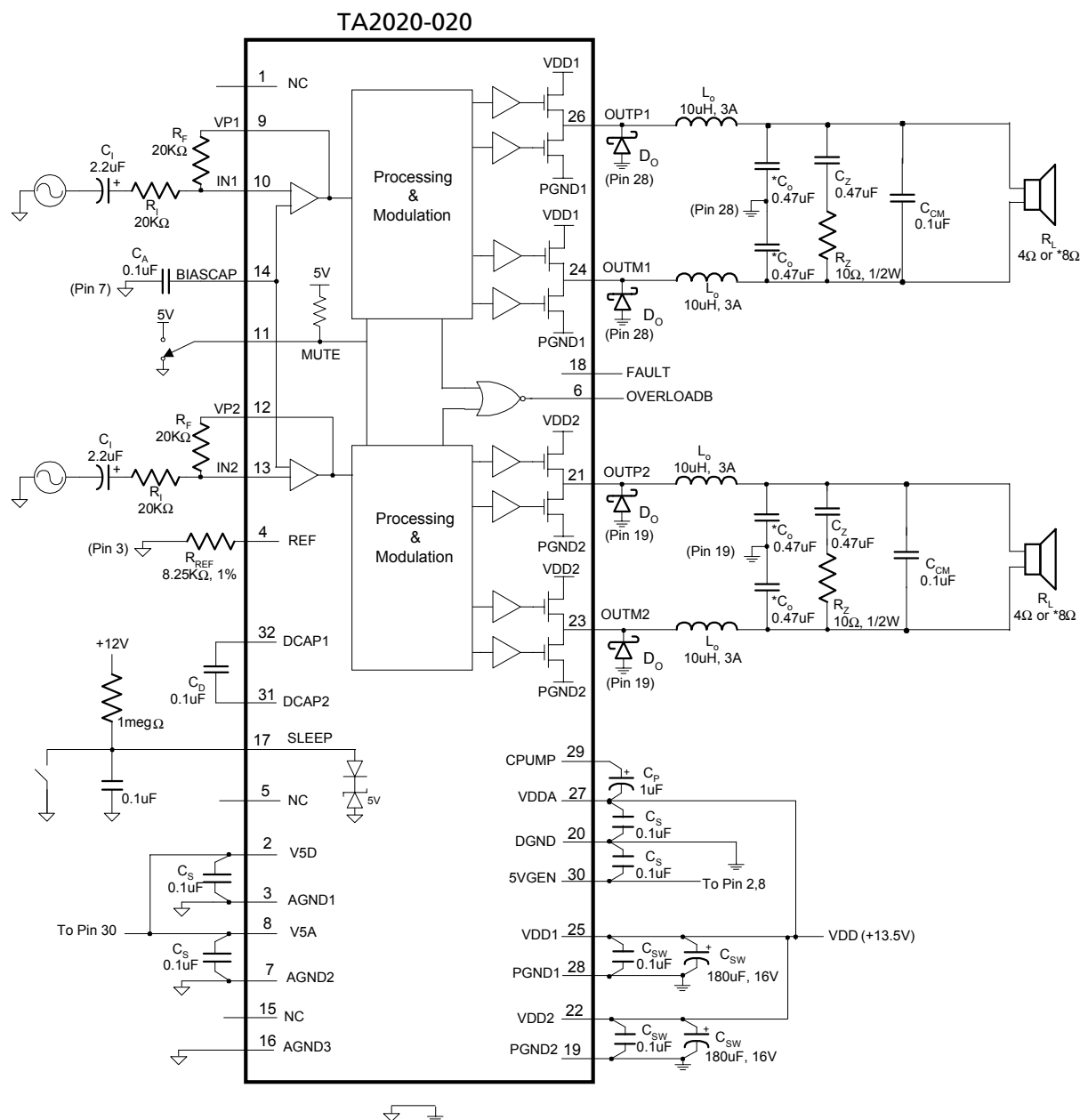
## Pin Description

| Pin            | Function                     | Description                                                                                                                                                                                                                                                      |
|----------------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2, 8           | V5D, V5A                     | Digital 5VDC, Analog 5VDC                                                                                                                                                                                                                                        |
| 3, 7, 16       | AGND1, AGND2, AGND3          | Analog Ground                                                                                                                                                                                                                                                    |
| 4              | REF                          | Internal reference voltage; approximately 1.0VDC                                                                                                                                                                                                                 |
| 6              | OVERLOADB                    | A logic low output indicates the input signal has overloaded the amplifier.                                                                                                                                                                                      |
| 9, 12          | VP1, VP2                     | Input stage output pins                                                                                                                                                                                                                                          |
| 10, 13         | IN1, IN2                     | Single-ended inputs. Inputs are a “virtual” ground of an inverting opamp with approximately 2.4VDC bias.                                                                                                                                                         |
| 11             | MUTE                         | When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. Ground if not used.                                                         |
| 14             | BIASCAP                      | Input stage bias voltage (approximately 2.4VDC).                                                                                                                                                                                                                 |
| 17             | SLEEP                        | When set to logic high, device goes into low power mode. If not used this pin should be grounded.                                                                                                                                                                |
| 18             | FAULT                        | A logic high output indicates thermal overload, or an output is shorted to ground, or another output.                                                                                                                                                            |
| 19, 28         | PGND2, PGND1                 | Power Ground (high current)                                                                                                                                                                                                                                      |
| 20             | DGND                         | Digital Ground                                                                                                                                                                                                                                                   |
| 21, 23, 26, 24 | OUTP2 & OUTM2; OUTP1 & OUTM1 | Bridged outputs                                                                                                                                                                                                                                                  |
| 22, 25         | VDD2, VDD1                   | Supply pin for high current H-bridges, nominally 13.5VDC.                                                                                                                                                                                                        |
| 1, 5, 15       | NC                           | Not connected                                                                                                                                                                                                                                                    |
| 27             | VDDA                         | Analog 13.5VDC                                                                                                                                                                                                                                                   |
| 29             | CPUMP                        | Charge pump output (nominally 10V above VDDA)                                                                                                                                                                                                                    |
| 30             | 5VGEN                        | Regulated 5VDC source used to supply power to the input section (pins 2 & 8).                                                                                                                                                                                    |
| 31, 32         | DCAP2, DCAP1                 | Charge pump switching pins. DCAP1 (pin 32) is a free running 300kHz square wave between VDDA and DGND (13.5Vpp nominal). DCAP2 (pin 31) is level shifted 10 volts above DCAP1 (pin 32) with the same amplitude (13.5Vpp nominal), frequency, and phase as DCAP1. |

32-pin SSIP Package  
(Front View)



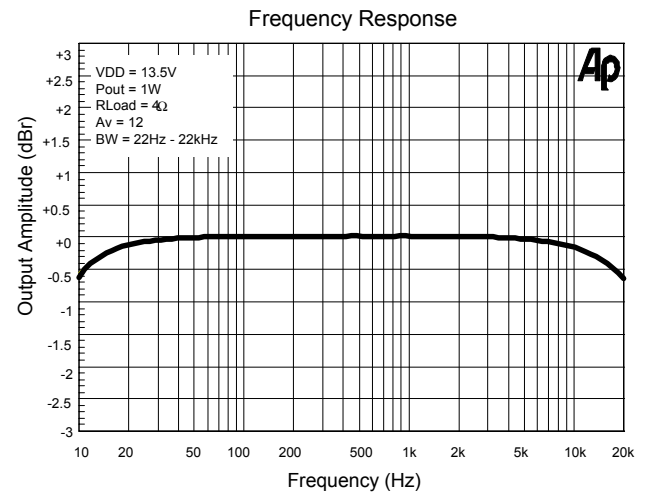
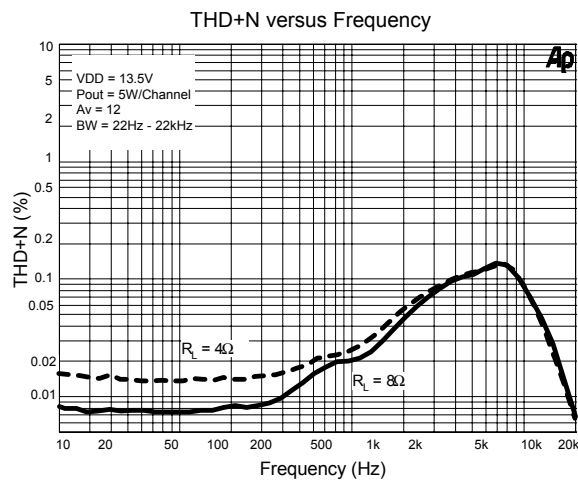
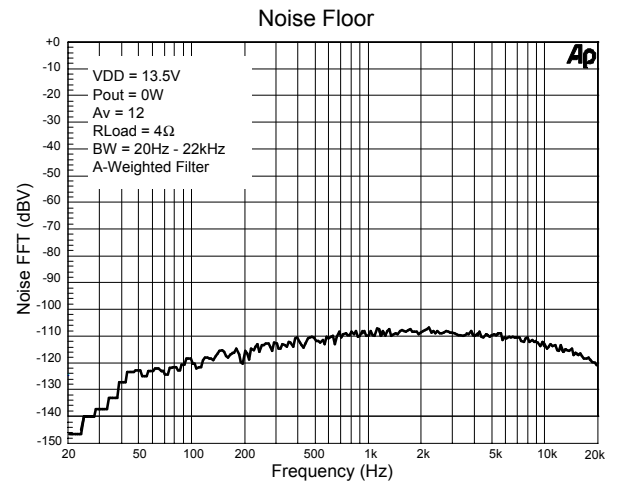
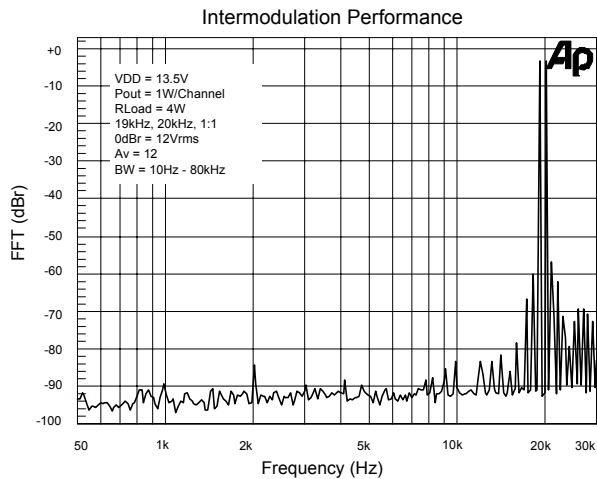
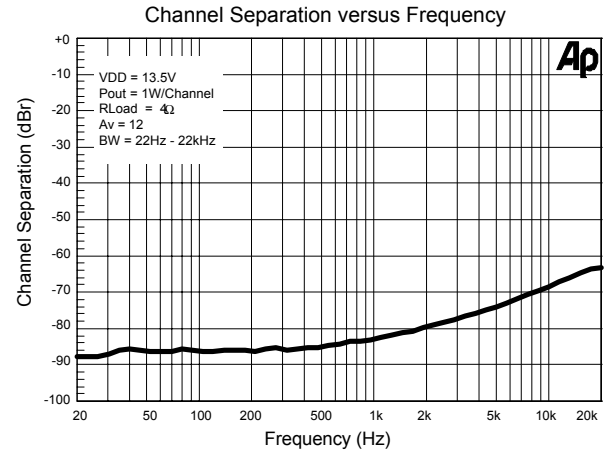
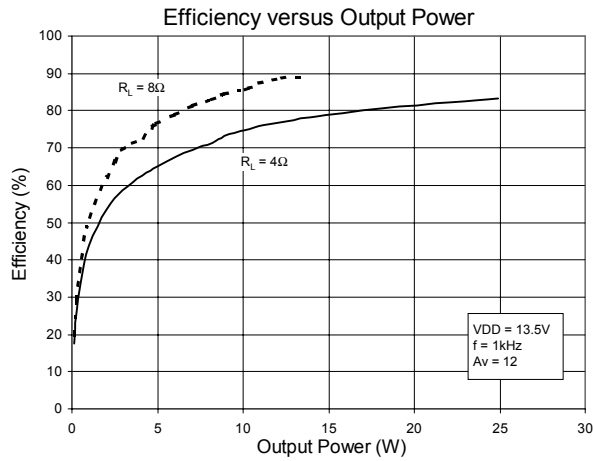
## Application/Test Circuit



## External Components Description (Refer to the Application/Test Circuit)

| Components | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $R_i$      | Inverting input resistance to provide AC gain in conjunction with $R_F$ . This input is biased at the BIASCAP voltage (approximately 2.4VDC).                                                                                                                                                                                                                                                                                                         |
| $R_F$      | Feedback resistor to set AC gain in conjunction with $R_i$ ; $A_v = 12(R_F / R_i)$ . Please refer to the Amplifier Gain paragraph, in the Application Information section.                                                                                                                                                                                                                                                                            |
| $C_i$      | AC input coupling capacitor which, in conjunction with $R_i$ , forms a highpass filter at $f_c = 1/(2\pi R_i C_i)$                                                                                                                                                                                                                                                                                                                                    |
| $R_{REF}$  | Bias resistor. Locate close to pin 4 and ground at pin 7.                                                                                                                                                                                                                                                                                                                                                                                             |
| $C_A$      | BIASCAP decoupling capacitor. Should be located close to pin 14 and grounded at pin 7.                                                                                                                                                                                                                                                                                                                                                                |
| $C_D$      | Charge pump input capacitor. This capacitor should be connected directly between pins 31 and 32 and located physically close to the TA2020-020.                                                                                                                                                                                                                                                                                                       |
| $C_P$      | Charge pump output capacitor that enables efficient high side gate drive for the internal H-bridges. To maximize performance, this capacitor should be connected directly between pin 29 (CPUMP) and pin 27 (VDDA). Please observe the polarity shown in the Application/Test Circuit.                                                                                                                                                                |
| $C_S$      | Supply decoupling for the low current power supply pins. For optimum performance, these components should be located close to the pin and returned to their respective ground as shown in the Application/Test Circuit.                                                                                                                                                                                                                               |
| $C_{SW}$   | Supply decoupling for the high current H-Bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. Both the high frequency bypassing (0.1uF) and bulk capacitor (180uF) should have good high frequency performance including low ESR and low ESL. Panasonic HFQ or FC capacitors are ideal for the bulk capacitor.                                       |
| $C_Z$      | Zobel capacitor, which in conjunction with $R_Z$ , terminates the output filter at high frequencies                                                                                                                                                                                                                                                                                                                                                   |
| $R_Z$      | Zobel resistor, which in conjunction with $C_Z$ , terminates the output filter at high frequencies. The combination of $R_Z$ and $C_Z$ minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. Depending on the program material, the power rating of $R_Z$ may need to be adjusted. The typical value is 1/2 watt. |
| $D_O$      | Schottky diodes that minimize undershoots of the outputs with respect to power ground during switching transitions. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective PGND. Please see Application/Test Circuit for ground return pin.                                                                                                                                                |
| $L_O$      | Output inductor, which in conjunction with $C_O$ , demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$ .                                                                                                                                                                                                                 |
| $C_O$      | Output capacitor which in conjunction with $L_O$ , demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_c = 1/(2\pi \sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$ .                                                                                                                                                                        |
| $C_{CM}$   | Common mode capacitor.                                                                                                                                                                                                                                                                                                                                                                                                                                |

## Typical Performance Characteristics

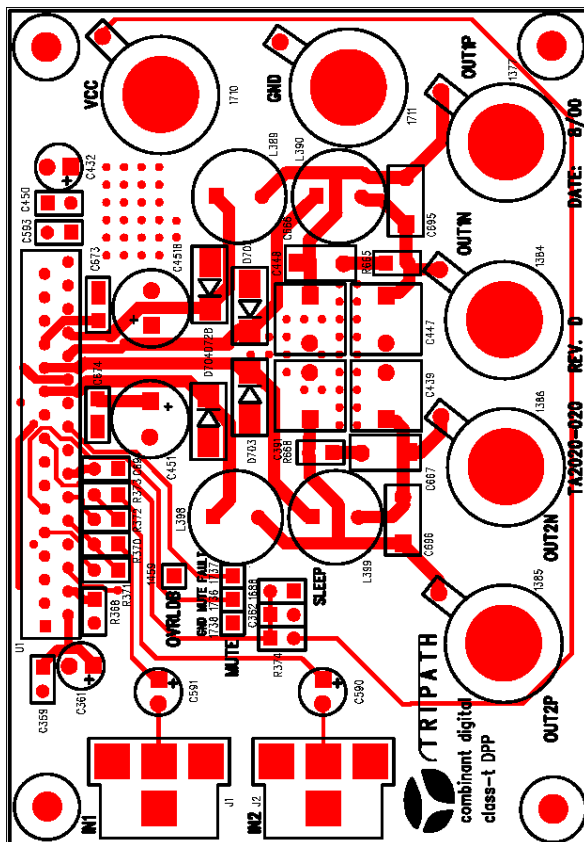


## Application Information

### Circuit Board Layout

The TA2020-020 is a power (high current) amplifier that operates at relatively high switching frequencies. The outputs of the amplifier switch between the supply voltage and ground at high speeds while driving high currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TA2020-020 to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes.

The figures below are the Tripath TA2020-020 evaluation board. Some of the most critical components on the board are the power supply decoupling capacitors. C674 and C451 must be placed right next to pins 22 and 19 as shown. C673 and C451B must be placed right next to pins 25 and 28 as shown. These power supply decoupling capacitors from the output stage not only help reject power supply noise, but they also absorb voltage spikes on the VDD pins caused by overshoots of the outputs of the amplifiers. Voltage overshoots can also be caused by output inductor flyback during high current switching events such as shorted outputs or driving low impedances at high levels. If these capacitors are not close enough to the pins, electrical overstress to the part can occur, possibly resulting in permanent damage to the TA2020-020.



## Amplifier Gain

The gain of the TA2020-020 is set by the ratio of two external resistors,  $R_I$  and  $R_F$ , and is given by the following formula:

$$\frac{V_O}{V_I} = 12 \frac{R_F}{R_I}$$

where  $V_I$  is the input signal level and  $V_O$  is the differential output signal level across the speaker.

20 watts of RMS output power results from an 8.944 V RMS signal across a four-ohm speaker load. If  $R_F = R_I$ , then 20 Watts will be achieved with 0.745 V RMS of input signal.

$$8.944 V_{RMS} = \sqrt{(R_L * P_O)} = \sqrt{(4\Omega * 20W)}$$

## Protection Circuits

The TA2020-020 is guarded against over-temperature and over-current conditions. When the device goes into an over-temperature or over-current state, the FAULT pin goes to a logic HIGH state indicating a fault condition. When this occurs, the amplifier is muted, all outputs are TRI-STATED, and will float to 1/2 of  $V_{DD}$ .

### Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 155°C. The thermal hysteresis of the part is approximately 45°C, therefore the fault will automatically clear when the junction temperature drops below 110°C.

### Over-current Protection

An over-current fault occurs if more than approximately 7 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground. An over-current fault sets an internal latch that can only be cleared if the MUTE pin is toggled or if the part is powered down. Alternately, if the MUTE pin is connected to the FAULT pin, the HIGH output of the FAULT pin will toggle the MUTE pin and automatically reset the fault condition.

### Overload

The OVERLOADB pin is a 5V logic output. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVERLOADB signal can be used to control a distortion indicator light or LED through a simple buffer circuit.

### Sleep Pin

The SLEEP pin is a 5V logic input that when pulled high (>3.5V) puts the part into a low quiescent current mode. This pin is internally clamped by a zener diode to approximately 6V thus allowing the

pin to be pulled up through a large valued resistor (1MΩ recommended) to V<sub>DD</sub>. To disable SLEEP mode, the sleep pin should be grounded.

## Fault Pin

The FAULT pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: low supply voltage, low charge pump voltage, low 5V regulator voltage, over current at any output, and junction temperature greater than approximately 155°C. The FAULT output is capable of directly driving an LED through a series 200Ω. The FAULT output is capable of directly driving an LED through a series 200Ω resistor. If the FAULT pin is connected directly to the MUTE input an automatic reset will occur in the event of an over-current condition.

## Heat Sink Requirements

In some applications it may be necessary to fasten the TA2020-020 to a heat sink. The determining factor is that the 150°C maximum junction temperature, T<sub>J(max)</sub> cannot be exceeded, as specified by the following equation:

$$P_{DISS} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where...

P<sub>DISS</sub> = maximum power dissipation

T<sub>JMAX</sub> = maximum junction temperature of TA2020-020

T<sub>A</sub> = operating ambient temperature

θ<sub>JC</sub> = junction-to-case thermal resistance of TA2020-020

Example:

What size heat sink is required to operate the TA2020-020 at 20W per channel continuously in a 70°C ambient temperature?

P<sub>DISS</sub> is determined by:

$$\text{Efficiency} = \eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} - P_{DISS}}$$

$$P_{DISS} \text{ (per channel)} = \frac{P_{OUT}}{\eta} - P_{OUT} = \frac{20}{0.8} - 20 = 5W$$

Thus, P<sub>DISS</sub> for two channels = 10W

$$\theta_{JA} = \frac{(T_{J(MAX)} - T_A)}{P_{DISS}} = \frac{150 - 70}{10} = 8^{\circ}\text{C/W}$$

The  $\theta_{JA}$  of the TA2020-020 in free air is 15°C/W. The  $\theta_{JC}$  of the TA2020-020 is 3.5°C/W, so a heat sink of 4.5°C/W is required for this example. In actual applications, other factors such as the average  $P_{DISS}$  with a music source (as opposed to a continuous sine wave) and regulatory agency testing requirements will determine the size of the heat sink required.

## Performance Measurements of the TA2020-020

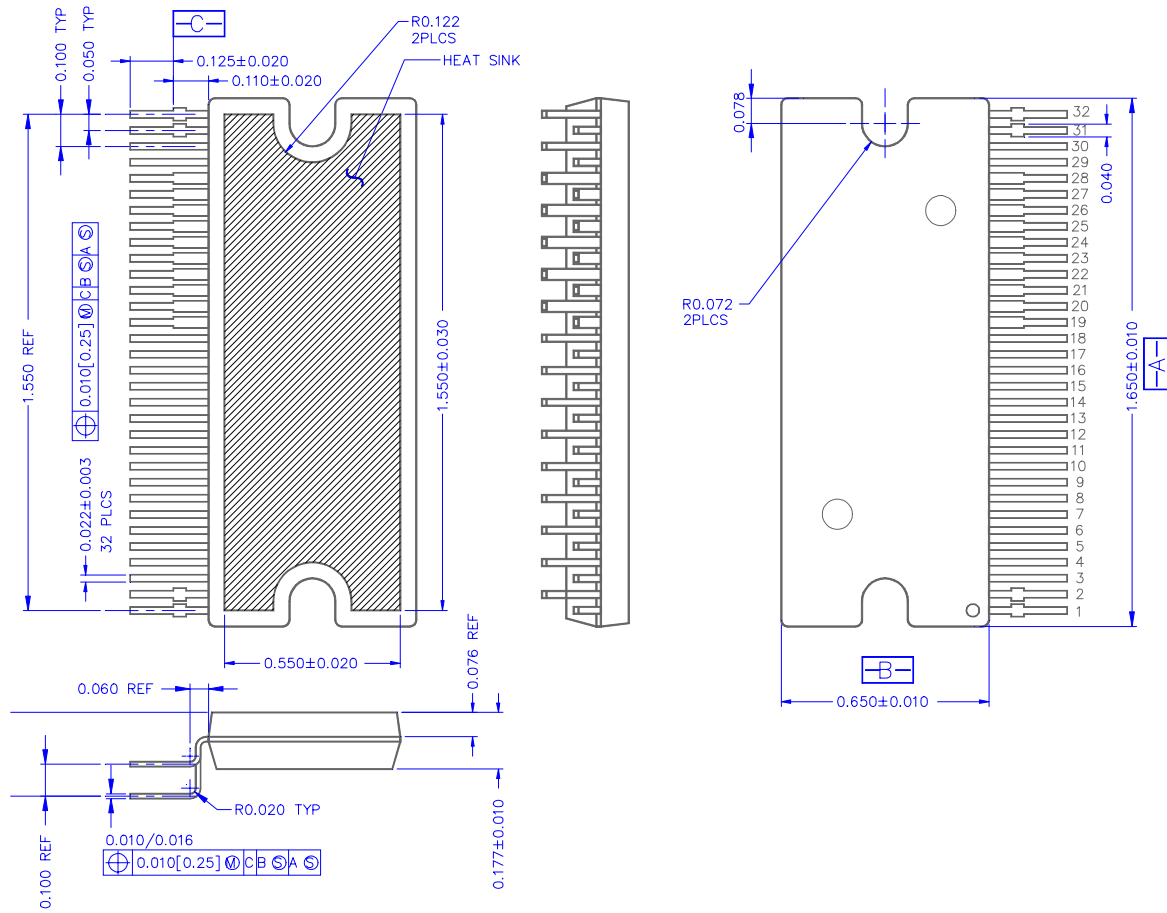
The TA2020-020 operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum in nature and typically varies between 100kHz and 1MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal, but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the TA2020-020 amplifier switching pattern will degrade the measurement.

One feature of the TA2020-020 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TA2020-020 Evaluation Board uses the Application/Test Circuit of this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

## Package Information

### 32-pin SSIP Package:



# TECHNICAL INFORMATION



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