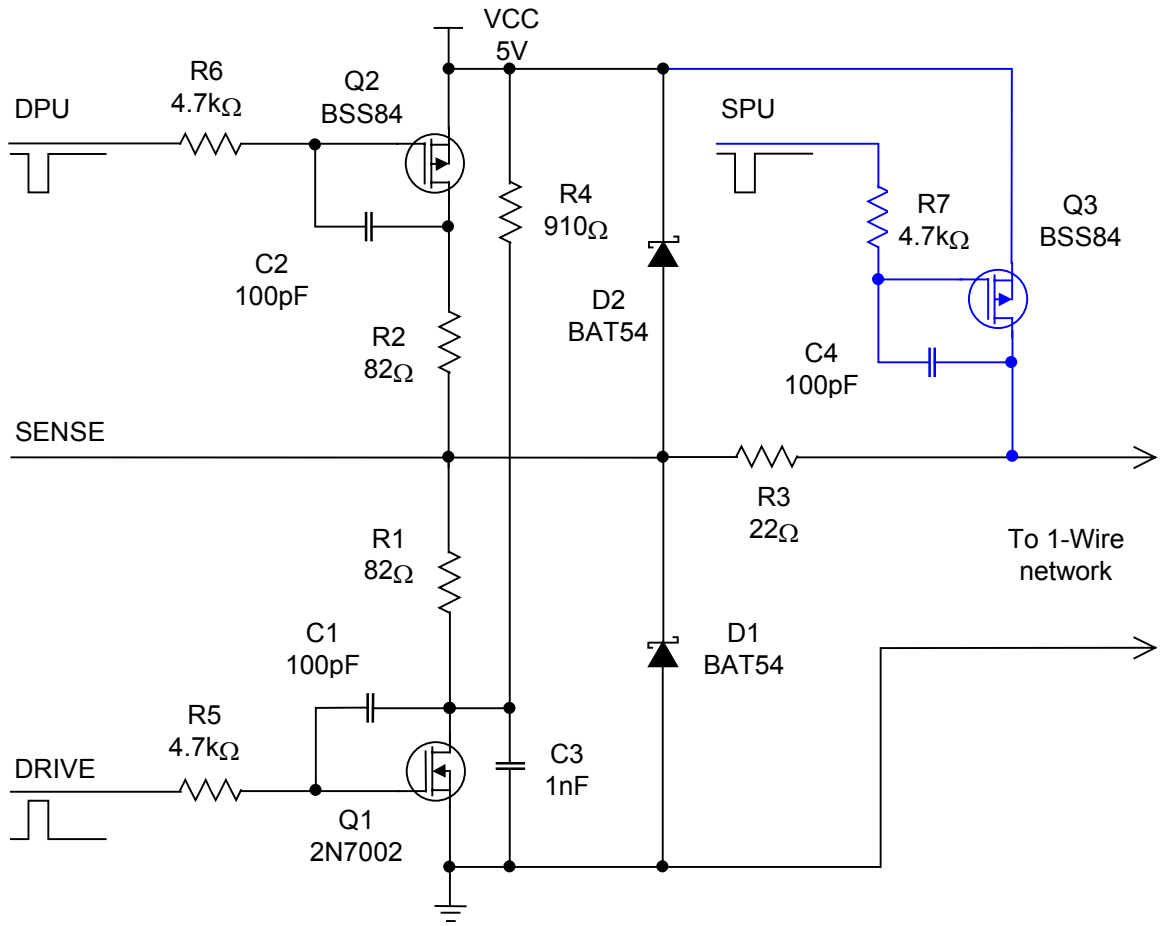
Application Note 244
Advanced 1-Wire Network Driver

INTRODUCTION

To a large degree, the reliability of a 1-Wire® network depends on the characteristics of the driver circuit that the host computer uses to communicate with 1-Wire slave devices. This document describes a 1-Wire master interface that uses careful impedance matching and an "intelligent" (software-controlled) strong pullup to accomplish reliable operation in networks from very lightweight to very heavy, up to 500m equivalent size. For guidelines on how to create reliable 1-Wire networks see Application Note 148.

Figure 1. DRIVER SCHEMATIC



CIRCUIT DESCRIPTION

The network driver (Figure 1) consists of a pulldown section (Q1, R1, C1, R5) and a pullup section (Q2, R2, C2, R6). A third transistor and surrounding components (Q3, C4, R7) form a strong pullup section to supply extra power for devices such as EEPROMs, or temperature sensors. This "strong-pullup" function is not discussed in this document. Of the three transistors, a maximum of one is conducting at any time. When there is no 1-Wire communication ("idle" state), all three transistors are nonconducting.

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The series path of R4, R1 and R3 provides the standard 1-Wire pullup to V_{CC}. With this circuit, the total pullup resistance is approximately 1kΩ. This value applies when the 1-Wire line is idle. Since R4 is connected to the drain of Q1, the current flowing through it when Q1 is conducting does not affect the low-level voltage on the 1-Wire line. R4+R1+R3 together with the load or "weight" of the 1-Wire network determine the speed at which the voltage on the 1-Wire rises to 5V. Lowering R4 is not recommended since it would raise the low-level voltage on the 1-Wire, which is undesirable. The Schottky-diodes D1 and D2 eliminate spikes from ESD hits or cross coupling from other cabling nearby by conducting them to GND and V_{CC}, respectively. R3 limits the ESD current and protects D1 and D2.

A special characteristic of this driver is the proper line termination of the 1-Wire cable on the master end. The category 5 unshielded twisted-pair data cable, which is recommended for 1-Wire applications, has a characteristic impedance of approximately 100Ω. Line termination is accomplished through R1 or R2 in series with R3 when Q1 or Q2 is conducting. C3 in series with R1 and R3 provide an AC-coupled termination for presence pulses. To adapt this driver to a different impedance, R1 and R2 need to be changed accordingly.

All three sections of this driver are slew-rate controlled when the associated transistor is turned on. R5 and C1 limit the slew rate when the driver pulls the 1-Wire line low, e. g., at the beginning of a time slot or a reset pulse. R6 and C2 limit the slew rate when the dynamic pullup becomes active. R7 and C4 limit the slew rate of the active pullup. The time constant of all three sections is 0.5µs. This value results in a slew rate of approximately 4V/µs. For details and scope traces see section *Performance Examples*.

CIRCUIT OPERATION

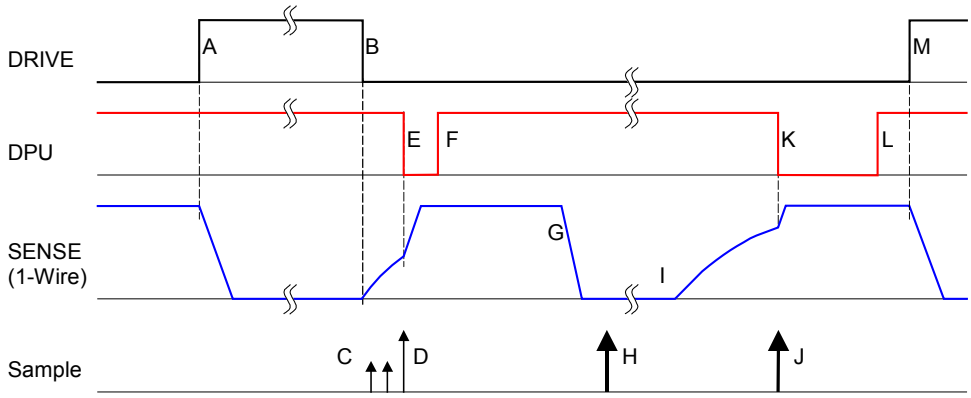
Disregarding the strong pullup circuitry (Q3, R7, C4) the driver requires three connections to a supervising microcontroller. These signals are called DRIVE, DPU, and SENSE. DRIVE is an active high signal that initiates 1-Wire communication by turning on Q1. DPU is an active low signal that activates the dynamic pullup Q2. SENSE is essentially a through-connection from the 1-Wire line to an input port of the microcontroller. 1-Wire ground and driver/microcontroller GND are the same. To perform 1-Wire communication it is necessary to properly generate the DRIVE and DPU signals and to read from the 1-Wire line through the SENSE input at the appropriate times. 1-Wire communication knows four cases of waveforms; these are reset/presence detect sequence, and the three cases of communication time slots.

Reset/Presence Detect Sequence

All 1-Wire communication begins with a reset pulse followed by a window for the presence pulse. Figure 2 shows the 1-Wire waveform. To generate the reset pulse, the DRIVE signal is activated for a duration from A to B (see Figure 2). Starting at A, the voltage on the 1-Wire ramps down to 0V. As DRIVE gets inactive at B, the voltage on the 1-Wire starts rising, unless a 1-Wire device pulls the line low to signal an interrupt condition (see DS1994/DS2404 data sheet, Type 2 Interrupt). To properly accommodate this interrupt case, the status of the 1-Wire is sampled repeatedly starting at C until the 1-Wire has reached a logic high level at D. Shortly after D, the dynamic pullup DPU is activated (point E). This quickly pulls the 1-Wire line to 5V. At F the dynamic pullup ends. Assuming that a 1-Wire device is present, it will generate a presence pulse, which begins at G and ends at I. At H, somewhere between G and I, the status on the 1-Wire is sampled to test whether a 1-Wire device is present. As the presence pulse ends, the voltage on the 1-Wire starts rising towards 5V. At J the logic status of the 1-Wire is sampled again to detect whether a Type 1A interrupt (see DS1994/DS2404 data sheet) is signaled. Without interrupt, the logic state will be high, as shown in Figure 2, and the dynamic pullup is activated again from K to L, which ensures that the 1-Wire line is fully recharged. With interrupt signal, the status sensed at J will be a logic zero and another series of repeated sampling, exactly like that at the end of the reset pulse is

necessary (i. e., going back to C and continue sampling). The interrupt pulse will be understood as a reset pulse by other 1-Wire devices. Therefore they will generate a presence pulse as the response, except for the interrupting device (i. e., when J is reached in the second pass, the logic status of the 1-Wire will be high, as shown in Figure 2. In any case, the reset/presence detect sequence ends at M, where a time slot begins.

Figure 2. RESET AND PRESENCE DETECT SEQUENCE



Recommended Timing Values for Reset/Presence Detect Sequence

A to B	B to C	D to E	E to F	E to H	H to J	J to K	K to L	L to M
480µs	0 to 2µs	0 to 2µs	8µs	72µs	240µs	0 to 2µs	60µs	>2µs

The sampling point H must be chosen to hit the presence pulse window, which is determined by the timing spread between the fastest and the slowest 1-Wire device present. Data sheets specify this window as t_{MSP}. The timing reference for t_{MSP} begins when the 1-Wire device detects logic HIGH level after the reset pulse is over. In Figure 2 this reference point approximately coincides with E. The duration from A to C is equivalent to the sum of t_F (fall time) and t_{RSTL} (reset low time). In case of a Type 2 interrupt, the effective reset low time is the sum of A to B and the duration of the interrupt pulse (see DS1994/DS2404 data sheet). The time from E to M is called reset high time t_{RSTH}. Data sheets specify t_{RSTL} and indicate how to determine the minimum duration of t_{RSTH}. There is no maximum for t_{RSTH}.

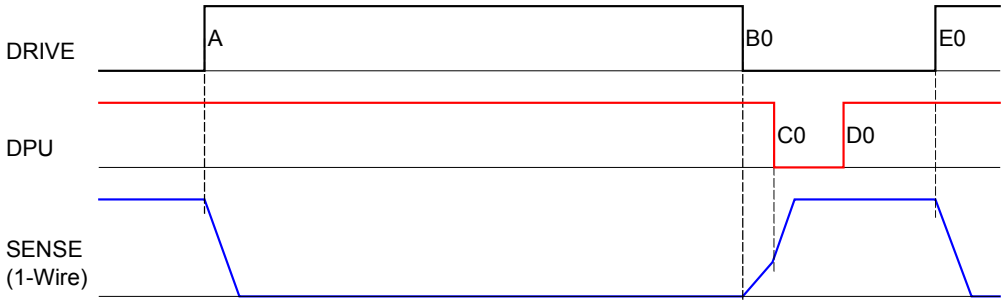
COMMUNICATION TIME SLOTS

Write Zero Time Slot

The write zero time slot transmits a 0-bit on the 1-Wire line. Figure 3 shows the 1-Wire waveform. To generate the write zero time slot, the DRIVE signal is activated for a duration from A to B0. Starting at A, the voltage on the 1-Wire ramps down to 0V. As DRIVE becomes inactive at B0, the voltage on the 1-Wire line starts rising. Shortly after B0, the dynamic pullup DPU is activated (point C0). This quickly pulls the 1-Wire line to 5V. At D0 the dynamic pullup ends. The next time slot or a reset/presence detect sequence may follow at E0.

A write zero time slot does not require sampling the data line. Therefore Figure 3 does not show any sampling point. However, it is definitely permissible to sample the 1-Wire line at the same point in time as with a read time slot (figure 4 or 5). The sampled logic state will always be 0, indicating that the circuit actually writes a 0 to the 1-Wire line. The duration from A to C0 is equivalent to the sum of t_F (fall time) and t_{W0L} (write zero low time). The time from C0 to E0 is called recovery time t_{REC}. Data sheets specify t_{W0L} and a minimum value for t_{REC}. The time from A to E0 is also referred to as time slot duration t_{SLOT}.

Figure 3. WRITE ZERO TIME SLOT



Recommended Timing Values for Write Zero Time Slot

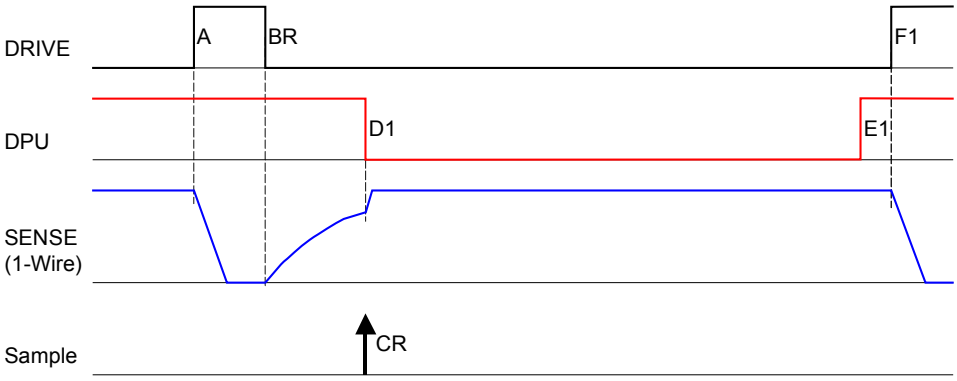
A to B0	B0 to C0	C0 to D0	A to E0
60µs	2µs	16µs	80µs

Write One/Read Time Slot (Read One)

The write one time slot transmits a 1-bit on the 1-Wire line. Figure 4 shows the 1-Wire waveform. Reading a 1-bit from the 1-Wire line results in exactly the same waveform as writing a 1-bit. Therefore, the write one and read one case are combined and discussed as a single case. To generate the write one or read time slot, the DRIVE signal is activated for a duration from A to BR. Starting at A, the voltage on the 1-Wire ramps down to 0V. As DRIVE becomes inactive at BR, in the case of reading or writing a 1-bit, the voltage on the 1-Wire line starts rising. At CR the status on the 1-Wire is sampled. Since the bit read is a 1, the dynamic pullup is activated immediately, lasting from D1 to E1. This quickly pulls the 1-Wire line to 5V. The next time slot or a reset/presence detect sequence may begin at F1.

The sampling point CR must be chosen to hit the master sampling window, which is determined by the timing of the fastest 1-Wire device. In data sheets this window is called t_{MSR}. The timing reference for t_{MSR} begins when the 1-Wire device detects logic LOW level after the beginning of the time slot. In Figure 4 this reference point is approximately A plus fall time t_F. The duration from A to BR is equivalent to the sum of t_F (fall time) and t_{RL} (read low time). Data sheets specify t_{RL} (equal to t_{W1L}) and t_{MSR}. The time from A to F1 is also referred to as time slot duration t_{SLOT}.

Figure 4. WRITE ONE/READ TIME SLOT (READ ONE)



Recommended Timing Values for Write One/Read Time Slot (Read One)

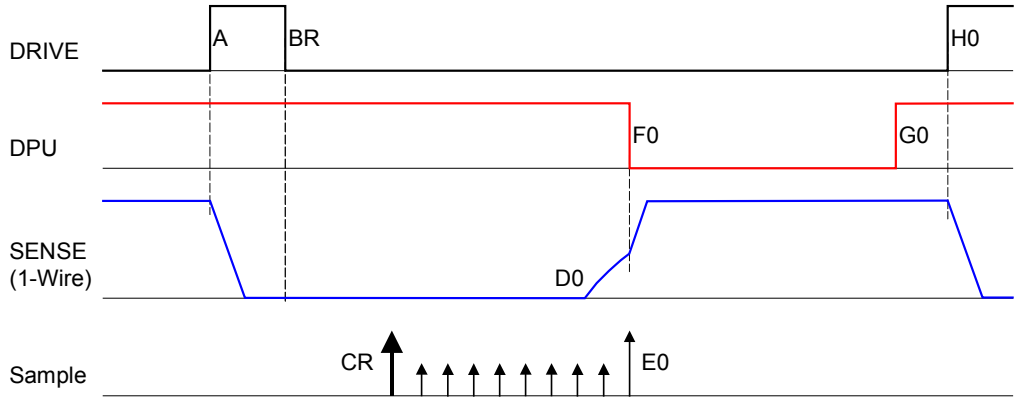
A to BR	A to CR	CR to D1	D1 to E1	A to F1
9µs	18µs	0 to 2µs	60µs	80µs

Read Time Slot (Read Zero)

The read zero time slot is a read time slot that reads a 0-bit from the 1-Wire line. Figure 5 shows the 1-Wire waveform. To generate the read time slot, the DRIVE signal is activated for a duration from A to BR. Starting at A, the voltage on the 1-Wire ramps down to 0V. To send a 0-bit, a 1-Wire device starts pulling the 1-Wire line low after A but before BR. The voltage on the 1-Wire line, therefore, is first driven low by the 1-Wire master and then remains held at a logic low by one or more 1-Wire devices. When BR has occurred, the master pulldown is turned off. At CR the status on the 1-Wire is sampled. Since the bit read is a 0, the 1-Wire is sampled repeatedly. At D0 the 1-Wire device stops pulling the line low, which allows the voltage to rise. A subsequent sampling at E0 determines that the line has reached logic high level. Now the dynamic pullup is activated, lasting from F0 to G0. This quickly pulls the 1-Wire line to 5V. The next time slot or a reset/presence detect sequence may begin at H0.

The sampling point CR is the same as with the write one/read time slot. The distance between the subsequent sampling points should be as short as the microcontroller and software allow. The time from A to H0 is also referred to as time slot duration t_{SLOT}.

Figure 5. READ TIME SLOT (READ ZERO)



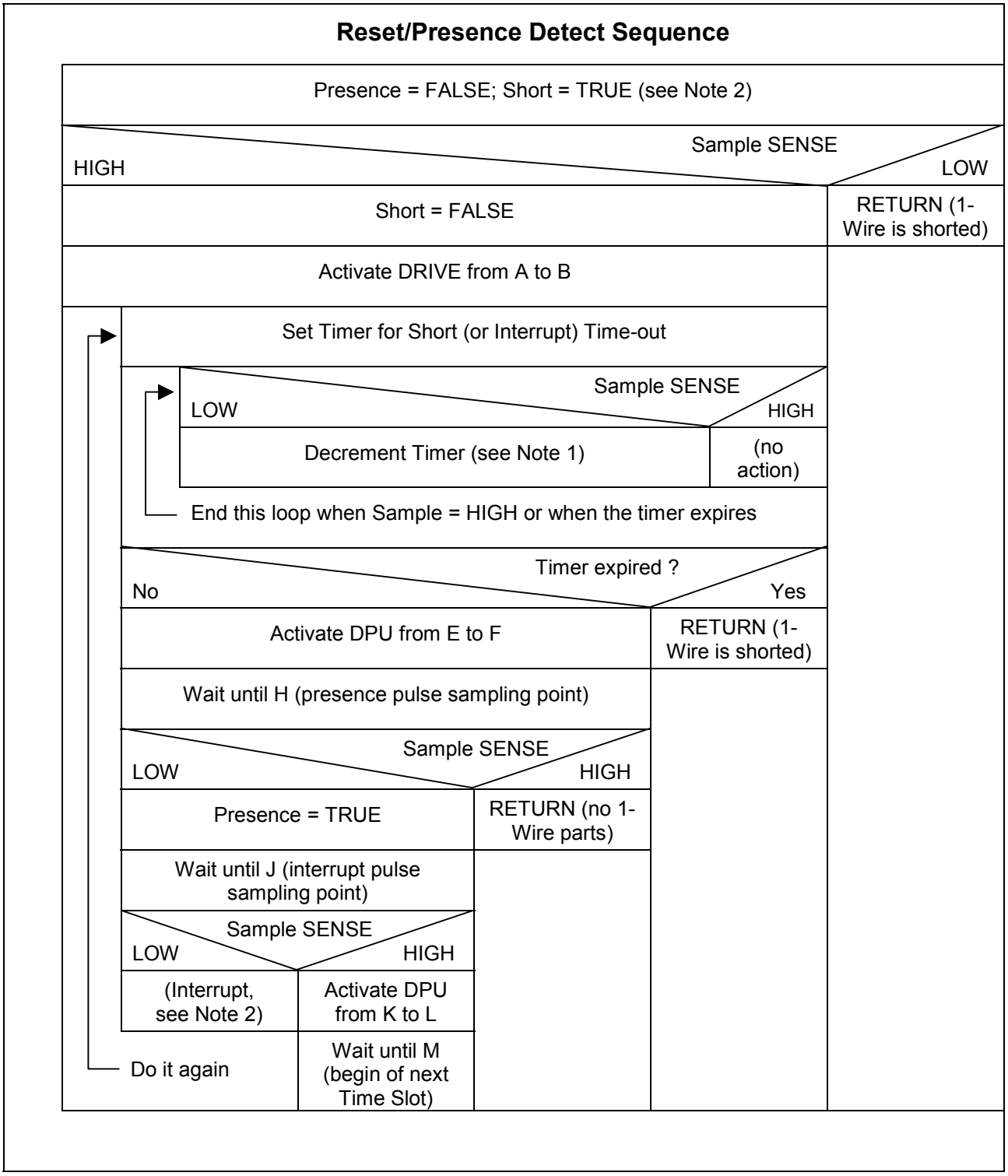
Recommended Timing Values for Read Time Slot (Read Zero)

A to BR	A to CR	E0 to F0	CR to G0	A to H0
9µs	18µs	0 to 2µs	60µs	82µs

PRACTICAL CONSIDERATIONS

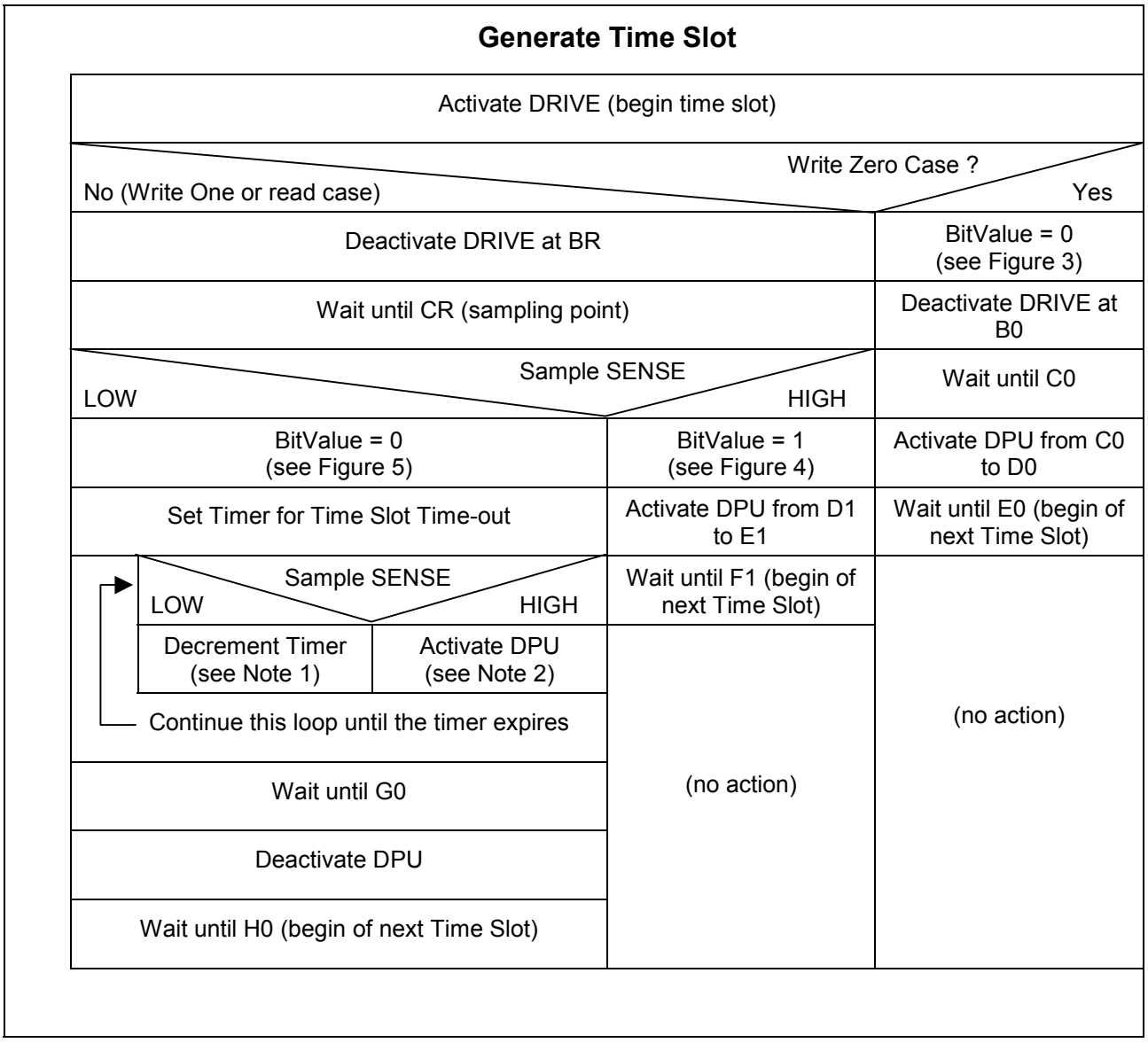
The structure of the signals that control the Advanced 1-Wire Network Driver is relatively complex. The algorithms, however, are straightforward. For this reason, this driver is typically implemented in software, using a microcontroller that is fast enough to generate the signals in **real-time**. The flow charts given below assist in implementing the advanced driver using any suitable microcontroller that the user is familiar with. The execution time of every command at the user-specified crystal frequency must be taken into account to generate the proper timing.

SOFTWARE FLOW CHARTS



Note 1: Decrementing is necessary only if the timer is implemented as a counter rather than a real timer. The timer should expire after 5000µs.

Note 2: *Presence* and *Short* are logical variables that report to the superordinated program the result of the reset/presence detect sequence. Interrupt is not reported as a variable since there is only one 1-Wire chip that can generate interrupts (DS1994/DS2404) and the use of interrupts can considerably reduce the effective speed of a 1-Wire network.



This flow chart assumes that there is a logical input variable that controls whether to generate a write zero or read time slot. The write one time slot is the same as a read time slot. The bit variable *BitValue* reports the result of the time slot to the superordinated program.

Note 1: Decrementing is necessary only if the timer is implemented as a counter rather than a real timer. The timer should expire after 45µs.

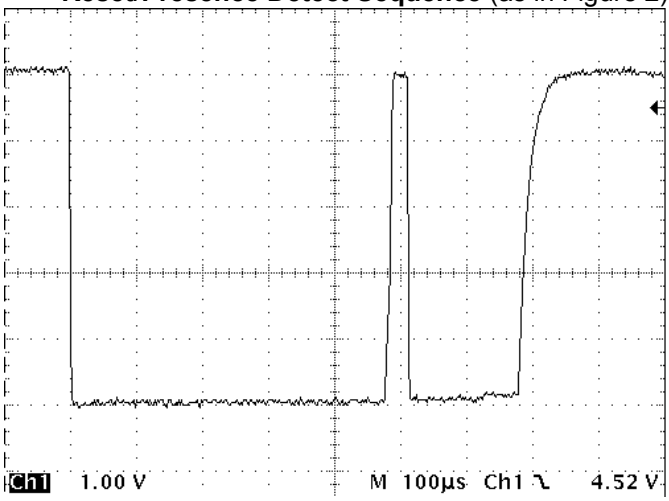
Note 2: According to the flow chart, DPU will repeatedly be activated before the timer expires. This is acceptable since activating a signal that is already active doesn't change the state of that signal. If desired, one can test whether DPU is already active, and if so, not activate it again while performing the loop.

PERFORMANCE EXAMPLES

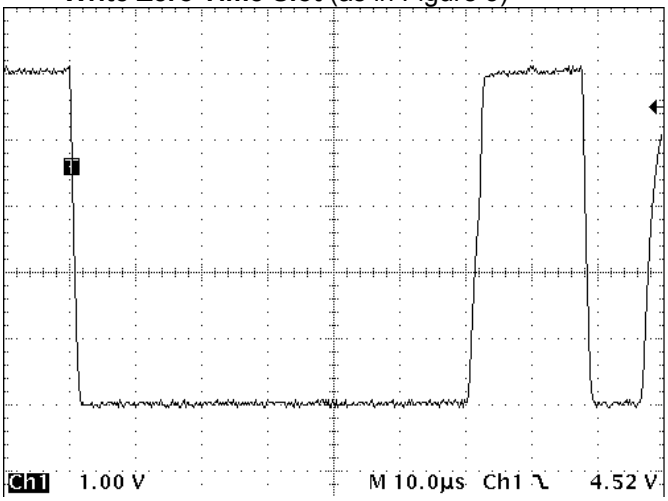
The scope traces on the next page show 1-Wire signals generated by the driver as described in this document. When verifying the signals, especially at the far end of a cable, it is necessary to use a differential probe, leaving the probe's ground reference floating. Otherwise the probe's ground connection would bypass the 1-Wire ground reference and change the topology of the system. If a differential probe is not available, one must isolate the oscilloscope-ground from mains-ground through a transformer or use a battery-operated oscilloscope. Alternatively one could disconnect the safety-ground of the oscilloscope's power supply cable.

SCOPE TRACES

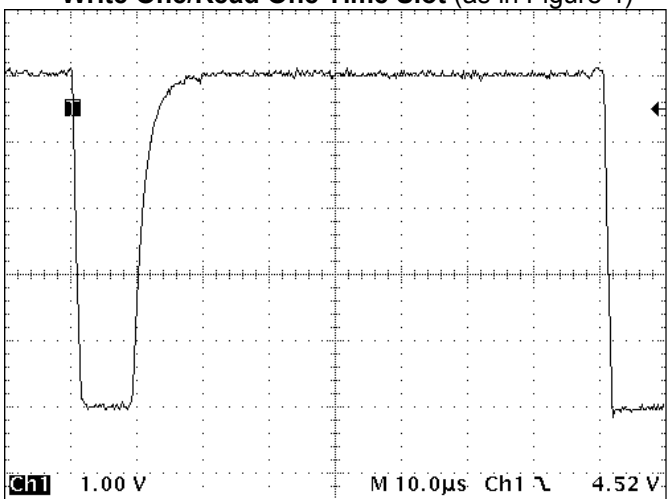
Reset/Presence Detect Sequence (as in Figure 2)



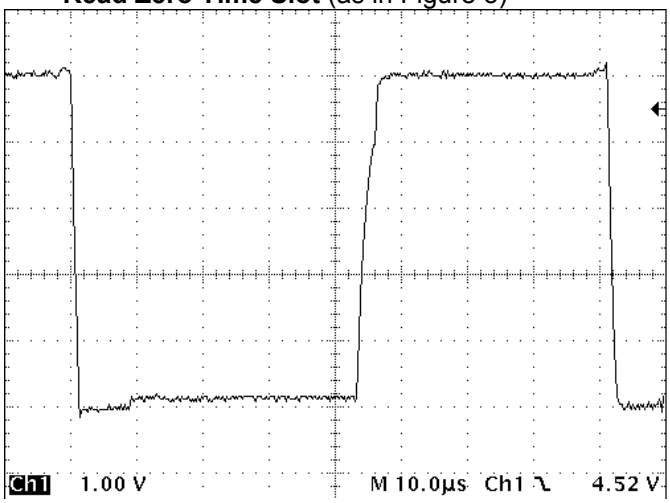
Write Zero Time Slot (as in Figure 3)



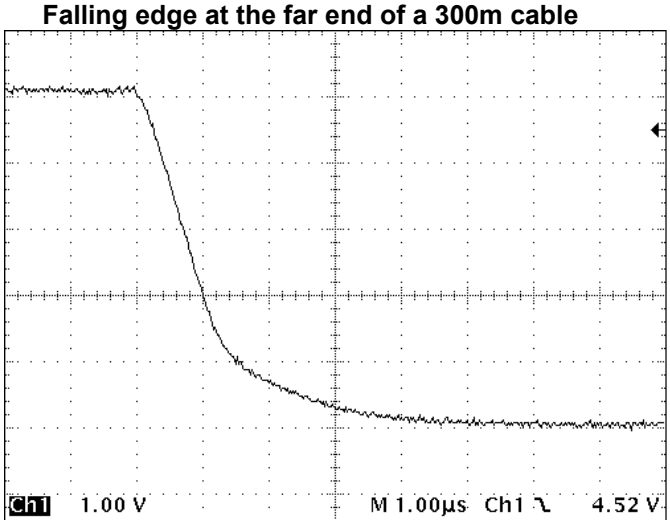
Write One/Read One Time Slot (as in Figure 4)



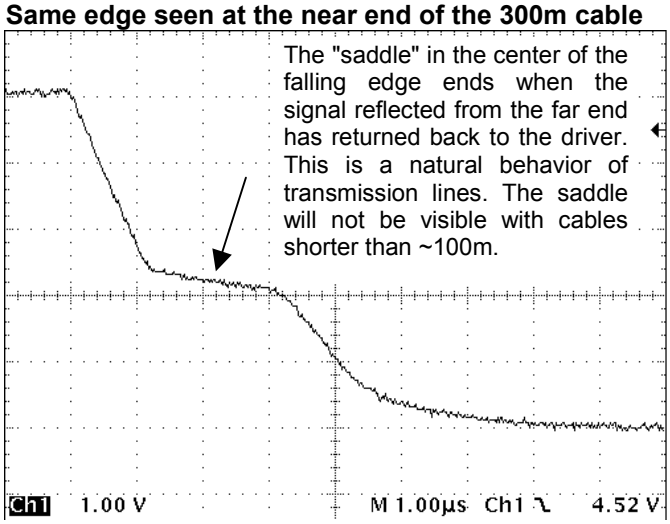
Read Zero Time Slot (as in Figure 5)



Falling edge at the far end of a 300m cable



Same edge seen at the near end of the 300m cable



Note: A product similar to the *Advanced 1-Wire Line Driver* is manufactured by Southwind Enterprises. See http://ibuttonlink.com/ for technical details and ordering information.