13.19 Radio Registers

This section describes all RF registers used for control and status for the radio.

0xDF2F: IOCFG2 - Radio Test Signal Configuration (P1_7)

Bit	Field Name	Reset	R/W	Description
7		-	R0	Not used
6	GDO2_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	000000	R/W	Debug output on P1_7 pin. See Table 73 for a description of internal signals which can be output on this pin for debug purpose

0xDF30: IOCFG1 - Radio Test Signal Configuration (P1_6)

Bit	Field Name	Reset	R/W	Description	
7	GDO_DS	0	R/W	Drive strength control for I/O pins in output mode. Selects output drive capability to account for low I/O supply voltage VDD on pin DVDD	
				0	Minimum drive capability. VDD equal or greater than 2.6 V
				1	Maximum drive capability. VDD less than 2.6 V
6	GDO1_INV	0	R/W	Invert output	
				0	Active high
				1	Active low
5:0	GDO1_CFG[5:0]	000000	R/W	Debug output on P1_6 pin. See Table 73 for a description of internal signals which can be output on this pin for debug purpose	

0xDF31: IOCFG0 - Radio Test Signal Configuration (P1_5)

Bit	Field Name	Reset	R/W	Description
7		-	R0	Not used
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	000000	R/W	Debug output on P1_5 pin. See Table 73 for a description of internal signals which can be output on this pin for debug purpose.

0xDF00: SYNC1 - Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	0xD3	R/W	8 MSB of 16-bit sync word

0xDF01: SYNC0 - Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	0x91	R/W	8 LSB of 16-bit sync word

0xDF02: PKTLEN - Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	0xFF	R/W	Indicates the packet length when fixed length packets are enabled. If variable length packets are used, this value indicates the maximum length packets allowed

0xDF03: PKTCTRL1 - Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7:5	PQT[2:0]	000	R/W	Preamble quality estimator threshold. The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 8 each time a bit is received that is the same as the last bit. A threshold of 4·PQT for this counter is used to gate sync word detection. When PQT=0 a sync word is always accepted
4:3		-	R0	Not used
2	APPEND_STATUS	1	R/W	When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain RSSI and LQI values, as well as the CRC OK flag
1:0	ADR_CHK[1:0]	00	R/W	Controls address check configuration of received packages.
				00 No address check
				01 Address check, no broadcast
				10 Address check, 0 (0x00) broadcast
				11 Address check, 0 (0x00) and 255 (0xFF) broadcast

0xDF04: PKTCTRL0 - Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7		-	R0	Not used
6	WHITE_DATA	1	R/W	Whitening enable. Data whitening can only be used when PKTCTRL0.CC2400_EN=0 (default).
				0 Disabled
				1 Enabled
5:4	PKT_FORMAT[1:0]	00	R/W	Packet format of RX and TX data
				00 Normal mode
				01 Reserved
				10 Random TX mode; sends random data using PN9 generator. Used for test. Works as normal mode, setting 00, in RX.
				11 Reserved
3		0	R/W	Reserved. Always write 0
2	CRC_EN	1	R/W	CRC calculation in TX and CRC check in RX enable
				0 Disable
				1 Enable
1:0	LENGTH_CONFIG[1:0]	01	R/W	Packet Length Configuration
				00 Fixed packet length mode. Length configured in PKTLEN register
				01 Variable packet length mode. Packet length configured by the first byte after sync word
				10 Reserved
				11 Reserved

0xDF05: ADDR - Device Address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0x00	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0xDF06: CHANNR - Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0x00	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0xDF07: FSCTRL1 - Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:6		-	R0	Not used
5		0	R/W	Reserved
4:0	FREQ_IF[4:0]	01111	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = \frac{f_{ref}}{2^{10}} \cdot FREQ\_IF$ The default value gives an IF frequency of 381 kHz when f_{Ref} = 26 MHz and 352 kHz when f_{Ref} = 24 MHz.

0xDF08: FSCTRL0 - Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0x00	R/W	Frequency offset added to the base frequency before being used by the FS. (2's complement). Resolution is $f_{Ref}/2^{14}$ Range is ±202 kHz to ±209 kHz for CC1110Fx and ±186 kHz for CC1111Fx

0xDF09: FREQ2 - Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	01	R	FREQ[23:22]
5:0	FREQ[21:16]	011110	R/W	FREQ[23:0] is the base frequency for the frequency synthesizer in increments of $f_{Ref}/2^{16}$. $f_{carrier} = \frac{f_{ref}}{2^{16}} \cdot FREQ[23:0]$

0xDF0A: FREQ1 - Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	11000100	R/W	Ref. `FREQ2` register

0xDF0B: FREQ0 - Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	11101100	R/W	Ref. `FREQ2` register

0xDF0C: MDMCFG4 - Modem configuration

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	10	R/W	
5:4	CHANBW_M[1:0]	00	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. $BW_{channel} = \frac{f_{ref}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$ The default values give 203 kHz channel filter bandwidth when f_{Ref} = 26 MHz and 188 kHz when f_{Ref} = 24 MHz.
3:0	DRATE_E[3:0]	1100	R/W	The exponent of the user specified symbol rate.

0xDF0D: MDMCFG3 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	0x22	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{ref}$ The default values give a data rate of 115.051 kBaud when f_{Ref} = 26 MHz and 106.201 kHz when f_{Ref} = 24 MHz.

0xDF0E: MDMCFG2 - Modem Configuration

Bit	Field Name	Reset	R/W	Description		
7	DEM_DCFILT_OFF	0	R/W	Disable digital DC blocking filter before demodulator. The recommended IF frequency changes when the DC blocking is disabled. Please use SmartRF® Studio [9] to calculate correct register setting.		
				0	Enable	Better Sensitivity
				1	Disable	Current optimized. Only for data rates ≤ 100 kBaud
6:4	MOD_FORMAT[2:0]	000	R/W	The modulation format of the radio signal		
				000	2-FSK	
				001	GFSK	
				010	Reserved	
				011	ASK/OOK	
				100	Reserved	
				101	Reserved	
				110	Reserved	
				111	MSK	
				Note that MSK is only supported for data rates above 26 kBaud and GFSK, ASK , and OOK is only supported for data rate up until 250 kBaud. MSK cannot be used if Manchester encoding/decoding is enabled.		
3	MANCHESTER_EN	0	R/W	Manchester encoding/decoding enable		
				0	Disable	
				1	Enable	
				Note that Manchester encoding/decoding cannot be used at the same time as using the FEC/Interleaver option or when using MSK modulation.		
2:0	SYNC_MODE[2:0]	010	R/W	Sync-word qualifier mode. The values 000 and 100 disables preamble and sync word transmission in TX and preamble and sync word detection in RX. The values 001, 010, 101 and 110 enables 16-bit sync word transmission in TX and 16-bits sync word detection in RX. Only 15 of 16 bits need to match in RX when using setting 001 or 101. The values 011 and 111 enables repeated sync word transmission in TX and 32-bits sync word detection in RX (only 30 of 32 bits need to match).		
				000	No preamble/sync	
				001	15/16 sync word bits detected	
				010	16/16 sync word bits detected	
				011	30/32 sync word bits detected	
				100	No preamble/sync, carrier-sense above threshold	
				101	15/16 + carrier-sense above threshold	
				110	16/16 + carrier-sense above threshold	
				111	30/32 + carrier-sense above threshold	

0xDF0F: MDMCFG1 - Modem Configuration

Bit	Field Name	Reset	R/W	Description	
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload. FEC is only supported for fixed packet length mode, i.e. PKTCTRL0.LENGTH_CONFIG=0	
				0	Disable
				1	Enable
6:4	NUM_PREAMBLE[2:0]	010	R/W	Sets the minimum number of preamble bytes to be transmitted	
				000	2
				001	3
				010	4
				011	6
				100	8
				101	12
				110	16
				111	24
3:2		-	R0	Not used	
1:0	CHANSPC_E[1:0]	10	R/W	2 bit exponent of channel spacing	

0xDF10: MDMCFG0 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	0xF8	R/W	8-bit mantissa of channel spacing (initial 1 assumed). The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{ref}}{2^{18}} \cdot (256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E}$ The default values give 199.951 kHz channel spacing when f_{Ref} = 26 MHz and 184.570 kHz when f_{Ref} = 24 MHz.

0xDF11: DEVIATN - Modem Deviation Setting

Bit	Field Name	Reset	R/W	Description	
7		-	R0	Not used	
6:4	DEVIATION_E[2:0]	100	R/W	Deviation exponent	
3		-	R0	Not used	
2:0	DEVIATION_M[2:0]	111	R/W	TX	
				2-FSK/ GFSK	Specifies the nominal frequency deviation from the carrier frequency for a '0' (-DEVIATN) and a '1' (+DEVIATN) in a mantissa-exponent format. The resulting deviation is given by: $f_{dev} = \frac{f_{ref}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$ The default values give ±47.607 kHz deviation when f_{Ref} = 26 MHz and 43.945 kHz when f_{Ref} = 24 MHz.
				MSK	Specifies the fraction of a symbol period (1/8-8/8) during which a phase change occurs ('0': +90deg, '1': -90deg). Refer to the SmartRF® Studio software [9] for correct DEVIATN setting when using MSK.
				ASK	This settings has no effect
				RX	
				2-FSK/ GFSK	Specifies the expected frequency deviation of incoming signal, must be approximately right for demodulation to be performed reliably and robustly
				MSK/ASK	This settings has no effect

0xDF12: MCSM2 - Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:5		-	R0	Not used
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense). For ASK/OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.
3	RX_TIME_QUAL	0	R/W	When the RX_TIME timer expires the chip stays in RX mode if sync word is found when RX_TIME_QUAL=0, or either sync word is found or PQT is reached when RX_TIME_QUAL=1.
2:0	RX_TIME[2:0]	111	R/W	Timeout for sync word search in RX. The timeout is relative to the programmed t_{Event0}.

The RX timeout in µs is given by EVENT0·C(RX_TIME, WOR_RES) ·26/X, where C is given by the table below and X is the reference frequency (f_{Ref}) in MHz:

RX_TIME[2:0]	WOR_RES=0	WOR_RES=1	WOR_RES=2	WOR_RES=3
000	3.6058	18.0288	32.4519	46.8750
001	1.8029	9.0144	16.2260	23.4375
010	0.9014	4.5072	8.1130	11.7188
011	0.4507	2.2536	4.0565	5.8594
100	0.2254	1.1268	2.0282	2.9297
101	0.1127	0.5634	1.0141	1.4648
110	0.0563	0.2817	0.5071	0.7324
111	Until end of packet			

As an example, EVENT0 = 34666, WOR_RES = 0 and RX_TIME = 6 corresponds to 1.96 ms RX timeout

0xDF13: MCSM1 - Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description	
7:6		-	R0	Not used	
5:4	CCA_MODE[1:0]	11	R/W	Selects CCA_MODE; Reflected in CCA signal	
				00	Always
				01	If RSSI below threshold
				10	Unless currently receiving a packet
				11	If RSSI below threshold unless currently receiving a packet
3:2	RXOFF_MODE[1:0]	00	R/W	Select what should happen (next state) when a packet has been received	
				00	IDLE
				01	FSTXON
				10	TX
				11	Stay in RX
				It is not possible to set RXOFF_MODE to be TX or FSTXON and at the same time use CCA.	
1:0	TXOFF_MODE[1:0]	00	R/W	Select what should happen (next state) when a packet has been sent (TX)	
				00	IDLE
				01	FSTXON
				10	Stay in TX (start sending preamble)
				11	RX

0xDF14: MCSM0 - Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description	
7:6		-	R0	Not used	
5:4	FS_AUTOCAL[1:0]	00	R/W	Select calibration mode (when to calibrate)	
				00	Never (manually calibrate using SCAL strobe)
				01	When going from IDLE to RX or TX (or FSTXON)
				10	When going from RX or TX back to IDLE automatically
				11	Every 4th time when going from RX or TX to IDLE automatically
3		0	R/W	Reserved. Refer to SmartRF® Studio software [9] for settings.	
2		1	R/W	Reserved. Refer to SmartRF® Studio software [9] for settings.	
1:0	CLOSE_IN_RX[1:0]	00	R/W	Sets RX attenuation. Used in order to avoid saturation in RX when two or more chips are close (within ~3 m). RX attenuation, typical values:	
				00	0 dB
				01	6 dB
				10	12 dB
				11	18 dB

0xDF15: FOCCFG - Frequency Offset Compensation Configuration

Bit	Field Name	Reset	R/W	Description
7		-	R0	Not used
6		1	R/W	Reserved. Always write 0
5	FOC_BS_CS_GATE	1	R/W	If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CARRIER_SENSE signal goes high.
4:3	FOC_PRE_K[1:0]	10	R/W	The frequency compensation loop gain to be used before a sync word is detected. 00 *K* 01 *2K* 10 *3K* 11 *4K*
2	FOC_POST_K	1	R/W	The frequency compensation loop gain to be used after a sync word is detected. 0 Same as `FOC_PRE_K` 1 *K/2*
1:0	FOC_LIMIT[1:0]	10	R/W	The saturation point for the frequency offset compensation algorithm: 00 ±0 (no frequency offset compensation) 01 $\pm BW_{CHAN} / 8$ 10 $\pm BW_{CHAN} / 4$ 11 $\pm BW_{CHAN} / 2$ Frequency offset compensation is not supported for ASK/OOK; Always use `FOC_LIMIT=0` with these modulation formats.

0xDF16: BSCFG - Bit Synchronization Configuration

Bit	Field Name	Reset	R/W	Description	
7:6	BS_PRE_KI[1:0]	01	R/W	The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):	
				00	K_I
				01	$2K_I$
				10	$3K_I$
				11	$4K_I$
5:4	BS_PRE_KP[1:0]	10	R/W	The clock recovery feedback loop proportional gain to be used before a sync word is detected	
				00	K_P
				01	$2K_P$
				10	$3K_P$
				11	$4K_P$
3	BS_POST_KI	1	R/W	The clock recovery feedback loop integral gain to be used after a sync word is detected.	
				0	Same as `BS_PRE_KI`
				1	$K_I/2$
2	BS_POST_KP	1	R/W	The clock recovery feedback loop proportional gain to be used after a sync word is detected.	
				0	Same as `BS_PRE_KP`
				1	K_P
1:0	BS_LIMIT[1:0]	00	R/W	The saturation point for the data rate offset compensation algorithm:	
				00	±0 (No data rate offset compensation performed)
				01	±3.125% data rate offset
				10	±6.25% data rate offset
				11	±12.5% data rate offset

0xDF17: AGCCTRL2 - AGC Control

Bit	Field Name	Reset	R/W	Description	
7:6	MAX_DVGA_GAIN[1:0]	00	R/W	Reduces the maximum allowable DVGA gain.	
				00	All gain settings can be used
				01	The highest gain setting can not be used
				10	The 2 highest gain settings can not be used
				11	The 3 highest gain settings can not be used
5:3	MAX_LNA_GAIN[2:0]	000	R/W	Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.	
				000	Maximum possible LNA + LNA 2 gain
				001	Approx. 2.6 dB below maximum possible gain
				010	Approx. 6.1 dB below maximum possible gain
				011	Approx. 7.4 dB below maximum possible gain
				100	Approx. 9.2 dB below maximum possible gain
				101	Approx. 11.5 dB below maximum possible gain
				110	Approx. 14.6 dB below maximum possible gain
				111	Approx. 17.1 dB below maximum possible gain
2:0	MAGN_TARGET[2:0]	011	R/W	These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).	
				000	24 dB
				001	27 dB
				010	30 dB
				011	33 dB
				100	36 dB
				101	38 dB
				110	40 dB
				111	42 dB

0xDF18: AGCCTRL1 - AGC Control

Bit	Field Name	Reset	R/W	Description	
7		-	R0	Not used	
6	AGC_LNA_PRIORITY	1	R/W	Selects between two different strategies for LNA and LNA2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA2 gain is decreased to minimum before decreasing LNA gain.	
5:4	CARRIER_SENSE_REL_THR[1:0]	00	R/W	Sets the relative change threshold for asserting carrier sense	
				00	Relative carrier sense threshold disabled
				01	6 dB increase in RSSI value
				10	10 dB increase in RSSI value
				11	14 dB increase in RSSI value
3:0	CARRIER_SENSE_ABS_THR[3:0]	0000	R/W	Sets the absolute RSSI threshold for asserting carrier sense (Equal to channel filter amplitude when AGC has not decreased gain). The 2-complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.	
				1000 (–8)	Absolute carrier sense threshold disabled
				1001 (–7)	7 dB below MAGN_TARGET setting
				…	…
				1111 (–1)	1 dB below MAGN_TARGET setting
				0000 (0)	At MAGN_TARGET setting
				0001 (1)	1 dB above MAGN_TARGET setting
				…	…
				0111 (7)	7 dB above MAGN_TARGET setting

0xDF19: AGCCTRL0 - AGC Control

Bit	Field Name	Reset	R/W	Description	
7:6	HYST_LEVEL[1:0]	10	R/W	Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determines gain changes).	
				00	No hysteresis, small symmetric dead zone, high gain
				01	Low hysteresis, small asymmetric dead zone, medium gain
				10	Medium hysteresis, medium asymmetric dead zone, medium gain
				11	Large hysteresis, large asymmetric dead zone, low gain
5:4	WAIT_TIME[1:0]	01	R/W	Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples.	
				00	8
				01	16
				10	24
				11	32
3:2	AGC_FREEZE[1:0]	00	R/W	Controls when the AGC gain should be frozen.	
				00	Normal operation. Always adjust gain when required.
				01	The gain setting is frozen when a sync word has been found.
				10	Manually freeze the analog gain setting and continue to adjust the digital gain.
				11	Manually freezes both the analog and the digital gain settings. Used for manually overriding the gain.
1:0	FILTER_LENGTH[1:0]	01	R/W	Sets the averaging length for the amplitude from the channel filter. Sets the OOK/ASK decision boundary for OOK/ASK reception. Please use the SmartRF® Studio software [9] for recommended settings.	
				00	8
				01	16
				10	32
				11	64

0xDF1A: FREND1 - Front End RX Configuration

Bit	Field Name	Reset	R/W	Description
7:6	LNA_CURRENT[1:0]	01	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	01	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	01	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	10	R/W	Adjusts current in mixer

0xDF1B: FREND0 - Front End TX Configuration

Bit	Field Name	Reset	R/W	Description
7:6		-	R0	Not used
5:4	LODIV_BUF_CURRENT_TX[1:0]	01	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF® Studio software [9].
3		-	R0	Not used
2:0	PA_POWER[2:0]	000	R/W	Selects PA power setting. This value is an index to the PATABLE (`PA_TABLE7` - `PA_TABLE0` registers), which can be programmed with up to 8 different PA settings. In ASK mode, this selects the PATABLE index to use when transmitting a '1'. PATABLE index zero is used in ASK when transmitting a '0'. The PATABLE settings from index '0' to the PA_POWER value are used for ASK TX shaping, and for power ramp-up/ramp-down at the start/end of transmission in all TX modulation formats.

0xDF1C: FSCAL3 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	10	R/W	Frequency synthesizer calibration configuration. The value to write in this register before calibration is given by the SmartRF® Studio software [9].
5:4	CHP_CURR_CAL_EN[1:0]	10	R/W	Disable charge pump calibration stage when 0
3:0	FSCAL3[3:0]	1001	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $IOUT=I_0 \cdot 2^{FSCAL3[3:0]/4}$ Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting `FSCAL3`, `FSCAL2` and `FSCAL1` register values. Between each frequency hop, calibration can be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values corresponding to the next RF frequency.
Note: This register will be in its reset state when returning to active mode from PM2 and PM3.				

0xDF1D: FSCAL2 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6		-	R0	Not used
5	VCO_CORE_H_EN	0	R/W	Select VCO 0 Low 1 High
4:0	FSCAL2[4:0]	01010	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting `FSCAL3`, `FSCAL2` and `FSCAL1` register values. Between each frequency hop, calibration can be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values corresponding to the next RF frequency.
Note: This register will be in its reset state when returning to active mode from PM2 and PM3.				

0xDF1E: FSCAL1 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6		-	R0	Not used
5:0	FSCAL1[5:0]	100000	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting `FSCAL3`, `FSCAL2` and `FSCAL1` register values. Between each frequency hop, calibration can be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values corresponding to the next RF frequency.
Note: This register will be in its reset state when returning to active mode from PM2 and PM3.				

0xDF1F: FSCAL0 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7		-	R0	Not used
6:0	FSCAL0[6:0]	0001101	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF® Studio software [9].

0xDF23: TEST2 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	0x88	R/W	At low data rates, the sensitivity can be improved by changing it to 0x81 (`MDMCFG2.DEM_DCFILT_OFF` should be 0).

0xDF24: TEST1 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	0x11	R/W	Always set this register to 0x31 when being in TX. At low data rates, the sensitivity can be improved by changing it to 0x35 in RX. (`MDMCFG2.DEM_DCFILT_OFF` should be 0).

0xDF25: TEST0 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	000010	R/W	The value to use in this register is given by the SmartRF® Studio software [9].
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	The value to use in this register is given by the SmartRF® Studio software [9].

0xDF27: PA_TABLE7 - PA Power Setting 7

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE7[7:0]	0x00	R/W	Power amplifier output power setting 7

0xDF28: PA_TABLE6 - PA Power Setting 6

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE6[7:0]	0x00	R/W	Power amplifier output power setting 6

0xDF29: PA_TABLE5 - PA Power Setting 5

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE5[7:0]	0x00	R/W	Power amplifier output power setting 5

0xDF2A: PA_TABLE4 - PA Power Setting 4

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE4[7:0]	0x00	R/W	Power amplifier output power setting 4

0xDF2B: PA_TABLE3 - PA Power Setting 3

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE3[7:0]	0x00	R/W	Power amplifier output power setting 3

0xDF2C: PA_TABLE2 - PA Power Setting 2

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE2[7:0]	0x00	R/W	Power amplifier output power setting 2

0xDF2D: PA_TABLE1 - PA Power Setting 1

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE1[7:0]	0x00	R/W	Power amplifier output power setting 1

0xDF2E: PA_TABLE0 - PA Power Setting 0

Bit	Field Name	Reset	R/W	Description
7:0	PA_TABLE0[7:0]	0x00	R/W	Power amplifier output power setting 0

0xDF36: PARTNUM - Chip ID[15:8]

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	0x01 CC1110Fx 0x11 CC1111Fx	R	Chip part number

0xDF37: VERSION - Chip ID[7:0]

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	0x03	R	Chip version number.

0xDF38: FREQEST - Frequency Offset Estimate from Demodulator

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST	0x00	R	The estimated frequency offset (2's complement) of the carrier. Resolution is $f_{Ref}/2^{14}$ Range is ±202 kHz to ±209 kHz for CC1110Fx and ±186 kHz for CC1111Fx Frequency offset compensation is only supported for 2-FSK, GFSK, and MSK modulation. This register will read 0 when using ASK or OOK modulation.

0xDF39: LQI - Demodulator Estimate for Link Quality

Bit	Field Name	Reset	R/W	Description
7	CRC_OK	0	R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0	LQI_EST[6:0]	0000000	R	The Link Quality Indicator estimates how easily a received signal can be demodulated. Calculated over the 64 symbols following the sync word.

0xDF3A: RSSI - Received Signal Strength Indication

Bit	Field Name	Reset	R/W	Description
7:0	RSSI	0x80	R	Received signal strength indicator

0xDF3B: MARCSTATE - Main Radio Control State Machine State

Bit	Field Name	Reset	R/W	Description		
7:5		-	R0	Not used		
4:0	MARC_STATE[4:0]	0001	R	Main Radio Control FSM State		
				Value	State Name	State (Figure 55, Page203)
				00000	SLEEP	SLEEP
				00001	IDLE	IDLE
				00010	Not used	
				00011	VCOON_MC	MANCAL
				00100	REGON_MC	MANCAL
				00101	MANCAL	MANCAL
				00110	VCOON	FS_WAKEUP
				00111	REGON	FS_WAKEUP
				01000	STARTCAL	CALIBRATE
				01001	BWBOOST	SETTLING
				01010	FS_LOCK	SETTLING
				01011	IFADCON	SETTLING
				01100	ENDCAL	CALIBRATE
				01101	RX	RX
				01110	RX_END	RX
				01111	RX_RST	RX
				10000	TXRX_SWITCH	TXRX_SETTLING
				10001	RX_OVERFLOW	RX_OVERFLOW
				10010	FSTXON	FSTXON
				10011	TX	TX
				10100	TX_END	TX
				10101	RXTX_SWITCH	RXTX_SETTLING
				10110	TX_UNDERFLOW	TX_UNDERFLOW

0xDF3C: PKTSTATUS - Packet Status

Bit	Field Name	Reset	R/W	Description
7	CRC_OK	0	R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS	0	R	Carrier sense
5	PQT_REACHED	0	R	Preamble Quality reached
4	CCA	0	R	Channel is clear
3	SFD	0	R	Asserted when sync word has been sent / received, and de-asserted at the end of the packet. In RX, this bit will de-assert when the optional address check fails or the radio enter RX_OVERFLOW state. In TX this bit will de-assert if the radio enters TX_UNDERFLOW state.
2:0		-	R0	Not used

0xDF3D: VCO_VC_DAC - Current Setting from PLL Calibration Module

Bit	Field Name	Reset	R/W	Description
7:0	VCO_VC_DAC[7:0]	0x94	R	Status register for test only.