CERAMATE APPROVAL SHEET

CUSTOMER : 金準數碼有限公司

BRAND : MXIC

PART : MX88V462UCG

CUSTOMER APPROVAL :

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MX88V462
Analog S-FPD Controller
Datasheet
(Preliminary Version)

Revision History

Version	Date	Author	Remark
0.10	2005/07/29	Jack Wu	Preliminary version
0.11	2005/8/16	Jack Wu	Correct Digital RGB input pin assignments

Content

Figure

1 General Description

1.1 General Description

MX88V462 is the low cost high performance solution for small and medium size LCD panel display. It accepts digital video input in 8/16-bit CCIR656/CCIR601, RGB565/666, and analog composite and S-video input. A flexible Timing controller (TCON) is embedded to supports variety analog LCD panel. It also includes programmable brightness, sharpness, contrast, saturation, hue, gamma and sharpness control for LCD display adjustment. Embedded AFE and TV decoder for TV input, embedded RGB DAC for low cost panel drive.

1.2 Application

- Portable DVD player with analog LCD panel
- Portable TV/DTV
- Car Entertainment System
- Rear Seat Display System

1.3 Main Feature

Features

- Data Processing
  - Support 8/16-bit CCIR-656 and CCIR-601 NTSC/PAL video standard
  - Support 16/18-bit digital RGB input
  - Built-in color space conversion
  - Programmable Contrast, Brightness, Saturation and Hue adjustment
  - Edge filter coefficient is fully programmable
  - Gamma adjustment coefficient is fully programmable
- Internal OSD Generator
  - 128 fixed characters and 64 programmable characters
  - Display 128 characters in valid display area.
  - Support Flip and Mirror functions
  - Composition of a character: 18 x 12 dots
  - Foreground color: 256 colors

    Selectable character-by-character or defined in sub window attribute registers

- Background color: 256 colors
  - Selectable character-by-character or defined in the sub window attribute registers
- Border color:
  - Only one color defined in the register
  - All charactersí border color is the same if the border switch is on.
- Two border type:
  - All direction character boundaries
  - Bottom-right character boundary
- Two border width:
  - One pixel width for all scale
  - Scale with OVS and OHS of OSD control register.
- Background can be transparent or opaque.
- Two read/write modes: single mode and burst mode.
- Horizontal/vertical scaling (x1, x2, x3, x4)
- Space:
  - Space position and size are programmable
  - Space can divide the main window into 4 sub windows. The 4 sub windowsí attribute is the same
- Shadow type
  - Bottom-right window boundary
- Shadow size
  - Shadow width and height are programmable
  - Shadow size of each window is the same
- Shadow color
  - Shadow color of each window is programmable respectively
- Main window display can be turn off or turn on
- 8 sub windows control
  - Sub window position is programmable respectively
  - Sub window size is programmable respectively
  - Sub window display can turn on or turn off respectively
  - Sub window attribute is programmable respectively. The attribute includes background color, foreground color and shadow color
- Blink period is programmable

- TV Decoder

- Support Macrovision copyright protected input with auto-detection and compensation
- Support NTSC, PAL and SECAM input
- 3 line adaptive comb filter
  a. Eliminates dot crawl from vertical or horizontal transitions
  b. Eliminates dot craw from single pixel lines.
  c. Eliminates false color from high frequency horizontal luma.
  d. No loss in horizontal or vertical chroma detail
  e. No loss in horizontal or vertical luma detail
  f. Performs well on real video images and on test patterns
- Adaptive horizontal PLL
  a. Automatically adjusts loop bandwidth for signal conditions
  b. Automatically detects VCR source and enters optimum tracking mode
  c. Automatically detects VCR special effects mode and compensates
  d. Comb filter automatically disabled when VCR source is detected
- Robust sync and dc setup acquisition
  a. DC setup and sync recovery is very robust even in the presence of noise, ghosting and unlock condition
  b. Automatic switch over to ì fineî mode operation once rough lock is acquired

- TCON
  - Built-in 3 channel RGB DAC with AMP
  - Embedded pattern generation
  - Built-in programmable Timing controller for flexible analog panel timing requirements
- MISC
  - Support external OSD generator interface
  - Embedded two channels 10 bit AFE with CLAMP and AGC
  - Embedded PLLs to generate clock for data-path and TV decoder
  - Support Autoloader for auto setting
- CPU Interface
  - Support 2-wire and 3-wire serial interface to communicate with external micro-controller.
- Other
  - Power supply
    - 3.3V ~5V for RGB DAC and Tcon pad output
    - 3.3V for other IO pad, and
    - 2.5V for core power

2 PIN Description

2.1 pin configuration

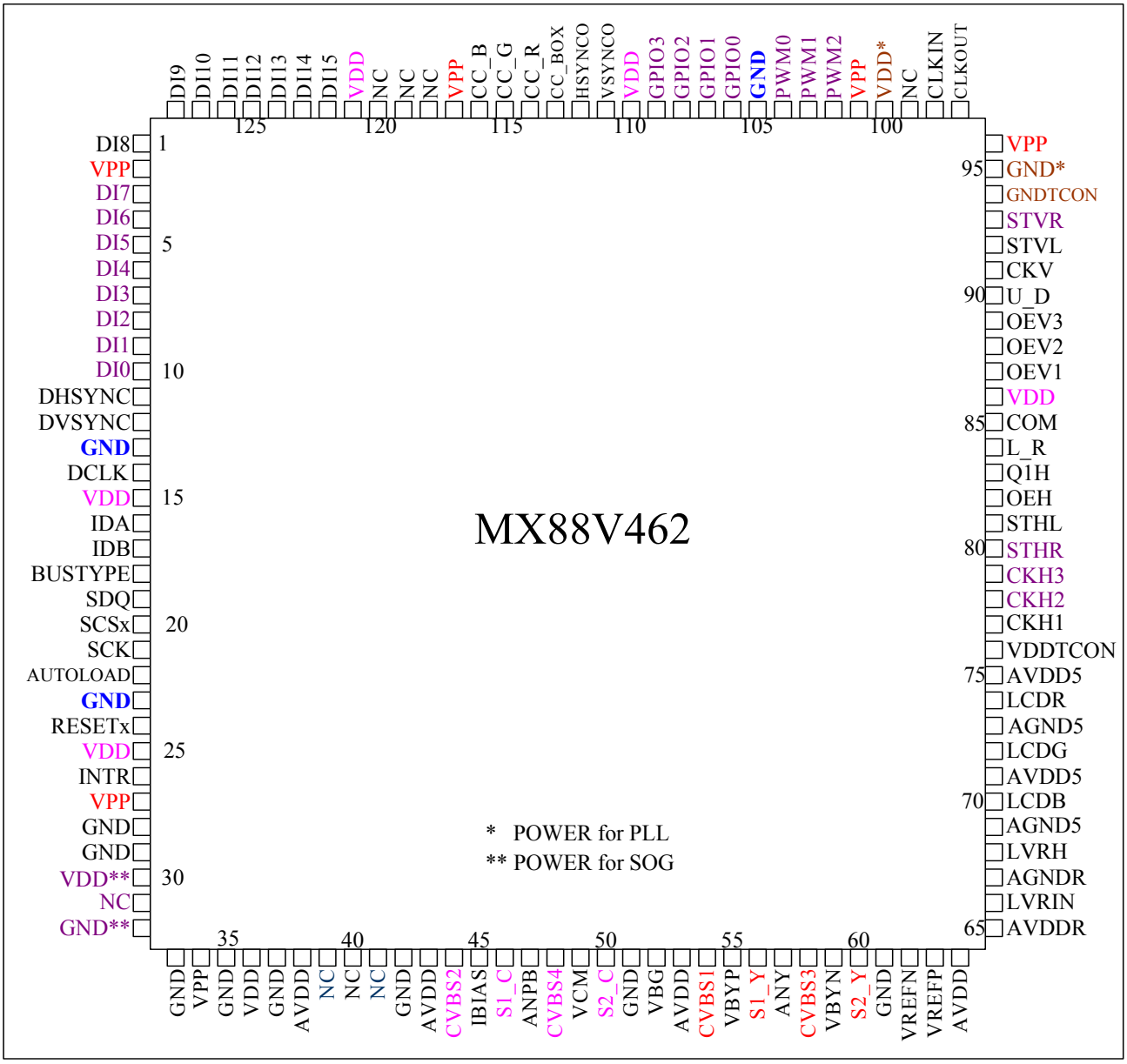


Figure 2.1-1 MX88V462 pin configuration

2.2 Pin list

Pin Name	Pin No.	I/O	Description
1. Digital Video Interface			
DCLK	14	I	Digital Video Input Clock
DHSYNC	11	I	Digital Video Input Hsync
DVSYNC	12	I	Digital Video Input Vsync/Csync
DI15	122	IO	*Digital video data input depends on different mode.
DI14	123	IO	*Digital video data input depends on different mode.
DI13	124	IO	*Digital video data input depends on different mode.
DI12	125	IO	*Digital video data input depends on different mode.
DI11	126	I	*Digital video data input depends on different mode.
DI10	127	I	*Digital video data input depends on different mode.
DI9	128	I	*Digital video data input depends on different mode.
DI8	1	I	*Digital video data input depends on different mode.
DI7	3	I	*Digital video data input depends on different mode.
DI6	4	I	*Digital video data input depends on different mode.
DI5	5	I	*Digital video data input depends on different mode.
DI4	6	I	*Digital video data input depends on different mode.
DI3	7	I	*Digital video data input depends on different mode.

Pin Name	Pin No.	I/O	Description
DI2	8	I	*Digital video data input depends on different mode.
DI1	9	I	*Digital video data input depends on different mode.
DI0	10	I	*Digital video data input depends on different mode.
2. External OSD interface			
CC_R	114	IO	**External OSD Red input
CC_G	115	IO	** External OSD Green input
CC_B	116	IO	** External OSD Blue input
CC_BOX	113	IO	External OSD data valid input (If no external OSD input, this pin must tie low)

*Digital input description:

1. Register 0x00 Bit7-5 =000b, CCIR601 8 bits mode
   DI7~0 = CCIR601 8 bits input
   **DI15~8 can use as external OSD input
2. Register 0x00 Bit7-5 =001b, CCIR656 mode
   DI7~0 = CCIR656 input
   **DI15~8 can use as external OSD input
3. Register 0x00 Bit7-5 =010b, CCIR601 16 bits mode
   DI15~0 = CCIR601 16 bits input
   **CC_R,CC_G,CC_B can use as 111 external OSD input
4. Register 0x00 Bit7-5 =100b, digital RGB 565 input mode
   DI15~DI11 = 5 bits B input
   DI10~DI5 =6 bits G input
   DI4~DI0 =5 bits R input
   **CC_R,CC_G,CC_B can use as 111 external OSD input
5. Register 0x00 Bit7-5 =100b, digital RGB 666 input mode
   { CC_G,CC_B,DI15~12} = 6 bits B input
   DI11~6 = 6 bits G input
   DI5~0 = 6 bits R input

**External OSD input mode

1. Register 0x2c Bit2-1 =00b, RGB 111 mode
   CC_R = 1 bit R input
   CC_G = 1 bit G input
   CC_B = 1 bit B input
2. Register 0x2c Bit2-1 =01b, RGB 343 mode
   {CC_R,CC_G,CC_B} = 3 bits R input
   DI14~11 = 4 bits G input
   DI10~8 = 3 bits B input
3. Register 0x2c Bit2-1 =10b, RGB 565 mode(This mode can only use when analog signal input)
   DI15~11 = 5 bits R input
   DI10~5 = 6 bits G input
   DI4~0 = 5 bits B input
4. Register 0x2c Bit2-1 =11b, RGB 666 mode(This mode can only use when analog signal input)
   {CC_R,CC_G,CC_B,DI15~13} = 6 bits R input
   DI12~7 = 6 bits G input
   DI6~1 = 6 bits B input

Pin Name	Pin No.	I/O	Description
3. Serial MIC Interface			
SCK	21	I	3-wire/2-wireClock
SCSx	20	I	3-wire Interface Chip Select Active high. When 1, means a valid serial transfer cycle
SDQ	19	IO	3-wir/2-wire Data Input/Output
BUSTYPE	18	I	3-wire or 2-wire select 0: 2-wire 1:3-wire
IDA	16	I	2-wire serial bus ID bit 7
IDB	17	I	2-wire serial bus ID bit 6
4. LCD TCON Interface			
CKH1	77	O	Clock Signal for source driver 1

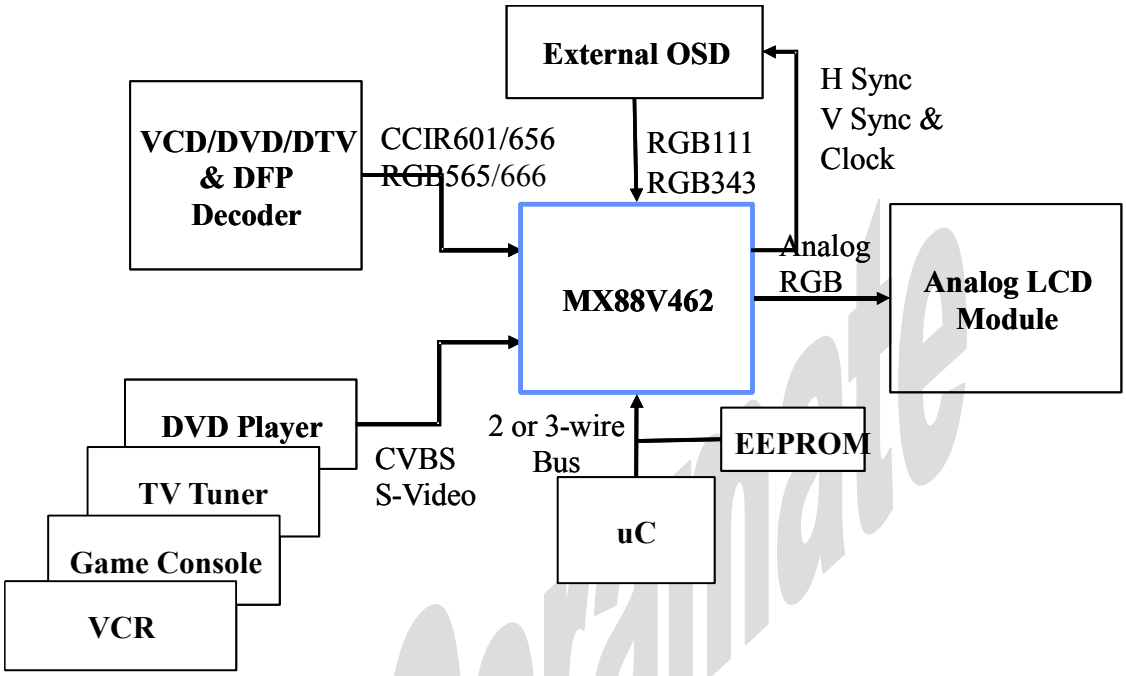
<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>CKH2</td><td>78</td><td>O</td><td>Clock Signal for source driver 2</td></tr>
<tr><td>CKH3</td><td>79</td><td>O</td><td>Clock Signal for source driver 3</td></tr>
<tr><td>Q1H / CTR</td><td>83</td><td>O</td><td>Control Signal for source driver</td></tr>
<tr><td>CKV</td><td>91</td><td>O</td><td>Clock Signal for gate driver</td></tr>
<tr><td>STVL</td><td>92</td><td>O</td><td>Start signal for gate driver</td></tr>
<tr><td>STVR</td><td>93</td><td>O</td><td>Start signal for gate driver</td></tr>
<tr><td>STHL</td><td>81</td><td>O</td><td>Start signal for source driver</td></tr>
<tr><td>STHR</td><td>80</td><td>O</td><td>Start signal for source driver</td></tr>
<tr><td>OEV2</td><td>88</td><td>O</td><td>Panasonic panel gate driver enable 2</td></tr>
<tr><td>OEV3</td><td>89</td><td>O</td><td>Panasonic panel gate driver enable 3</td></tr>
<tr><td>OEH / MOD1/ HSYNC</td><td>82</td><td>O</td><td rowspan="2">MOD1 and MOD2 control the line write mode for gate driver<table><tr><td>MOD2</td><td>MOD1</td><td>Output Mode</td></tr><tr><td>0</td><td>0</td><td>No output</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>2 lines writing at the same time</td></tr><tr><td>1</td><td>1</td><td>1 line writing</td></tr></table></td></tr>
<tr><td>OEV1/ MOD2/ VSYNC</td><td>87</td><td>O</td></tr>
<tr><td>COM/ VCOM*</td><td>85</td><td>O</td><td>COM electrode driving signal, which can be used to control the LCD brightness</td></tr>
<tr><td>L_R</td><td>84</td><td>O</td><td>Left and Right mirror control</td></tr>
<tr><td>U_D</td><td>90</td><td>O</td><td>Up and Down convert control</td></tr>
<tr><td colspan="4">5. TV input interface</td></tr>
<tr><td>CVBS1</td><td>54</td><td>A</td><td>Analog Composite video input 1</td></tr>
<tr><td>CVBS2</td><td>44</td><td>A</td><td>Analog Composite video input 2</td></tr>
<tr><td>S2_C</td><td>50</td><td>A</td><td>S-video2 Chroma. Input</td></tr>
<tr><td>S2_Y</td><td>60</td><td>A</td><td>S-video2 luma input</td></tr>
</table>

Pin Name	Pin No.	I/O	Description
CVBS3	58	A	Analog Composite video input 3
CVBS4	48	A	Analog Composite video input 4
S1_Y	56	A	S-video1 luma input
S1_C	46	A	S-video1 Chroma. Input
ANY	57	A	Video composite analog input reference
ANPB	47	A	Chroma analog input reference
VREFP	63	A	Output for decoupling or input for bypass of internal positive reference voltage
VREFN	62	A	Output for decoupling or input for bypass of internal negative reference voltage
VBG	52	A	Output for decoupling or input for bypass of internal reference bandgap voltage
VCM	49	A	Output for decoupling or input for bypass of common mode voltage
IBIAS	45	A	Output for monitoring or input for bypass of internal bias current
VBYP	55	A	Positive bypass PGA input voltage
VBYN	59	A	Negative bypass PGA input voltage
CSYNC	28		NC pin, must tie low
VSYNC	29		NC pin, must tie low
INTR	26	O	Interrupt for detecting the video source
6. System Interface			
CLKIN	98	I	Oscillator input. 13.5MHZ is required. (CLK1 is for VOP clock)
CLKOUT	97	O	Oscillator output. It forms the oscillator feedback circuit with CLKIN. Itís effective only when external crystal is used.
VSYNCO	111	IO	Vsync output for External OSD
HSYNCO	112	IO	Hsync output for External OSD
RESETx	24	I	Master reset signal. Active low.
PWM0	104	IO	If register 0x31 bit 0 =1,this pin is PWM output 0,else this pin can use as GPIO 6

Pin Name	Pin No.	I/O	Description
PWM1	103	IO	If register 0x31 bit 1 =1,this pin is PWM output 1,else this pin can use as GPIO 5
PWM2	102	IO	If register 0x31 bit 2 =1,this pin is PWM output 2,else this pin can use as GPIO 4
GPIO0	106	IO	GPIO 0
GPIO1	107	IO	GPIO 1
GPIO2	108	IO	GPIO 2
GPIO3	109	IO	GPIO 3
AUTOLOAD	22	I	Auto load enable. 0: disable 1:enable
NC	31,39, 40,41, 99,118, 119, 120		
7. Power/Ground (ADC power TBD)			
VDD	15,25, 86,110, 121	I	Digital Power
GND	13,23, 105	I	Digital Ground
VDD	30	I	Digital Power for SOG
GND	32	I	Digital Ground for SOG
VDD	100	I	Power for PLL and oscillator core
GND	95	I	Ground for PLL and oscillator core
VPP	2,27, 96, 101, 117	I	PAD Power
VPP	34	I	Ring Power for ADC(5V tolrance)
GND	33	I	Ring Power for ADC

Pin Name	Pin No.	I/O	Description
VDD	36,38, 43,53, 64	I	ADC power
GND	35,37, 42,51, 61	I	ADC ground
VDD5V	71,75	I	5V RGBDAC power
GND	69,73	I	RGBDAC ground
VDD5V	65	I	5V DAC trace power
GND	67	I	DAC trace ground
VDDTCON	76	I	TCON PAD power
GNDTCON	94	I	Ground for TCON PAD

3 System Diagram



4 Register Definition

4.1 Video input formatter and power down control

Base address: 0x00

4.1.1. Formatter control register 0

Address	**0x00**
Default	**60H**

7	6	5	4	3	2	1	0
id_mode[2:0]			vsync_pol	hsync_pol	cbcrswap	Yswap	reserved

id_mode[2:0]: Input data mode selection

000 = CCIR601 8bit

001 = CCIR656

010 = CCIR601 16bit

011 = TVDECODER(CVBS , S-video , YPbPr)

100 = Digital RGB565

101 = Digital RGB666

110 = Reserved

111 = Reserved

(Note: in the mode 0,1,2,4,5 the ADC will power down automatically)

vsync_pol: Input vsync polarity selection

0 = active low (default)

1 = active high

hsync_pol: Input hsync polarity selection

0 = active low (default)

1 = active high

cbcrswap: Swap Cb/Cr outputs

0 = Donít swap

1 = Swap

yswap: Swap Y/C outputs

4.1.2. Formatter control register 1

Address	0x01
Default	**00H**

7	6	5	4	3	2	1	0
Reserve					no_signal_digital	Pin100	clk_inv_form

no_signal_digital(read only):To detect whether digital video source input or not

0= have digital signal input

1= no digital signal input

Pin100: Must be set to 1.

clk_inv_form: invert DCLK for internal use

0 = donít invert

1 = invert

4.1.3. Power Down Control

Address	**0x02**
Default	**05H**

7	6	5	4	3	2	1	0
Reserve				burst_en	TV_PLL_EN	PDB_EN	SCL_PLL_EN

burst_en: I2L burst mode enable

0 = Enable

1 = Disable (default)

TV_PLL_EN: Tvdecoder PLL Enable

0 = Disable, the CLKIN will be used as tvdecoder clock.

1 = Enable (default)

PDB_EN: RGBDAC Enable

0 = Disable.

1 = Enable (default)

SCL_PLL_EN: SCL PLL Enable

0 = Disable , the DCLK will be selected as the scaling clock.

1 = Enable (default)

4.2 TV PLL control register

4.2.1. TV PLL M value

Address	**0x03**
Default	**00H**

7	6	5	4	3	2	1	0
TV_PLL_M[7:0]							

TV_PLL_M[7:0]: M value of the TV PLL

4.2.2. TV PLL N value

Address	**0x04**
Default	**00H**

7	6	5	4	3	2	1	0
TV_PLL_N[7:0]							

TV_PLL_N[7:0]: N value of the TV PLL

*Fout = Fin * (TV_PLL_N + 1)/(TV_PLL_M + 1)*

Fin = input clock frequency

Fout= output clock frequency

4.2.3. TV PLL PHASE control register

Address	**0x05**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve	TV_PHS_DLY[4:0]					TVHSPOL	TV_COAST

TV_PHS_DLY[4:0]:choose phase delay , scale is 1/32 clock cycle

TVHSPOL: HSYNC in-phase edge select

0= falling edge

1= rising edge

TV_COAST: in-phase enable

0 = disable

1 =enable

4.2.4. TV PLL Control register 1

Address	**0x06**
Default	**00H**

7	6	5	4	3	2	1	0
tv_pwrdnb1	tv_div	tv_vcorange[1:0]		tv_current[3:0]			

tv_pwrdnb1:

0 = pll power down

1 = pll power on

tv_div:

0 = donít divide frequency

1 = tcon_pll divided by 2

tv_vcorange[1:0]: output clock frequency range select

00 = 16 ~ 73 MHz

01 = 20 ~ 90 MHz

10 = 30 ~ 124 MHz

11 = 46 ~ 172 MHz

tv_current[3:0]: Charge pump current , the value is tv_current * 7.5uA

4.2.5. TV PLL Control register 2

Address	**0x07**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve					tv_si[2:0]		

tv_si[2:0]: VCO gain control

4.3 SCL PLL control register

4.3.1. SCALING PLL M value

Address	**0x08**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve	SCL_PLL_M[6:0]						

SCL_PLL_M[6:0]: M value of the SCL PLL

4.3.2. SCALING PLL N value

Address	**0x09**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve	SCL_PLL_N[6:0]						

SCL_PLL_N[6:0]: N value of the SCL PLL

*Fout = Fin * (SCL_PLL_N + 1)/(SCL_PLL_M + 1)*

Fin = input clock frequency

Fout= output clock frequency

4.3.3. SCALING PLL Control register 1

Address	**0x0A**
Default	**00H**

7	6	5	4	3	2	1	0
scl_pwrdnb1	Scl_div	Scl_vcorange[1:0]		scl_current[3:0]			

scl_pwrdnb1:

0 = pll power down

1 = pll power on

Scl_div:

0 = donít divide frequency

1 = tcon_pll divided by 2

Scl_vcorange[1:0]: output clock frequency range select

00 = 12~137 MHz

01 = 14.5~172 MHz

10 = 23~237 MHz

11 = 37~343 MHz

scl_current[3:0]: Charge pump current

CURRENT[3:0]	Current (uA)
0000	1
0001	2
0010	4
0011	6
0100	8
0101	10
0110	12
0111	14
1000	16
1001	18
1010	20
1011	22
1100	24
1101	26
1110	28
1111	30

4.3.4. SCALING PLL Control register 2

Address	**0x0B**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve					Scl_si[2:0]		

Scl_si[2:0]: Fine Tune VCO gain control, 111b = Max. fine tune gain.

4.4 Output effect control

4.4.1. Output effect function control

Address	**0x0C**
Default	**00H**

7	6	5	4	3	2	1	0
contrast_en	brightness_en	saturation_en	hue_en	gamma_en	gamma_accen	Sharp_en	Con_bri_change

Color adjustment control:

0= disable

1=enable

contrast_en: Contrast Adjustment Enable

brightness_en: Brightness Adjustment Enable

saturation_en: Saturation Adjustment Enable

hue_en: Hue Adjustment Enable

gamma_en: GAMMA Correction Enable

gamma_accent: Gammma Table set access enable

sharp_en: Edge filter adjustment enable

Con_bri_change: Change first adjust contrast or brightness

0 = First Brightness second Contrast

1 = First Contrast second Brightness

4.4.2. Contrast coefficient red

Address	**0x0D**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_C_R[7:0]							

Coeff_C_R[7:0]: Contrast Coefficient-Red, active when Contrast_EN = 1

4.4.3. Contrast coefficient green

Address	**0x0E**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_C_G[7:0]							

Coeff_C_G[7:0]: Contrast Coefficient-Green , active when Contrast_EN = 1

4.4.4. Contrast coefficient blue

Ddress	**0x0F**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_C_B[7:0]							

Coeff_C_B[7:0]: Contrast Coefficient-Blue ,active when Contrast_EN = 1

4.4.5. Brightness coefficient red

Address	**0x10**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_B_R[7:0]							

Coeff_B_R[7:0] Brightness Coefficient-Red , active when Brightness_EN = 1

This value is offset by ñ128 , i.e., a value of 80h(the default) implies a brightness level of 0, and a value of 0 implies a brightness of -128

4.4.6. Brightness coefficient green

Address	**0x11**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_B_G[7:0]							

Coeff_B_G[7:0]: Brightness Coefficient-Green , active when Brightness_EN = 1

This value is offset by ñ128 , i.e., a value of 80h(the default) implies a brightness level of 0, and a value of 0 implies a brightness of -128

4.4.7. Brightness coefficient blue

Address	**0x12**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_B_B[7:0]							

Coeff_B_B[7:0]: Brightness Coefficient-Blue , active when Brightness_EN = 1

This value is offset by ñ128 , i.e., a value of 80h(the default) implies a brightness level of 0, and a value of 0 implies a brightness of -128

4.4.8. Saturation coefficient

Address	**0x13**
Default	**80H**

7	6	5	4	3	2	1	0
Coeff_Sat[7:0]							

Coeff_Sat[7:0]: Saturation Coefficient , active when Saturation_EN = 1

4.4.9. Hue coefficient

Address	**0x14**
Default	**00H**

7	6	5	4	3	2	1	0
Coeff_H[7:0]							

Coeff_H[7:0]: Hue Coefficient, active when Hue_EN = 1

1 step means 360/256 degree

4.4.10. Gamma Data Port

Address	**0x15**
Default	

7	6	5	4	3	2	1	0
Gamma_Dport[7:0]							

Gamma_Dport[7:0]: GAMMA Coefficient data port register

Gamma table write sequence:

1. Set 0x0C D2=1
2. Write data to 0x15
3. The data order is R0,G0,B0,R1,G1,B1Ö Ö R255,G255,B255. The address increases automatically.
4. After write all gamma table , set 0x0C D2=0
5. Set 0x0C D3=1 to enable gamma correct function

4.5 OSD control register

4.5.1. OSD blending control register

Address	**0x16**
Default	**00H**

7	6	5	4	3	2	1	0
OSD_EN	Color_Logic[1:0]		Foreground_EN	Background_EN	Blending[2:0]		

OSD_EN: OSD Enable

0 = OSD disable

1 = OSD enable

Color_Logic[1:0]: Color key alpha blending selection

00 = disable color key alpha blending

01 = enable color key alpha blending

10 = enable NOT color key alpha blending

11 = not defined, reserved

Foreground_EN: OSD foreground alpha blending

0 = disable

1 = enable

Background_EN: OSD background alpha blending

0 = disable

1 = enable

Blending[2:0]: OSD alpha blending mode

000 = 00.0% transparency (default)

001 = 12.5% transparency

010 = 25.0% transparency

011 = 37.5% transparency

100 = 50.0% transparency

101 = 62.5% transparency

110 = 75.0% transparency

111 = 87.5% transparency

4.5.2. OSD color key red

Address	**0x17**
Default	**00H**

7	6	5	4	3	2	1	0
ColorKey_R[7:0]							

ColorKey_R[7:0]: Color key Red color for alpha blending

4.5.3. OSD color key green

Address	**0x18**
Default	**00H**

7	6	5	4	3	2	1	0
ColorKey_G[7:0]							

ColorKey_G[7:0]: Color key Green color for alpha blending

4.5.4. OSD color key blue

Address	**0x19**
Default	**00H**

7	6	5	4	3	2	1	0
ColorKey_B[7:0]							

ColorKey_B[7:0] Color key Blue color for alpha blending

4.6 Output display select register

4.6.1. Output display control

Address	**0x1A**
Default	**40H**

7	6	5	4	3	2	1	0
Screen_Off	Data_SEL	Frame_EN	Reserved				

Screen_Off: Screen-Off Enable (output data set to 0)

0 = Disable (Screen-On)

1 = Enable (Screen-Off)

Data_SEL: Output pixel data source select

0 = Generate by internal frame window color

1 = Generated by input data

Frame_EN: Frame window color

0= OFF

1= ON

4.6.2. Frame color red

Address	**0x1B**
Default	**00H**

7	6	5	4	3	2	1	0
FrameCol_R[7:0]							

FrameCol_R[7:0]: Frame window color-Red , active when Frame_EN = 1

4.6.3. Frame color green

Address	**0x1C**
Default	**00H**

7	6	5	4	3	2	1	0
FrameCol_G[7:0]							

FrameCol_G[7:0]: Frame window color-Green , active when Frame_EN = 1

4.6.4. Frame color blue

Address	**0x1D**
Default	**00H**

7	6	5	4	3	2	1	0
FrameCol_B[7:0]							

FrameCol_B[7:0]: Frame window color-Blue , active when Frame_EN = 1

4.7 Sharpness edge filter coefficient

This three taps filter is provided to do video edge enhancement to let image become sharp or blur.

4.7.1. Edge filter Coefficient N-1

Address	**0x1E**
Default	**E0H**

7	6	5	4	3	2	1	0
Edge filter Coefficient A[7:0]							

Edge filter Coefficient A[7:0]: Edge filter coefficient A

This is a 2ís complement number.

The coefficient is the number divided by 128, i.e. the value E0H (the default) implies a coefficient of -32/128= -0.25 .

4.7.2. Edge filter Coefficient N

Address	**0x1F**
Default	**60H**

7	6	5	4	3	2	1	0
Edge filter Coefficient B[7:0]							

Edge filter Coefficient B[7:0]: Edge filter coefficient B

D7~D6: integer part, D5~0: fraction part , range: 0 (0H) ~3.984375 (FFH)

The value 60H(the default) implies a coefficient of 1.5 .

4.7.3. Edge filter Coefficient N+1

Address	**0x20**
Default	**E0H**

7	6	5	4	3	2	1	0
Edge filter Coefficient C[7:0]							

Edge filter Coefficient C[7:0]: Edge filter coefficient C

This is a 2ís complement number.

The coefficient is the number divided by 128, i.e. the value E0H (the default) implies a coefficient

of -32/128= -0.25 .

4.8 Color space convert

YCbCr to RGB color space convert equation parameters

4.8.1. Color space convert Y_RGB_COEF

Address	**0x21**
Default	**95H**

7	6	5	4	3	2	1	0
y_rgb_coef[7:0]							

y_rgb_coef[7:0] : each scale is 1/128, default = 95H /128 = 1.164

4.8.2. Color space convert CR_R_COEF

Address	**0x22**
Default	**CCH**

7	6	5	4	3	2	1	0
cr_r_coef[7:0]							

cr_r_coef[7:0]: each scale is 1/128, default = CCH /128 = 1.59375

4.8.3. Color space convert CB_G_COEF

Address	**0x23**
Default	**32H**

7	6	5	4	3	2	1	0
cb_g_coef[7:0]							

cb_g_coef[7:0]: each scale is 1/128, default = 32H /128 = 0.390625

4.8.4. Color space convert CR_G_COEF

Address	**0x24**
Default	**68H**

7	6	5	4	3	2	1	0
cr_g_coef[7:0]							

cr_g_coef[7:0]: each scale is 1/128, default = 68H /128 = 0.8125

4.8.5. Color space convert CB_B_COEF low byte

Address	**0x25**
Default	**02H**

7	6	5	4	3	2	1	0
cb_b_coef[7:0]							

cb_b_coef[7:0]: cb_b_coef bit 7-0 ,bit 8 is 0x26 D0

4.8.6. Color space convert CB_B_COEF high byte and y sub control

Address	**0x26**
Default	**61H**

7	6	5	4	3	2	1	0
Reserved	range_sel	y_sub_coef[4-0]					cb_b_coef[8]

cb_b_coef[8]: cb_b_coef bit 8

each scale is 1/128, default cb_b_coef = 102H /128 = 2.015625

y_sub_coef[4-0]: Y sub coef , default is (10h)

range_sel: Select input y Cb Cr range

0 = y range 0 ~ 255 , Cb Cr range 0 ~255

1 = y range 16 ~235 , Cb Cr range 16 ~240

4.9 Black and White Level extension register

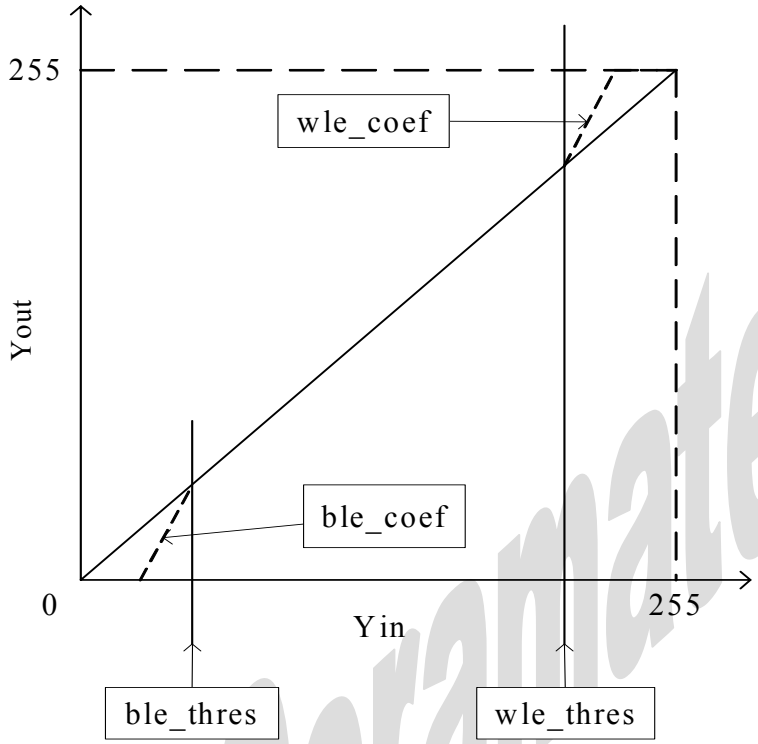


Figure 4.9-1 Level extension

4.9.1. Level extension control

Address	**0x27**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved						en_ble	en_wle

en_wle: Enable white level extension

0 = Disable (default)

1 = Enable

en_ble: Enable black level extension

0 = Disable (default)

1 = Enable

4.9.2. Level extension black level threshold

Address	**0x28**
Default	**00H**

7	6	5	4	3	2	1	0
ble_thres[7:0]							

ble_thres[7:0]: Black level extension threshold

4.9.3. Level extension black level coefficient

Address	**0x29**
Default	**00H**

7	6	5	4	3	2	1	0
ble_coef[7:0]							

ble_coef[7:0]: Black level extension coefficient* 128

4.9.4. Level extension white level threshold

Address	**0x2A**
Default	**00H**

7	6	5	4	3	2	1	0
wle_thres[7:0]							

wle_thres[7:0]: White level extension threshold

4.9.5. Level extension white level coefficient

Address	**0x2B**
Default	**00H**

7	6	5	4	3	2	1	0
wle_coef[7:0]							

wle_coef[7:0]: White level extension coefficient* 128

4.10 External OSD registers

4.10.1. External OSD Control 1

Address	**0x2C**
Default	**00H**

7	6	5	4	3	1	2	0
ex_osd_c_mode	ex_osd_c_en	ex_osd_bmode	osd_disp_mode	ext_osd_en	ext_osd_for[1:0]		ex_osd_mode

ex_osd_c_mode: External OSD color key mode select

1 = meet color key display blending

0 = meet color key display OSD all.

ex_osd_c_en: External OSD color key enable

ex_osd_bmode: External OSD background control signal

0 = background pin is low active

1 = background pin is high active

osd_disp_mode: External OSD display mode OSD priority select.

0 = Internal OSD is high priority

1 = External OSD is high priority

When ex_osd_mode set after scaler this pin is useable unless it is unuseable

ext_osd_en: External OSD enable

0: Disable

1: Enable

ext_osd_for[1:0]: External osd formtter select

00 = RGB 111 in CC_R,CC_G,CC_B pin

01 = RGB 343

10 = RGB 565

11 = RGB 666

ex_osd_mode: Select external OSD before scaling or after scaling

0 = Before Scaling

1 = After Scaling

4.10.2. External OSD Control 2

Address	**0x2D**
Default	**00H**

7	6	5	4	3	1	2	0
reserve		ex_osd_blend[2:0]			ex_osd_fen	reserve	ex_osd_bl_en

ex_osd_bl_en: OSD background alpha blending enable

ex_osd_fen: OSD all image alpha blending

0 = disable (default)

1 = enable

ex_osd_blend[2:0]: OSD alpha blending mode

000 = 00.0% transparency (default)

001 = 12.5% transparency

010 = 25.0% transparency

011 = 37.5% transparency

100 = 50.0% transparency

101 = 62.5% transparency

110 = 75.0% transparency

111 = 87.5% transparency

4.10.3. External OSD Color key red

Address	**0x2E**
Default	**00H**

7	6	5	4	3	1	2	0
ex_osd_rkey[7:0]							

ex_osd_rkey[0:7]: External OSD color key Red Coef.

4.10.4. External OSD Color key green

Address	**0x2F**
Default	**00H**

7	6	5	4	3	1	2	0
ex_osd_gkey[7:0]							

ex_osd_gkey[7:0]: External OSD color key Green Coef.

4.10.5. External OSD Color key blue

Address	**0x30**
Default	**00H**

7	6	5	4	3	1	2	0
EX_OSD_BKEY[7:0]							

ex_osd_bkey [7:0]: External OSD color key Blue Coef.

4.11 PWM (Pulse Width Modulation)register

4.11.1. PWM control register

Address	**0x31**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved		Reserved	Ovsync_en	Ovsync_dir	PWM2_en	PWM1_en	PWM0_en

Ovsync_en: enable scaler output field shift one line

0:disable 1:enable

Ovsync_dir: scaler output field shift direction,this will work when Ovsync_en set to 1.

0:odd field will shift up one line

1:odd field will shift down one line

PWM2_en: PWM2 enable

PWM1_en: PWM1 enable

PWM0_en: PWM0 enable

4.11.2. PWM0 duty cycle

Address	**0x32**
Default	**00H**

7	6	5	4	3	2	1	0
PWM0_DUTY[7:0]							

PWM0_DUTY[7:0]: PWM0 duty cycle , a value of 40H implies that duty cycle = 64 / 256 = 0.25.

4.11.3. PWM0 frequency divider

Address	**0x33**
Default	**00H**

7	6	5	4	3	2	1	0
PWM0_FDIV[7:0]							

PWM0_FDIV[7:0]:PWM0 frequency divider factor , a value of 10H implies the PWM clock frequency is divided by 16.

4.11.4. PWM1 duty cycle

Address	**0x34**
Default	**00H**

7	6	5	4	3	2	1	0
PWM1_DUTY[7:0]							

PWM1_DUTY[7:0]: PWM1 duty cycle , a value of 40H implies that duty cycle = 64 / 256 = 0.25.

4.11.5. PWM1 Frequency divider

Address	**0x35**
Default	**00H**

7	6	5	4	3	2	1	0
PWM1_FDIV[7:0]							

PWM1_FDIV[7:0]:PWM1 frequency divider factor a value of 10H implies the PWM clock frequency is divided by 16.

4.11.6. PWM2 duty cycle

Address	**0x36**
Default	**00H**

7	6	5	4	3	2	1	0
PWM2_DUTY[7:0]							

PWM2_DUTY[7:0]: PWM1 duty cycle , a value of 40H implies that duty cycle = 64 / 256 = 0.25.

4.11.7. PWM2 Frequency divider

Address	**0x37**
Default	**00H**

7	6	5	4	3	2	1	0
PWM2_FDIV[7:0]							

PWM2_FDIV[7:0]: PWM1 frequency divider factor a value of 10H implies the PWM clock frequency is divided by 16.

4.12 SCALER

4.12.1. Input image horizontal sample start low byte

Address	**0x38**
Default	**8FH**

7	6	5	4	3	2	1	0
ISSPH_LO[7:0]							

ISSPH_LO[7:0]: Input image horizontal sample start point.

Counting by input dot clock, and start from the HSYNC.

4.12.2. Input image horizontal sample start high byte

Address	**0x39**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved						ISSPH_HI[1:0]	

ISSPH_HI[1:0]: Input image horizontal sample start point.

Counting by input dot clock, and start from the HSYNC.

4.12.3. Input image horizontal sample count low byte

Address	**0x3A**
Default	**C1H**

7	6	5	4	3	2	1	0
ISDCH_LO[7:0]							

ISDCH_LO[7:0]: Input image horizontal sample point count. Input image display enable.

4.12.4. Input image horizontal sample count high byte

Address	**0x3B**
Default	**02H**

7	6	5	4	3	2	1	0
Reserved						ISDCH_HI[1:0]	

ISDCH_HI[1:0]: Input image horizontal sample point count. Input image display enable.

4.12.5. Input image vertical sample start point low byte

Address	**0x3C**
Default	**0DH**

7	6	5	4	3	2	1	0
ISSPV_LO[7:0]							

ISSPV_LO[7:0]: Input image vertical sample start point.

Counting by input dot clock, and start from the VSYNC.

4.12.6. Input image vertical sample start point high byte

Address	**0x3D**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve						ISSPV_HI[1:0]	

ISSPV_HI[1:0]: Input image vertical sample start point.

Counting by input dot clock, and start from the VSYNC.

4.12.7. Input image vertical sample point count low byte

Address	**0x3E**
Default	**F7H**

7	6	5	4	3	2	1	0
ISDCV_LO[7:0]							

ISDCV_LO[7:0]: Input image vertical sample point count. Input image display enable.

4.12.8. Input image vertical sample point count high byte

Address	**0x3F**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved						ISDCV_HI[1:0]	

ISDCV_HI[1:0]: Input image vertical sample point count. Input image display enable.

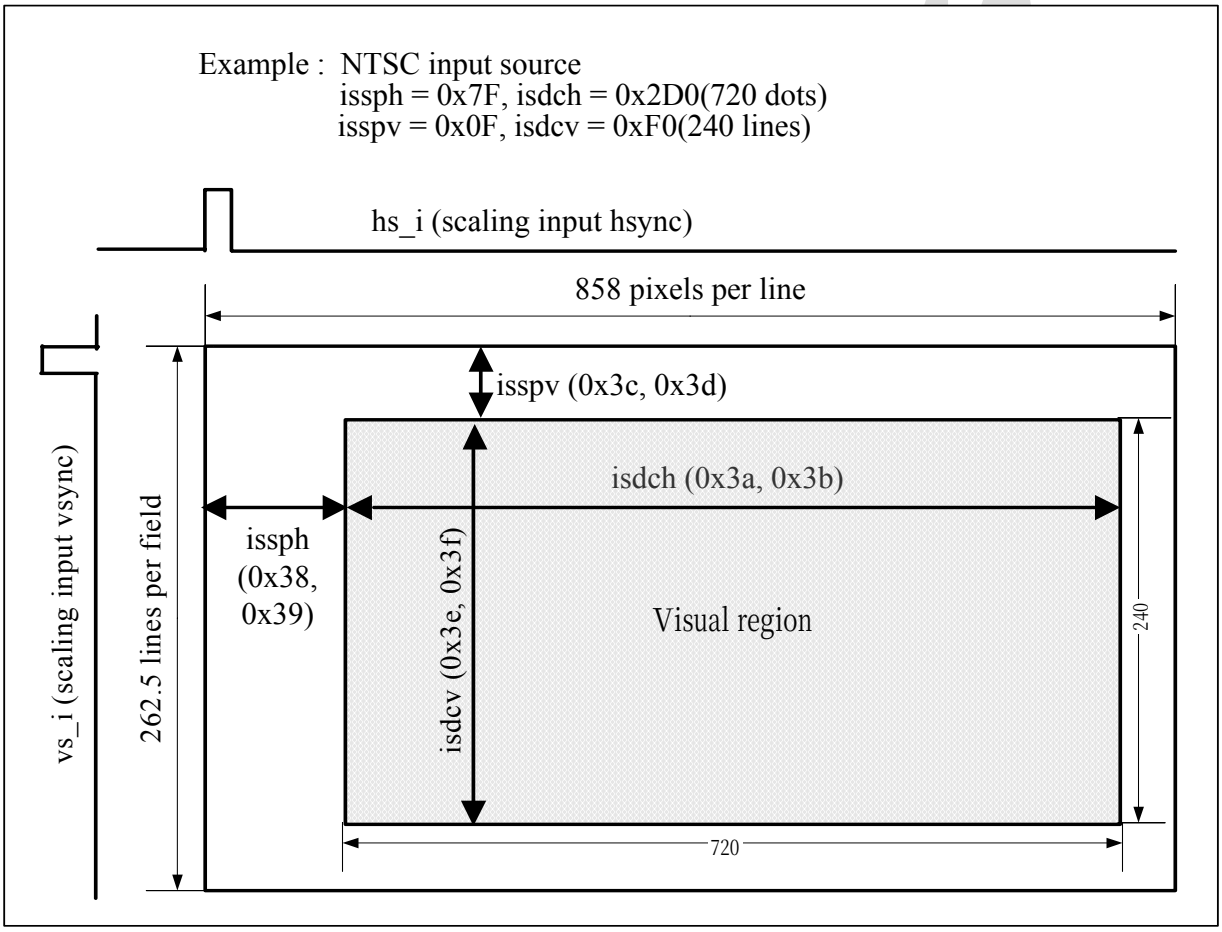


Figure 4.12-1 Scaling input image register setting diagram

4.12.9. Scaling vertical factor bit 0 ~ 7

Address	**0x40**
Default	**45H**

7	6	5	4	3	2	1	0
VSF_0_7[7:0]							

VSF_0_7[7:0]: Scaling vertical factor

4.12.10. Scaling vertical factor bit 8 ~ 15

Address	**0x41**
Default	**06H**

7	6	5	4	3	2	1	0
VSF_8_15[7:0]							

VSF_8_15[7:0]: Scaling vertical factor

4.12.11. Scaling vertical factor bit 16 ~ 17

Address	**0x42**
Default	**01H**

7	6	5	4	3	2	1	0
VSF_16_17[7:0]							

VSF_16_17[7:0]: Scaling vertical factor. (Integer part)

4.12.12. Output image horizontal total dot number low byte

Address	**0x43**
Default	**D3H**

7	6	5	4	3	2	1	0
HTOTAL_LO[7:0]							

HTOTAL_LO[7:0]: Output image horizontal total dot number

4.12.13. Output image horizontal total dot number high byte

Address	**0x44**
Default	**02H**

7	6	5	4	3	2	1	0
Reserved				HTOTAL_HI[3:0]			

HTOTAL_HI[3:0]: Output image horizontal total dot number

4.12.14. Output image horizontal display area start point low byte

Address	**0x45**
Default	**98H**

7	6	5	4	3	2	1	0
HDSTA_LO[7:0]							

HDSTA_LO[7:0]: Output image horizontal display area start point.

4.12.15. Output image horizontal display area start point high byte

Address	**0x46**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve					HDSTA_HI[2:0]		

HDSTA_HI[2:0]: Output image horizontal display area start point.

4.12.16. Output image horizontal display area end point low byte

Address	**0x47**
Default	**D0H**

7	6	5	4	3	2	1	0
HDEND_LO[7:0]							

HDEND_LO[7:0]: Output image horizontal display area end point.

4.12.17. Output image horizontal display area end point high byte

Address	**0x48**
Default	**02H**

7	6	5	4	3	2	1	0
Reserved					HDEND_HI[2:0]		

HDEND_HI[2:0]: Output image horizontal display area end point.

4.12.18. Output image horizontal valid area start point low byte

Address	**0x49**
Default	**98H**

7	6	5	4	3	2	1	0
HVSTA_LO[7:0]							

HVSTA_LO[7:0]: Output image horizontal valid area start point.

4.12.19. Output image horizontal valid area start point high byte

Address	**0x4A**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved					HVSTA_HI[2:0]		

HVSTA_HI[2:0]: Output image horizontal valid area start point.

4.12.20. Output image horizontal valid area end point low byte

Address	**0x4B**
Default	**D0H**

7	6	5	4	3	2	1	0
HVEND_LO[7:0]							

HVEND_LO[7:0]: Output image horizontal valid area end point.

4.12.21. Output image horizontal valid area end point high byte

Address	**0x4C**
Default	**02H**

7	6	5	4	3	2	1	0
Reserved					HVEND_HI[2:0]		

HVEND_HI[2:0]: Output image horizontal valid area end point.

4.12.22. Output image vertical total line number low byte

Address	**0x4D**
Default	**20H**

7	6	5	4	3	2	1	0
VTOTAL_LO[7:0]							

VTOTAL_LO[7:0]: Output image vertical total line number.

p.s. total line number is determined by input image frame rate, but if not input image it determined by this register. (Default = 0x20) low byte

ps. It cannot set lower than input image total timing. It maybe impacts the image on the panel.

4.12.23. Output image vertical total line number high byte

Address	**0x4E**
Default	**01H**

7	6	5	4	3	2	1	0
Reserved					VTOTAL_HI[2:0]		

4.12.24. Output image vertical display area end line low byte

Address	**0x4F**
Default	**FDH**

7	6	5	4	3	2	1	0
VDEND_LO[7:0]							

VDEND_LO[7:0]: Output image vertical display area end line

4.12.25. Output image vertical display area end line high byte

Address	**0x50**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved					VDEND_HI[2:0]		

VDEND_HI[2:0]: Output image vertical display area end line.

4.12.26. Output image vertical valid area start line low byte

Address	**0x51**
Default	**00H**

7	6	5	4	3	2	1	0
VVSTA_LO[7:0]							

VVSTA_LO[7:0]: Output image vertical valid area start line.

4.12.27. Output image vertical valid area start line high byte

Address	**0x52**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved					VVSTA_HI[2:0]		

VVSTA_HI[2:0]: Output image vertical valid area start line.

4.12.28. Output image vertical valid area end line low byte

Address	**0x53**
Default	**FCH**

7	6	5	4	3	2	1	0
VVEND_LO[7:0]							

VVEND_LO[7:0]: Output image vertical valid area end line.

4.12.29. Output image vertical valid area end line high byte

Address	**0x54**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved					VVEND_HI[2:0]		

VVEND_HI[2:0]: Output image vertical valid area end line.

4.12.30. Scaling vsync start low byte

Address	**0x55**
Default	**00H**

7	6	5	4	3	2	1	0
VSSTA_LO[7:0]							

VSSTA_LO[7:0]: Scaling vsync start register to tcon and osd.

p.s. normally it is unnecessary to set.

4.12.31. Scaling vsync start high byte

Address	**0x56**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved					VSSTA_HI[2:0]		

VSSTA_HI[2:0]: Scaling vsync start register to tcon and osd.

p.s. normally it is unnecessary to set.

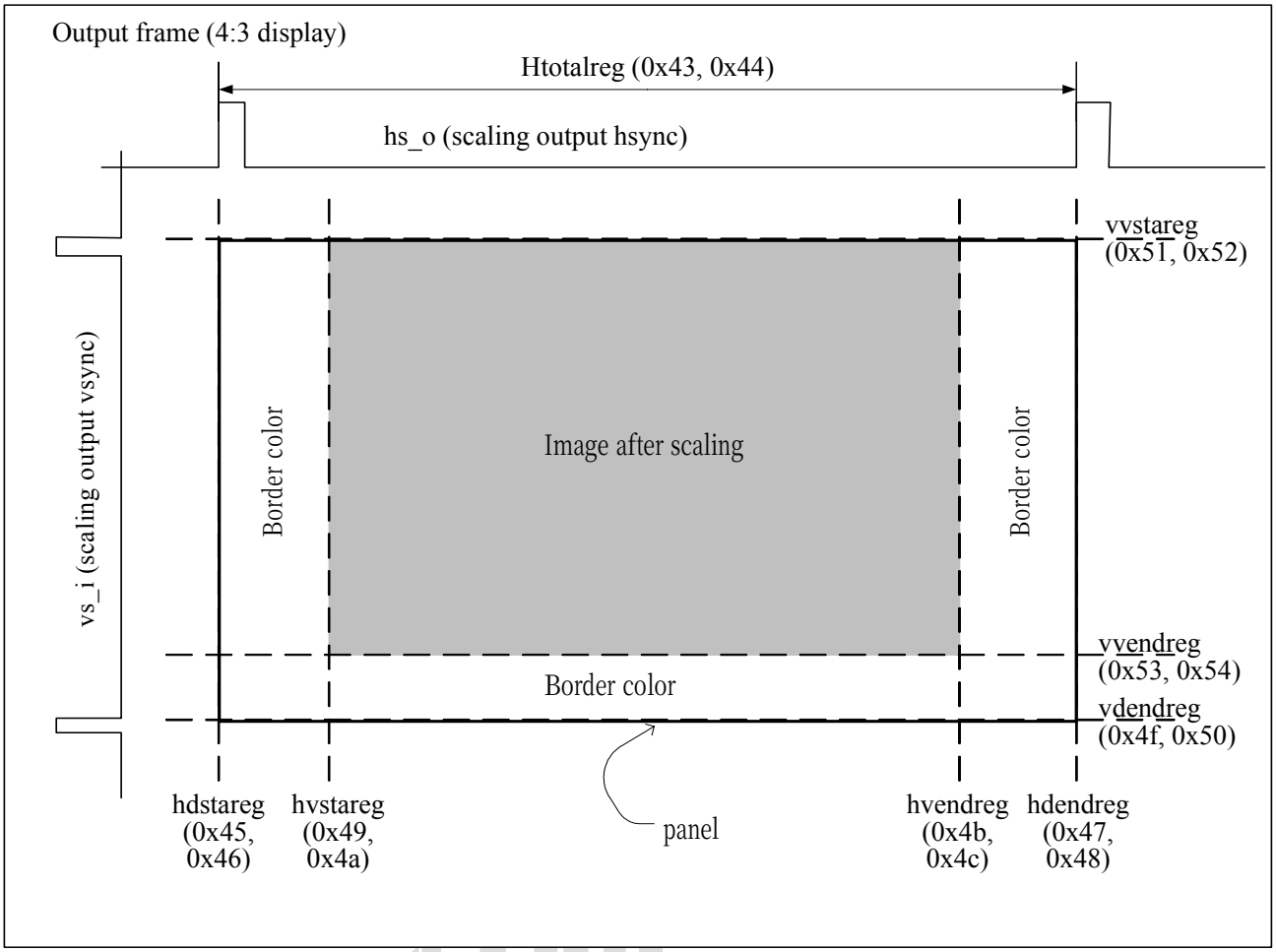


Figure 4.12-2 Scaling output frame register setting diagram

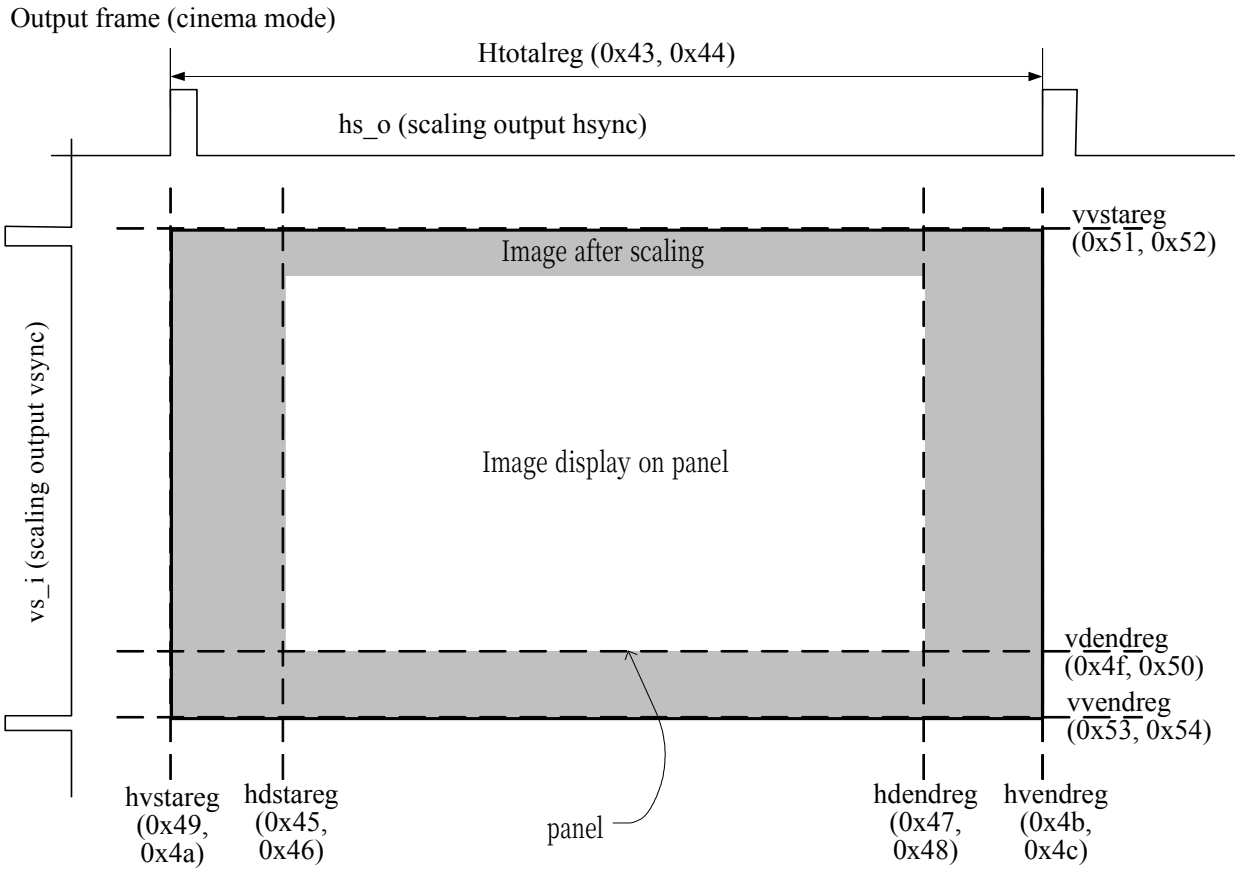


Figure 4.12-3 Scaling output frame register setting for cinema mode

4.12.32. Horizontal scaling region

Address	**0x57**
Default	**28H**

7	6	5	4	3	2	1	0
HSCL_REGION[7:0]							

HSCL_REGION[7:0]:

4.12.33. Horizontal scaling vector bit 7~ 0

Address	**0x58**
Default	**70H**

7	6	5	4	3	2	1	0
HSF_0_7[7:0]							

HSF_0_7[7:0]:

4.12.34. Horizontal scaling vector bit 8~ 15

Address	**0x59**
Default	**78H**

7	6	5	4	3	2	1	0
HSF_8_15[7:0]							

HSF_8_15[7:0]:

4.12.35. Horizontal scaling vector bit 16~ 18

Address	**0x5A**
Default	**01H**

7	6	5	4	3	2	1	0
Reserved					HSF_16_18[2:0]		

HSF_16_18[2:0]:

4.12.36. Horizontal scaling vector delta low byte

Address	**0x5B**
Default	**00H**

7	6	5	4	3	2	1	0
HSF_DELTA_LO[7:0]							

HSF_DELTA_LO[7:0]:

4.12.37. Horizontal scaling vector delta high byte

Address	**0x5C**
Default	**00H**

7	6	5	4	3	2	1	0
HSF_DELTA_HI[7:0]							

4.12.38. Scaling control register 1

Address	**0x5D**
Default	**18H**

7	6	5	4	3	2	1	0
interlace_en	letterbox_en	Hcmpfilter[1:0]		hybrid_coef_h[3:0]			

interlace_en: Select odd or even field to delay lines. (See 0x5f delay_field)

0 = odd

1 = even

letterbox_en: It can speed up the tcon clock to increase the output line number in the bolder color. But it is limited by VBI timing and by panel spec.

0 = disable

1 = enable

Hcmpfilter[1:0]: Scaling horizontal filter function.

00 = filter off

01 = smart scaling 1 (bilinear, default)

10 = smart scaling 2 (dual)

11 = hybrid mode

hybrid_coef_h[3:0]: Fine-tune the horizontal scaling up curve.

Scaling up adjustment (this function is enable just in hybrid mode)

A = scaling2 B = scaling1

Hybrid_coef = 0000 => B

Hybrid_coef = 0001 => 1/16A + 15/16B

Hybrid_coef = 0010 => 2/16A + 14/16B

Hybrid_coef = 0011 => 3/16A + 13/16B

Hybrid_coef = 0100 => 4/16A + 12/16B

Hybrid_coef = 0101 => 5/16A + 11/16B
Hybrid_coef = 0110 => 6/16A + 10/16B
Hybrid_coef = 0111 => 7/16A + 9/16B
Hybrid_coef = 1000 => 8/16A + 8/16B
Hybrid_coef = 1001 => 9/16A + 7/16B
Hybrid_coef = 1010 => 10/16A + 6/16B
Hybrid_coef = 1011 => 11/16A + 5/16B
Hybrid_coef = 1100 => 12/16A + 4/16B
Hybrid_coef = 1101 => 13/16A + 3/16B
Hybrid_coef = 1110 => 14/16A + 2/16B
Hybrid_coef = 1111 => 15/16A + 1/16B

4.12.39. Scaling control register 2

Address	**0x5E**
Default	**18H**

7	6	5	4	3	2	1	0
Elaen	weighten	vcmpfilter[1:0]		hybrid_coef_v[3:0]			

elaen: ELA select.
0 = disable
1 = enable
weighten: Vertical interpolation weight control function
0 = disable
1 = enable
vcmpfilter[1:0]: Scaling vertical filter function.
00 = filter off
01 = smart scaling 1 (bilinear)
10 = smart scaling 2 (dual)
11 = hybrid mode
hybrid_coef_v[3:0]: Fine-tune the vertical scaling up curve.
p.s. the same as the hybrid_coef_h register.

4.12.40. Scaling control register 3

Address	**0x5FH**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved					lb4en	delay_field[1:0]	

lb4en:

0 = NTSC scaling engine

1 = PAL and delta panel scaling engine

delay_field[1:0]: Delay input odd/even field

4.13 TFT LCD timing control register

4.13.1. TCON CONTROL REGISTER 1(TCON_CTR1)

Address	**0x60**
Default	00H

D7	D6	D5	D4	D3	D2	D1	D0
Panel_sel	u_d	stv_out_sel	l_r	sth_out_sel	hs_pol	vs_pol	tcon_off

D7: Panel_sel :select lcd panel output select

1:Pin OEV1 output is MOD1 for SHARP panel. OEH output is MOD2. Q1H pin is CTR. Set

0:Normal operation.

D6: Up down control

0: panel UP_DOWN control pin is Lo.

1: control pin is HI.

D5: Tcon signal STVL STVR output select.

0: STVL is output, STVR is Hi-Z.

1: STVR is output, STVL is Hi-Z

D4: Left right control

0: panel LEFT_RIGHT control pin is Lo.

1 control pin is Hi.

D3: Tcon signal STHL STHR output select.

0: STHL is output, STHR is Hi-Z.

1: STHR is output, STHL is Hi-Z.

D2: HSYNCO pin polarity select.

0: active low

1: active high.

D1: VSYNCO pin polarity select.

0: active low

1: active high.

D0: TCON_OFF: Turn off tcon . When panel with TCON we can turn off this V46 TCON only send HSYNCO and VSYNCO control signal.

4.13.2. TCON CONTROL REGISTER2(TCON_CTR2)

Address	**0x61**
Default	00H

D7	D6	D5	D4	D3	D2	D1	D0
Reserve		lg_sel	drop_clk_sel	clk_inv	Delta_en	delta_linedelay	THREE_EN

D5:LG panel select when set this bit the TCON can create special wave form in vertical start(see also register (0x84~86)

D4: when scaler drop line select this line clock drop or not

D3: select output clock invert or not

D2: delta type panel enable

D1: select output rgb pixel delay one pixel time or not.

D0: When panel should connect CKH1 CKH2 CKH3 should enable this pin.

*D2 and D0 canít set at the same time.

4.13.3. OEH timing control register

Address	**0x62~69**
Default	All 00H

0x62 OEH start time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
Oeh_start D7~D0							

0x63 OEH start time high byte and OEH output polarity.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve				Oeh_pol	Oeh_start D10 ~ D8		

0x64 OEH duration time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
Oeh dur D7~D0							

0x65 OEH duration time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					Oeh_dur D10 ~ D8		

0x66 OEH vertical start time register

D7	D6	D5	D4	D3	D2	D1	D0

Oeh_vstart D7~D0

0x67 OEH vertical start time register

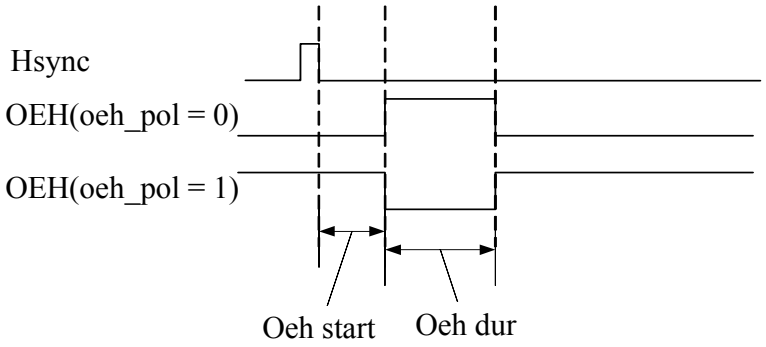
D7	D6	D5	D4	D3	D2	D1	D0
Reserve						Oeh_vstart D10~D8	

0x68 OEH duration time register

D7	D6	D5	D4	D3	D2	D1	D0
Oeh_vdur D7~D0							

0x69 OEH duration time register

D7	D6	D5	D4	D3	D2	D1	D0
Reserve						Oeh_vdur D10~D8	



Oeh start time = oeh_start * 1/27Mhz
Oeh duration time = oeh_dur * 1/27Mhz

Figure 4.13-1 OEH register setting diagram 1

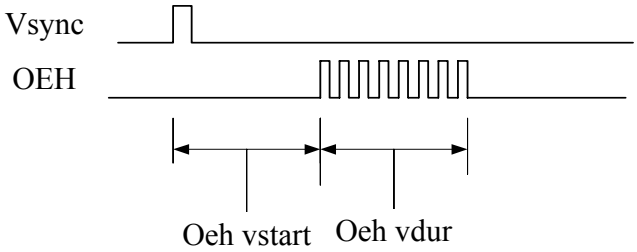


Figure 4.13-2 OEH register setting diagram 2

4.13.4. STH timing control register

Address	**0x6a~6d**
Default	All 00H

0x6aSTH start time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
STH start D7~D0							

0x6b STH start time high byte and STH output polarity.

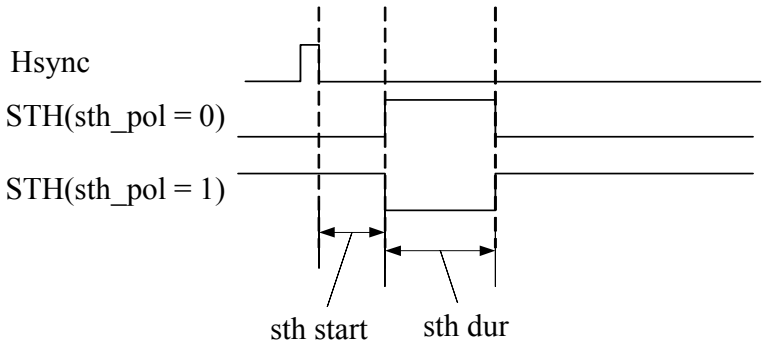
D7	D6	D5	D4	D3	D2	D1	D0
Reserve				STH_pol	STH_start D10 ~ D8		

0x6c STH duration time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
STH dur D7~D0							

0x6d STH duration time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					STH _dur D10 ~ D8		



sth start time = sth_start * 1/27Mhz
sth duration time = sth_dur * 1/27Mhz

Figure 4.13-3 STH register setting diagram

4.13.5. Q1H timing control register

Q1H(Rotate control register) and CTR timing control register.

Address	**0x6e~6f**
Default	All 00H

0x6e Q1H toggle time low byte.

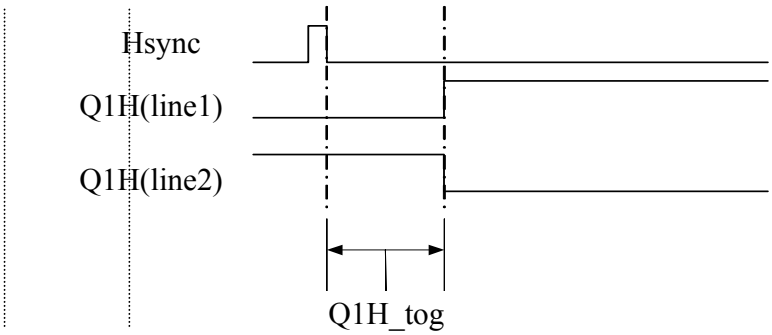
D7	D6	D5	D4	D3	D2	D1	D0
Q1H tog D7~D0							

0x6f Q1H toggle time high byte and Q1H change control.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve			Q1H_inv	Q1H_chg	Q1H tog D10 ~ D8		

Q1h_chg :Select Q1H level change every field or not.

Q1H_inv :Q1H invert or not.



Q1h toggle time = q1h_tog * 1/27Mhz

Figure 4.13-4 Q1H register setting diagram

4.13.6. OEV timing control register

OEV(Output enable for gate driver) timing control register.

Address	**0x70~73**
Default	All 00H

0x70 OEV start time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
OEV_start D7~D0							

0x71 OEV start time high byte and OEV output polarity.

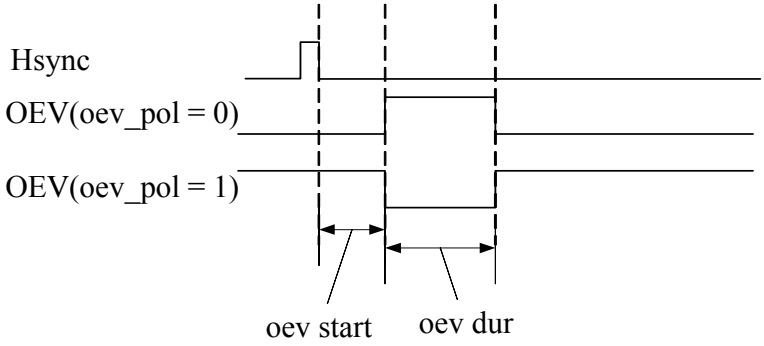
D7	D6	D5	D4	D3	D2	D1	D0
Reserve				OEV_pol	OEV_start D10 ~ D8		

0x72 OEV duration time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
OEV_dur D7~D0							

0x73 OEV duration time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					OEV_dur D10 ~ D8		



oev start time = oev_start * 1/27Mhz
oev duration time = oev_dur * 1/27Mhz

Figure 4.13-5 OEV register setting diagram

4.13.7. CKV timing control register

CKV(Clock for gate driver) timing control register.

Address	**0x74~77**
Default	All 00H

0x74 CKV start time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
CKV_start D7~D0							

0x75 CKV start time high byte and OEV output polarity.

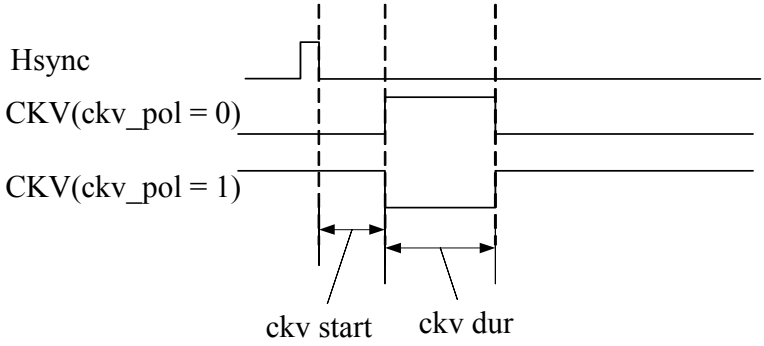
D7	D6	D5	D4	D3	D2	D1	D0
Reserve				CKV_pol	CKV_start D10 ~ D8		

0x76 CKV duration time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
CKV_dur D7~D0							

0x77 CKV duration time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					CKV_dur D10 ~ D8		



ckv start time = ckv_start * 1/27Mhz
ckv duration time = ckv_dur * 1/27Mhz

Figure 4.13-6 CKV register setting diagram

4.13.8. STV timing control register

STV(Start pulse for gate driver) timing control register.

Address	**0x78~7f**
Default	All 00H

0x78 STV start time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
STV_start D7~D0							

0x79 STV start time high byte and OEV output polarity.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve			prechg_en	field_en	STV _pol	STV _start D9 ~ D8	

0x7a STV duration time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
STV _dur D7~D0							

0x7b STV duration time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve						STV _dur D9 ~ D8	

0x7c STV horizontal start time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
STV_hstart D7 ~ D0							

0x7d STV horizontal start time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					STV _hstart D10 ~ D8		

0x7e STV horizontal end time low byte.

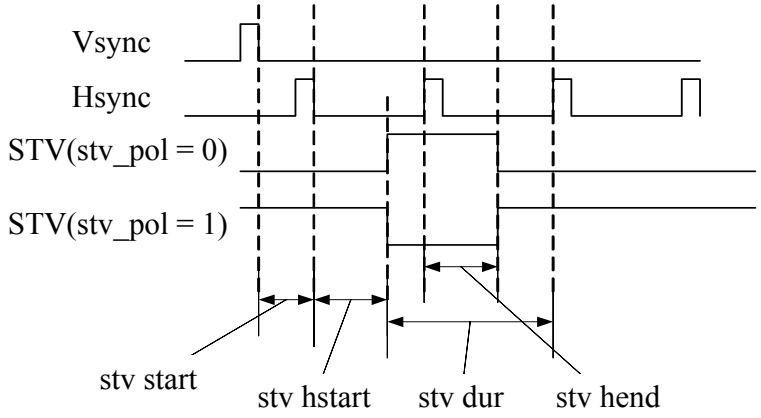
D7	D6	D5	D4	D3	D2	D1	D0
STV_hend D7 ~ D0							

0x7f STV horizontal end time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					STV_hend D10 ~ D8		

field_en : set this bit stv can set like interlace video vsync include field information

prechg_en : set this bit stv waveform can set like follow figure add one pulse before two line vertical start do precharge



stv start time = stv_start * 1 line time
stv duration time = stv_dur *1 line_time

Figure 4.13-7 STV register setting diagram

4.13.9. COM timing control register

COM timing control register.

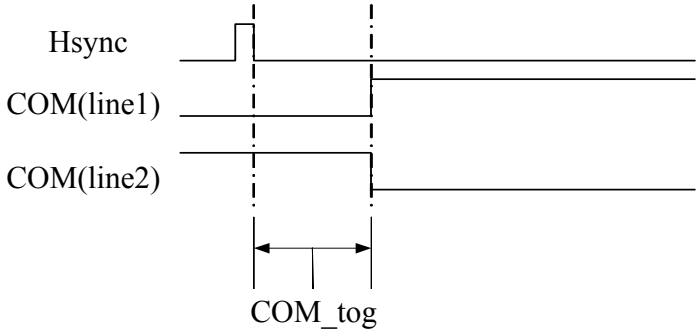
Address	**0x80~81**
Default	All 00H

0x80 COM toggle time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
COM_tog D7~D0							

0x81 COM toggle time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					COM_tog D10 ~ D8		



COM toggle time = com_tog * 1/27Mhz

Figure 4.13-8 COM register setting diagram

4.13.10. RGB invert time timing control register

RGB invert time control register.

Address	**0x82~83**
Default	All 00H

0x82 RGB_inv toggle time low byte.

D7	D6	D5	D4	D3	D2	D1	D0
RGB_inv_tog D7~D0							

0x83 RGB_inv toggle time high byte.

D7	D6	D5	D4	D3	D2	D1	D0
Reserve					RGB_inv_tog D10 ~ D8		

4.14 TPG(test pattern generator) control register

4.14.1. Test pattern generator control register 1

Address	**0xA0**
Default	**00H**

7	6	5	4	3	2	1	0
TPG enable	pattern select[2:0]			Pattern invert	c_change	c_direct	Reserve

TPG enable:

1 = enable

0 = disable

pattern select[2:0]:

000 = 16 step vertical gray scale

001 = 8 vertical color bar

010 = chessboard

011 = frame

100 = 16 step horizontal gray scale

101 = 8 horizontal color bar

110 =  pattern

111 = X pattern

Pattern invert: invert pattern sequence or color when pattern select is

0 or 1 or 4 or 5: invert the pattern sequence

2 or 3 or 6 or 7: invert the black and white

c_change: Gradual change color pattern enable

1 = enable

0 = disable

c_direct: Color change direction

0 = vertical

1 = horizontal

4.14.2. Test pattern generator control register 2

Address	**0xA1**
Default	**00H**

IF 0xA0(D2)=0

7	6	5	4	3	2	1	0
space_h[3:0]				space_v[3:0]			

space_h[3:0]: if pattern select is

000 = no effect

001 = no effect

010 = define the rectangle width (width = 2*space_h)

011 = define the horizontal border width

100 = no effect

101 = no effect

110 = define the vertical line width

space_v[3:0]: if pattern select is

000 = no effect

001 = no effect

010 = define the rectangle height (height = 2 * space_v)

011 = define the vertical border width

100 = no effect

101 = no effect

110 = define the horizontal line width

IF 0xA0(D2)=1

7	6	5	4	3	2	1	0
R_st[7:0]							

R_st[7:0]: Red start color(0~255)

4.14.3. Test pattern generator control register 3

Address	**0xA2**
Default	**00H**

IF 0xA0(D2)=0

7	6	5	4	3	2	1	0
Reserved				Pattern start color[3:0]			

Pattern start color[3:0]: if pattern select is

000 = define the first step of the gray bar

001 = define the first color of color bar(only bits [2:0] is used)

010 = define the line width

011 = no effect

100 = define the first step of the gray bar

101 = define the first color of color bar (only bits [2:0] is used)

110 = no effect

IF 0xA0(D2)=1

7	6	5	4	3	2	1	0
R_end[7:0]							

R_end[7:0]: Red end color(0~255)

4.14.4. Test pattern generator control register 4

Address	**0xA3**
Default	**00H**

7	6	5	4	3	2	1	0
G_st[7:0]							

G_st[7:0]: Green start color(0~255)

4.14.5. Test pattern generator control register 5

Address	**0xA4**
Default	**00H**

7	6	5	4	3	2	1	0
G_end[7:0]							

G_end[7:0]: Green end color(0~255)

4.14.6. Test pattern generator control register 6

Address	**0xA5**
Default	**00H**

7	6	5	4	3	2	1	0
B_st[7:0]							

B_st[7:0]: Blue start color(0~255)

4.14.7. Test pattern generator control register 7

Address	**0xA6**
Default	**00H**

7	6	5	4	3	2	1	0
B_end[7:0]							

B_end[7:0]: Blue end color(0~255)

4.15 RGBDAC control register

4.15.1. RGBDAC control register

Address	**0xA7**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve		PP_4V	SEL_P2	SEL_P1	SEL_P0	SEL_D1	SEL_D0

PP_4V: select 3V or 4V output

SEL_P2,SEL_P1,SEL_P0: select output voltage

SEL_D1,SEL_D0: select output DAC driver current

4.16 GPIO registers

4.16.1. GPIO control register

Address	**0xA8**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve	GPIO_CTL[6:0]						

GPIO_CTL: GPIO control register(1:GPI 0:GPO)

D6:PWM2 port control (If PWM2 is disable ,it is used as gpio)

D5:PWM1 port control (If PWM1 is disable ,it is used as gpio)

D4:PWM0 port control (If PWM0 is disable ,it is used as gpio)

D3: GPIO3 port control

D2: GPIO2 port control

D1: GPIO1 port control

D0: GPIO0 port control

4.16.2. GPI control register

Address	**0xA9**
Default	**Read only**

7	6	5	4	3	2	1	0
Reserve	GPI[6:0]						

GPI[6:0]: GPI value

4.16.3. GPO value register

Address	**0xAA**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve	GPO[6:0]						

GPO[6:0]: GPO value

4.16.4. Interrupt 1 control register

Address	**0xAB**
Default	**00H**

7	6	5	4	3	2	1	0
Intr_en[7:0]							

Intr_en[7:0]: Interrupt enable

1:enable

0: disable

D7: to detect reg.0x01 D2 (no_signal_digital) change or not

D6-0: to detect GPI[6:0] change or not

4.16.5. Interrupt 1 state register

Address	**0xAC**
Default	**00H**

7	6	5	4	3	2	1	0
Intr_state[7:0]							

Intr_state[7:0]: interrupt status of 0xAB

0: no interrupt

1: interrupt occur

Write: clear interrupt state

Read: interrupt state

4.16.6. Interrupt 2 control register

Address	**0xAD**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve		intr_en[5:0]					

Intr_en:interrupt enable

0:disable

1:enable

intr_en[5]: Enable the interrupt to detect if scaler memory read/write collision .

intr_en[4]: Reserved

intr_en[3]: Enable the interrupt to detect if input source vertical line change between two field.

intr_en[2]: Enable the interrupt to detect if register 0x3C(D3 chromalock) change or not.

intr_en[1]: Enable the interrupt to detect if register 0x3C(D2 625lines_detected) change or not.

intr_en[0]: Enable the interrupt to detect if register 0x3A(D0 no_signal) change or not.

4.16.7. Interrupt 2 Status register

Address	**0xAE**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve		intr_s[5:0]					

Intr_s : interrupt status of 0xAD

0 = no interrupt

1 = interrupt occur

Write: clear interrupt state

Read: interrupt state

4.17 Auto tracking and position register

4.17.1. Auto tracking and position control register

Address	**0xB0**
Default	00H

7	6	5	4	3	2	1	0
Reserve				auto_t_finish	auto_t_start	auto_p_enable	gain_en

auto_t_finish: Auto tracking finish(read only)

auto_t_start: Auto tracking start

auto_p_enable: Auto position enable

gain_en: Auto gain enable

4.17.2. Auto tracking sum register

Address	**0xB1-0xB4**
Default	**Read only**

7	6	5	4	3	2	1	0
auto_t_sum3[7:0]							
auto_t_sum2[7:0]							
auto_t_sum1[7:0]							
auto_t_sum0[7:0]							

auto_t_sum3[7:0]: Auto tracking sum[31:24]

auto_t_sum2[7:0]: Auto tracking sum[23:16]

auto_t_sum1[7:0]: Auto tracking sum[15:8]

auto_t_sum0[7:0]: Auto tracking sum[7:0]

4.17.3. Auto position threshold register

Address	**0xB5**
Default	**80H**

7	6	5	4	3	2	1	0
auto_p_threshold[7:0]							

auto_p_threshold[7:0]: Auto position threshold

4.17.4. Auto position up border register

Address	**0xB6**
Default	**Read only**

7	6	5	4	3	2	1	0
auto_p_up_border[7:0]							

auto_p_up_border[7:0]: Auto position upper border

4.17.5. Auto position down border register

Address	**0xB7**
Default	**Read only**

7	6	5	4	3	2	1	0
auto_p_dn_border[7:0]							

auto_p_dn_border[7:0]: Auto position down border

4.17.6. Auto position left border register low byte

Address	**0xB8**
Default	**Read only**

7	6	5	4	3	2	1	0
auto_p_l_border_lo[7:0]							

auto_p_l_border_lo[7:0]: Auto position left border [7:0]

4.17.7. Auto position left border register high byte and active pixel high byte

Address	**0xB9**
Default	**Read only**

7	6	5	4	3	2	1	0
Reserve		auto_p_l_border_hi[2:0]			auto_p_active_hi[2:0]		

auto_p_l_border_hi[2:0]: Auto position left border [10:8]

auto_p_active_hi[2:0]: Auto position active pixel[10:8]

4.17.8. Auto position active pixel low byte

Address	**0xBA**
Default	**Read only**

7	6	5	4	3	2	1	0
auto_p_active_lo[7:0]							

auto_p_active_lo[7:0]: Auto position active pixel[7:0]

4.17.9. Auto gain max red value

Address	**0xBB**
Default	**Read only**

7	6	5	4	3	2	1	0
gain_max_r[7:0]							

gain_max_r[7:0]: Auto gain max red value

4.17.10. Auto gain max green value

Address	**0xBC**
Default	**Read only**

7	6	5	4	3	2	1	0
gain_max_g[7:0]							

gain_max_g[7:0]: Auto gain max green value

4.17.11. Auto gain max blue value

Address	**0xBD**
Default	**Read only**

7	6	5	4	3	2	1	0
gain_max_b[7:0]							

gain_max_b[7:0]: Auto gain max blue value

4.17.12. Auto gain min red value

Address	**0xBE**
Default	**Read only**

7	6	5	4	3	2	1	0
gain_min_r[7:0]							

gain_min_r[7:0]: Auto gain min red value

4.17.13. Auto gain min green value

Address	**0xBF**
Default	**Read only**

7	6	5	4	3	2	1	0
gain_min_g[7:0]							

gain_min_g[7:0]: Auto gain min green value

4.17.14. Auto gain min blue value

Address	**0xC0**
Default	**Read only**

7	6	5	4	3	2	1	0
gain_min_b[7:0]							

gain_min_b[7:0]: Auto gain min blue value

4.17.15. Auto detect total line number low byte

Address	**0xC1**
Default	**Read only**

7	6	5	4	3	2	1	0
TOTAL_LINE_NUM_LO[7:0]							

TOTAL_LINE_NUM_LO: detect the total line number of the input source.

4.17.16. Auto detect total line number high byte

Address	**0xC2**
Default	**Read only**

7	6	5	4	3	2	1	0
Reserve					TOTAL_LINE_NUM_HI[2:0]		

TOTAL_LINE_NUM_HI[2:0]:

4.17.17. Detect the collide line buffer in scaling engine

Address	**0xC3**
Default	**00H**

7	6	5	4	3	2	1	0
Reserve							COL_DET_REG

COL_DET_REG: enable to detect the line buffer in scaling engine

4.17.18. Scaling line buffer colliding situation

Address	**0xC4**
Default	**Read only**

7	6	5	4	3	2	1	0
Reserve				STATE_REG[3:0]			

STATE_REG[3:0]: detect the read and write line buffer situation.

0: line buffer ok

b: It must be increase the htotalreg.

c: It must be decrease the htotalreg.

4.18 TV Decoder registers

Base address: 0xF0

Address	Bit	Name	Function Description
0xF0	TV decoder Address port		
	D7-0	TV_Addrport	Used to send tvdecoder registers address
0xF1	TV Decoder Data port		
	D7-0	TV_Dataport	Used to access tvdecoder registers data

4.18.1. VIDEO DECODER CONTROL0

Address	0x00
Default	00H

7	6	5	4	3	2	1	0
hv_delay	Hpixel[1:0]		vline_625	colour_mode[2:0]			yc_src

hv_delay:This bit emulates the HV-delay mode found Sony studio monitors

0 = disabled

1 = enabled

Hpixel[1:0]: These bits select the output display format.

Standard	pixels/line
00 = NTSC, PAL(M)	858
01 = PAL(B, D, G, H, I, N, CN), SECAM	864
10 = NTSC Square Pixel, PAL(M) Square Pixel	780
11 = PAL(B, D, G, H, I, N) Square Pixel	944

vline_625: This bit selects the number of scan lines per frame.

0 = 525

1 = 625

colour_mode[2:0]: These bits select video colour standard.

000 = NTSC

001 = PAL (I, B, G, H, D, N)

010 = PAL (M)

011 = PAL (CN)

100 = SECAM

yc_src: This bit selects input video format.

0 = composite

1 = S-Video (separated Y/C)

4.18.2. VIDEO DECODER CONTROL1

Address	0x01
Default	01H

7	6	5	4	3	2	1	0
cv_inv	cv_src	luma_notcha_bw[1:0]		chroma_bw_lo[1:0]		Chroma_burst5or10	ped

cv_inv: This bit inverts the select signal for the analog input multiplexer during component video mode.

0 = not inverted

1 = inverted

cv_src: This bit enables the component video input format.

0 = Disable the component video input

1 = Component-Video (Y,Pb,Pr)

luma_notcha_bw[1:0]: These bits select luma notch width

00 = none

01 = narrow

10 = medium

11 = wide

chroma_bw_lo[1:0]: This bit set the chroma low pass filter to wide or narrow

00 = narrow

01 = wide

10 = extra wide

11 = reserve

chroma_burst5or10: This bit selects the burst gate width

0 = 5 subcarrier clock cycles

1 = 10 subcarrier clock cycles

ped: This bit enables black level correction for 7.5 blank-to-black setup (pedestal).

0 = no pedestal subtraction

1 = pedestal subtraction(only NTSC mode must set this value)

4.18.3. VIDEO DECODER CONTROL2

Address	0x02
Default	4FH

7	6	5	4	3	2	1	0
hagc_field	Mv_hagc	dc_clamp_mode[1:0]		dagc_en	agc_half_en	cagc_en	hagc_en

hagc_field: When this bit is ì0î (the default), then the gain is updated once per line, after DC clamping. When this bit is set, then the gain is only updated once per field, at the start of vertical blank.

0 = off

1 = on

mv_hagc: This bit, when set, automatically reduces the gain (set in register 4) by 25% when macro-vision encoded signals are detected

0 = off

1 = on

dc_clamp_mode[1:0]: This bit sets the mode for the analog front end DC clamping

00 = auto

01 = backporch only

10 = synctip only

11 = off

dagc_en: This bit, when set, enables the digital AGC. The digital AGC is used in series with the analog gain.

0 = off

1 = on

agc_half_en: This bit, when set, enables the half gain mode, when unlocked, for the analog front end.

0 = off

1 = on

cagc_en: This bit when set enables the chroma AGC. If disabled, then the AGC target is used to drive directly the AGC gain.

0 = off

1 = on

hagc_en: This bit when set enables the luma/composite AGC. If disabled, then the AGC target (register 04h) is used to drive directly the AGC gain.

0 = off

1 = on

4.18.4. YC-Separation Control Registers

Address	0x03
Default	00H

7	6	5	4	3	2	1	0
Reserved				colour_trap	adaptive_mode[2:0]		

colour_trap: This bit enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting.

0 = Disabled (default)

1 = Enabled

adaptive_mode[2:0]: These bits select modes for the composite signalís luma (Y) and chroma (C) separation before colour demodulation.

000 = fully adaptive comb (2-D adaptive comb)

001 = vertical adaptive comb (1-D adaptive comb, vertical comb only)

010 = 5-tap adaptive comb filter (PAL mode only)

011 = basic luma notch filter mode (for very noisy and unstable pictures)

100 = simple 2-tap comb

101 = simple 3-tap comb

110 = 5-tap hybrid adaptive comb filter (PAL mode only)

4.18.5. Horizontal Acquisition Registers

Address	0x04
Default	DDH

7	6	5	4	3	2	1	0
Hagc[7:0]							

hagc: These bits specify the luma AGC target value. The gain of the AGC is modified until the horizontal sync height is equal to this value. Note that if a MacroVision signal is detected and ìmv_hagc_modeî (02.6h) is set, then this value is automatically reduced by 25%.

Standard	Programming Value
NTSC M	DDh (221d) (default)

NTSC J	CDh (205d)
PAL B,D,G,H,I,	DCh (220d)
COMB N,	
SECAM	
PAL M,N	DDh (221d)
NTSC M (MACROVISIOIN)	A6h (166d)
PAL B,D,G,H,I,	AEh (174d)
COMB N (MACROVISION)	

If ìhagc_enî (register 02.0h) is ì0î, then ìhagcî is used to directly drive the analog gain. In this case, a value of 64 represents a unity gain, 32 represents a one-half gain, and 128 denotes a double gain.

4.18.6. NOISE_THRESHOLD

Address	0x05
Default	32H

7	6	5	4	3	2	1	0
noise_thresh[7:0]							

noise_thresh: This value sets the noise value at which the circuit considers a signal noisy. The detected noise value may be read back through register 7Fh (ìstatus_noiseî). If the detected noise value is greater than ìnoise_threshî, then register bit 3C.3h (ìnoisyî) is set. Larger values of ìstatus_noiseî indicate noisier signals, so larger values of ìnoise_threshî decreases the likelihood of ìnoisyî being set while smaller values of ìnoise_threshî increases the likelihood of ìnoisyî being set.

4.18.7. AGC_GATE_THRESHOLD and ADC_SWAP

Address	0x06
Default	0AH

7	6	5	4	3	2	1	0
adc_updn_swap	adc_input_swap	adc_cbcr_pump_swap	agc_gate_thresh[4:0]				

adc_updn_swap: This bit swaps the DC clamp up/down controls to the analog front-end.

0 = Disabled

1 = Enabled

adc_input_swap: This bit swaps the MSBs and LSBs from the analog front-endís ADC

0 = Disabled

1 = Enabled

adc_cbcr_pump_swap : This bit swaps the Pb/Pr charge pump pairs to the analog front-end

0 = Disabled

1 = Enabled

agc_gate_thresh[4:0]: This specifies the threshold at which the rough gate generator creates a sync gate.

4.18.8. Output Control Registers

Address	**0x07**
Default	**20H**

7	6	5	4	3	2	1	0
reserved	cbcr_swap	blue_mode[1:0]		yc_delay[3:0]			

cbcr_swap: This bit swaps Cb/Cr outputs.

0 = donít swap Cb/Cr

1 = swap Cb/Cr

blue_mode[1:0]: This bit controls the blue screen mode.

00 = Disabled

01 = Enabled

10 = Auto

11 = reserved

yc_delay[3:0]: This 2ís complement number controls the output delay between luma and chroma. Negative values shift luma outputs to the left while positive values shift luma values to the right. The range is [-5,7].

4.18.9. LUMA CONTRAST ADJUSTMENT

Address	**0x08**
Default	**80H**

7	6	5	4	3	2	1	0
Contrast[7:0]							

Contrast[7:0]: These bits control the adjustable gain to the luma output path

4.18.10. LUMA BRIGHTNESS ADJUSTMENT

Address	**0x09**
Default	**20H**

7	6	5	4	3	2	1	0
Brightness[7:0]							

Brightness[7:0]: These bits control the adjustable brightness level to the luma output path.
This value is offset by -32, i.e., a value of 32 (the default) implies a brightness level of 0, and a value of 0 implies a brightness level of -32.Chroma Adjustment Registers

4.18.11. CHROMA SATURATION ADJUSTMENT

Address	**0x0A**
Default	**80H**

7	6	5	4	3	2	1	0
saturation[7:0]							

Saturation[7:0]: These bits adjust the colour saturation

4.18.12. CHROMA HUE PHASE ADJUSTMENT

Address	**0x0B**
Default	**00H**

7	6	5	4	3	2	1	0
hue[7:0]							

Hue[7:0]:This 2ís complement number adjusts the hue phase offset.

4.18.13. CHROMA AGC

Address	**0x0C**
Default	**8AH**

7	6	5	4	3	2	1	0
cagc[7:0]							

cagc[7:0]: These bits set the chroma AGC target.

4.18.14. CHROMA KILL

Address	**0x0D**
Default	**07H**

7	6	5	4	3	2	1	0
user_ckill_mode[1:0]		vbi_ckill	hlock_ckill	chroma_kill[3:0]			

user_ckill_mode[1:0]:

00: uses auto hardware chroma kill

01: forces chroma kill on and

10: forces chroma kill off.

vbi_ckill: When set, chroma is killed during VBI.

hlock_ckill: When set, chroma is killed whenever horizontal lock is lost.

chroma_kill[3:0]: These bits set the chroma kill level.

4.18.15. CHROMA AUTOPOSITION

Address	**0x0F**
Default	**2CH**

7	6	5	4	3	2	1	0
Reserved		fixed_burstgate	Cautopos[4:0]				

fixed_burstgate: The manual burstgate window position is defined by the burst_gate_start(0x2c) and burst_gate_end(0x2d) register.

Cautopos[4:0]: These bits set the chroma burst gate position relative to the auto centre position

When set, this bit disables the burst gate autoposition.

4.18.16. Front End Control

4.18.17. AGC PEAK NOMINAL

Address	**0x10**
Default	**0AH**

7	6	5	4	3	2	1	0
reserved	Agc_peak_nominal[6:0]						

agc_peak_nominal[6:0]: These bits set the luma peak white detectionís AGC nominal peak white value.This value is added to 128 and then the result is multiplied by 4

4.18.18. AGC PEAK AND GATE CONTROLS

Address	**0x11**
Default	**99H**

7	6	5	4	3	2	1	0
agc_gate_vsync_coarse	gc_gate_vsync_stip	agc_gate_kill_mode[1:0]		agc_peak_en	agc_peak_cntl[2:0]		

agc_gate_vsync_coarse: This bit forces coarse sync-tip and backporch gates to be used during vsync when VCRs are detected.

gc_gate_vsync_stip: This bit forces sync-tip clamping during vsync.

agc_gate_kill_mode[1:0]: These bits determine the method that sync-tip and backporch gates are suppressed:

00 = off

01 = enabled ñ if sync-tip gate is killed, kill backporch gate(default)

10 = enabled ñ if sync-tip gate is killed, kill backporch gate, except during vsync

11 = enabled ñ if sync-tip gate is killed, do not kill backporch gate

agc_peak_en: This bit enables the AGC peak white detector.

agc_peak_cntl[2:0]: These bits set the time constant for the AGC peak white detector.

4.18.19. AGC GATE START

Address	**0x12-0x13**
Default	**0682H**

Address	7	6	5	4	3	2	1	0
0x12	reserved					agc_gate_start[10:8]		
0x13	agc_gate_start[7:0]							

agc_gate_start[10:0]: These high-order bits set the delay from the detected hsync for the rough gate generator

4.18.20. AGC GATE WIDTH

Address	**0x14**
Default	**40H**

7	6	5	4	3	2	1	0
reserved	Agc_gate_width[6:0]						

agc_gate_width[6:0]: These bits set the width of the rough gates

4.18.21. AGC BP DELAY

Address	**0x15**
Default	**64H**

7	6	5	4	3	2	1	0
agc_bp_delay[7:0]							

agc_bp_delay[7:0]: These bits set the time delay from the sync tip gate to the backporch gate for the rough gate generator.

4.18.25. Chroma DTO Registers

CHROMA DTO INCREMENT

Address	**0x18-0x1B**
Default	**21F07C1FH**

Address	7	6	5	4	3	2	1	0
0x18	cdto_fixed	reserved	cdto_inc[29:24]					
0x19	cdto_inc[23:16]							
0x1A	cdto_inc[15:8]							
0x1B	cdto_inc[7:0]							

cdto_fixed: This bit, when set, fixes the chroma DTO at its center frequency.

cdto_inc[29:0]: These bits contain bits 29:24 of the 30-bit-wide chroma DTO increment.

4.18.26. Horizontal Sync DTO Registers

4.18.27. HORIZONTAL SYNC DTO INCREMENT

Address	**0x1C-0x1F**
Default	**20000000H**

Address	7	6	5	4	3	2	1	0
0x1C	hdto_fixed	reserved	hdto_inc[29:24]					
0x1D	hdto_inc[23:16]							
0x1E	hdto_inc[15:8]							
0x1F	hdto_inc[7:0]							

hdto_fixed: This bit, when set, fixes the horizontal sync DTO at its center frequency.

hdto_inc[29:0]: These bits contain bits 29:24 of the 30-bit-wide horizontal sync DTO increment.

4.18.28. Horizontal Sync Detection Registers

4.18.29. HORIZONTAL SYNC RISING-EDGE OCCURRENCE TIME

Address	**0x20**
Default	**3EH**

7	6	5	4	3	2	1	0
hsync_rising[7:0]							

hsync_rising[7:0]: These bits set the position of the expected hsync rising edge. It is used by the fine hsync detector. The fine detector uses this time position to sample the video signal for the rising edge of the hsync.

4.18.30. HORIZONTAL SYNC PHASE OFFSET

Address	**0x21**
Default	**3EH**

7	6	5	4	3	2	1	0
hsync_phase_offset[7:0]							

hsync_phase_offset[7:0]: This register sets the offset value between the coarse hsync detector and the fine hsync detector. Nominally set to 62. The course detector actually finds the middle of the hsync so we need to subtract the nominal hsync width to find the beginning of the hsync.

4.18.31. HORIZONTAL SYNC DETECT WINDOW START TIME

Address	**0x22**
Default	**00H**

7	6	5	4	3	2	1	0
hsync_gate_start[7:0]							

hsync_gate_start[7:0]: These bits control the PLL horizontal sync detect window for coarse sync detection. This specifies the beginning of the window.

4.18.32. HORIZONTAL SYNC DETECT WINDOW END TIME

Address	**0x23**
Default	**80H**

7	6	5	4	3	2	1	0
hsync_gate_end[7:0]							

hsync_gate_end[7:0]: These bits control the PLL horizontal sync detect window for coarse sync detection. This specifies the end of the window.

4.18.33. HORIZONTAL SYNC TIP DETECT WINDOW START TIME

Address	**0x24**
Default	**E9H**

7	6	5	4	3	2	1	0
hsync_tip_start[7:0]							

hsync_tip_start[7:0]:These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the beginning of the window.

4.18.34. HORIZONTAL SYNC TIP DETECT WINDOW END TIME

Address	**0x25**
Default	**0FH**

7	6	5	4	3	2	1	0
hsync_tip_end[7:0]							

hsync_tip_end[7:0]: These bits control the PLL horizontal sync tip detect window used for AGC control.This specifies the end of the window.

4.18.35. HORIZONTAL SYNC RISING-EDGE DETECT WINDOW START TIME

Address	**0x26**
Default	**2DH**

7	6	5	4	3	2	1	0
hsync_rising_start[7:0]							

hsync_rising_start[7:0]: These bits provide a programmable start time of the window that looks for the rising edge of the hsync. This is used by the coarse hsync detector.

4.18.36. HORIZONTAL SYNC RISING-EDGE DETECT WINDOW END TIME

Address	**0x27**
Default	**50H**

7	6	5	4	3	2	1	0
hsync_rising_end[7:0]							

hsync_rising_end[7:0]: These bits provide a programmable end time for the window which spans across the rising-edge of the horizontal sync pulse.

4.18.37. BACKPORCH INTERVAL START TIME

Address	**0x28**
Default	**22H**

7	6	5	4	3	2	1	0
backporch_start[7:0]							

backporch_start[7:0]: These bits control the backporch detect window. This specifies the beginning of the window.

4.18.38. BACKPORCH INTERVAL END TIME

Address	**0x29**
Default	**4EH**

7	6	5	4	3	2	1	0
backporch_end[7:0]							

backporch_end[7:0]: These bits control the backporch detect window. This specifies the end of the window

4.18.39. HSYNC FILTER GATE START TIME

Address	**0x2A**
Default	**D6H**

7	6	5	4	3	2	1	0
hblank_start[7:0]							

hblank_start[7:0]: These bits specify the beginning of the horizontal-blank-interval window.

4.18.40. HSYNC FILTER GATE END TIME

Address	**0x2B**
Default	**4EH**

7	6	5	4	3	2	1	0
hblank_end[7:0]							

hblank_end[7:0]: These bits specify the end of the horizontal-blank-interval window.

4.18.41. CHROMA BURST GATE START TIME

Address	**0x2C**
Default	**32H**

7	6	5	4	3	2	1	0
burst_gate_start[7:0]							

burst_gate_start[7:0]: This specifies the beginning of the burst gate window. Note that this window is set to be bigger than the burst. The automatic burst position tracker finds the burst within this window.

4.18.42. CHROMA BURST GATE END TIME

Address	**0x2D**
Default	**46H**

7	6	5	4	3	2	1	0
burst_gate_end[7:0]							

burst_gate_end[7:0]: These bits specifies the end of the burst gate window

4.18.43. ACTIVE VIDEO HORIZONTAL START TIME

Address	**0x2E**
Default	**82H**

7	6	5	4	3	2	1	0
hactive_start[7:0]							

hactive_start[7:0]: These bits control the active video line time interval. This specifies the beginning of active line. This register is used to centre the horizontal position, and should *not* be used to crop the image to a smaller size.

4.18.44. ACTIVE VIDEO HORIZONTAL WIDTH

Address	**0x2F**
Default	**50H**

7	6	5	4	3	2	1	0
hactive_width[7:0]							

hactive_width[7:0]: These bits control the active video line time interval. This register specifies the width of
the active line, and should *not* be used to crop the image to a smaller size. The value 640
is added to this register.

4.18.45. Vertical Sync and Field Detection Registers

4.18.46. ACTIVE VIDEO VERTICAL START

Address	**0x30**
Default	**22H**

7	6	5	4	3	2	1	0
vactive_start[7:0]							

vactive_start[7:0]: These bits control the first active video line in a field. This specifies the number of halflines from the start of a field.

4.18.47. ACTIVE VIDEO VERTICAL HIGHT

Address	**0x31**
Default	**61H**

7	6	5	4	3	2	1	0
vactive_height[7:0]							

vactive_height[7:0]: These bits control the active video height. This specifies the height by the number of half lines. The value 384 is added to this register.

4.18.48. VSYNC H LOCKOUT START

Address	**0x32**
Default	**F0H**

7	6	5	4	3	2	1	0
vsync_h_min[7:0]							

vsync_h_min[7:0]: This register defines the number of half-lines before the vsync that the hsync detector circuit is disabled. This is to make sure that the HPLL is not confused by the equalization pulses and the broad pulses. Also in VCR trick modes the VSYNC is just one 3 line wide pulse with no hsync structure so it must be ignored.

4.18.49. VSYNC H LOCKOUT END

Address	**0x33**
Default	**0EH**

7	6	5	4	3	2	1	0
vsync_h_max[7:0]							

vsync_h_max[7:0]: This register defines the number of half-lines after the vsync that the hsync detector circuit is re-enabled.

4.18.50. VSYNC AGC LOCKOUT START

Address	**0x34**
Default	**ECH**

7	6	5	4	3	2	1	0
vsync_agc_min[7:0]							

vsync_agc_min[7:0]: This register defines the number of half-lines before the vsync that the AGC, SYNCTIP, and BACKPORCH gates are disabled.

4.18.51. VSYNC AGC LOCKOUT END

Address	**0x35**
Default	**90H**

7	6	5	4	3	2	1	0
vsync_agc_mode[1:0]		vsync_agc_max[5:0]					

vsync_agc_mode[1:0]:These bits control DC clamping during the vertical blanking interval.

00 = disabled

01 = enabled

10 = enabled except for noisy signals (default)

11 = enabled except for noisy signals and VCRs

vsync_agc_max[5:0]: This register defines the number of half-lines after the vsync that the AGC, SYNCTIP, and BACKPORCH gates are re-enabled.

4.18.52. VSYNC VBI LOCKOUT START

Address	**0x36**
Default	**F0H**

7	6	5	4	3	2	1	0
vsync_vbi_min[7:0]							

vsync_vbi_min[7:0]: This register defines the number of half-lines before the VSYNC that VBI data is valid.

4.18.53. VSYNC VBI LOCKOUT END

Address	**0x37**
Default	**0EH**

7	6	5	4	3	2	1	0
vsync_vbi_max[7:0]							

vsync_vbi_max[7:0]: after the VSYNC that VBI data is valid.

4.18.54. VSYNC PLL Control

4.18.55. VSYNC_CNTL

Address	**0x38**
Default	**00H**

7	6	5	4	3	2	1	0
vsync_cntl[1:0]		vsync_threshold[5:0]					

vsync_cntl[1:0]: These bits set the vsync output mode

00 = output the vertical PLL vsync when the signal is noisy; otherwise use directly derived vsync (default)

01 = output the directly detected vsync

10 = output the vertical PLL derived vsync

11 = output the PLL vsync in alternate mode

vsync_threshold[5:0]: This register specifies a relative threshold to add to the slice level for the purpose of vsync detection. Default = 0 (2ís complement value)

4.18.56. VSYNC TIME CONSTANT

Address	**0x39**
Default	**0AH**

7	6	5	4	3	2	1	0
field_polarity	flip_field	veven_delayed	vodd_delayed	field_detect_mode[1:0]		vloop_tc[1:0]	

field_polarity: This bit sets the output field polarity.

0 ⇒ field=1 for odd fields, field=0 for even fields (default)

1 ⇒ field=0 for odd fields, field=1 for even fields

flip_field: This bit flips even/odd fields

veven_delayed: This bit delays detection of even fields by 1 vertical line.

vodd_delayed: This bit delays detection of odd fields by 1 vertical line.

field_detect_mode[1:0]: These bits control the field detection logic.

vloop_tc[1:0]: These bits set the vertical PLL time constant

00 = fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1.

01 = moderate. Internal values are 1 and º .

10 = slow. Internal values are Ω and 1/16 (default)

11 = very slow. Most useful for noisy signals. Internal values are º and Ω

4.18.57. Status Registers

4.18.58. VIDEO DECODER STATUS REGISERT 1

Address	**0x3A**
Default	**Read only**

7	6	5	4	3	2	1	0
mv_colourstripes[2:0]			mv_vbi_detected	chromalock	vlock	hlock	no_signal

mv_colourstripes[2:0]: Macrovision colour stripes detected. The number indicates the number of colour stripe lines in each group

mv_vbi_detected: MacroVision VBI pseudo-sync pulses detection

1 = Detected

0 = Undetected

chromalock: Chroma PLL locked to colour burst

1 = Locked

0 = Unlocked

vlock: Vertical lock

1 = Locked

0 = Unlocked

hlock: Horizontal line locked

1 = Locked

0 = Unlocked

no_signal: No signal detection

1 = No Signal Detected

0 = Signal Detected

4.18.59. VIDEO DECODER STATUS REGISERT 2

Address	**0x3B**
Default	**Read only**

7	6	5	4	3	2	1	0
reserved							proscan_detected

proscan_detected: Progressive Scan Detected

4.18.60. VIDEO DECODER STATUS REGISERT 3

Address	**0x3C**
Default	**Read only**

7	6	5	4	3	2	1	0
vcr_rew	vcr_ff	vcr_trick	vcr	noisy	625lines_detected	SECAM_detected	PAL_detected

vcr_rew: VCR Rewind Detected

vcr_ff: VCR Fast-Forward Detected

vcr_trick: VCR Trick-Mode Detected

vcr: VCR Detected

noisy: Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the ìnoise_threshî register (05h).

625lines_detected: 625 Scan Lines Detected

SECAM_detected: SECAM Colour Mode Detected

PAL_detected: PAL Colour Mode Detected

4.18.61. HORIZONTAL SYNC DTO INCREMENT STATUS

Address	**0x70-0x73**
Default	**Read only**

Address	7	6	5	4	3	2	1	0
0x70	reserved		status_hdto_inc[29:24]					
0x71	status_hdto_inc[23:16]							
0x72	status_hdto_inc[15:8]							
0x73	status_hdto_inc[7:0]							

status_hdto_inc[29:0]: These bits contain status bits 29:24 of the 30-bit-wide horizontal sync DTO increment.

4.18.62. CHROMA SYNC DTO INCREMENT STATUS

Address	**0x74-0x77**
Default	**Read only**

Address	7	6	5	4	3	2	1	0
0x74	reserved		status_cdto_inc [29:24]					
0x75	status_cdto_inc [23:16]							
0x76	status_cdto_inc [15:8]							
0x77	status_cdto_inc [7:0]							

status_cdto_inc [29:0]: These bits contain status bits 29:24 of the 30-bit-wide chroma sync DTO increment.

4.18.63. AGC ANALOG GAIN STATUS

Address	**0x78**
Default	**Read only**

7	6	5	4	3	2	1	0
agc_again[7:0]							

agc_again[7:0]: These bits contain the analog AGC gain value.

4.18.64. AGC DIGITAL GAIN STATUS

Address	**0x79**
Default	**Read only**

7	6	5	4	3	2	1	0
agc_dgain[7:0]							

agc_dgain[7:0]: These bits contain the digital AGC gain value.

4.18.65. CHROMA MAGNITUDE STATUS

Address	**0x7A**
Default	**Read only**

7	6	5	4	3	2	1	0
status_cmag[7:0]							

status_cmag[7:0]: These bits contain the chroma magnitude.

4.18.66. CHROMA GAIN STATUS

Address	**0x7B-0x7C**
Default	**Read only**

Address	7	6	5	4	3	2	1	0
0x7B	reserved		status_cgain[13:8]					
0x7C	status_cgain[7:0]							

status_cgain[13:0]: These bits contain the high order of the chroma gain.

4.18.67. CORDIC FREQUENCY STATUS

Address	**0x7D**
Default	**Read only**

7	6	5	4	3	2	1	0
status_cordiq_frerq[7:0]							

status_cordiq_frerq[7:0]:These bits contain the SECAM cordic frequency.

4.18.68. VIDEO DECODER STATUS

Address	**0x7F**
Default	**Read only**

7	6	5	4	3	2	1	0
status _noise[7:0]							

status _noise[7:0]: This registers indicates how noisy the signal is. Larger values indicate noisier signals. This register is used in conjunction with programmable register 05h, ìnoise_threshî and status bit 3C.3h, ìnoisyî.

4.18.69. Luma Peaking Registers

LUMA PEAKING

Address	**0x80**
Default	**04H**

7	6	5	4	3	2	1	0
Reserved		peak_range[1:0]		peak_gain[2:0]			peak_en

peak_range[1:0]: These bits set the range of peak_gain.

Setting	peak_range value
00	1
01	2
10	4
11	8

Ypeak = Y + YH *(peak_gain/peak_range) where Y is the luma and YH is the high frequency luma only

peak_gain[2:0]: These bits set the gain for the luma horizontal peaking control. This allows adjustable gain to the luma around the colour subcarrier frequency.

peak_en: This bit enables the luma horizontal peaking control around the colour subcarrier frequency

0 = Disabled

1 = Enabled

4.18.70. Comb Filter Configuration Registers

4.18.71. VIDEO DECODER COMB FILTER CONFIG

Address	**0x82**
Default	**42H**

7	6	5	4	3	2	1	0
reserved	pal_perr	pal_perr_auto_en	comb_wide_band	reserved		palsw_level	

pal_perr: This bit is used to reduce phase-error artifacts in the comb filterís luma-path. It should be set for VCR signals.

pal_perr_auto_en: When set, this will turn on the pal_perr when VCR signals is detected.

comb_wide_band: This bit is used to select the bandpass filter used in the comb-filter. This should be set to 1 for PAL mode.

palsw_level[1:0]: This bit is used to determine how many incorrect lines are used for the pal switch circuit before switching. Use a higher level for noisy signals.

4.18.72. Chroma-Lock Configuration Registers

VIDEO DECODER CHROMA_LOCK CONFIG

Address	**0x83**
Default	**6FH**

7	6	5	4	3	2	1	0
lose_chromalock_count[3:0]				lose_chromalock_level[2:0]			lose_chromalock_ckill

lose_chromalock_count[3:0]: This register is used to tune the chromakill, higher values are more sensitive to losing lock.

lose_chromalock_level[2:0]: Set the level for chromakill.

lose_chromalock_ckill: When set, chroma is killed whenever chromlock is lost.

4.18.73. Comb Filter Threshold Registers

VIDEO DECODER COMB FILTER THRESHOLD1

Address	**0x84**
Default	**07H**

7	6	5	4	3	2	1	0
noise_ntsc_c[7:0]							

noise_ntsc_c[7:0]: These register bits are used to tune the noise_threshold used by the comb filter for NTSC.

4.18.74. VIDEO DECODER COMB FILTER THRESHOLD2

Address	**0x85**
Default	**20H**

7	6	5	4	3	2	1	0
noise_pal_c[7:0]							

noise_pal_c[7:0]: These register bits are used to tune the noise_threshold used by the comb filter for PAL.

4.18.75. VIDEO DECODER COMB FILTER THRESHOLD3

Address	**0X86**
Default	**03H**

7	6	5	4	3	2	1	0
noise_phase_c[7:0]							

noise_phase_c[7:0]: These register bits are used to tune the noise_threshold used by the chroma comb filter.

4.18.76. VIDEO DECODER COMB FILTER THRESHOLD4

Address	**0x87**
Default	**10H**

7	6	5	4	3	2	1	0
noise_phase_y[7:0]							

noise_phase_y[7:0]: These register bits are used to tune the noise_threshold used by the luma comb filter.

4.18.77. VIDEO DECODER CHROMA LOOPFIL STATE

Address	**0x8A**
Default	**0AH**

7	6	5	4	3	2	1	0
reserved				Cstate[2:0]			fixed_state

Cstate[2:0]: This register sets the chroma loopfilter bandwidth state, larger state has a slower response.
fixed_state: This register fixes the state of chroma loopfilter to cstate.

4.18.78. VIDEO DECODER CHROMA HRESAMPLER CONTROL

Address	**0x8B**
Default	**01H**

7	6	5	4	3	2	1	0
reserved							hresampler_2up

hresampler_2up: Upsample the chroma by 2 before going into the hresampler.

4.18.79. VIDEO DECODER CHARGE PUMP DELAY CONTROL

Address	**0x8D**
Default	**28H**

7	6	5	4	3	2	1	0
cpump_adjust_delay[5:0]						cpump_adjust_polarity	cpump_delay_en

cpump_adjust_delay[5:0]: Delay, relative to charge-pump pulses, before adjustment, used to

compensate for possible visible artefacts caused by charge-pump pulses, is applied.

cpump_adjust_polarity: Polarity of adjustment used to compensate for possible visible artefacts caused by charge-pump pulses.

cpump_delay_en:Enable delay of charge-pump up/down pulses.

4.18.80. VIDEO DECODER CHARGE PUMP ADJUSTMENT

Address	**0x8E**
Default	**C8H**

7	6	5	4	3	2	1	0
cpump_adjust[7:0]							

cpump_adjust[7:0]: Value used to compensate for possible visible artefacts caused by charge-pump pulses.

4.18.81. VIDEO DECODER CHARGE PUMP DELAY

Address	**0x8F**
Default	**B9H**

7	6	5	4	3	2	1	0
cpump_delay[7:0]							

cpump_delay[7:0]: If ìcpump_delay_en == 1î, then the charge pump up/down pulses are delayed by ì4 ×cpump_delayî output pixels.

Default = 185 ➔ 740 output pixel delay.

4.18.82. VIDEO DECODER RESET REGISTER

Address	**0x3F**
Default	**01H**

7	6	5	4	3	2	1	0
reserve							Soft_reset

soft_reset: reset the status of Video Decoder,but do not reset registers

4.18.83. General ADC Control Register

Address	**0x90**
Default	**1CH**

7	6	5	4	3	2	1	0
reserve		swann	envbg	enref	envcm	swib	bypass

swann: External analog input reference selector

Normal operation swann = 0

envbg: Power On for Bandgap Generator

enref: Power On for Reference Generator

envcm: Power On for Reference Generator

swib: External Current Reference selector

bypass: Bypass PGA for testing purpose only(normal operation bypass=0)

4.18.84. Luma ADC control 1

Address	**0x91**
Default	**00H**

7	6	5	4	3	2	1	0
CVBS_sel	Anysel[1:0]		Pgay[2:0]			Da0[1:0]	

CVBS_sel: This bit select the CVBS source.

0: CVBS1

1: CVBS2

Anysel[1:0]: Luma channel mux selector

Pgay[2:0]: Channel DAC Clamp Current Setting

Da0[1:0]: Luma current setting

4.18.85. Luma ADC control 2

Address	**0x92**
Default	**04H**

7	6	5	4	3	2	1	0
Reserved				enchy	enclpy	clpyref	clpysel

enchy: Luma(Y) power down

Normal operation enchy = 1

enclpy: Luma(Y) clamp enable

Enable clamp enclpy = 1

clpyref: Luma(Y) clamp level

Bottom clamp clpyref = 0

clpysel: Luma(Y) clamp type select

DAC type clpysel = 0

4.18.86. ADC2 CONTROL 1

Address	**0x93**
Default	**00H**

7	6	5	4	3	2	1	0
reserved	Anpbsel[1:0]		Pgapb[2:0]			da1[1:0]	

Anpbsel[1:0]:Chroma(C) input selector

Pgapb[2:0]: Chroma(C) PGA Input Gain settings

da1[1:0]:Chroma(C) current setting

4.18.87. ADC2 CONTROL 2

Address	**0x94**
Default	**04H**

7	6	5	4	3	2	1	0
Reserved				enchpb	enclppb	clppbref	clppbsel

enchpb: Chroma(C) power down

Normal operation enchpb = 1

enclppb: Chroma(C) clamp enable

Enable clamp enclppb = 1

clppbref: Chroma(C) clamp level

Bottom clamp clppbref = 0

clppbsel: Chroma(C) clamp type select

DAC type clppbsel = 0

ADC operating modes

Mode	Objective	Configuration								
		enchy	enchpb	enchpr	envbg	enref	envcm	swib	swann	bypass
0	Complete Power Down	0	0	0	0	0	0	0	X	X
1	Normal operating mode with the three channels active	1	1	1	1	1	1	0	0	0
2	Luminance channel (Y) off	0	1	1	X	X	X	X	X	0
3	Chroma (C) channel off	1	0	1	X	X	X	X	X	0
4	Reserved	1	1	0	X	X	X	X	X	0
5	Normal operation with bypass of internal bandgap	1	1	1	0	1	1	0	0	0
6	Normal operation with bypass of internal vcm buffer	1	1	1	1	1	0	0	0	0
7	Normal operation with bypass of internal vrefn and vrefp	1	1	1	1	0	1	0	0	0
8	Normal operation with external bias current generation	1	1	1	1	1	1	1	0	0
9	Normal operation with external analog input reference	1	1	1	X	X	X	X	1	0
10	Bypass of Luma PGA-S/H (testing purposes only)	1	0	0	X	X	X	X	X	1

Mode 0 - Power Down

In this mode all the circuitry is in power-down (including references). The power dissipation is reduced to a minimum value.

Mode 1 - Normal operation with the three channels active and no bypassing

This is the normal mode of operation where the three channels are active.

Modes 2, 3 and 4 ñ Individual channel Power Down

Each one of the channels can be selectively bypassed. The bypass of voltage and current references are still possible (modes 5 to 8).

Mode 5 to 9 - Conversion Mode with different reference and bias bypassing

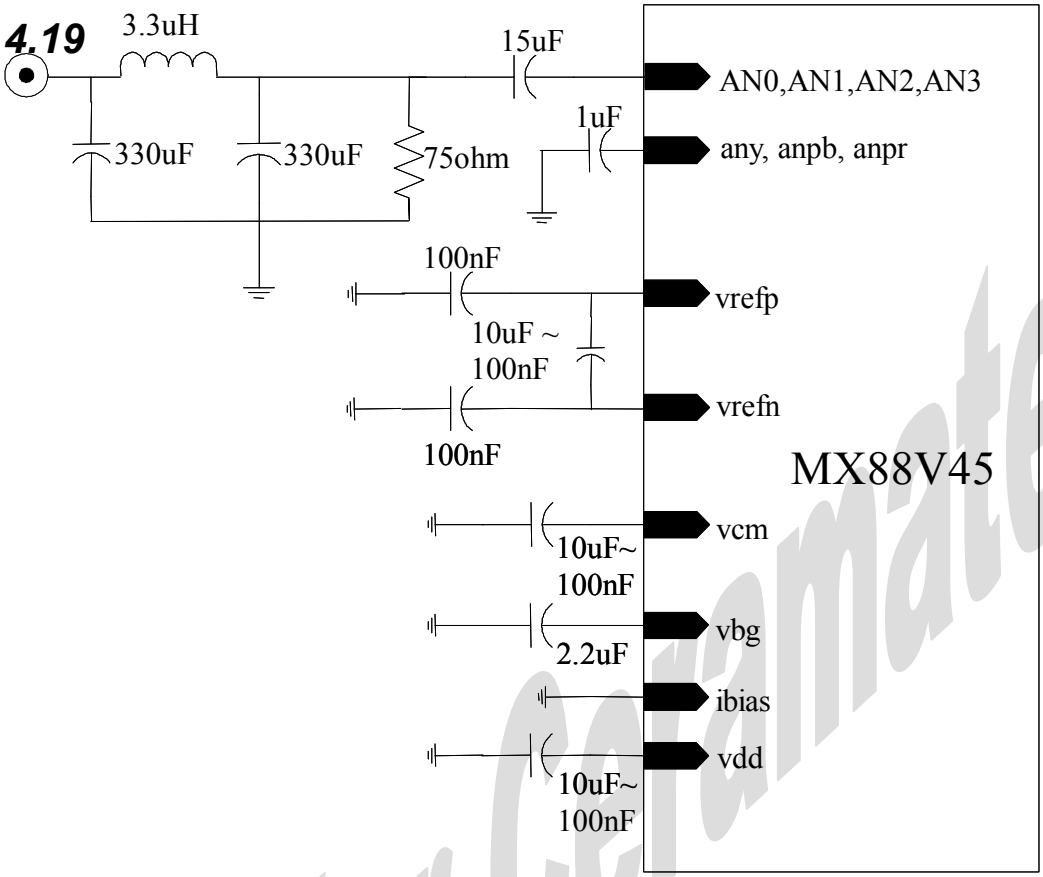
Several different bypassing options can be selected with the pins envbg, enref, envcm, swib and swann.

Mode 10 - Conversion Mode with PGA/S&H bypassing

These operating modes are for testing purposes. In conjunction with the signals enchy, enchpb and enchpr, the PGA-S/H for each channel can be selectively bypassed. The differential inputs Vbyn and Vbyp) are connected directly to the output of the powered-down PGA-S/H. Vbyn and Vbyp must have 1 Vpp range and are centered in avdd/2. Only the selected channel for bypass is turned on.

The bypass of voltage and current references are still possible (modes 5 to 8).

4.18.88. ADC application reference circuit



OSD External registers

Base address: 0xF2

Address	Bit	Name	Description
0xF2	AddrLSBSel (Address LSB of internal OSD) The meaning of this register depends of Reg. 0xF6[1:0](default= 8íh0)		
	bit	0xF6[1:0]	Reg. 0xF2 description
	D7-0	00	Address of Internal OSD control register
	D5-0	01	Char code of font table RAM
	D6-0	10	Address of code buffer
	D6-0	11	Address of attribute buffer
0xF3	AddrMSBSel (Address MSB of internal OSD) The meaning of this register depends of reg. 0xA4[1:0](default = 8íh0)		
	bit	0x F6 [1:0]	Reg. 0xF3 description
		00	Not used
	D4-0	01	Scan line of the font appointed by reg0xA0 (0 to 0x11)
		10	Not used
		11	Not used
0xF4	DataLSBSel (Data LSB of internal OSD) The meaning of this register depends of reg. 0xF6[1:0](default = 8íh0)		
	bit	0x F6 [1:0]	Reg. 0xF4 description
	D7-0	00	Data port of internal OSD control register
	D7-0	01	Data LSB of font table RAM
	D7-0	10	Data LSB of code buffer
	D7-0	11	Data LSB of attribute buffer
0xF5	DataMSBSel (Data MSB of internal OSD) The meaning of this register depends of reg. 0xF6[1:0](default = 8íh0)		
	bit	0x F6 [1:0]	Reg. 0xF5 description
		00	Not used
	D3-0	01	Data MSB of font table RAM
	D2-0	10	Data MSB of code buffer
	D7-0	11	Data MSB of attribute buffer
0xF6	ORWCtrl (OSD Read/Write control) (default = 8íh0)		

	D7	burstmode	Internal OSD read/write mode select 0: single mode (default) 1: burst mode enable
	D6	clrpulse (Write Only)	Internal OSD clear buffer bit 0: normal (default) 1: clear code buffer with 0x59 clear attribute buffer with 0x00
	D5	rwmode	Indicates read/write mode, ì1î is read mode, ì0î is write mode.
	D4-3		Reserved
	D2	accosd	Internal OSD Read/Write enable 0: enable accessing internal OSD registers and buffer (default) 1: disable
	D1-0	accsel	Internal OSD accessing select 00: internal OSD control register (default) 01: internal OSD RAM font buffer 10: internal OSD display code buffer 11: internal OSD display attribute buffer

4.20 OSD internal control register:

4.20.1. OSD window horizontal start position

Address	**0x00**
Default	**30H**

7	6	5	4	3	2	1	0
OHSTA[7:0]							

OHSTA[7:0]: OSD window horizontal start position

Start position = 4*OHSTA +12(pixel)

4.20.2. OSD window vertical start position

Address	**0x01**
Default	**10H**

7	6	5	4	3	2	1	0
OVSTA[7:0]							

OVSTA[7:0]: OSD window vertical start position (default value is 0x10)

Start position = 4*OVSTA+1 (line)

4.20.3. OSD window horizontal width

Address	**0x02**
Default	**0FH**

7	6	5	4	3	2	1	0
Reserved	OWIDTH[6:0]						

OWIDTH[6:0]: OSD window horizontal width (default value is 0x0f)

Display width = OWIDTH+1(char)

4.20.4. OSD window vertical height

Address	**0x03**
Default	**07H**

7	6	5	4	3	2	1	0
Reserved	OWIDTH[6:0]						

OWIDTH[6:0]: OSD window vertical height

Display height = OHEIGHT+1(char)

4.20.5. Horizontal flip and OSD horizontal space start position

Address	**0x04**
Default	**00H**

7	6	5	4	3	2	1	0
MIRROR	OHSTP[6:0]						

MIRROR: Horizontal flip

OHSTP[6:0]: OSD horizontal space start position (unit: char)

4.20.6. Vertical flip and OSD vertical space start position

Address	**0x05**
Default	**00H**

7	6	5	4	3	2	1	0
MIRROR	OVSTP[6:0]						

MIRROR: Vertical flip

OVSTP[6:0]: OSD vertical space start position (unit: char)

4.20.7. OSD space width Space width

Address	**0x06**
Default	**00H**

7	6	5	4	3	2	1	0
OSPW[7:0]							

OSPW[7:0]:OSD space width Space width = 8*OSPW (pixel)

4.20.8. OSD space height Space height

Address	**0x07**
Default	**00H**

7	6	5	4	3	2	1	0
OSPH[7:0]							

OSPH[7:0]: OSD space height Space height = 8*OSPH (line)

4.20.9. OSD control register

Address	**0x08**
Default	**02H**

7	6	5	4	3	2	1	0
OVS[1:0]		OHS[1:0]		Reserved	SWDON	BDTYPE	MWDON

OVS[1:0]: Vertical scaling

00 = vertical enlarged x1 by repeated pixels

01 = vertical enlarged x2 by repeated pixels

10 = vertical enlarged x3 by repeated pixels

11 = vertical enlarged x4 by repeated pixels

OHS[1:0]: Horizontal scaling

00 = horizontal enlarged x1 by repeated pixels

01 = horizontal enlarged x2 by repeated pixels

10 = horizontal enlarged x3 by repeated pixels

11 = horizontal enlarged x4 by repeated pixels

SWDON: All OSD sub window display

0 = all OSD sub window display OFF

1 = all OSD sub window display ON

BDTYPE: Type of character border

0 = all direction font boundary

1 = bottom-right font boundary

MWDON: OSD main window display

0 = main window OFF

1 = main window ON

4.20.10. OSD misc. control

Address	**0x09**
Default	**80H**

7	6	5	4	3	2	1	0
MATTRSEL	FILLEN	SHAON	BDWIDTH	MBGSEL	Reserved		

MATTRSEL: Main OSD window color attribute select

0 = from main window attribute registers

1 = from attribute buffer

FILLEN: Enable signal, filled the display area with the color defined by Reg0x11

0 = disable

1 = enable

SHAON: OSD window shadow control

0 = off

1 = on

BDWIDTH: Border width control if font scale up

0 = one pixel width for all scale

1 = scale with OVS and OHS

MBGSEL: Main OSD window background color enable

0 = background off

1 = background on

4.20.11. Code buffer offset select and Code buffer offset value

Address	**0x0A**
Default	**00H**

7	6	5	4	3	2	1	0
OFSEL	OFFSET[6:0]						

OFSEL:Code buffer offset select

0 = code buffer offset is equal to OWIDTH

1 = code buffer offset is equal to OFFSET

OFFSET[6:0]: Code buffer offset value

4.20.12. OSD code base

Address	**0x0B**
Default	**00H**

7	6	5	4	3	2	1	0
CODEBASE[7:0]							

CODEBASE[7:0]: OSD code base

4.20.13. OSD border color index

Address	**0x0C**
Default	**00H**

7	6	5	4	3	2	1	0
BDSEL[7:0]							

BDSEL[7:0]: OSD border color index

4.20.14. Main OSD window foreground color index

Address	**0x0D**
Default	**00H**

7	6	5	4	3	2	1	0
MFGSEL[7:0]							

MFGSEL[7:0]: Main OSD window foreground color index

4.20.15. Main OSD window background color index

Address	**0x0E**
Default	**00H**

7	6	5	4	3	2	1	0
MBGSEL[7:0]							

MBGSEL[7:0]: Main OSD window background color index

4.20.16. OSD window shadow size

Address	**0x0F**
Default	**00H**

7	6	5	4	3	2	1	0
SHAWIDTH[3:0]				SHAHEIGHT[3:0]			

SHAWIDTH[3:0]: OSD window shadow width

SHAHEIGHT[3:0]: OSD window shadow height

4.20.17. Main OSD window shadow color index

Address	**0x10**
Default	**00H**

7	6	5	4	3	2	1	0
SHASEL[7:0]							

SHASEL[7:0]: Main OSD window shadow color index

4.20.18. The color index filled the display area

Address	**0x11**
Default	**00H**

7	6	5	4	3	2	1	0
FCSEL[7:0]							

FCSEL[7:0]: The color index filled the display area

4.20.19. Field control

Address	**0x12**
Default	**00H**

7	6	5	4	3	2	1	0
ODDFIELD[3:0]				EVENFIELD[3:0]			

ODDFIELD[3:0]: The line number in odd field

EVENFIELD[3:0]: The line number in even field

4.20.20. Set blink period if blink enable

Address	**0x13**
Default	**20H**

7	6	5	4	3	2	1	0
BLINKPRD[7:0]							

BLINKPRD[7:0]:Set blink period if blink enable

4.20.21. Sub window control register

Address	**0x14**
Default	**00H**

7	6	5	4	3	2	1	0
WEN7	WEN6	WEN5	WEN4	WEN3	WEN2	WEN1	WEN0

WEN7: OSD sub window7 enable(0 = disable 1 = enable)
WEN6: OSD sub window6 enable(0 = disable 1 = enable)
WEN5: OSD sub window5 enable(0 = disable 1 = enable)
WEN4: OSD sub window4 enable(0 = disable 1 = enable)
WEN3: OSD sub window3 enable(0 = disable 1 = enable)
WEN2: OSD sub window2 enable(0 = disable 1 = enable)
WEN1: OSD sub window1 enable(0 = disable 1 = enable)
WEN0: OSD sub window0 enable(0 = disable 1 = enable)

4.20.22. OSD sub window background enable

Address	**0x15**
Default	**00H**

7	6	5	4	3	2	1	0
WBGEN7	WBGEN6	WBGEN5	WBGEN4	WBGEN3	WBGEN2	WBGEN1	WBGEN0

WBGEN7: OSD sub window7 background enable(0 = disable 1 = enable)
WBGEN6: OSD sub window6 background enable(0 = disable 1 = enable)
WBGEN5: OSD sub window5 background enable(0 = disable 1 = enable)
WBGEN4: OSD sub window4 background enable(0 = disable 1 = enable)
WBGEN3: OSD sub window3 background enable(0 = disable 1 = enable)
WBGEN2: OSD sub window2 background enable(0 = disable 1 = enable)
WBGEN1: OSD sub window1 background enable(0 = disable 1 = enable)
WBGEN0: OSD sub window0 background enable(0 = disable 1 = enable)

4.20.23. OSD sub window attribute select

Address	**0x16**
Default	**00H**

7	6	5	4	3	2	1	0
WATTRSEL[7:0]							

WATTRSEL7: OSD sub window7 attribute select

0 = from sub window7 attribute registers 1 = from attribute buffer

WATTRSEL6: OSD sub window6 attribute select

0 = from sub window6 attribute registers 1 = from attribute buffer

WATTRSEL5: OSD sub window5 attribute select

0 = from sub window5 attribute registers 1 = from attribute buffer

WATTRSEL4: OSD sub window4 attribute select

0 = from sub window4 attribute registers 1 = from attribute buffer

WATTRSEL3: OSD sub window3 attribute select

0 = from sub window3 attribute registers 1 = from attribute buffer

WATTRSEL2: OSD sub window2 attribute select

0 = from sub window2 attribute registers 1 = from attribute buffer

WATTRSEL1: OSD sub window1 attribute select

0 = from sub window1 attribute registers 1 = from attribute buffer

WATTRSEL0: OSD sub window0 attribute select

0 = from sub window0 attribute registers 1 = from attribute buffer

4.20.24. OSD sub window0 horizontal start position

Address	**0x20**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA0[7:0]							

SHSTA0[7:0]: OSD sub window0 horizontal start position

Sub window0 start position = 4 * SHSTA0 +12(pixel)

4.20.25. OSD sub window0 horizontal width

Address	**0x21**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH0[6:0]						

SWIDTH0[6:0]: OSD sub window0 horizontal width

Sub window0 display width = SWIDTH0+1(char)

4.20.26. OSD sub window0 vertical start position

Address	**0x22**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA0[7:0]							

SVSTA0[7:0]: OSD sub window0 vertical start position

Sub window0 start position = 4*SVSTA0+1 (line)

4.20.27. OSD sub window0 vertical height

Address	**0x23**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT0[6:0]						

SHEIGHT0[6:0]: OSD sub window0 vertical height

Sub window0 display height = SHEIGHT0+1(char)

4.20.28. OSD sub window0 foreground color index

Address	**0x24**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL0[7:0]							

WFGSEL0[7:0]: OSD sub window0 foreground color index

4.20.29. OSD sub window0 background color index

Address	**0x25**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL0[7:0]							

WBGSEL0[7:0]: OSD sub window0 background color index

4.20.30. OSD sub window0 shadow color index

Address	**0x26**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL0[7:0]							

WSHASEL0[7:0]: OSD sub window0 shadow color index

4.20.31. The char code of the first character in OSD sub window0

Address	**0x27**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE0[6:0]						

WBASE0[6:0]: The char code of the first character in OSD sub window0

4.20.32. OSD sub window1 horizontal start position

Address	**0x28**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA1[7:0]							

SHSTA1[7:0]: OSD sub window1 horizontal start position

Sub window1 start position = 4 * SHSTA1 +12(pixel)

4.20.33. OSD sub window1 horizontal width

Address	**0x29**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH1[6:0]						

SWIDTH1[6:0]: OSD sub window1 horizontal width

Sub window1 display width = SWIDTH1 + 1(char)

4.20.34. OSD sub window1 vertical start position

Address	**0x2A**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA1[7:0]							

SVSTA1[7:0]: OSD sub window1 vertical start position

Sub window1 start position = 4*SVSTA1+1 (line)

4.20.35. OSD sub window1 vertical height

Address	**0x2B**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT1[6:0]						

SHEIGHT1[6:0]: OSD sub window1 vertical height

Sub window1 display height = SHEIGHT1+ 1(char)

4.20.36. OSD sub window1 foreground color index

Address	**0x2C**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL1[7:0]							

WFGSEL1[7:0]: OSD sub window1 foreground color index

4.20.37. OSD sub window1 background color index

Address	**0x2D**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL1[7:0]							

WBGSEL1[7:0]: OSD sub window1 background color index

4.20.38. OSD sub window1 shadow color index

Address	**0x2E**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL1[7:0]							

WSHASEL1[7:0]: OSD sub window1 shadow color index

4.20.39. The char code of the first character in OSD sub window1

Address	**0x2F**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE1[6:0]						

WBASE1[6:0]: The char code of the first character in OSD sub window1

4.20.40. OSD sub window2 horizontal start position

Address	**0x30**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA2[7:0]							

SHSTA2[7:0]: OSD sub window2 horizontal start position

Sub window2 start position = 4 * SHSTA2 +12(pixel)

4.20.41. OSD sub window2 horizontal width

Address	**0x31**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH2[6:0]						

SWIDTH2[6:0]: OSD sub window2 horizontal width

Sub window2 display width = SWIDTH2 + 1(char)

4.20.42. OSD sub window2 vertical start position

Address	**0x32**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA2[7:0]							

SVSTA2[7:0]: OSD sub window2 vertical start position

Sub window2 start position = 4*SVSTA2 + 1 (line)

4.20.43. OSD sub window2 vertical height

Address	**0x33**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT2[6:0]						

SHEIGHT2[6:0]: OSD sub window2 vertical height

Sub window2 display height = SHEIGHT2 + 1(char)

4.20.44. OSD sub window2 foreground color index

Address	**0x34**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL2[7:0]							

WFGSEL2[7:0]: OSD sub window2 foreground color index

4.20.45. OSD sub window2 background color index

Address	**0x35**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL2[7:0]							

WBGSEL2[7:0]: OSD sub window2 background color index

4.20.46. OSD sub window2 shadow color index

Address	**0x36**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL2[7:0]							

WSHASEL2[7:0]: OSD sub window2 shadow color index

4.20.47. The char code of the first character in OSD sub window2

Address	**0x37**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE2[6:0]						

WBASE2[6:0]: The char code of the first character in OSD sub window2

4.20.48. OSD sub window3 horizontal start position

Address	**0x38**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA3[7:0]							

SHSTA3[7:0]: OSD sub window3 horizontal start position

Sub window3 start position = 4 * SHSTA3 +12(pixel)

4.20.49. OSD sub window3 horizontal width

Address	**0x39**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH3[6:0]						

SWIDTH3[6:0]: OSD sub window3 horizontal width

Sub window3 display width = SWIDTH3+1(char)

4.20.50. OSD sub window3 vertical start position

Address	**0x3A**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA3[7:0]							

SVSTA3[7:0]: OSD sub window3 vertical start position

Sub window3 start position = 4*SVSTA3+1 (line)

4.20.51. OSD sub window3 vertical height

Address	**0x3B**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT3[6:0]						

SHEIGHT3[6:0]: OSD sub window3 vertical height

Sub window3 display height = SHEIGHT3 + 1(char)

4.20.52. OSD sub window3 foreground color index

Address	**0x3C**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL3[7:0]							

WFGSEL3[7:0]: OSD sub window3 foreground color index

4.20.53. OSD sub window3 background color index

Address	**0x3D**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL3[7:0]							

WBGSEL3[7:0]: OSD sub window3 background color index

4.20.54. OSD sub window3 shadow color index

Address	**0x3E**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL3[7:0]							

WSHASEL3[7:0]: OSD sub window3 shadow color index

4.20.55. The char code of the first character in OSD sub window3

Address	**0x3F**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE3[6:0]						

WBASE3[6:0]: The char code of the first character in OSD sub window3

4.20.56. OSD sub window4 horizontal start position

Address	**0x40**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA4[7:0]							

SHSTA4[7:0]: OSD sub window4 horizontal start position

Sub window4 start position = 4 * SHSTA4 +12(pixel)

4.20.57. OSD sub window4 horizontal width

Address	**0x41**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH4[6:0]						

SWIDTH4[6:0]: OSD sub window4 horizontal width

Sub window4 display width = SWIDTH4 + 1(char)

4.20.58. OSD sub window4 vertical start position

Address	**0x42**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA4[7:0]							

SVSTA4[7:0]: OSD sub window4 vertical start position

Sub window4 start position = 4*SVSTA4 + 1 (line)

4.20.59. OSD sub window4 vertical height

Address	**0x43**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT4[6:0]						

SHEIGHT4[6:0]: OSD sub window4 vertical height

Sub window4 display height = SHEIGHT4 + 1(char)

4.20.60. OSD sub window4 foreground color index

Address	**0x44**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL4[7:0]							

WFGSEL4[7:0]: OSD sub window4 foreground color index

4.20.61. OSD sub window4 background color index

Address	**0x45**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL4[7:0]							

WBGSEL4[7:0]: OSD sub window4 background color index

4.20.62. OSD sub window4 shadow color index

Address	**0x46**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL4[7:0]							

WSHASEL0[7:0]: OSD sub window4 shadow color index

4.20.63. The char code of the first character in OSD sub window4

Address	**0x47**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE4[6:0]						

WBASE4[6:0]: The char code of the first character in OSD sub window4

4.20.64. OSD sub window5 horizontal start position

Address	**0x48**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA0[7:0]							

SHSTA5[7:0]: OSD sub window5 horizontal start position

Sub window5 start position = 4 * SHSTA5 +12(pixel)

4.20.65. OSD sub window5 horizontal width

Address	**0x49**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH5[6:0]						

SWIDTH5[6:0]: OSD sub window5 horizontal width

Sub window5 display width = SWIDTH5+1(char)

4.20.66. OSD sub window5 vertical start position

Address	**0x4A**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA5[7:0]							

SVSTA5[7:0]: OSD sub window5 vertical start position

Sub window5 start position = 4*SVSTA5 + 1 (line)

4.20.67. OSD sub window5 vertical height

Address	**0x4B**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT5[6:0]						

SHEIGHT5[6:0]: OSD sub window5 vertical height

Sub window5 display height = SHEIGHT5 + 1(char)

4.20.68. OSD sub window5 foreground color index

Address	**0x4C**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL5[7:0]							

WFGSEL5[7:0]: OSD sub window5 foreground color index

4.20.69. OSD sub window5 background color index

Address	**0x4D**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL5[7:0]							

WBGSEL5[7:0]: OSD sub window5 background color index

4.20.70. OSD sub window5 shadow color index

Address	**0x4E**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL5[7:0]							

WSHASEL5[7:0]: OSD sub window5 shadow color index

4.20.71. The char code of the first character in OSD sub window5

Address	**0x4F**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE5[6:0]						

WBASE5[6:0]: The char code of the first character in OSD sub window5

4.20.72. OSD sub window6 horizontal start position

Address	**0x50**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA6[7:0]							

SHSTA6[7:0]: OSD sub window6 horizontal start position

Sub window6 start position = 4 * SHSTA6 +12(pixel)

4.20.73. OSD sub window6 horizontal width

Address	**0x51**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH6[6:0]						

SWIDTH6[6:0]: OSD sub window6 horizontal width

Sub window6 display width = SWIDTH6 + 1(char)

4.20.74. OSD sub window6 vertical start position

Address	**0x52**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA6[7:0]							

SVSTA6[7:0]: OSD sub window6 vertical start position

Sub window6 start position = 4*SVSTA6 + 1 (line)

4.20.75. OSD sub window6 vertical height

Address	**0x53**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT6[6:0]						

SHEIGHT6[6:0]: OSD sub window6 vertical height

Sub window6 display height = SHEIGHT6 + 1(char)

4.20.76. OSD sub window6 foreground color index

Address	**0x54**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL6[7:0]							

WFGSEL6[7:0]: OSD sub window6 foreground color index

4.20.77. OSD sub window6 background color index

Address	**0x55**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL6[7:0]							

WBGSEL6[7:0]: OSD sub window6 background color index

4.20.78. OSD sub window6 shadow color index

Address	**0x56**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL6[7:0]							

WSHASEL6[7:0]: OSD sub window6 shadow color index

4.20.79. The char code of the first character in OSD sub window6

Address	**0x57**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE6[6:0]						

WBASE6[6:0]: The char code of the first character in OSD sub window6

4.20.80. OSD sub window7 horizontal start position

Address	**0x58**
Default	**00H**

7	6	5	4	3	2	1	0
SHSTA7[7:0]							

SHSTA7[7:0]: OSD sub window7 horizontal start position

Sub window7 start position = 4 * SHSTA7 +12(pixel)

4.20.81. OSD sub window7 horizontal width

Address	**0x59**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SWIDTH7[6:0]						

SWIDTH7[6:0]: OSD sub window7 horizontal width

Sub window7 display width = SWIDTH7+1(char)

4.20.82. OSD sub window7 vertical start position

Address	**0x5A**
Default	**00H**

7	6	5	4	3	2	1	0
SVSTA7[7:0]							

SVSTA7[7:0]: OSD sub window7 vertical start position

Sub window7 start position = 4*SVSTA7 + 1 (line)

4.20.83. OSD sub window7 vertical height

Address	**0x5B**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	SHEIGHT7[6:0]						

SHEIGHT7[6:0]: OSD sub window7 vertical height

Sub window7 display height = SHEIGHT7 + 1(char)

4.20.84. OSD sub window7 foreground color index

Address	**0x5C**
Default	**00H**

7	6	5	4	3	2	1	0
WFGSEL7[7:0]							

WFGSEL7[7:0]: OSD sub window7 foreground color index

4.20.85. OSD sub window7 background color index

Address	**0x5D**
Default	**00H**

7	6	5	4	3	2	1	0
WBGSEL7[7:0]							

WBGSEL7[7:0]: OSD sub window7 background color index

4.20.86. OSD sub window7 shadow color index

Address	**0x5E**
Default	**00H**

7	6	5	4	3	2	1	0
WSHASEL7[7:0]							

WSHASEL7[7:0]: OSD sub window7 shadow color index

4.20.87. The char code of the first character in OSD sub window7

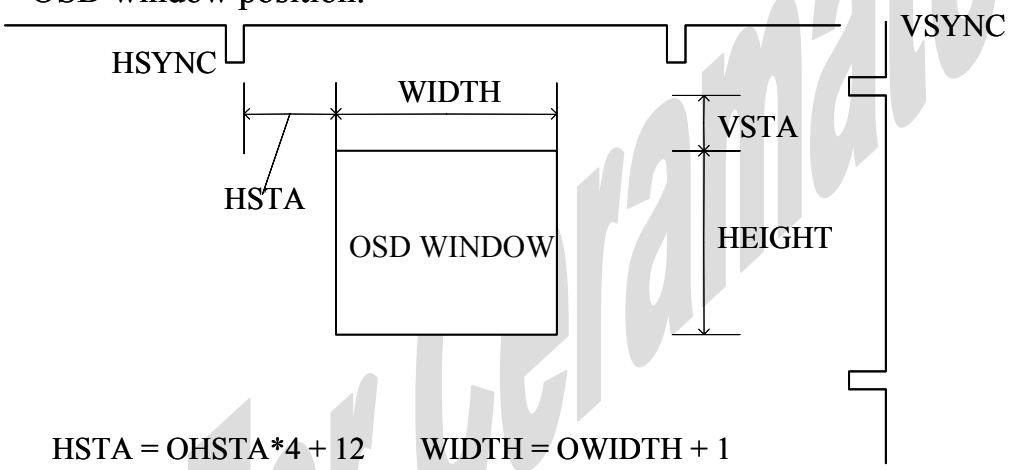
Address	**0x5F**
Default	**00H**

7	6	5	4	3	2	1	0
Reserved	WBASE7[6:0]						

WBASE7[6:0]: The char code of the first character in OSD sub window7

OSD window and register define

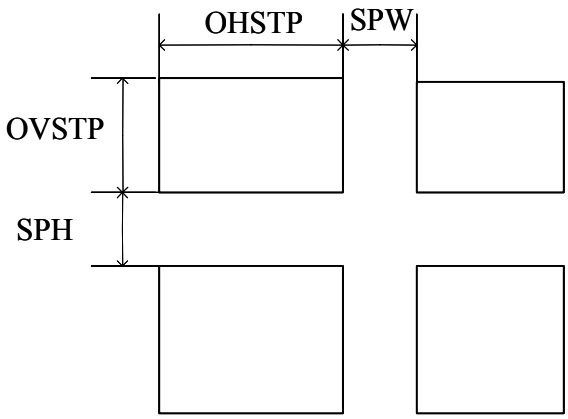
OSD window position:



HSTA = OHSTA*4 + 12 WIDTH = OWIDTH + 1

VSTA = OVSTA*4 + 1 HEIGHT = OHEIGHT + 1

SPACE:



SPW = OSPW * 8

SPH = OSPH *8

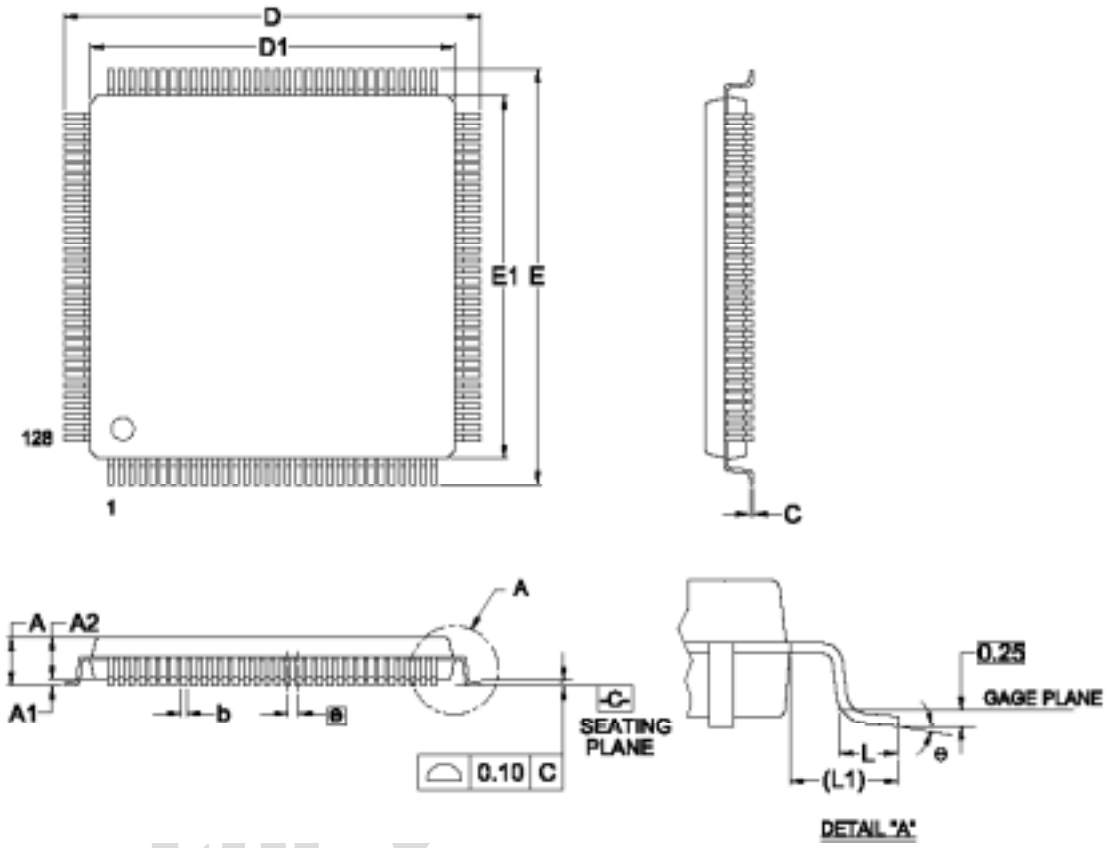
5 AC/DC Characteristics

TBD

6 Ordering information

Part Number	Package	Pb Free	Operating Temperature
MX88V462UC	LQFP128	No	0°C ~ 70°C
MX88V462UCG	LQFP128	Yes	0°C ~ 70°C

7 Package outline:



SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	E1	e	L	L1	θ
mm	Min.	—	0.05	1.35	0.13	0.09	15.80	13.90	15.80	13.90		0.45	0.85	0
	Nom.	—	0.10	1.40	0.16	0.13	16.00	14.00	16.00	14.00	0.40	0.60	1.00	3.5
	Max.	1.60	0.15	1.45	0.23	0.20	16.20	14.10	16.20	14.10		0.75	1.15	7
inch	Min.	—	0.002	0.053	0.005	0.004	0.622	0.547	0.622	0.547		0.018	0.033	0
	Nom.	—	0.004	0.055	0.006	0.005	0.630	0.551	0.630	0.551	0.016	0.024	0.039	3.5
	Max.	0.063	0.006	0.057	0.009	0.006	0.638	0.555	0.638	0.555		0.030	0.045	7

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TEST REPORT

REPORT NO.KA/2005/62386
DATE: 2005/06/29

THE FOLLOWING MERCHANDISE WAS(WERE) SUBMITTED AND IDENTIFIED BY THE CLIENT AS :

CLIENT	: ADVANCED SEMICONDUCTOR ENGINEERING INC..
PRODUCT	: IC COMPONENT PACKAGE.
PACKAGE TYPE	: TQFP/LQFP(GREEN/RoHS COMPLIANCE).
BOM	: COMPOUND:HITACHI 9200THF.
EPOXY	: ABLESTIK 2288A.
LEAD FRAME	: OLIN C7025(Cu).
LEAD FINISH	: MATT Sn.
INK	: INK/LASER.
GOLD WIRE	: 99.99%Au.
DIE	: SILICONE.
SAMPLE	: AS ATTACHED PHOTO.
TESTING DATE	: 2005/06/22 TO 2005/06/29.
SAMPLE RECEIVED	: 2005/06/22.

==========

WE HAVE TESTED THE SAMPLE(S) SUBMITTED AS REQUESTED AND THE FOLLOWING RESULTS WERE OBTAINED.

TEST ITEM(S)	UNIT	METHOD	EQUIPMENT	MDL	RESULT
CADMIUM	ppm	USEPA 3051 OR AQUA REGIA	ICP-AES	2	<MDL
CHROMIUM VI	ppm	USEPA 3060A / USEPA 7196A	UV/VIS	2	<MDL
MERCURY	ppm	USEPA 3051 OR AQUA REGIA	ICP-AES	2	<MDL
LEAD	ppm	USEPA 3051 OR AQUA REGIA	ICP-AES	2	<MDL

SGS TAIWAN LTD SGS TAIWAN

Katherine Ho / Supervisor
Sign for and on behalf of
SGS Taiwan Limited

SGS

TEST REPORT

REPORT NO.KA/2005/62386
DATE: 2005/06/29

TEST ITEM(S)	UNIT	METHOD	EQUIPMENT	MDL	RESULT
PBBs(Polybrominated biphenyls)	---	---	---	---	---
Bromobiphenyl	ppm	With reference to USEPA3540C or USEPA3550C. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	HPLC/DAD/MS OR GC/MS	5	<MDL
Dibromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Tribromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Tetrabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Pentabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Hexabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Heptabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Octabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Nonabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Decabromobiphenyl	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL

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TEST REPORT

REPORT NO.KA/2005/62386
DATE: 2005/06/29

TEST ITEM(S)	UNIT	METHOD	EQUIPMENT	MDL	RESULT
PBDEs(Polybrominated biphenyl ethers)	---	---	---	---	---
Monobromobiphenyl ether	ppm	With reference to USEPA3540C or USEPA3550C. Analysis was performed by HPLC/DAD, LC/MS or GC/MS. (prohibited by 2002/95/EC (RoHS), 83/264/EEC, and 76/769/EEC)	HPLC/DAD/MS OR GC/MS	5	<MDL
Dibromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Tribromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Tetrabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Pentabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Hexabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Heptabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Octabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Nonabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL
Decabromobiphenyl ether	ppm		HPLC/DAD/MS OR GC/MS	5	<MDL

NOTE:(1)AQUA REGIA IS SPECIFICALLY FOR METAL MATERIALS.
(2)n.d. = not detected.
(3)MDL=method detective limit

<END>

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