PS113

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3-Channel Secondary Monitoring IC

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PS113

3-Channel Secondary Monitoring IC

General Description

PS113 is specially designed for switching power supply system. Three important functions of PS113 are the following: over-voltage protection, short circuit protection and power good signal generating.

OVP (Over Voltage Protection) monitors 5V, 12V and 3.3V to protect our power supply and PC, when one of these supply voltages exceeds their normal operation voltage.

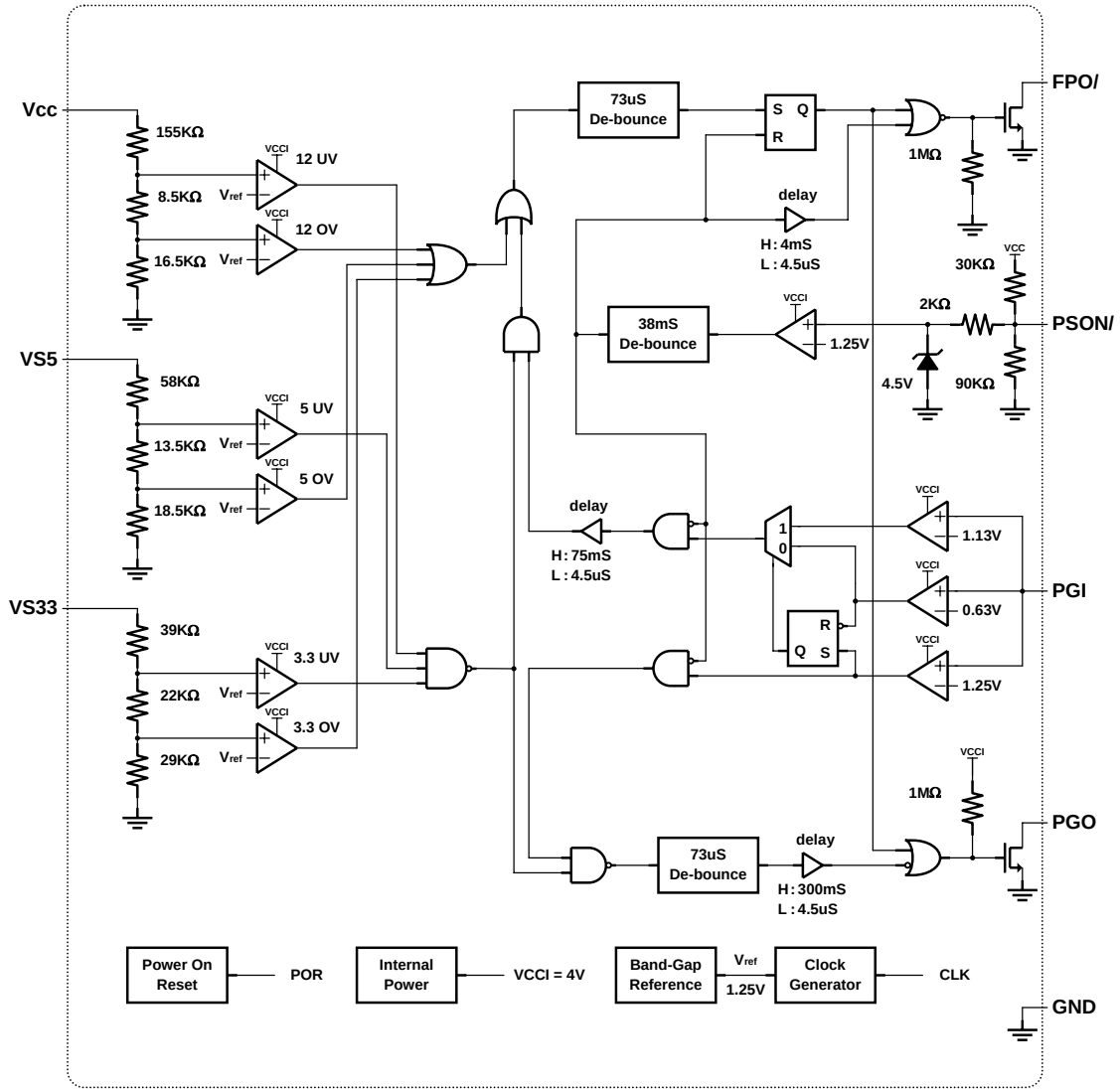
Short circuit protection is done by UVP (Under Voltage Protection). When power supply is in short circuit, the supply voltages will be much smaller than their normal operation voltages .We can use UVP to monitor our power supply whether it is in the dangerous power load.

Power good signal generating notifies personal computer when power supply is ready or power supply is going to shutdown, therefore it can provide a reliable power supply environment.

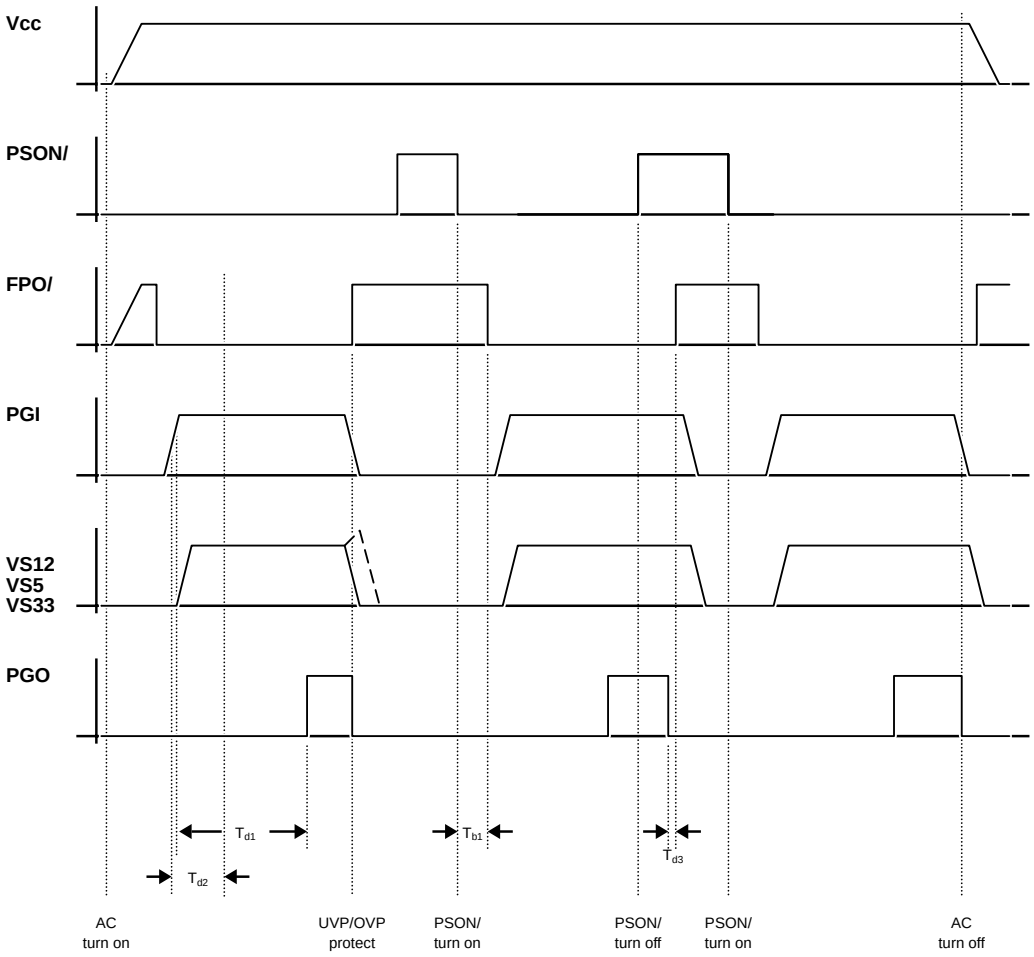
Features

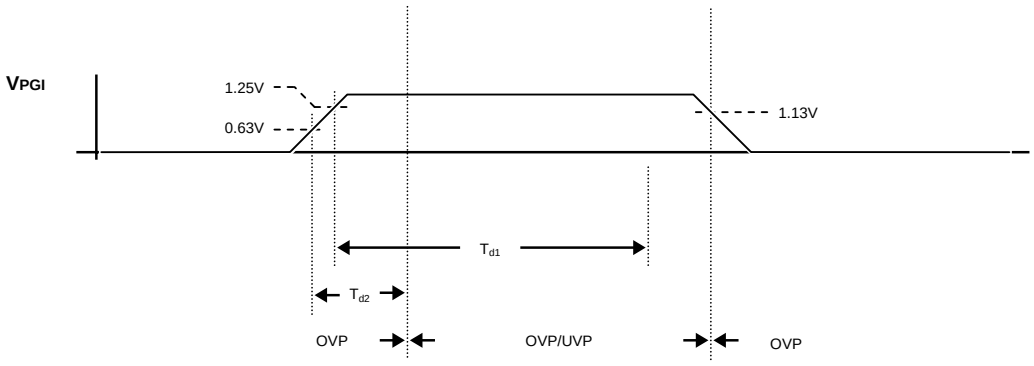
- Over voltage protection and lock out
- Short circuit protection and lock out
- Fault protection output with open drain output stage
- Open drain power good output signal for power good input
- Built-in 300ms power good delay
- 75ms delay for short-circuit turn on protection
- 38ms PSON control de-bounce
- 73us de-bounce for noise immunity
- Wide power supply range from 4V to 16V
- Pin to pin compatible with TPS3510
- Special care for AC power off
- Additional 12V UVP protection

Block Diagram



Timing Chart





Pin Descriptions

Pin No	PIN NAME	Descriptions
1	PGI	Power good input signal pin
2	GND	Ground
3	FPO	Inverted fault protection output ,open drain output stage
4	PSON	ON/OFF control input pin
5	VS33	3.3V over/under voltage protection input pin
6	VS5	5.0V over/under voltage protection input pin
7	VCC	Supply voltage/12V over voltage protection input pin
8	PGO	Power good output signal pin , open drain output stage

Absolute Maximum Ratings

Parameter			Rating			Unit
Storage Temperature	(T_{stg})		-40	to	+125	°C
Operating Temperature	(T_{opr})		-30	to	+90	°C
Supply Voltage	(V_{CC})	VCC	-0.5	to	+16.0	V
Input Voltage Range	(V_I)	VS33,VS5	-0.5	to	Vcc+0.5	V
		PGI	-0.5	to	+16.0	V
		PSON/	-0.5	to	Vcc+0.5	V
Output Voltage Range	(V_O)	FPO/	-0.5	to	+16.0	V
		PGO	-0.5	to	Vcc+0.5	V
ESD Susceptibility*	(V_{ESD})			>	2500	V

*** Human Body Model (HBM).**

Electrical characteristics, Vcc=12V, T_a = 25°C. (unless otherwise specified)

Power Supply Section

Parameter	Conditions	MIN	TYP	MAX	Unit
Supply Voltage		3.8	5.0	16.0	V
Supply Current	$V_{PSON/}$ = 5V		2	3	mA
Power On Reset Threshold Voltage (V_{POR})			3.6		V
Power On Reset Hysteresis (V_{HYST})				±0.6	V

Electrical Characteristics (Continued)

Over-Voltage Section

Parameter		Conditions	MIN	TYP	MAX	Unit
Over-Voltage Threshold	VS33		3.7	3.9	4.1	V
	VS5		5.7	6.1	6.5	V
	VS12		13.2	13.8	14.4	V

Under-Voltage Section

Parameter		Conditions	MIN	TYP	MAX	Unit
Under-Voltage Threshold	VS33		2.0	2.2	2.4	V
	VS5		3.3	3.5	3.7	V
	VS12		8.5	9.0	9.5	V

PSON/, Analog Input

Parameter	Conditions	MIN	TYP	MAX	Unit
Threshold Voltage		0.9	1.2	1.5	V
Hysteresis (V_{HYST})			±50		mV

PGI, Analog Input

Parameter	Conditions	MIN	TYP	MAX	Unit
Threshold Voltage for start T_{d1}		1.16	1.25	1.33	V
Threshold Voltage for start T_{d2}		0.60	0.63	0.75	V
Threshold Voltage for mask OC,UV		1.05	1.13	1.21	V
Hysteresis (V_{HYST})*			±50		mV

*** All of the comparator for PGI input in block diagram.**

PGO, Open Drain Digital Output

Parameter	Conditions	MIN	TYP	MAX	Unit
Leakage Current (I_{LKG})	V_{PGO}=5V			5	uA
Low Level Output Voltage (V_{OL})	I_{SINK}=10mA			0.4	V

Electrical Characteristics (Continued)

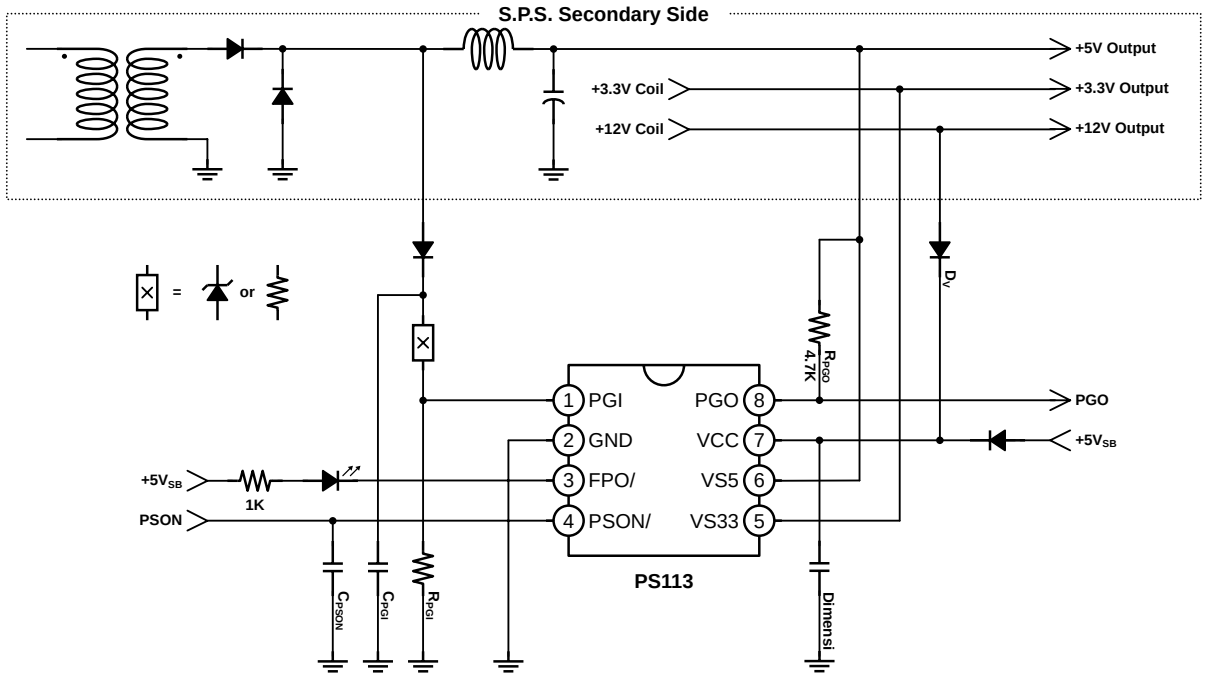
FPO/, Open Drain Digital Output

Parameter	Conditions	MIN	TYP	MAX	Unit
Leakage Current (I_{LKG})	$V_{FPO/}$=5V			5	uA
Low Level Output Voltage (V_{OL})	I_{SINK}=10mA			0.3	V
	I_{SINK}=30mA			0.7	V

Switching Characteristics, Vcc=5V, T_a = 25˚C.

Parameter	Conditions	MIN	TYP	MAX	Unit
PGI to PGO Delay Time (T_{d1})		200	300	480	mS
Short Circuit Delay Time (T_{d2})		49	75	100	mS
PGO to FPO/ Delay Time (T_{d3})		2	4	6	mS
PSON/ De-bounce Time (T_{b1})		24	38	61	mS
Noise De-glitch Time (T_{b2})		47	73	120	uS

Application

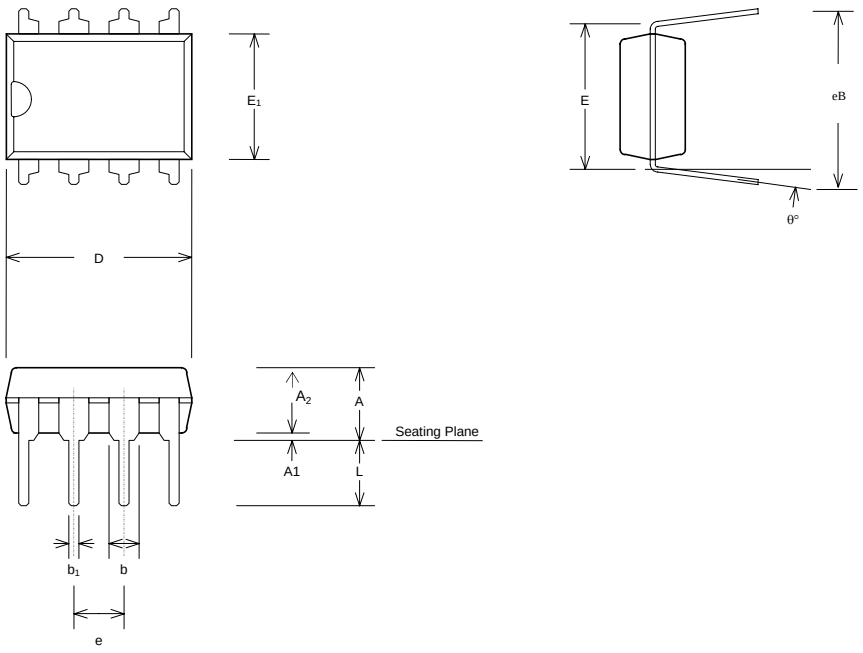


Note1: Zener diode or resistor or both of them can be used in component X.

Note2: The bypass capacitor C_{by} suggests to be 0.1uF~ 10uF and layout nearby pin VCC.

Package Specification

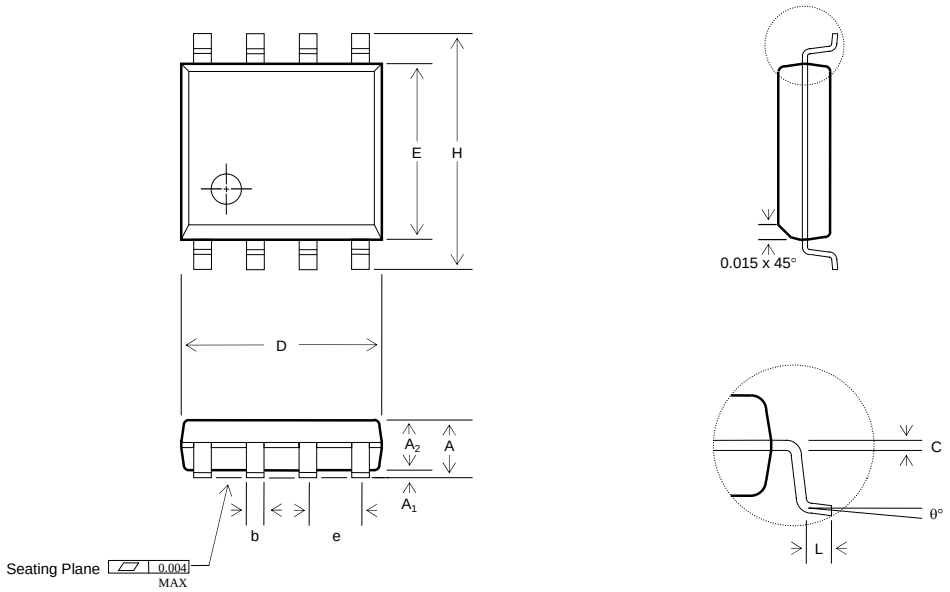
(8-pin DIP)



Symbol	Dimension in mm			Dimension in inch			NOTE
	Min	Normal	Max	Min	Normal	Max	
A			5.334			0.210	
A_1	0.381			0.015			
A_2	3.175	3.302	3.429	0.125	0.13	0.135	
b		1.524			0.06		
b_1		0.457			0.018		
D	9.017	9.271	10.160	0.355	0.365	0.4	
E	7.366	7.620	7.874	0.290	0.300	0.310	
E_1	6.223	6.376	6.528	0.245	0.251	0.257	
e		2.540			0.100		
eB	8.509	9.017	9.525	0.335	0.355	0.375	
L	2.921	3.302	3.810	0.115	0.13	0.150	
θ°	0	7	15	0	7	15	

Package Specification (Continued)

(8-pin SOP)



Symbol	Dimension in mm			Dimension in inch			NOTE
	Min	Normal	Max	Min	Normal	Max	
A	1.346		1.753	0.053		0.069	
A_1	0.102		0.254	0.004		0.010	
A_2	1.346		1.499	0.053		0.059	
b		0.406			0.016		
c		0.203			0.008		
D	4.801		4.978	0.189		0.196	
E	3.810		3.988	0.150		0.157	
e		1.270			0.050		
H	5.791		6.198	0.228		0.244	
L	0.406		1.270	0.016		0.050	
θ°	0		8	0		8	

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