

IRFZ46NS

IRFZ46NL

HEXFET® Power MOSFET

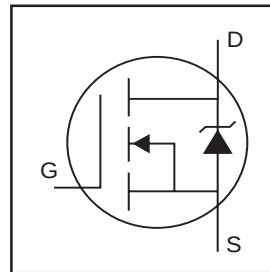
- Advanced Process Technology
- Surface Mount (IRFZ46NS)
- Low-profile through-hole (IRFZ46NL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

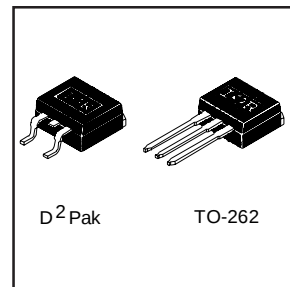
The through-hole version (IRFZ46NL) is available for low-profile applications.



$$V_{DS} = 55V$$

$$R_{DS(on)} = 0.0165\Omega$$

$$I_D = 53A^{\circ}$$



D²Pak

TO-262

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^{\circ}$	53 $^{\circ}$	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^{\circ}$	37	
I_{DM}	Pulsed Drain Current $^{\circ} \text{ } ^{\circ}$	180	
$P_D @ T_A = 25^{\circ}C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^{\circ}C$	Power Dissipation	107	W
	Linear Derating Factor	0.71	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current $^{\circ}$	28	A
E_{AR}	Repetitive Avalanche Energy $^{\circ}$	11	mJ
dv/dt	Peak Diode Recovery dv/dt $^{\circ} \text{ } ^{\circ}$	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	$^{\circ}C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.4	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	

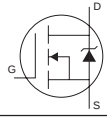
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C , $I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	.0165	Ω	$V_{GS} = 10V, I_D = 28A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	19	—	—	S	$V_{DS} = 25V, I_D = 28A$ ④ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	72	nC	$I_D = 28A$
Q_{gs}	Gate-to-Source Charge	—	—	11		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	26		$V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	76	—		$I_D = 28A$
$t_{d(off)}$	Turn-Off Delay Time	—	52	—		$R_G = 12\Omega$
t_f	Fall Time	—	57	—		$R_D = 0.98\Omega$, See Fig. 10 ④ ⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1696	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	407	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	110	—		$f = 1.0MHz$, See Fig. 5 ⑤
E_{AS}	Single Pulse Avalanche Energy ②	—	583 ⑥	152 ⑦		$I_{AS} = 28A, L = 389mH$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	53	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 28A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	67	101	ns	$T_J = 25^\circ\text{C}, I_F = 28A$
Q_{rr}	Reverse Recovery Charge	—	208	312	nC	$di/dt = 100A/\mu s$ ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 389\mu H$
 $R_G = 25\Omega$, $I_{AS} = 28A$. (See Figure 12)
- ③ $I_{SD} \leq 28A$, $di/dt \leq 220A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRFZ46N data and test conditions.
- ⑥ This is a typical value at device destruction and represents operation outside rated limits.
- ⑦ This is a calculated value limited to $T_J = 175^\circ\text{C}$.
- ⑧ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 39A.

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

IRFZ46NS/IRFZ46NL

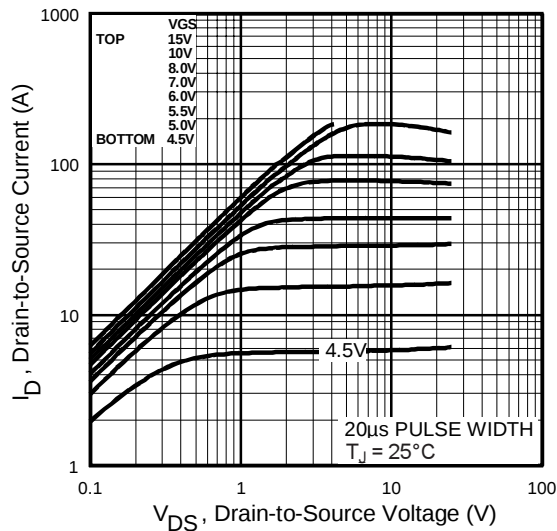


Fig 1. Typical Output Characteristics

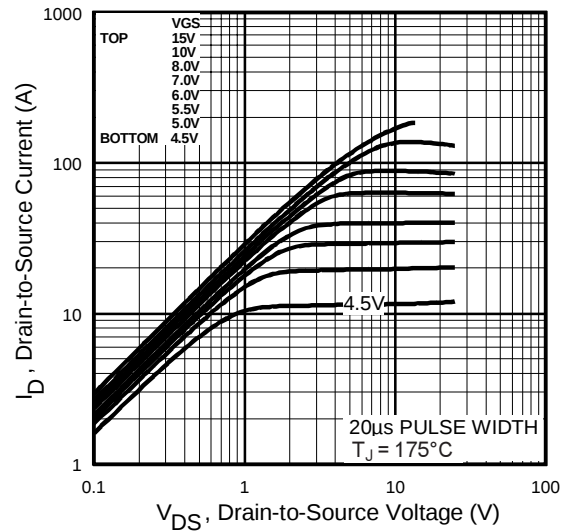


Fig 2. Typical Output Characteristics

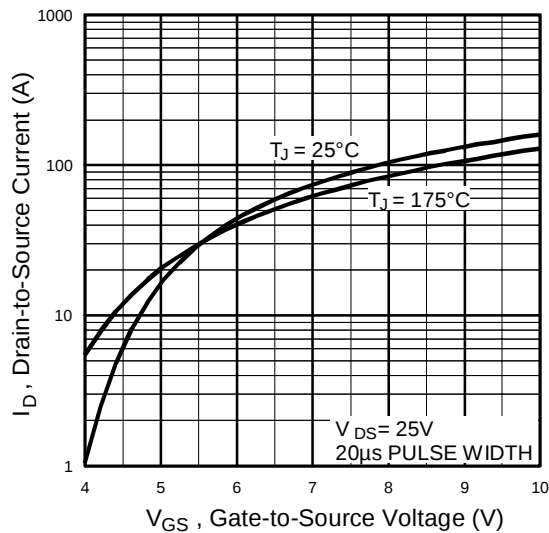


Fig 3. Typical Transfer Characteristics

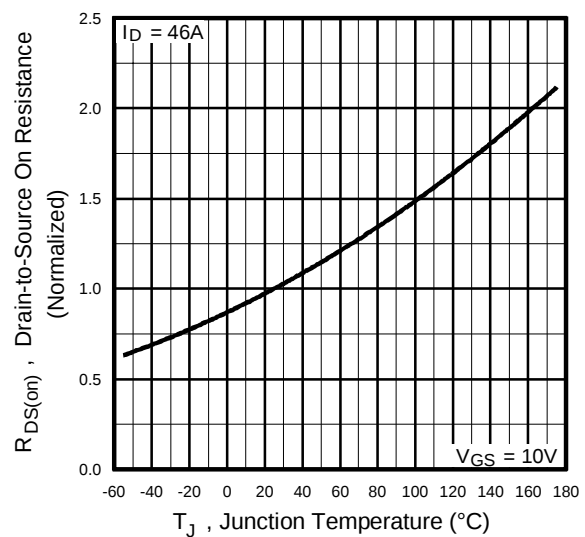


Fig 4. Normalized On-Resistance Vs. Temperature

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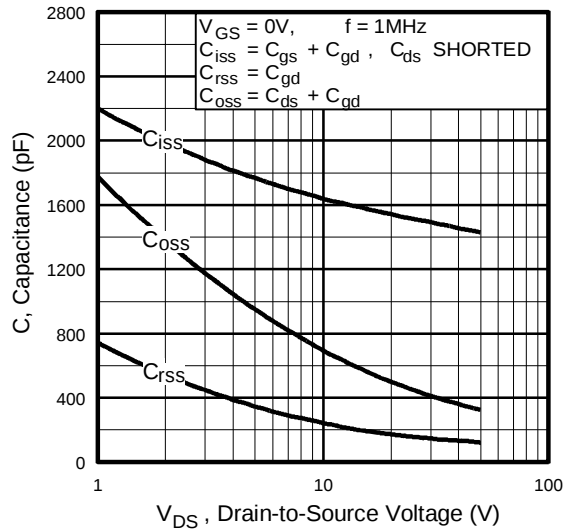


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

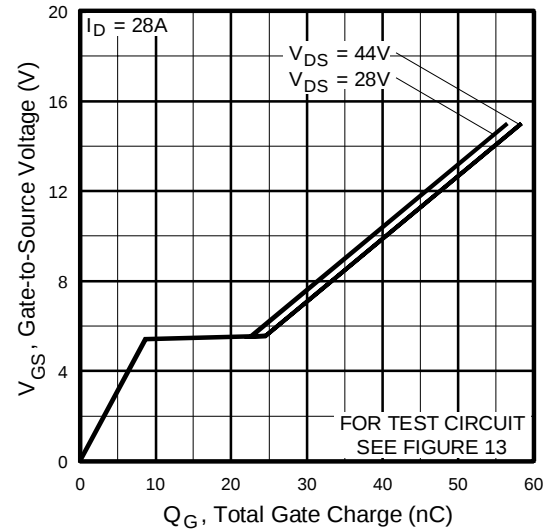


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

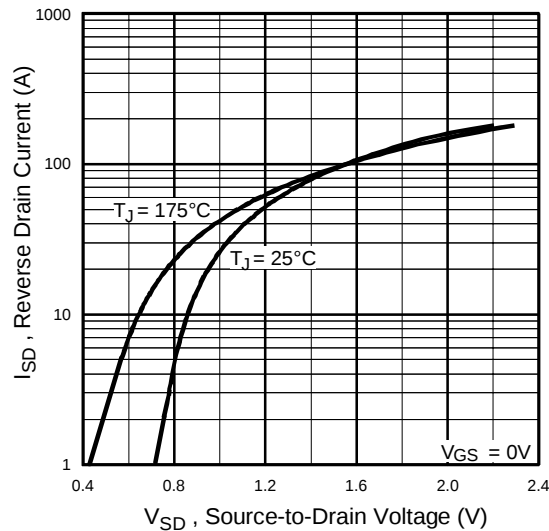


Fig 7. Typical Source-Drain Diode Forward Voltage

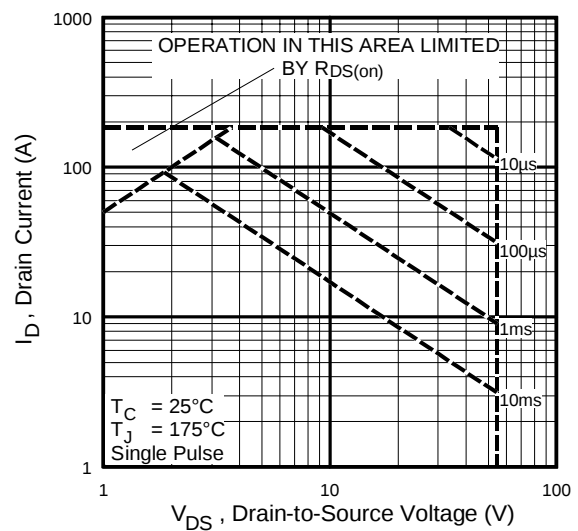


Fig 8. Maximum Safe Operating Area

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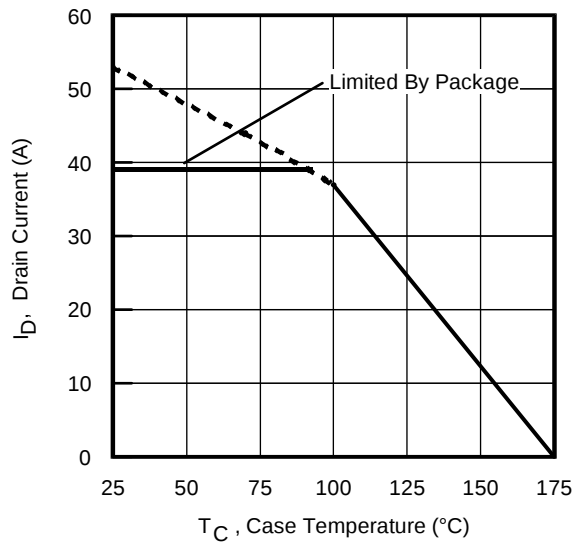


Fig 9. Maximum Drain Current Vs. Case Temperature

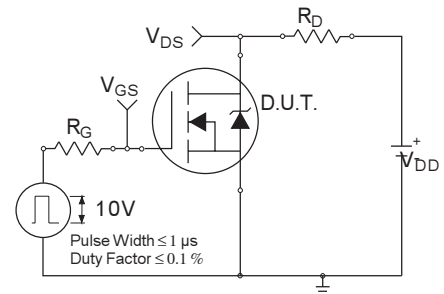


Fig 10a. Switching Time Test Circuit

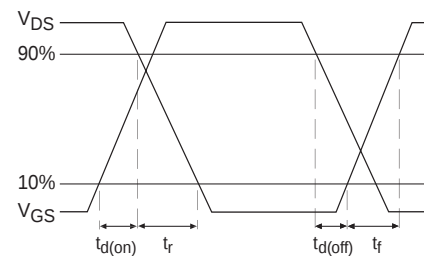


Fig 10b. Switching Time Waveforms

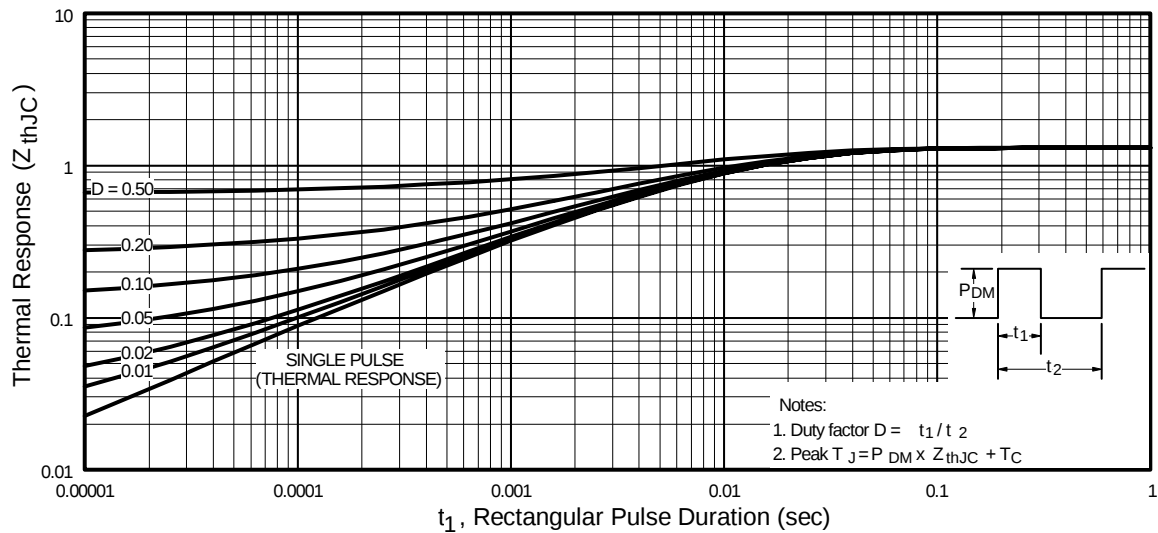


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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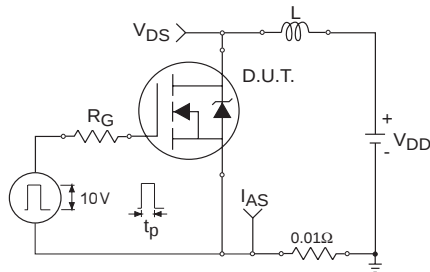


Fig 12a. Unclamped Inductive Test Circuit

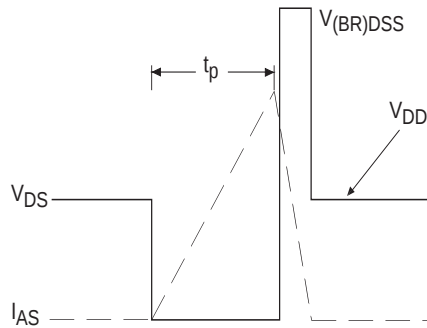


Fig 12b. Unclamped Inductive Waveforms

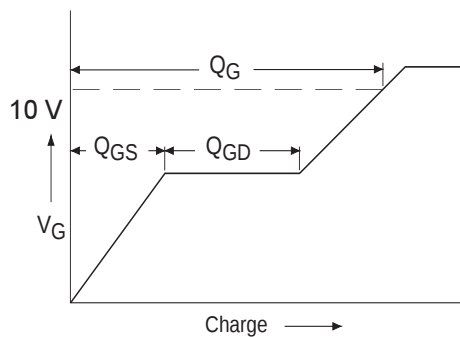


Fig 13a. Basic Gate Charge Waveform

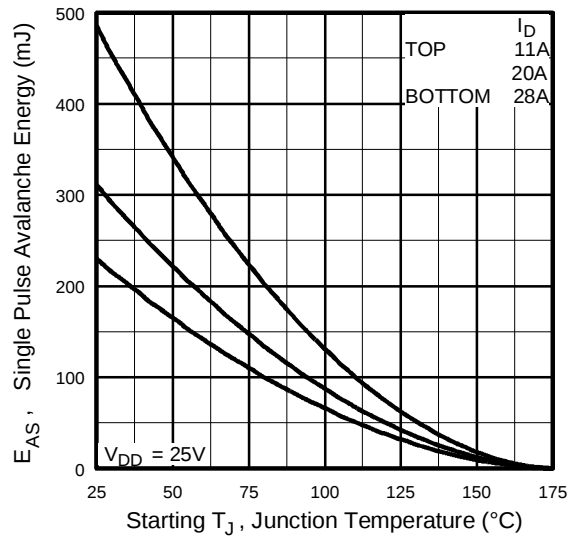


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

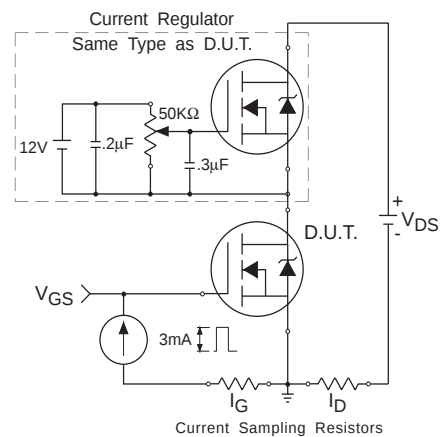
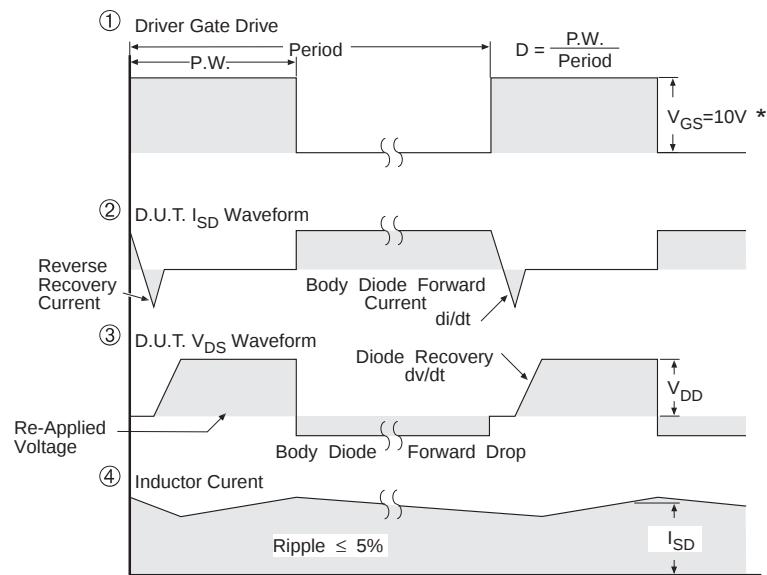
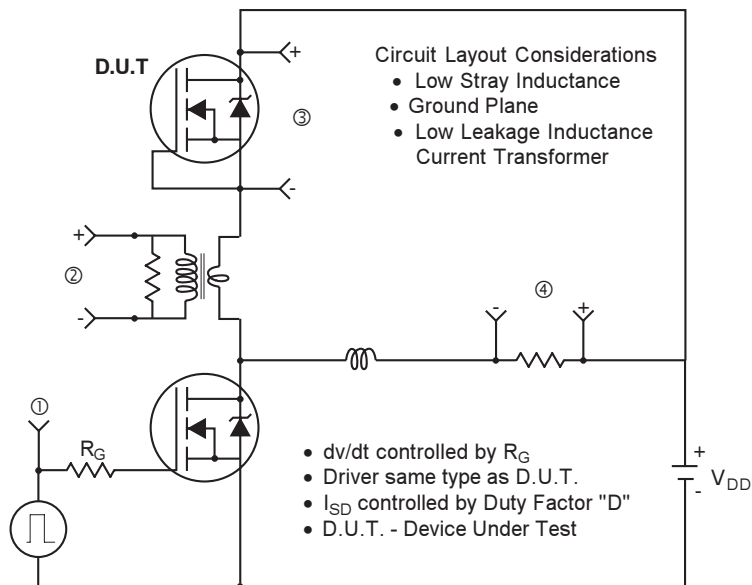


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



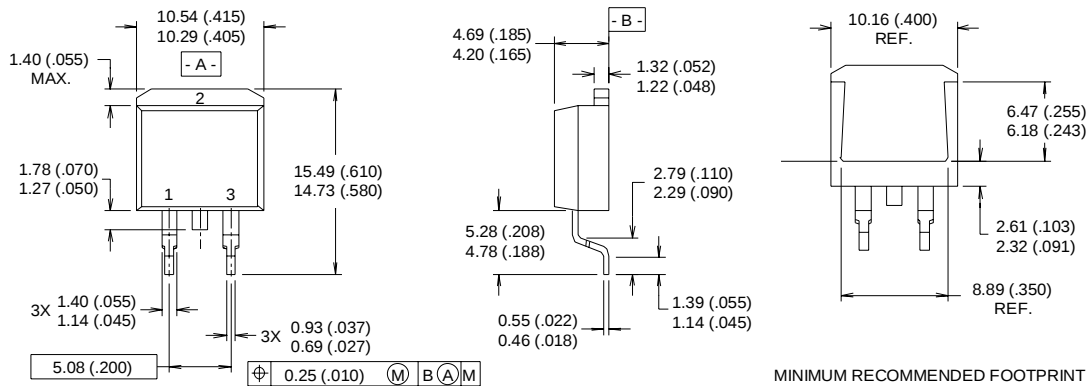
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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D²Pak Package Outline



NOTES:

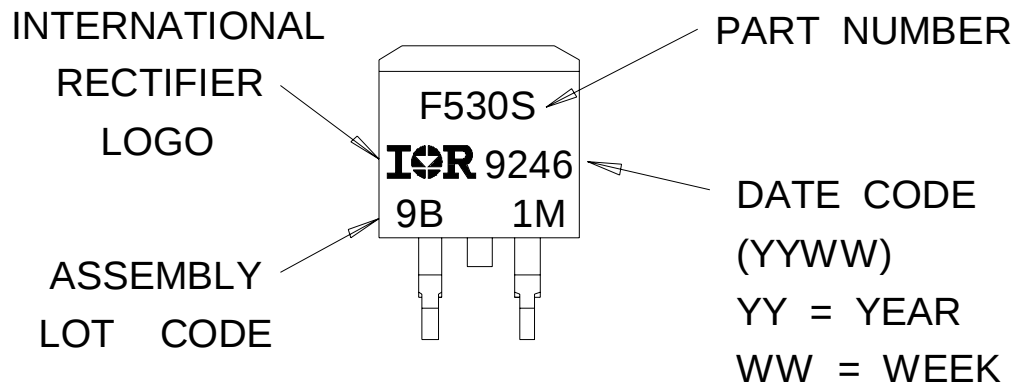
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

Part Marking Information

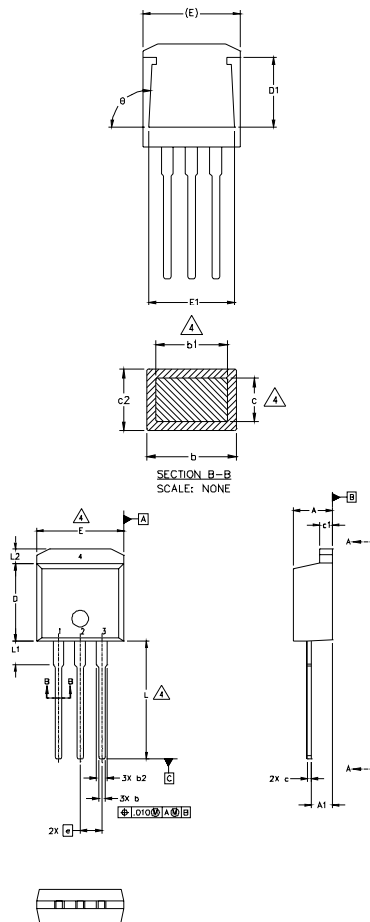
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TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT

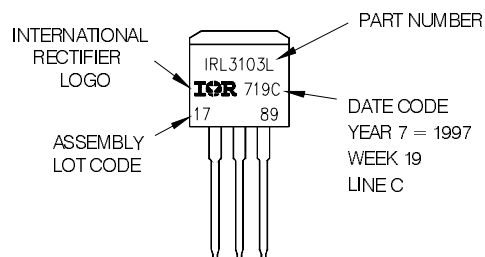
- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

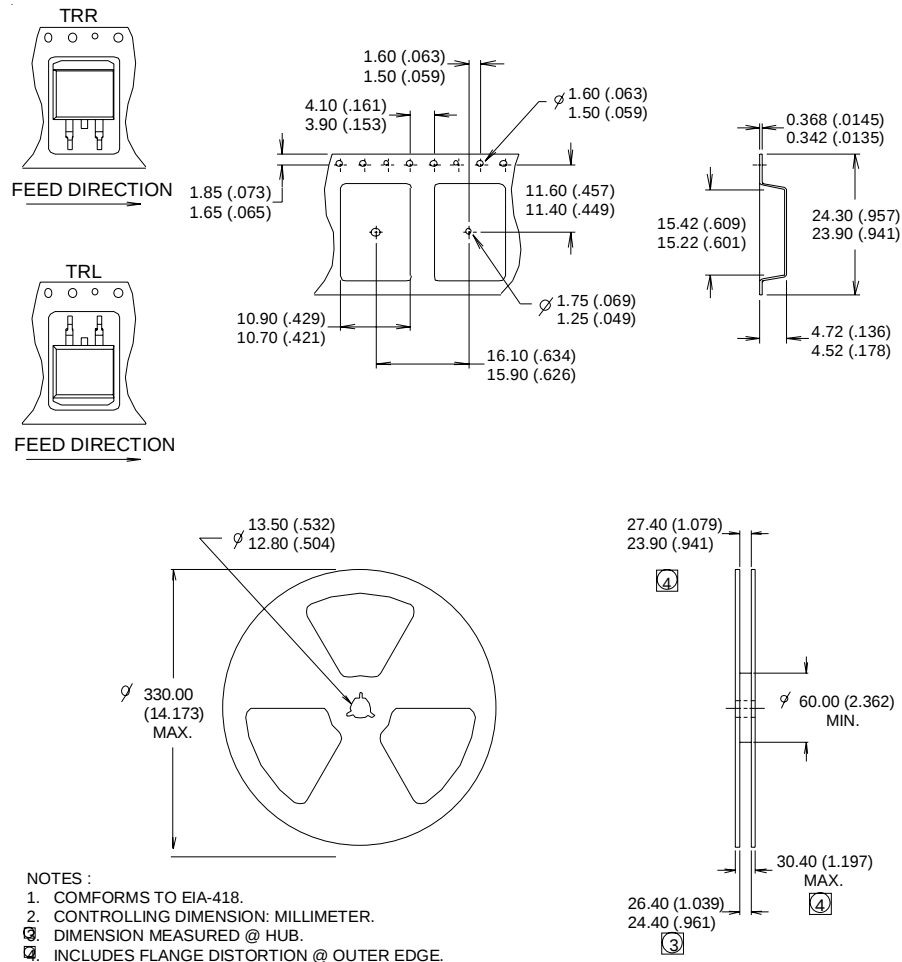


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Tape & Reel Information

D²Pak



Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

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