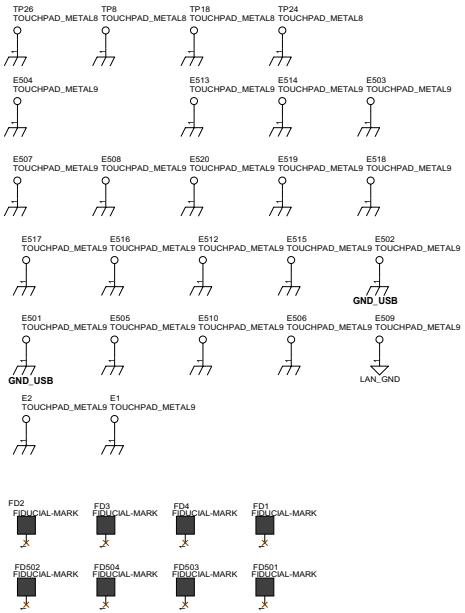
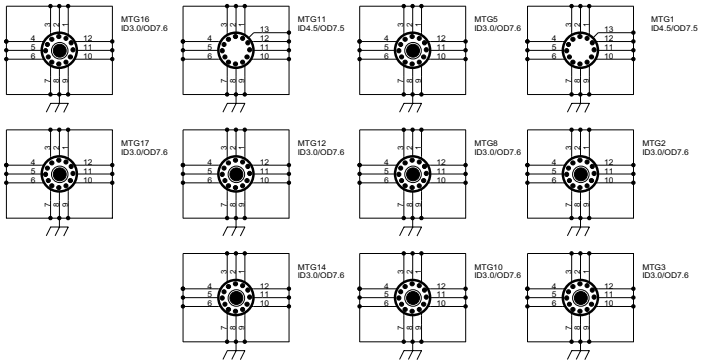
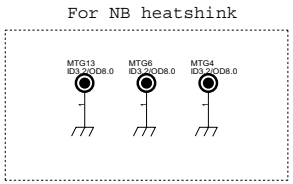
MODEL : 8640

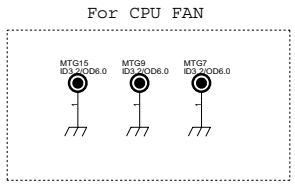
Revision 02

Contexts









POWER STATES

SIGNAL \ STATE	VOTAGE	FULL ON	STR	STD	MEC-OFF	REMARK
-SUSB	-	HIGH	LOW	LOW	LOW	
-SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
+VCC_RTC	+3.3V	O	O	O	O	
+VCC_CORE	+1.75V	O	O	X	X	
+1.8VS	+1.8V	O	X	X	X	
+1.8V	+1.8V	O	O	X	X	
+1.8VA	+1.8V	O	O	O	O	
+2.5V_DDR	+2.5V	O	O	X	X	
+3VS	+3.3V	O	X	X	X	
+3V	+3.3V	O	O	X	X	
+3VA	+3.3V	O	O	O	0	
+5VS	+5V	O	X	X	X	
+5V	+5V	O	O	X	X	
+5VA	+5V	O	O	0	0	
+12VS	+12V	O	X	X	X	
+12V	+12V	O	O	X	X	

IDSEL

IDSEL	CHIP
AD20	TI1410
AD21	MINI PCI
AD22	MINI PCI

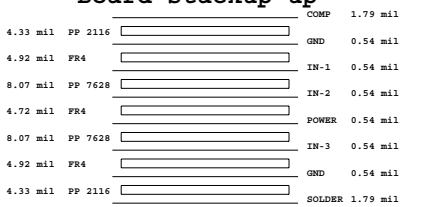
BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	TI1410
-REQ2/-GNT2	MINI PCI
-REQ3/-GNT3	MINI PCI

PCIINT

PCIINT	CHIP
INTA#	SIS 650 / MAP17
INTB#	PCMCIA (TI1410)
INTC#	MINI PCI
INTD#	MINI PCI

Board Stackup-up



DRAW	DESIGN	CHECK	ISSUED

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Title: COVER SHEET & SCREW HOLD

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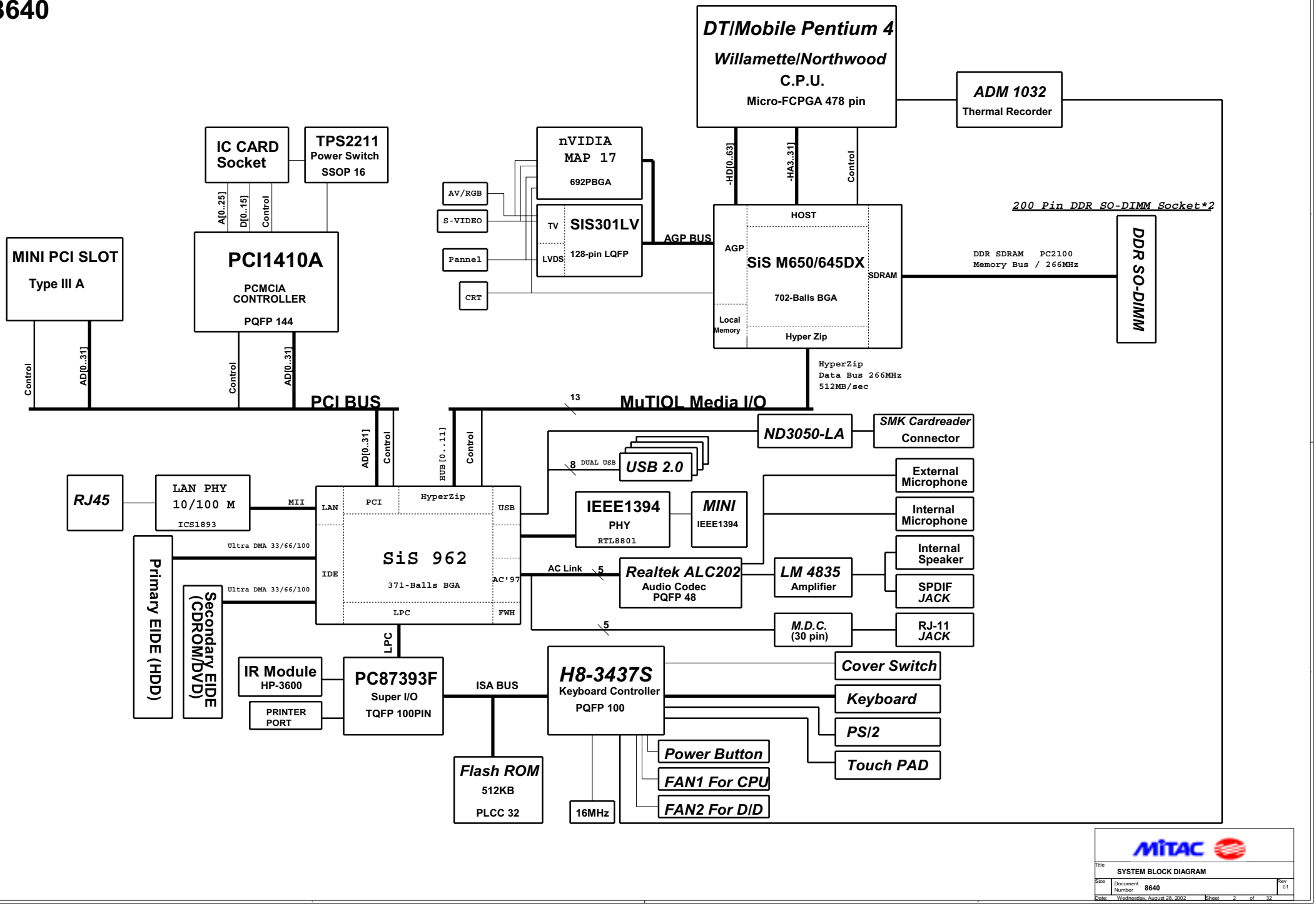
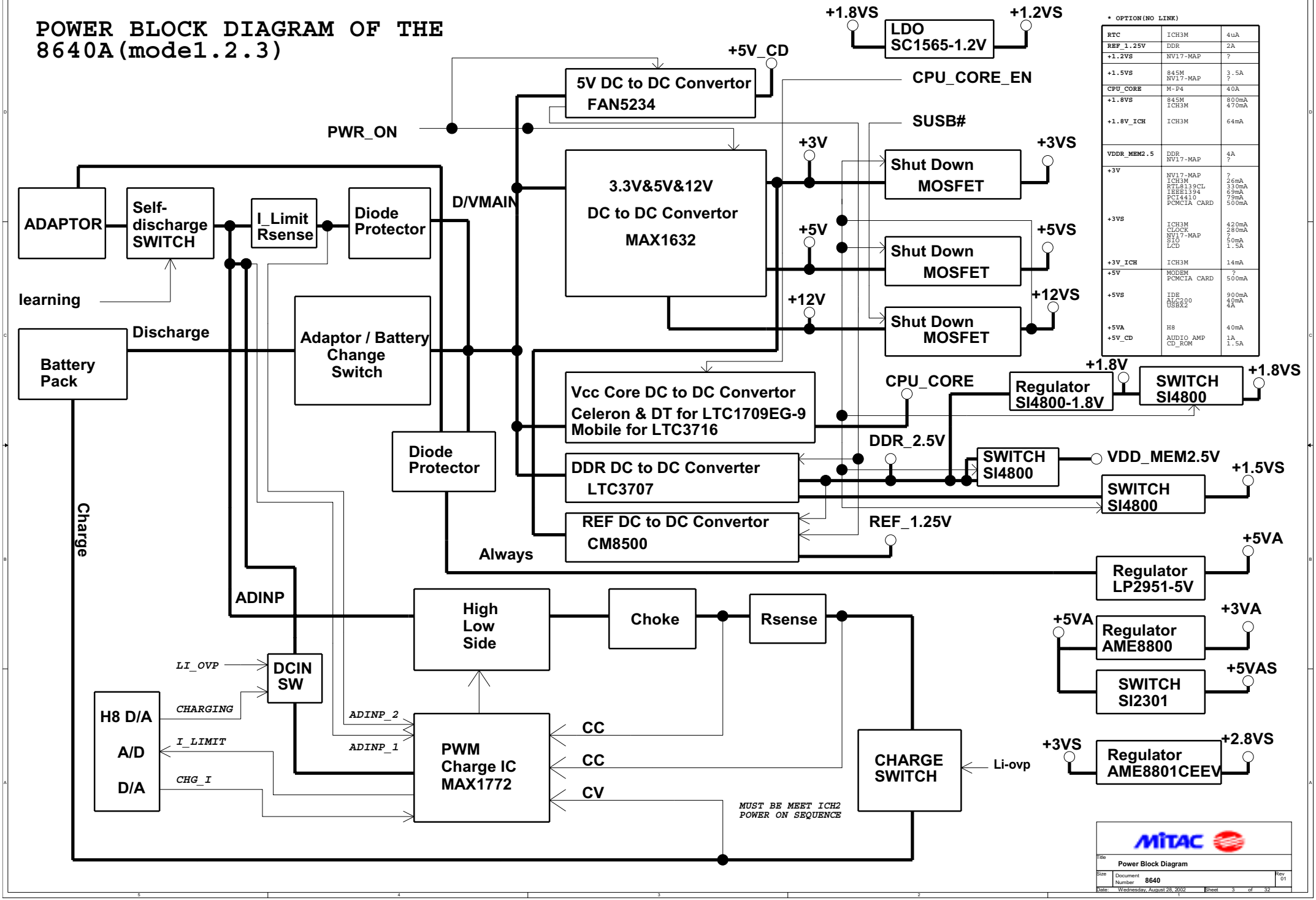


POWER BLOCK DIAGRAM OF THE 8640A(mode1.2.3)



* OPTION(NO LINK)

RTC	ICH3M	4uA
REF_1.25V	DDR	2A
+1.2VS	NV17-MAP	?
+1.5VS	845M NV17-MAP	3.5A ?
CPU_CORE	M-P4	40A
+1.8VS	845M ICH3M	800mA 470mA
+1.8V_ICH	ICH3M	64mA
VDDR_MEM2.5	DDR NV17-MAP	4A ?
+3V	NV17-MAP ICH3M RTL8139CL IEEE1394 PCI4410 PCMCIA CARD	? 26mA 330mA 69mA 79mA 500mA
+3VS	ICH3M CLOCK NV17-MAP SIO LCD	420mA 280mA ? 50mA 1.5A
+3V_ICH	ICH3M	14mA
+5V	MODEM PCMCIA CARD	? 500mA
+5VS	IDE ALC200 USBX2	900mA 40mA 4A
+5VA	H8	40mA
+5V_CD	AUDIO AMP CD_ROM	1A 1.5A

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Title: Power Block Diagram

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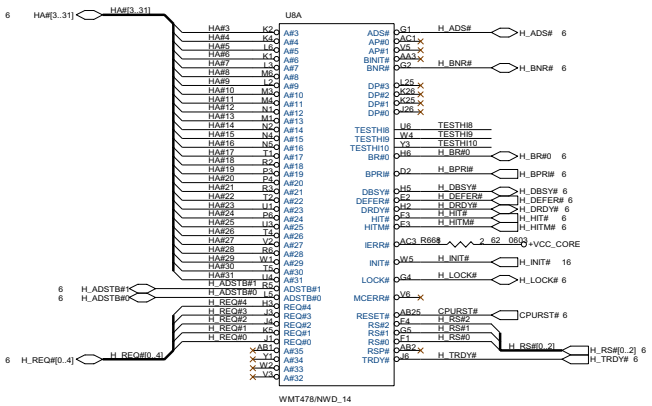
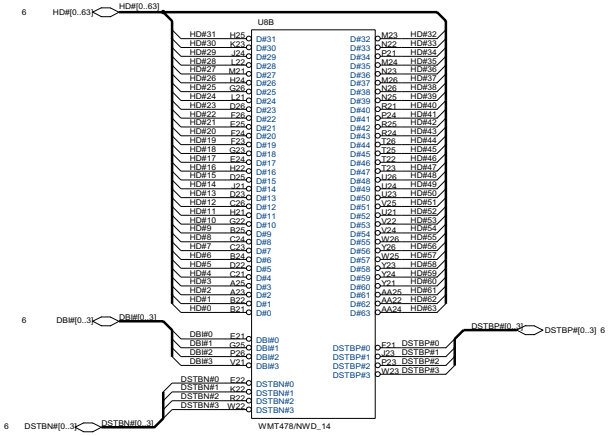
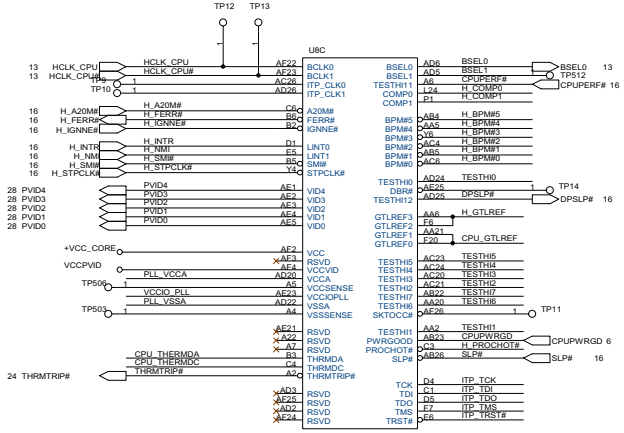
CPU (1/2)



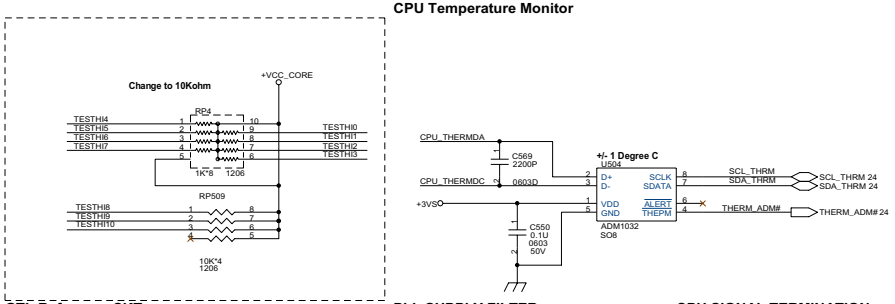




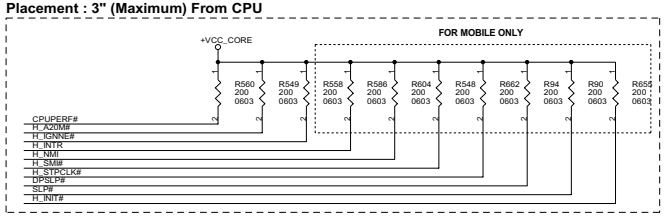
FSB SELECTION

BSEL1	BSEL0	FUNCTION
0	0	100MHz
0	1	133MHz
1	0	RESERVED
1	1	RESERVED

CPU Temperature Monitor

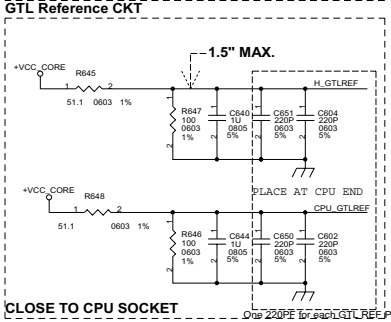


Placement : 3" (Maximum) From CPU

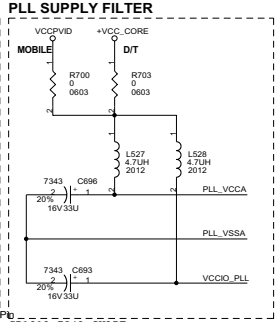


R94 must be pull hi at DT.Because the signal was input of TEST_HI12.

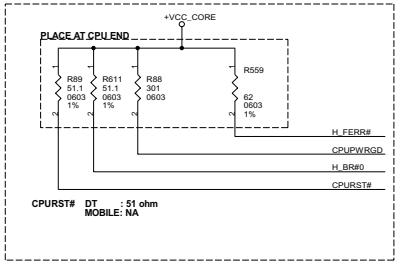
GTL Reference CKT



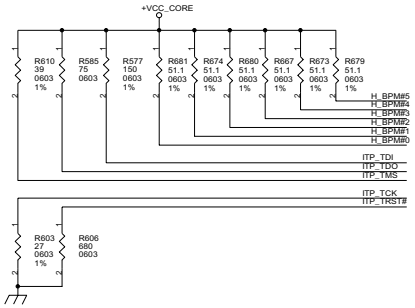
PLL SUPPLY FILTER



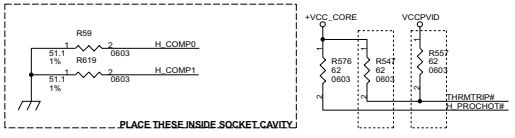
CPU SIGNAL TERMINATION



PLACE CLOSE TO CPU SOCKET



PRECISION FSB COMPENSATION RESISTORS



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Title: PENTIUM4 (1/2)

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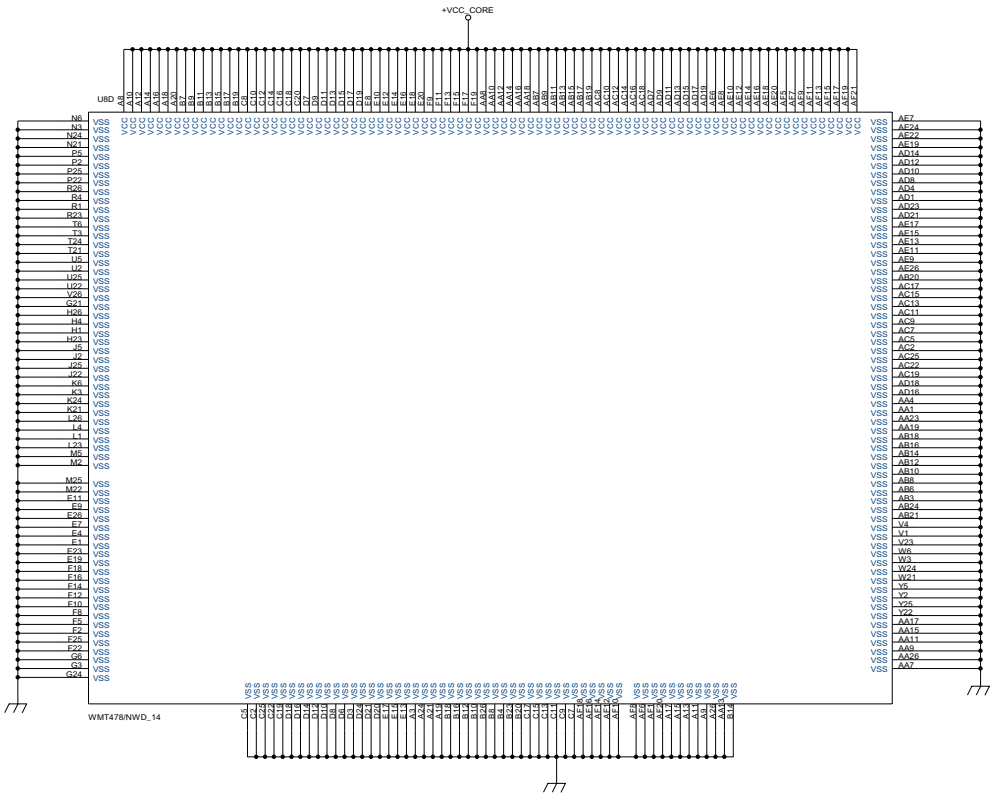
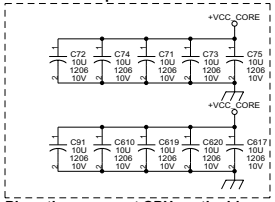
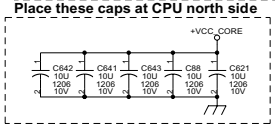
CPU (2/2)



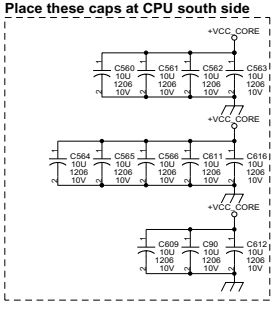
Place these caps at CPU solder side

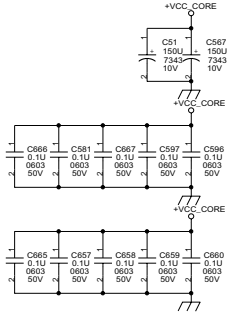


Place these caps at CPU north side

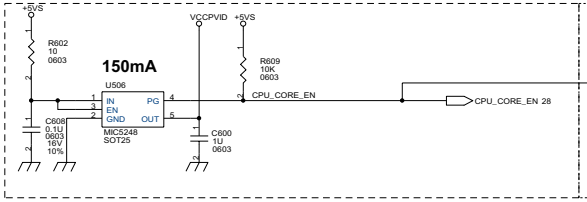


Place these caps at CPU south side

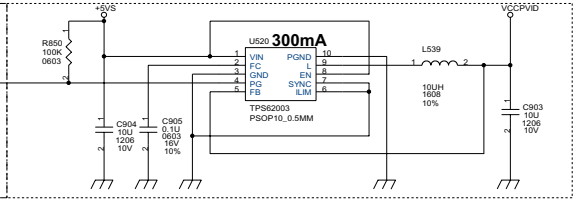




FOR D/T CPU VID



FOR Mobile CPU VID



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Title	PENTIUM4 (2/2)	
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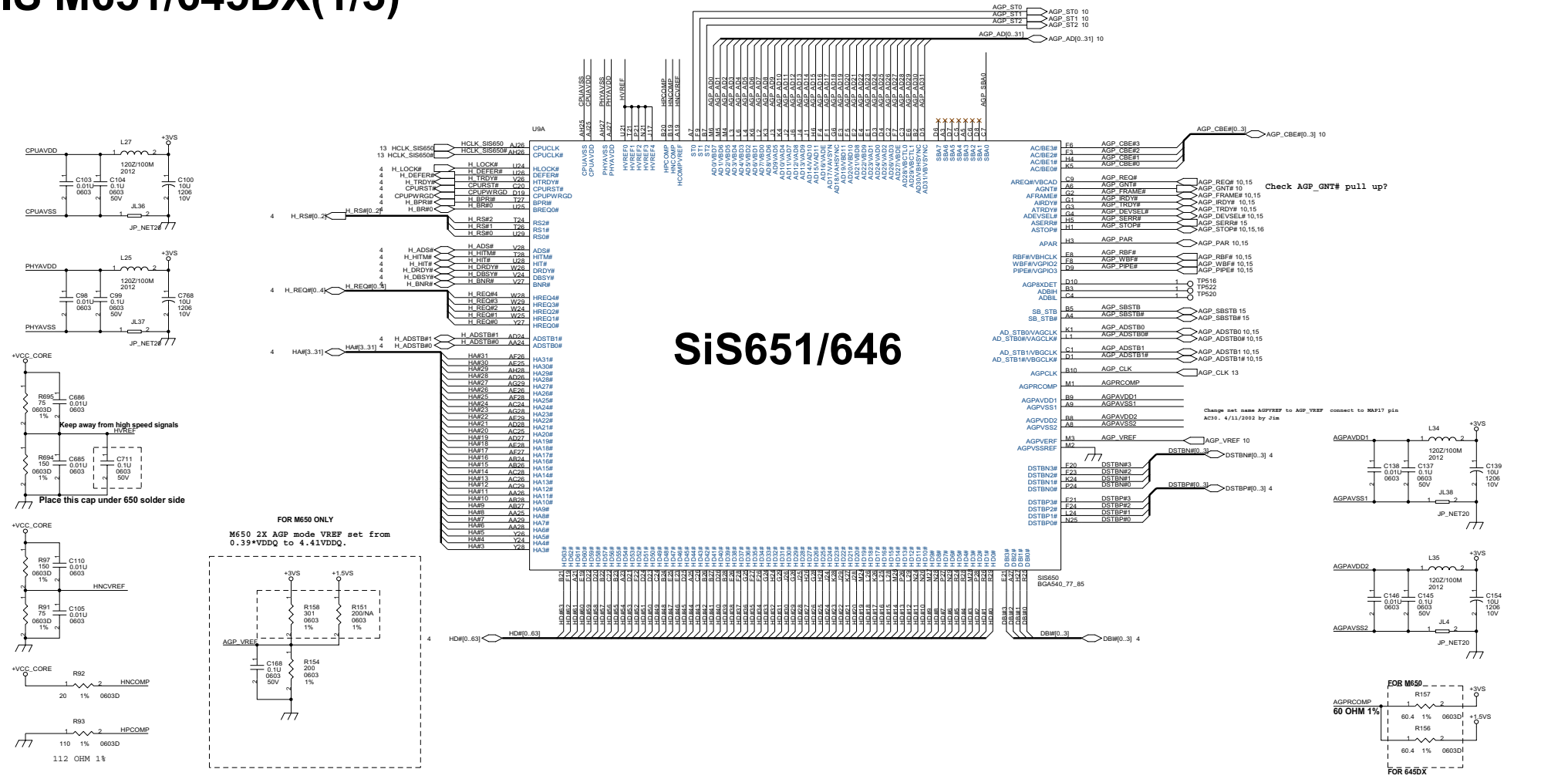
SIS M651/645DX(1/3)



Title	SIS M650/645DX (1/3)
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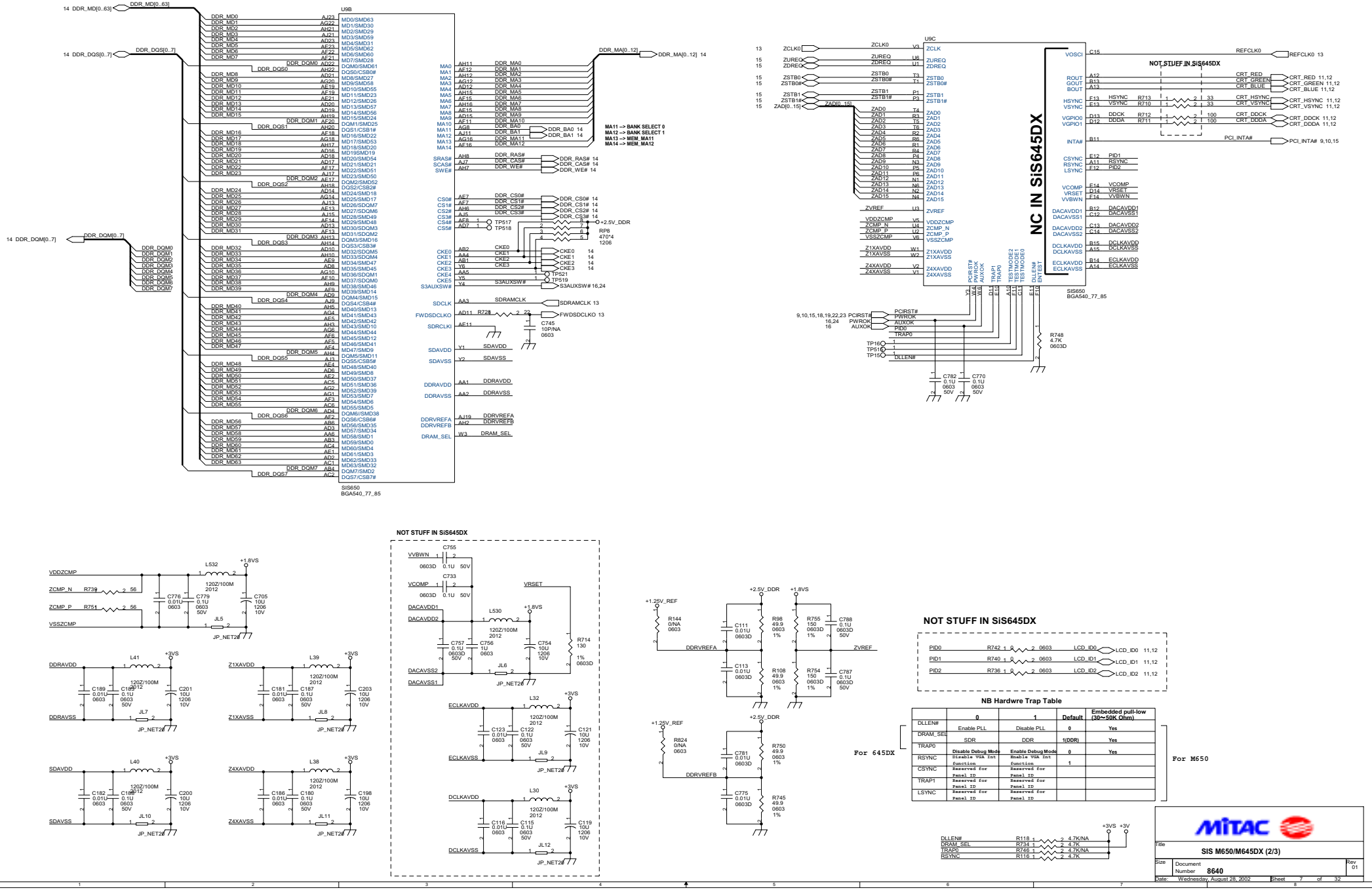
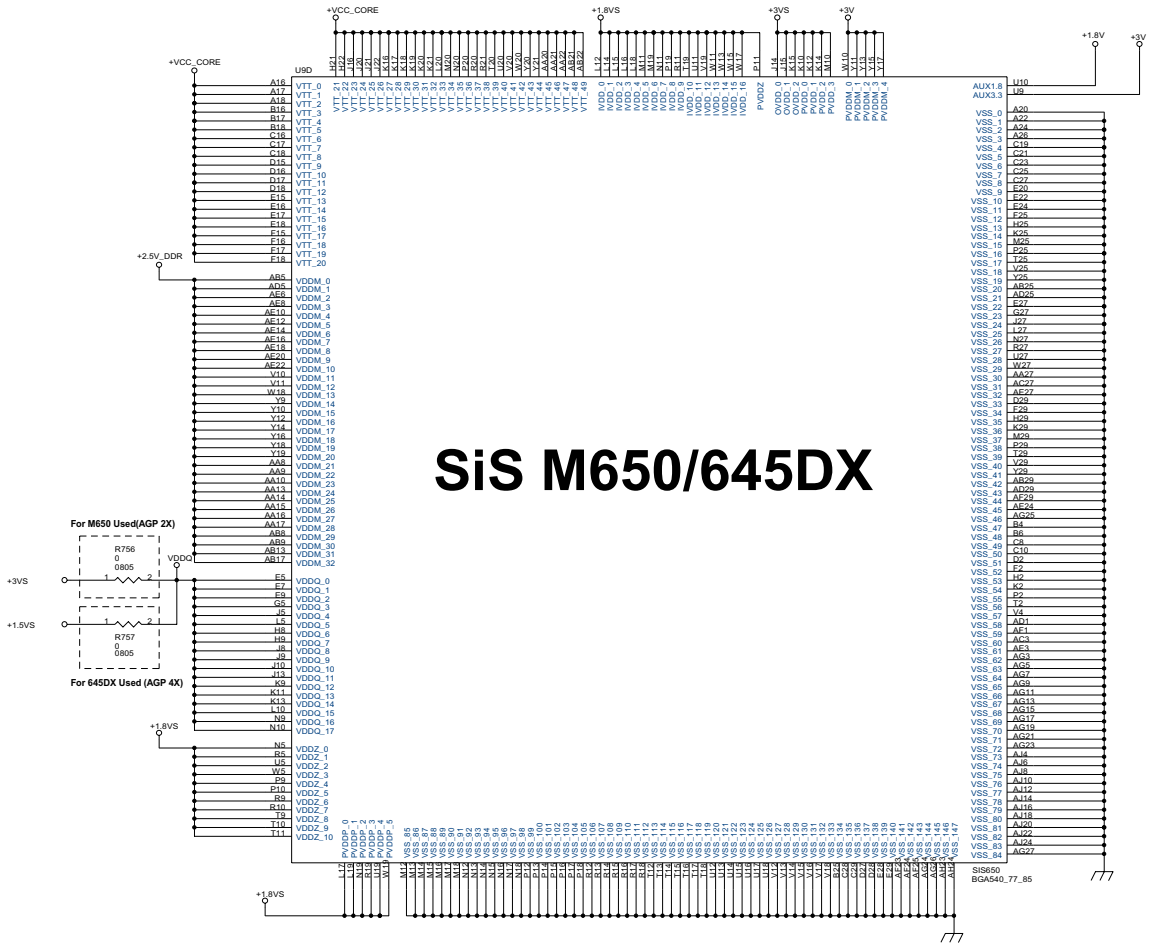
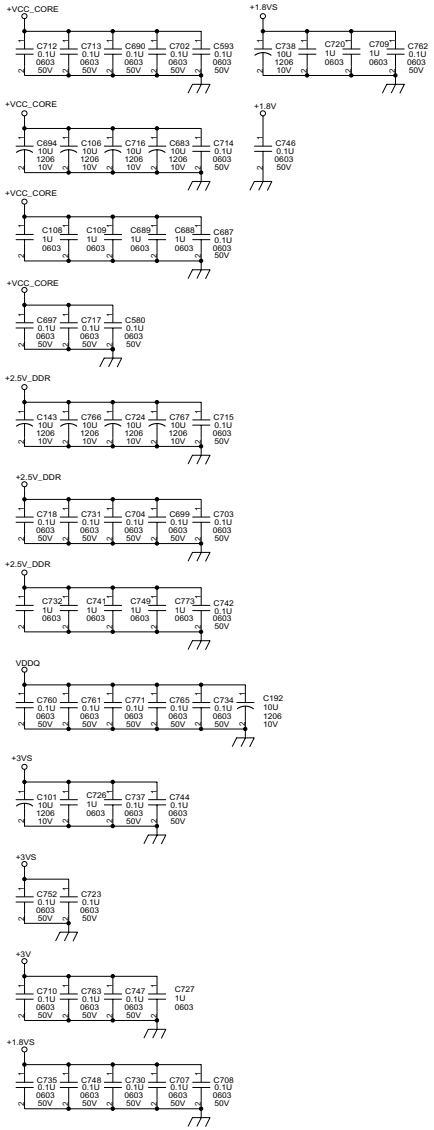
SIS M650/645DX(2/3)



SIS M650/645DX(3/3)





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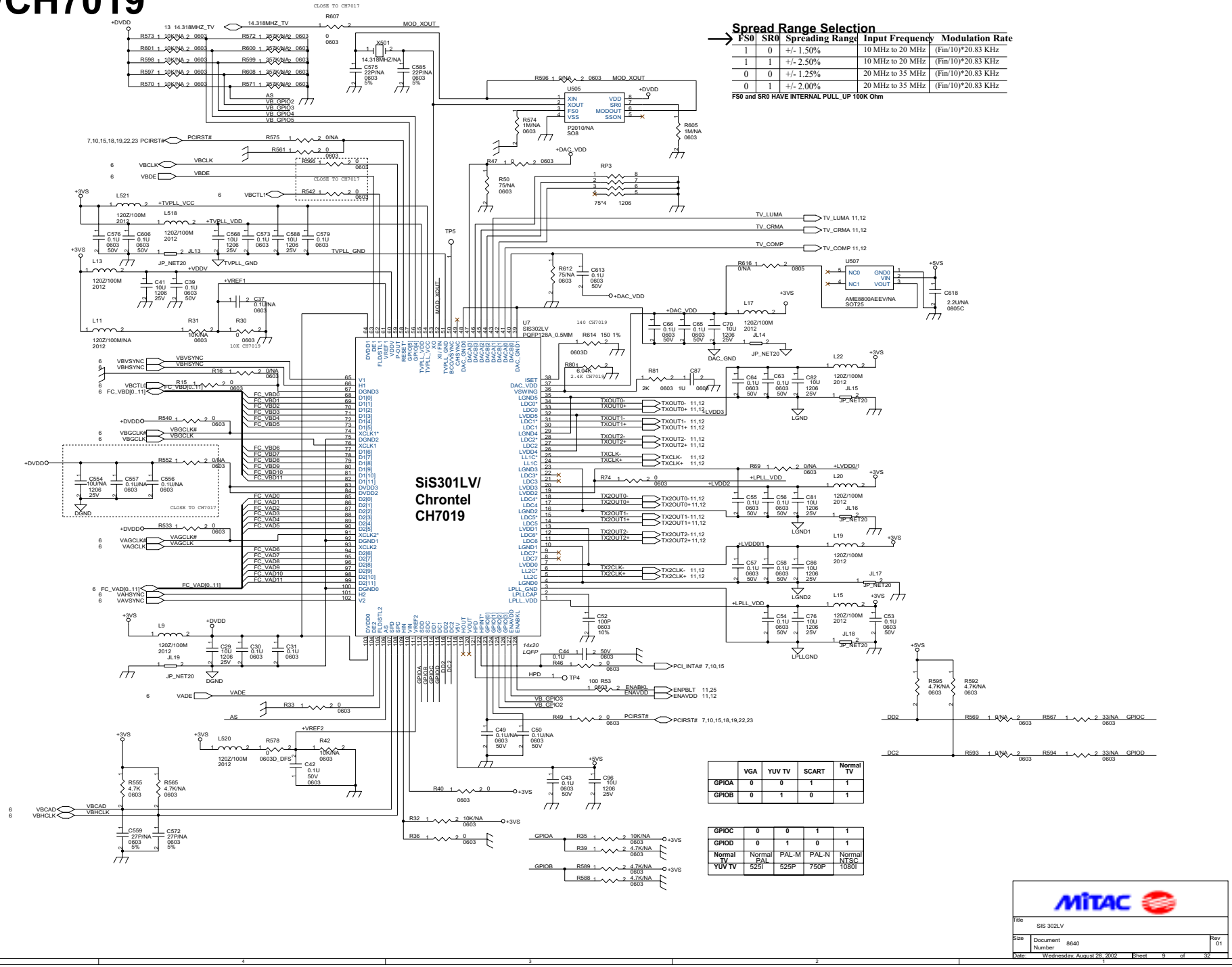
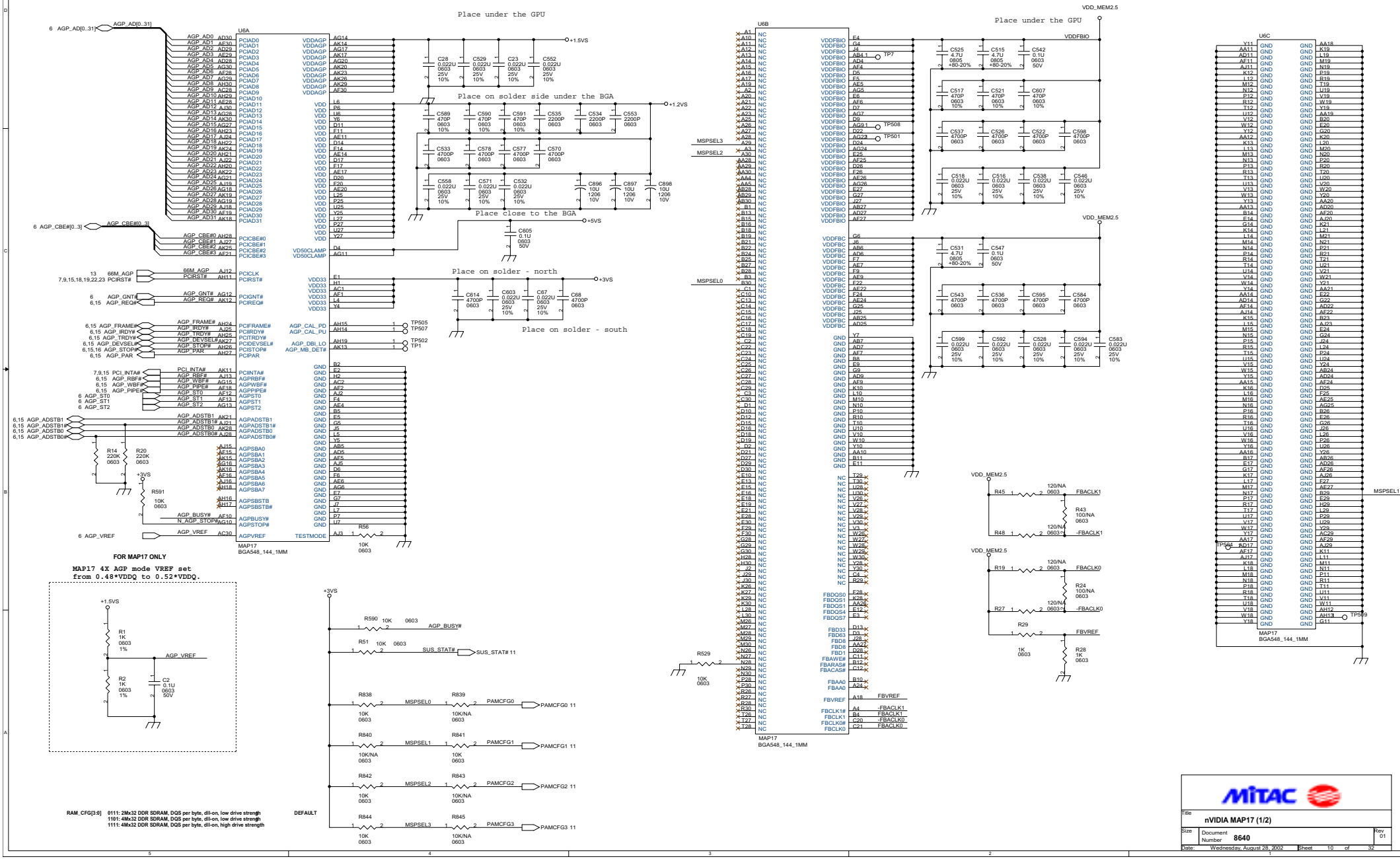
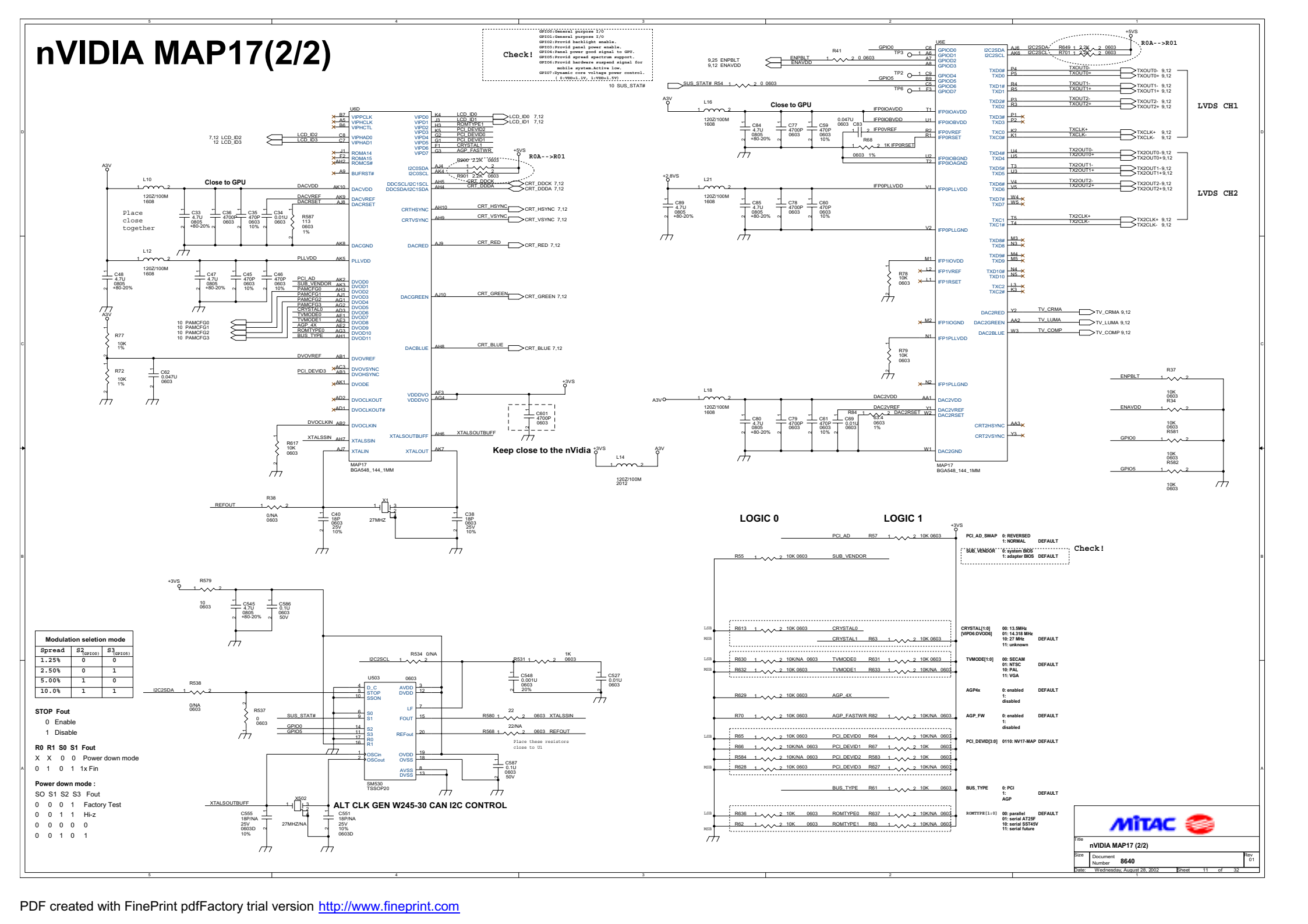
SiS302LV/CH7019



nVIDIA MAP17(1/2)



nVIDIA MAP17(2/2)



Modulation seletion mode		
Spread	S2 (GPIO0)	S3 (GPIO5)
1.25%	0	0
2.50%	0	1
5.00%	1	0
10.0%	1	1

STOP Fout

0 Enable

1 Disable

R0 R1 S0 S1 Fout

X X 0 0 Power down mode

0 1 0 1 1x Fin

Power down mode :

SO S1 S2 S3 Fout

0 0 0 1 Factory Test

0 0 1 1 Hi-z

0 0 0 0 0

0 0 1 0 1

Title	nVIDIA MAP17 (2/2)
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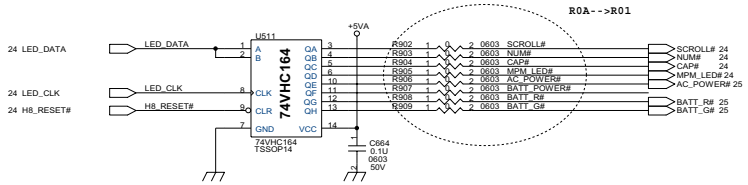
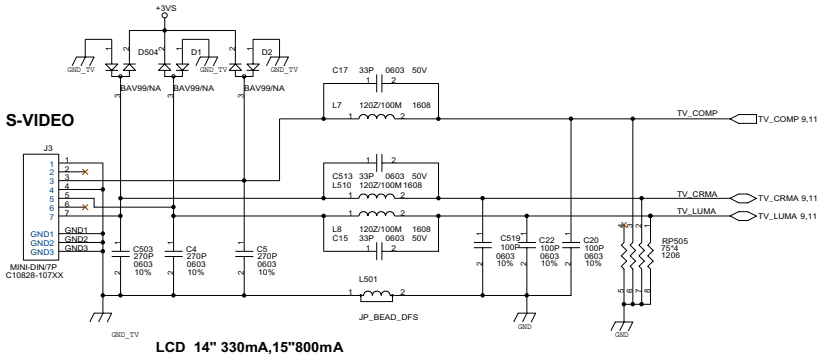
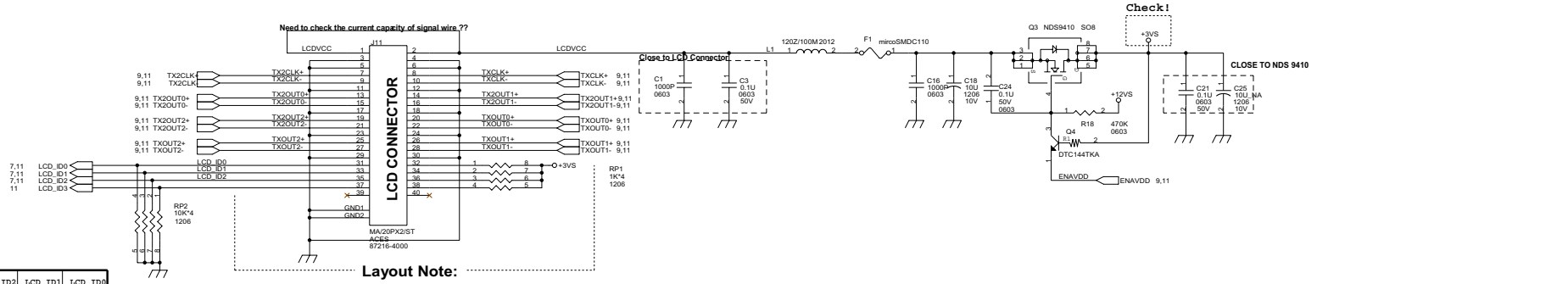
LCD & CRT INTERFACE





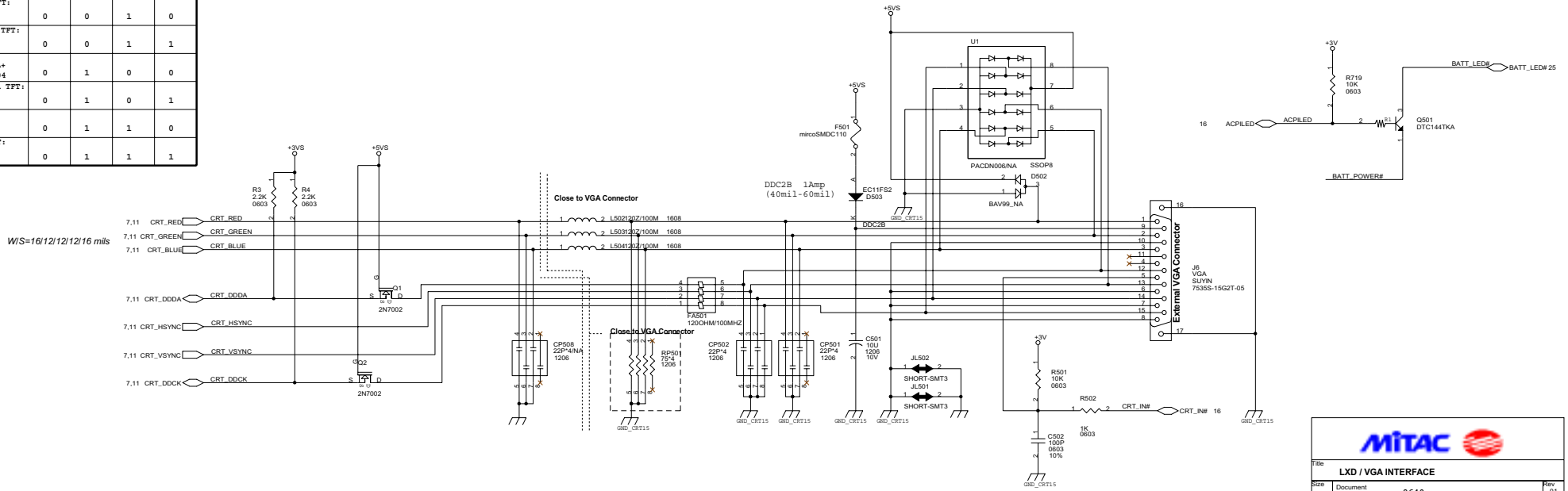


Layout Note:

S/W/W/S=12/6/6/12 mils as short as possible

四組各自平行走線等長

Display	LCD_ID3	LCD_ID2	LCD_ID1	LCD_ID0
QDI 14.1" XGA TFT: QD141X1LH03-MP01/03	0	0	0	0
AU 14.1" XGA TFT: B141XN04-2 (UB141X03)	0	0	0	1
CMO 14.1" XGA TFT: N141X6	0	0	1	0
Sumsung 15" XGA TFT: LT150X3-124	0	0	1	1
Sumsung 15" SXGA+ TFT: LTN150P1-L04	0	1	0	0
HannStar 15" XGA TFT: HSD151PX11-B	0	1	0	1
AU 15" XGA TFT: (TBD)	0	1	1	0
AU 15" SXGA+ TFT: B150PN01	0	1	1	1



Title	LXD / VGA INTERFACE		
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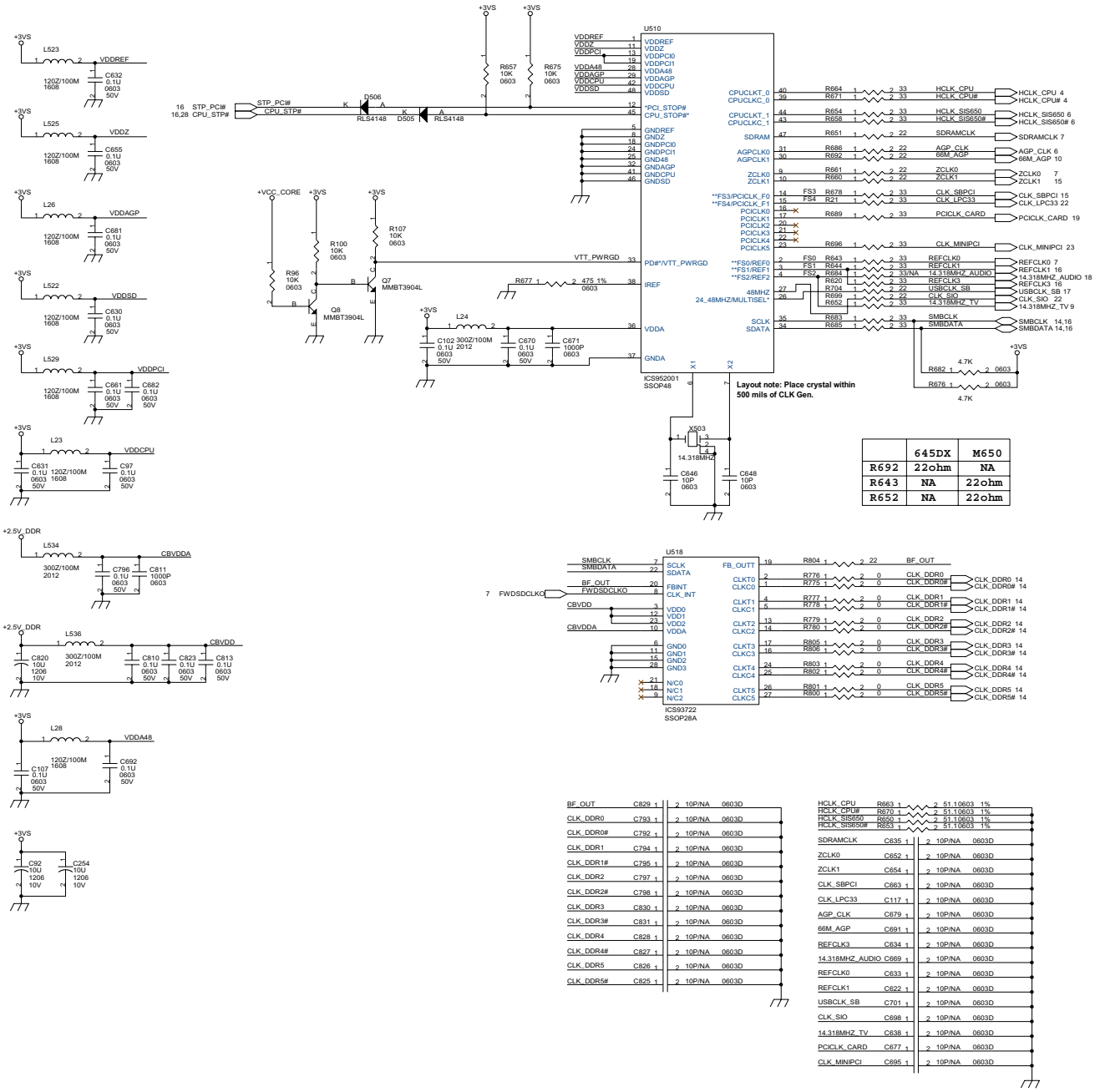
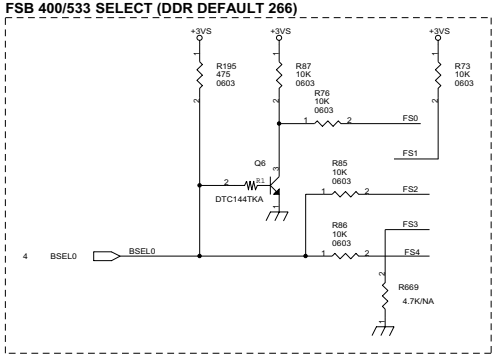
CLOCK GEN/BUFFER



	645DX	M650
R692	22ohm	NA
R643	NA	22ohm
R652	NA	22ohm

FSB 400/533 SELECT (DDR DEFAULT 266)



Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	SDRAM	ZCLK	AGP	PCI		
0	0	0	0	0	66.67	66.67	66.67	66.67	33.33		
0	0	0	0	1	100.00	100.00	66.67	66.67	33.33		
0	0	0	1	0	100.00	200.00	66.67	66.67	33.33		
0	0	0	1	1	100.00	133.33	66.67	66.67	33.33	FSB400/DDR266	DEFAULT 1
0	0	1	0	0	100.00	150.00	60.00	60.00	30.00		
0	0	1	0	1	100.00	125.00	62.50	62.50	31.25		
0	0	1	1	0	100.00	160.00	66.67	66.67	33.33		
0	0	1	1	1	100.00	133.33	80.00	66.67	33.33		
0	1	0	0	0	100.00	200.00	66.67	66.67	33.33		
0	1	0	0	1	100.00	166.67	62.50	62.50	31.25	FSB400/DDR333	
0	1	0	1	0	100.00	166.67	71.43	83.33	41.67		
0	1	0	1	1	80.00	133.33	66.67	66.67	33.33		
0	1	1	0	0	80.00	133.33	66.67	66.67	33.33		
0	1	1	0	1	95.00	95.00	63.33	63.33	31.67		
0	1	1	1	0	95.00	126.67	63.33	63.33	31.67		
0	1	1	1	1	66.67	66.67	50.00	50.00	25.00		
1	0	0	0	0	105.00	140.00	70.00	70.00	35.00		
1	0	0	0	1	100.90	100.90	67.27	67.27	33.63		
1	0	0	1	0	108.00	144.00	72.00	72.00	36.00		
1	0	0	1	1	100.90	134.53	67.27	67.27	33.63		
1	0	1	0	0	112.00	149.33	74.67	74.67	37.33		
1	0	1	0	1	133.33	100.00	66.67	66.67	33.33		
1	0	1	1	0	133.33	133.33	66.67	66.67	33.33	FSB533/DDR266	DEFAULT 2
1	0	1	1	1	133.33	166.67	66.67	66.67	33.33	FSB533/DDR333	
1	1	0	0	0	100.00	133.00	80.00	66.67	33.33		
1	1	0	0	1	100.00	100.00	80.00	66.67	33.33		
1	1	0	1	0	100.00	166.67	83.33	62.50	31.25		
1	1	0	1	1	133.33	160.00	80.00	66.67	33.33		
1	1	1	0	0	100.00	133.00	100.00	66.67	33.33		
1	1	1	0	1	100.00	100.00	100.00	66.67	33.33		
1	1	1	1	0	100.00	166.67	100.00	62.50	31.25		
1	1	1	1	1	133.33	160.00	100.00	66.67	33.33		

MiTAC

Title: CLOCK GENERATOR

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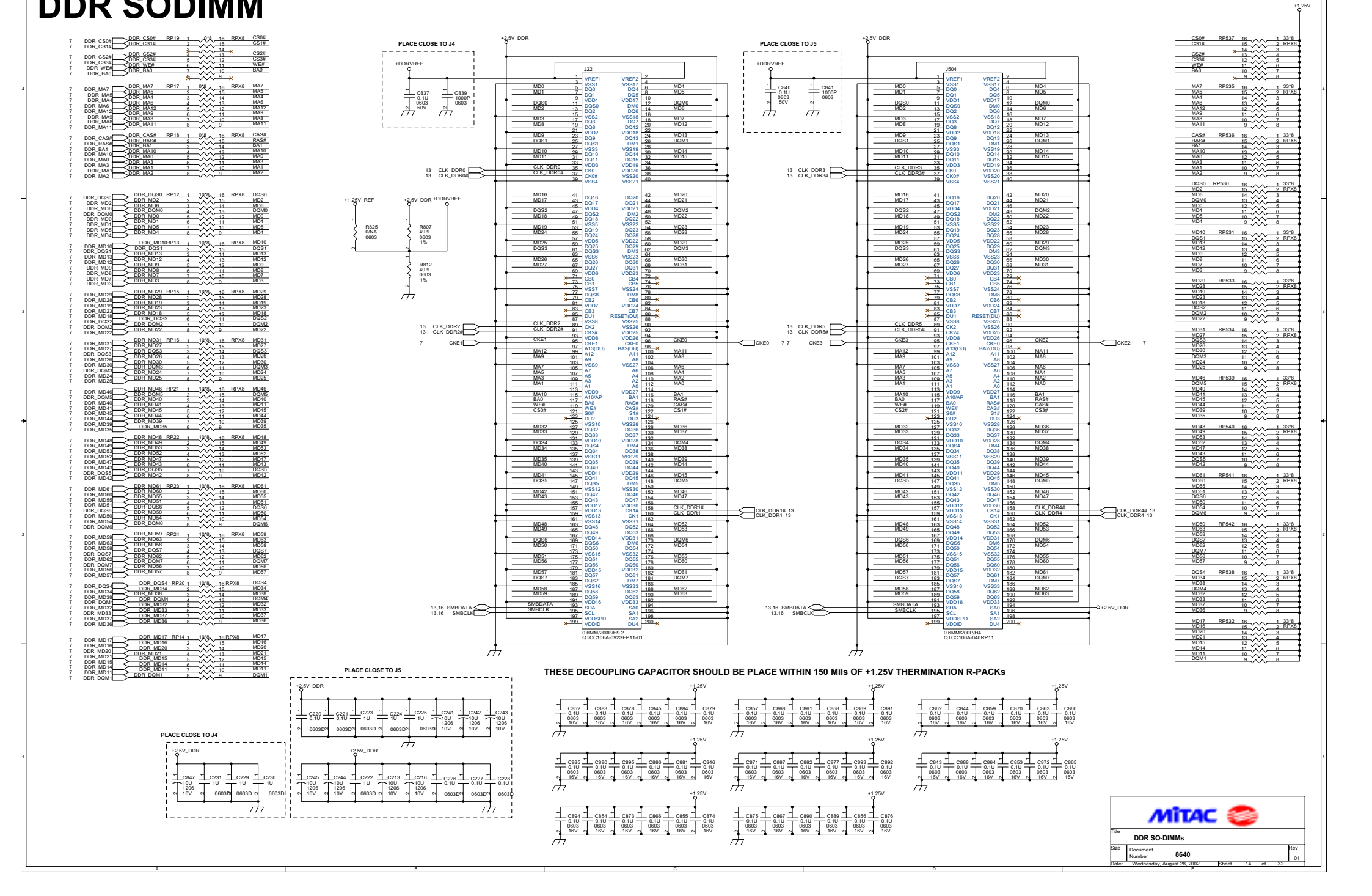
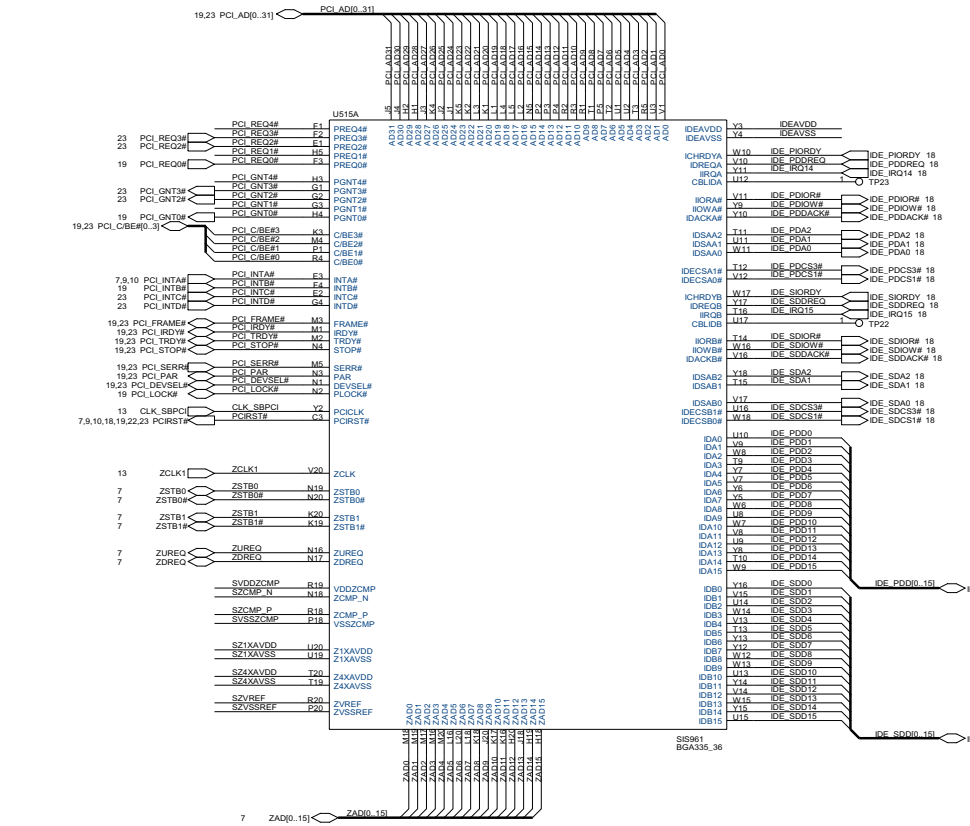
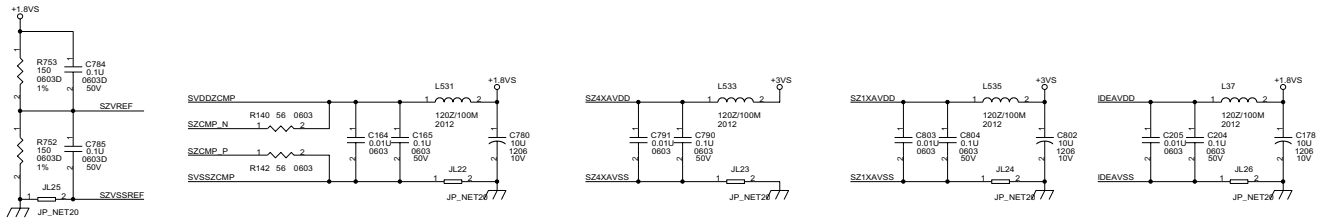
DDR SODIMM

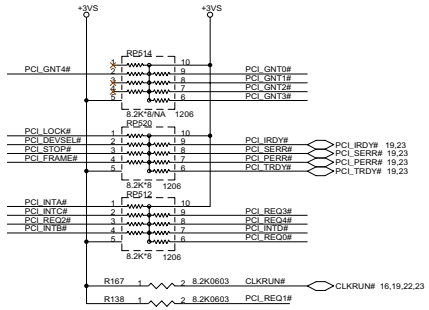


SIS962(1/3)

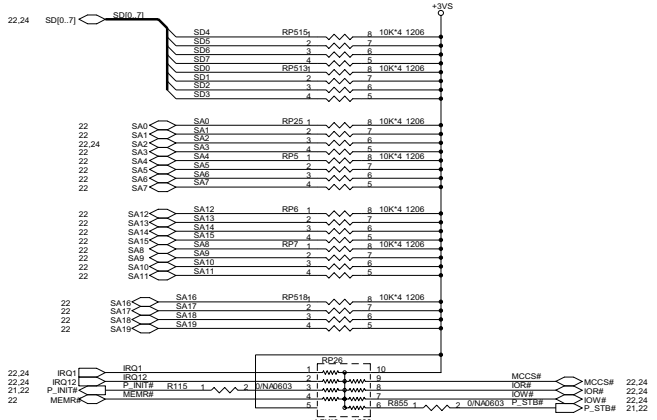




PCI BUS PULL UP RESISTERS

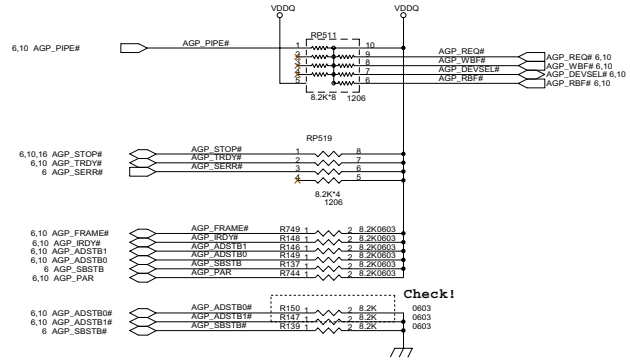


ISA BUS PULL UP RESISTERS



AGP BUS PULL UP/DOWN RESISTORS

FOR 645DX ONLY



Title	SIS962 (1/3)	
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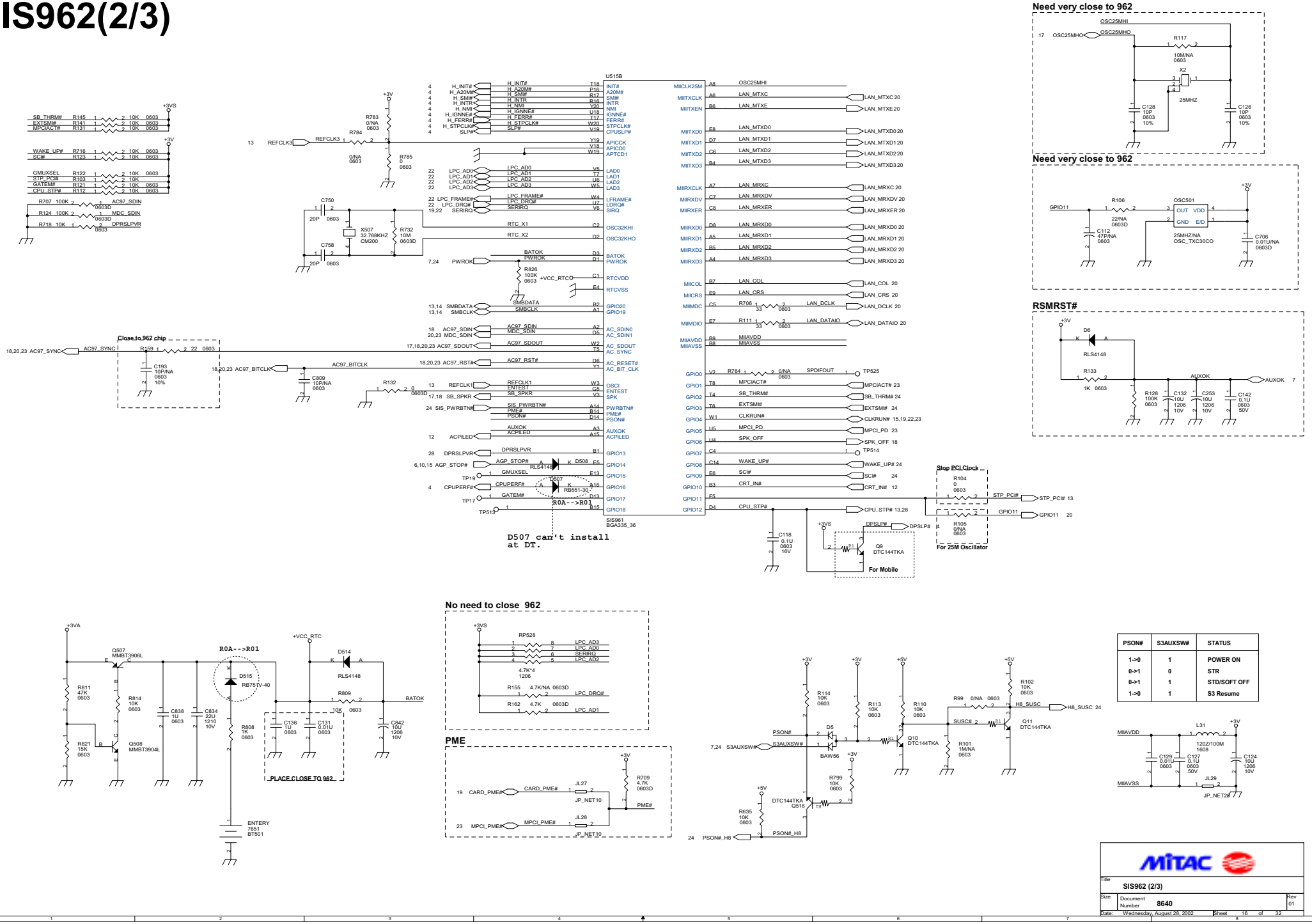
SIS962(2/3)



PSON#	S3AUXSW#	STATUS
1->0	1	POWER ON
0->1	0	STR
0->1	1	STD/SOFT OFF
1->0	1	S3 Resume

MiTAC

Title	SIS962 (2/3)	
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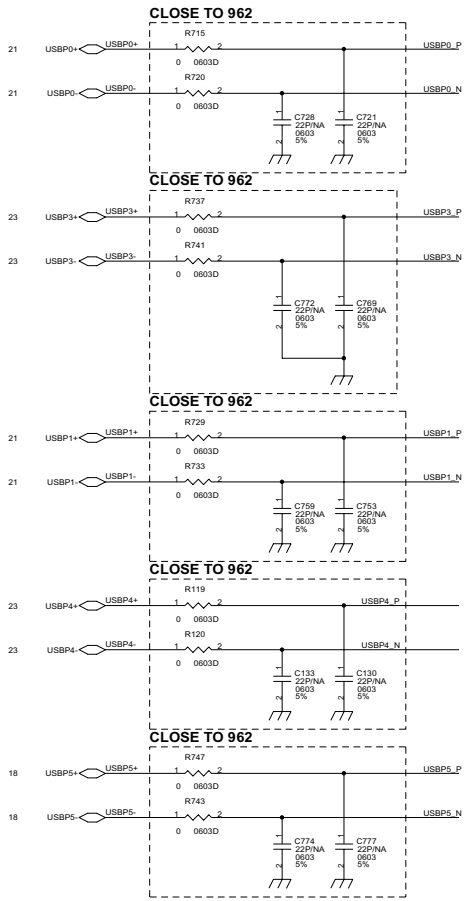
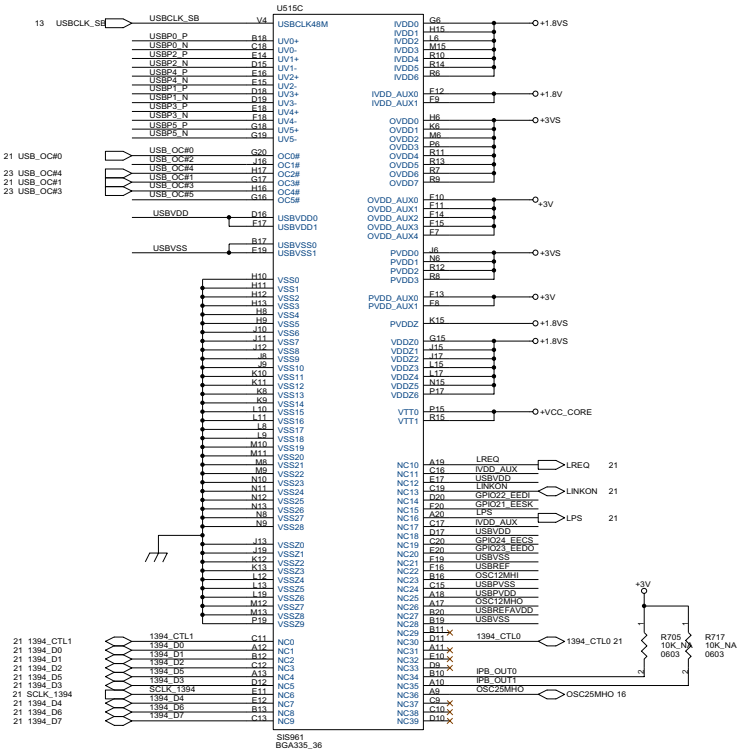
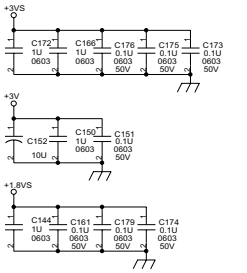
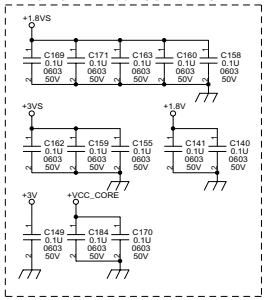
SIS962(3/3)



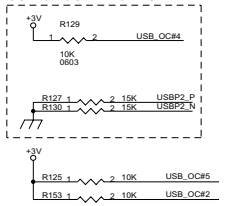


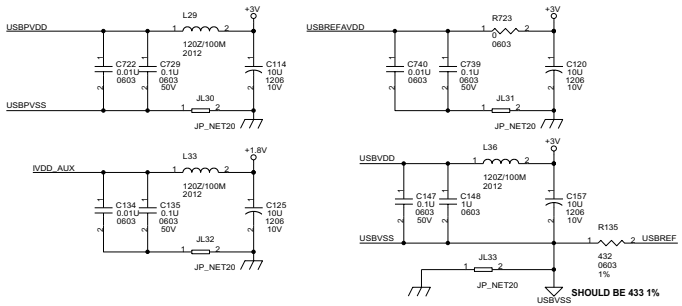


PLACE UNDER 962 SOLDER SIDE

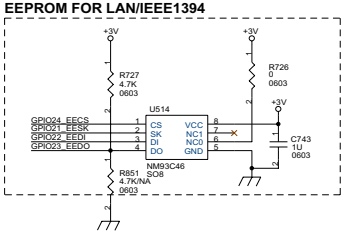


USB UNUSED PORTS

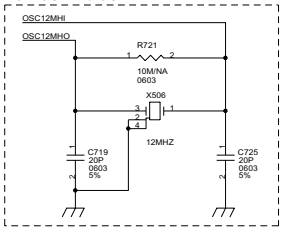




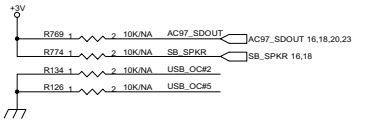
EEPROM FOR LAN/IEEE1394



FOR USB 2.0 USED



Hardware Strap



Symbol	0	1	Default	Notes
SB_SPKR (LPC addr mapping)	disable	enable	0	Internal Pull-down
AC97_SDOUT (Trap mode)	ROM	Reserved	0	Internal Pull-down
USB_OC4# (South bridge debug mode)	enable	disable	1	
IPB_OUT0(MuTIOL clock PLL)	enable	disable	0	Internal Pull-down
IPB_OUT1(MuTIOL operation mode select)	Full-swing	Partial-swing	0	Internal Pull-down
AC97_SYNC (PCICLK PLL)	enable	disable	0	Internal Pull-down

MiTAC

Title	SIS962 (3/3)	
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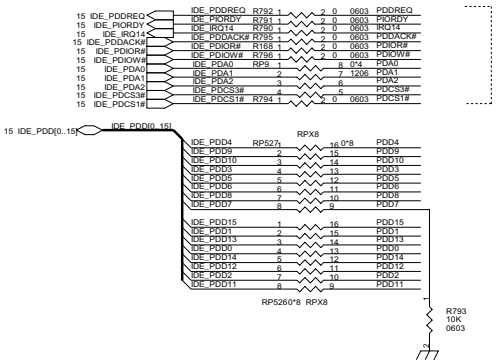
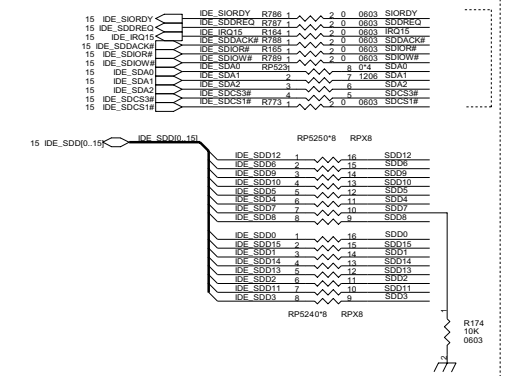
IDE INTERFACE

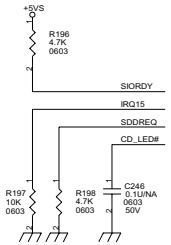
CHANGE TO 0 ohm

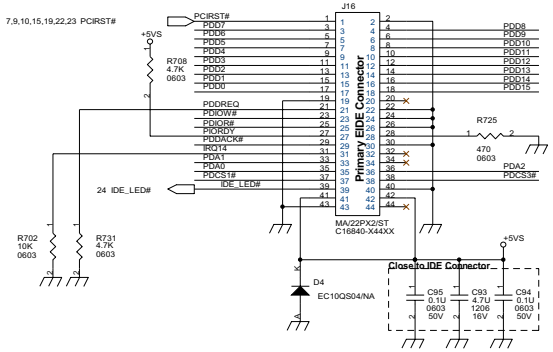
Terminating resistors should be place close to South Bridge



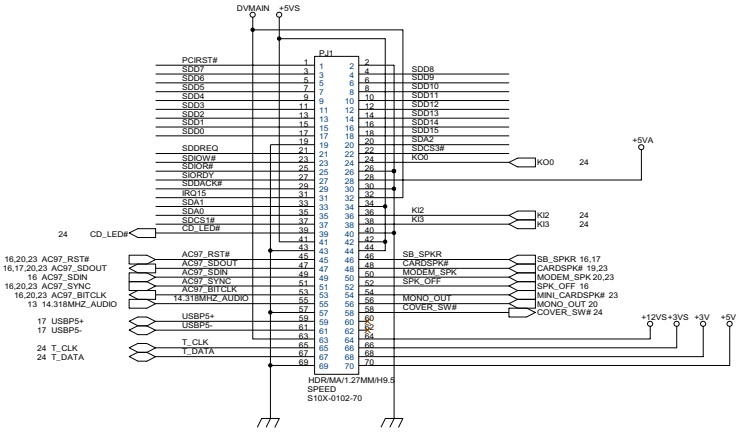
Trminating resistors should be place close to South Bridge



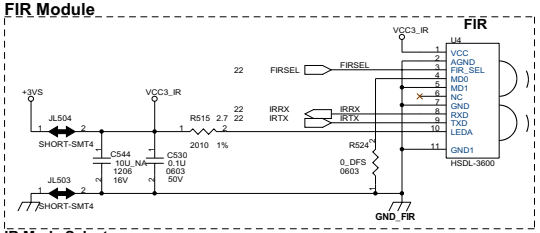




BTB CONNECTOR



FIR Module



IR Mode Select

IRMODE0	IRMODE1	FIRSEL	RX Function	TX Function
HI	LOW	X	Shutdown	Shutdown
LOW	LOW	LOW		Full Distance Power
LOW	HI	LOW	SIR	2/3 Distance Power
HI	HI	LOW	SIR	1/3 Distance Power
LOW	LOW	HI	MIR/FIR	Full Distance Power
LOW	HI	HI	MIR/FIR	2/3 Distance Power
HI	HI	HI	MIR/FIR	1/3 Distance Power

MiTAC

Title: IDE INTERFACE & PULL UPs

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PCMCIA CONTROLLER & CARDBUS SCOKET

PCI1410A

AD20

PCI_INTB#

REQ0#/GNT0#

SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE

U12 PCI1410A PQFP144_0.5MM

J19 Card Bus Socket 0.635/H7.9/68P CL640-1009-9 HIROSE

U11 TPS2211 SSOP16

Close to TPS2211

Title	PCI4410 & 1394 PHY	
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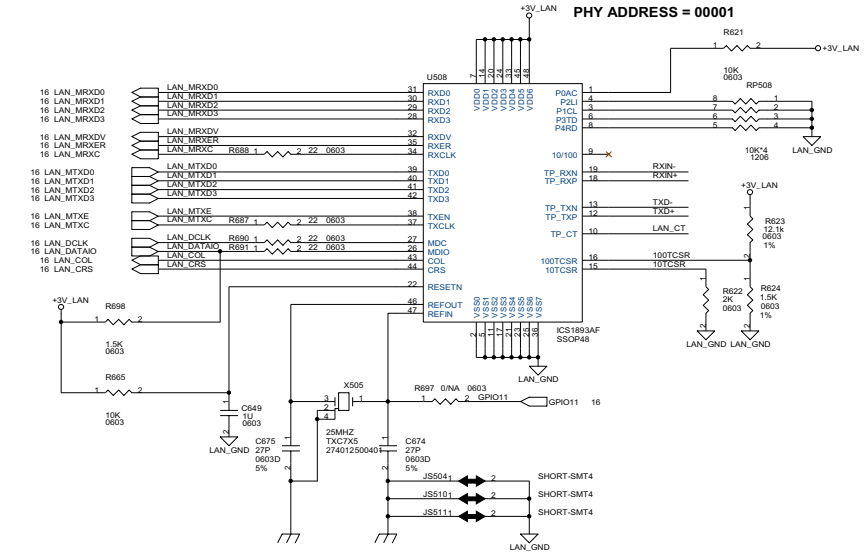
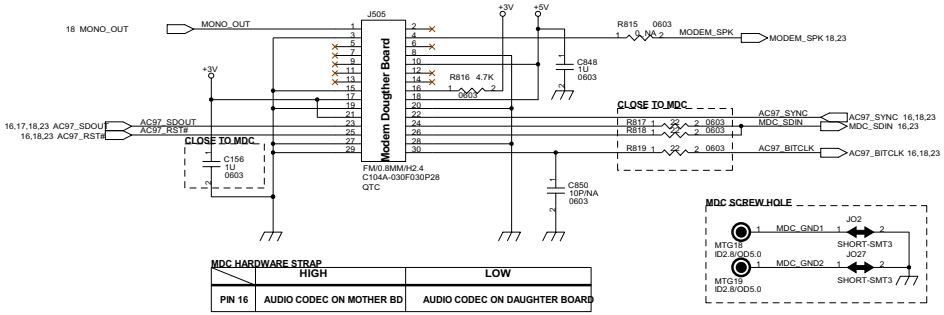
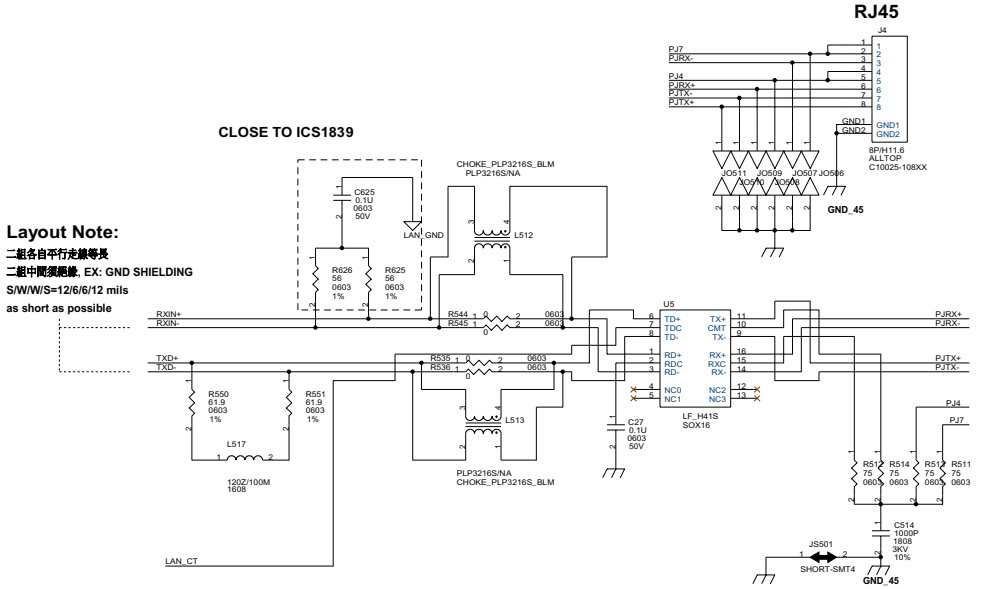
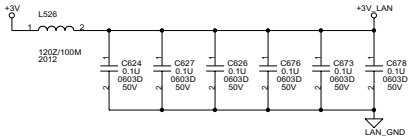
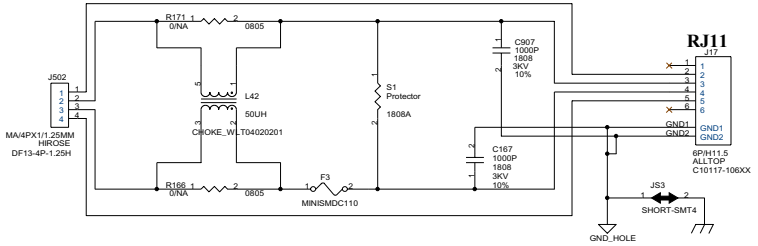
LAN AND MDC











Title	LAN PHY (ICS1893)& MDC	
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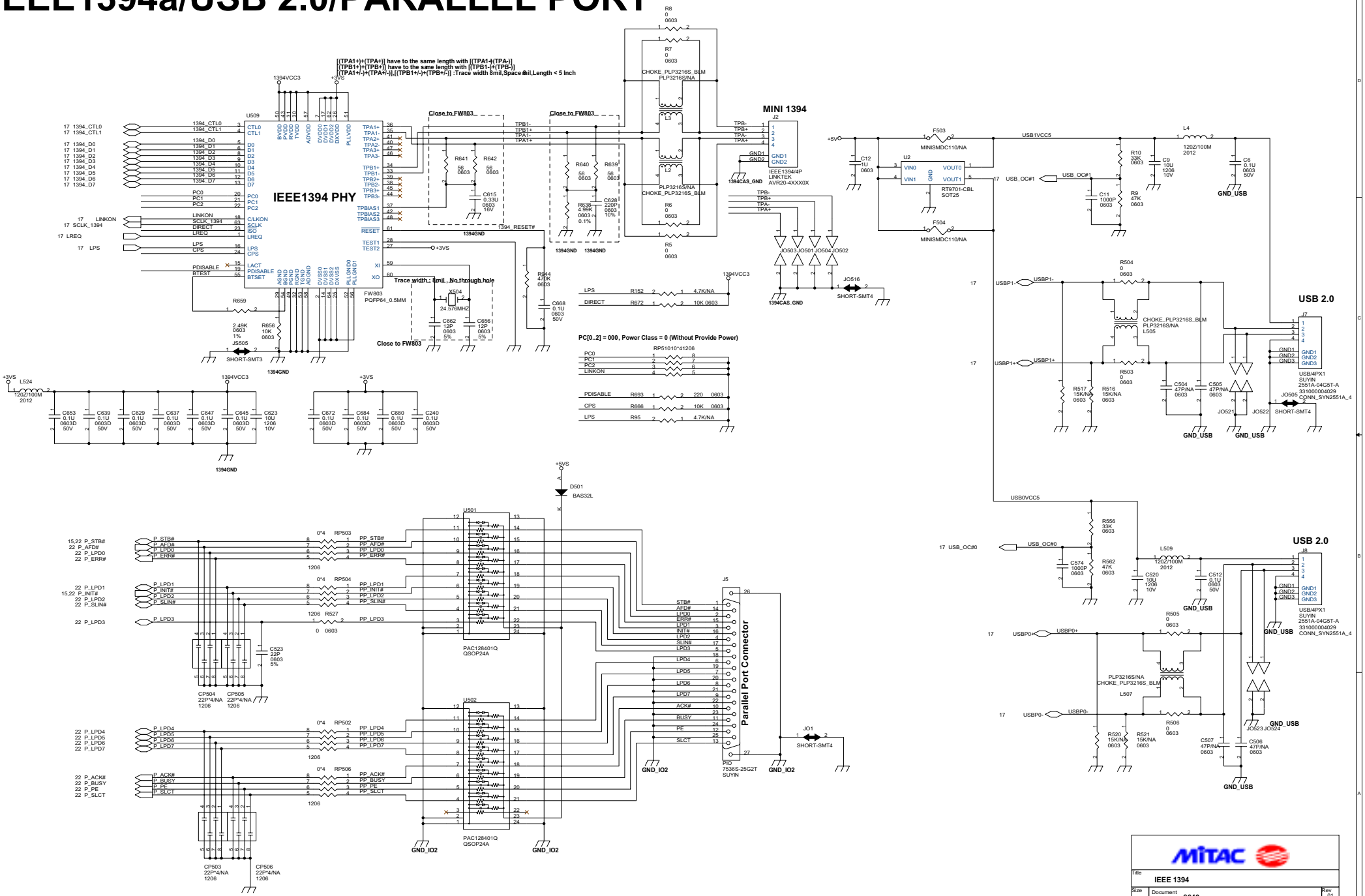
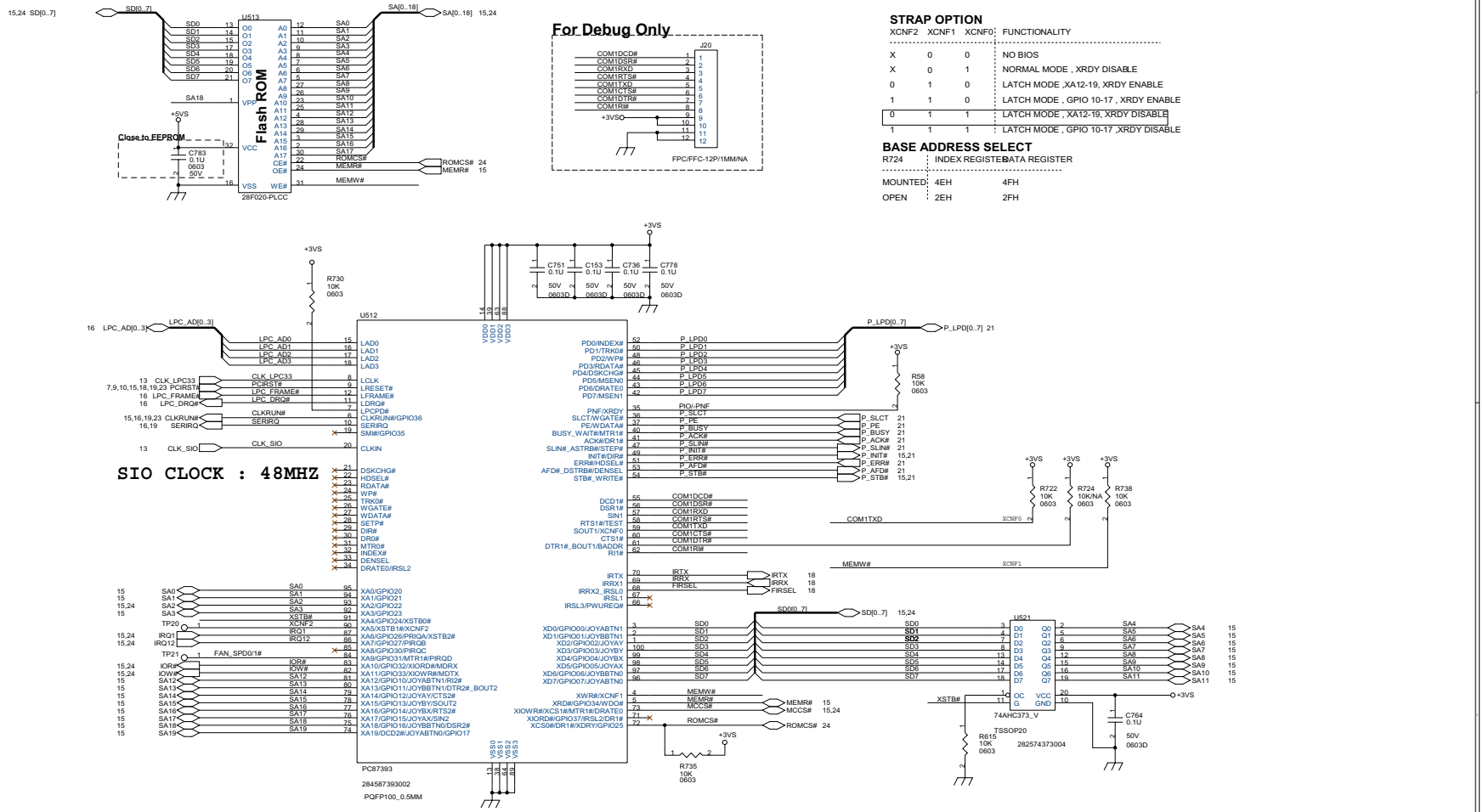
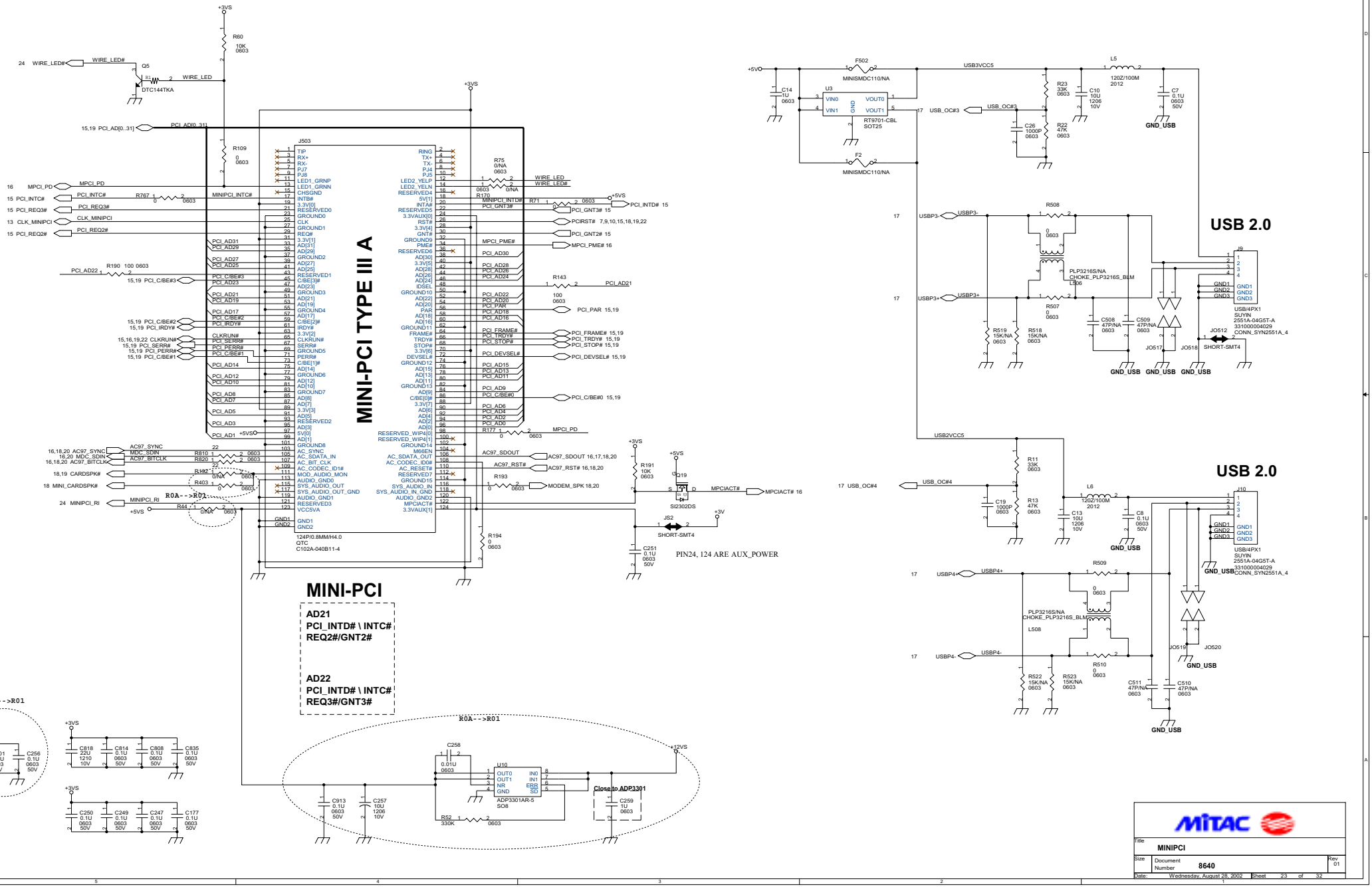
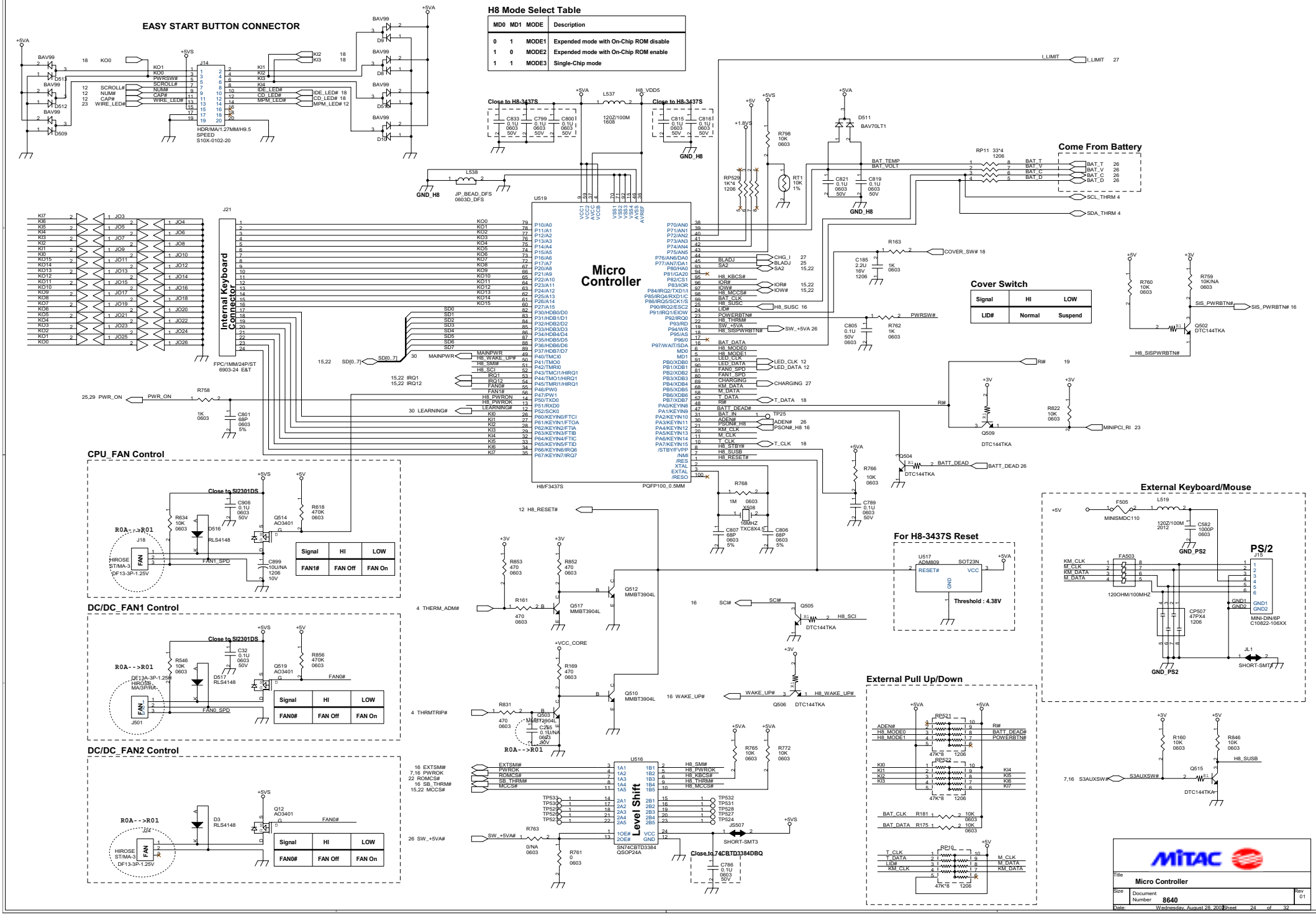
IEEE1394a/USB 2.0/PARALLEL PORT

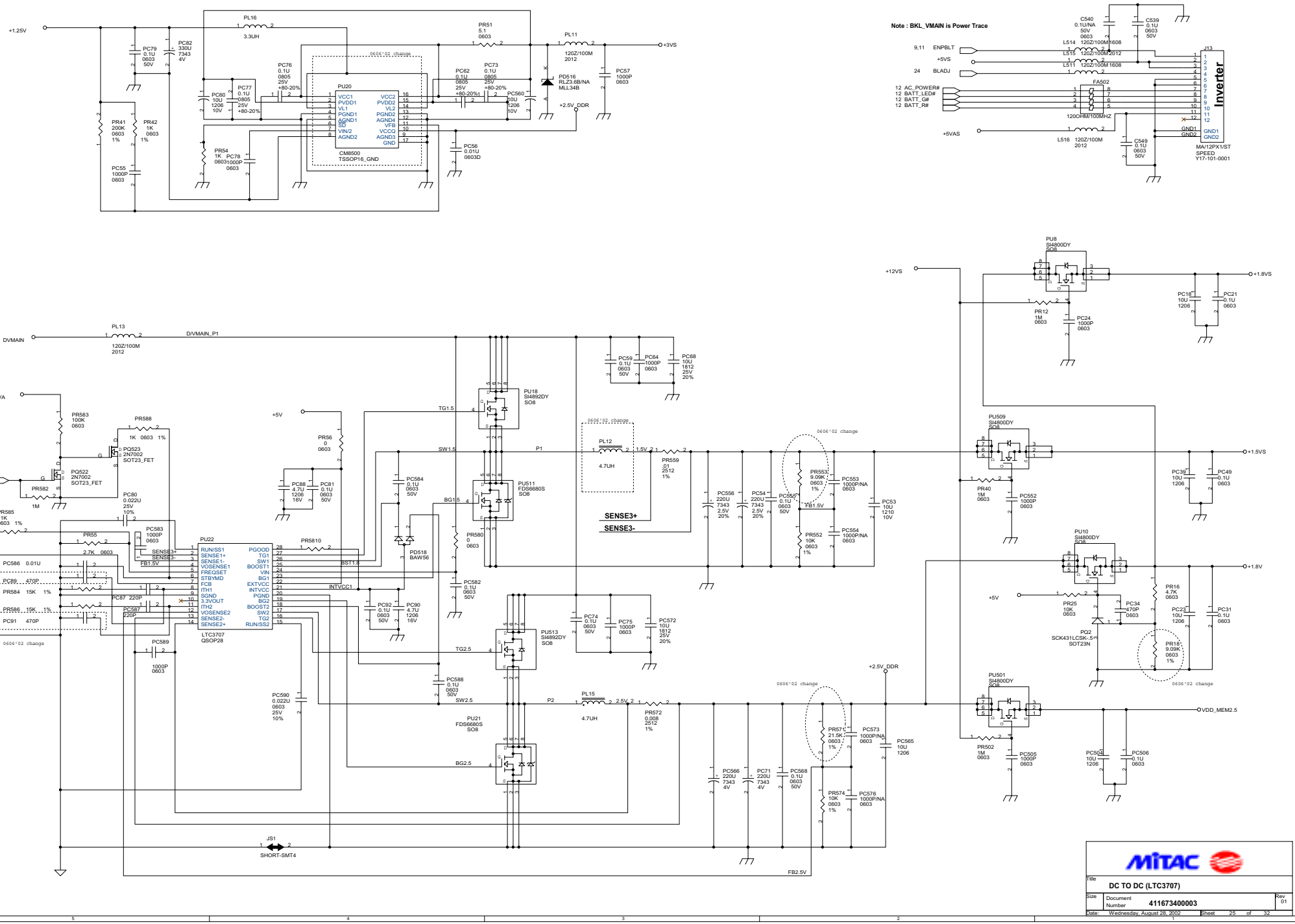


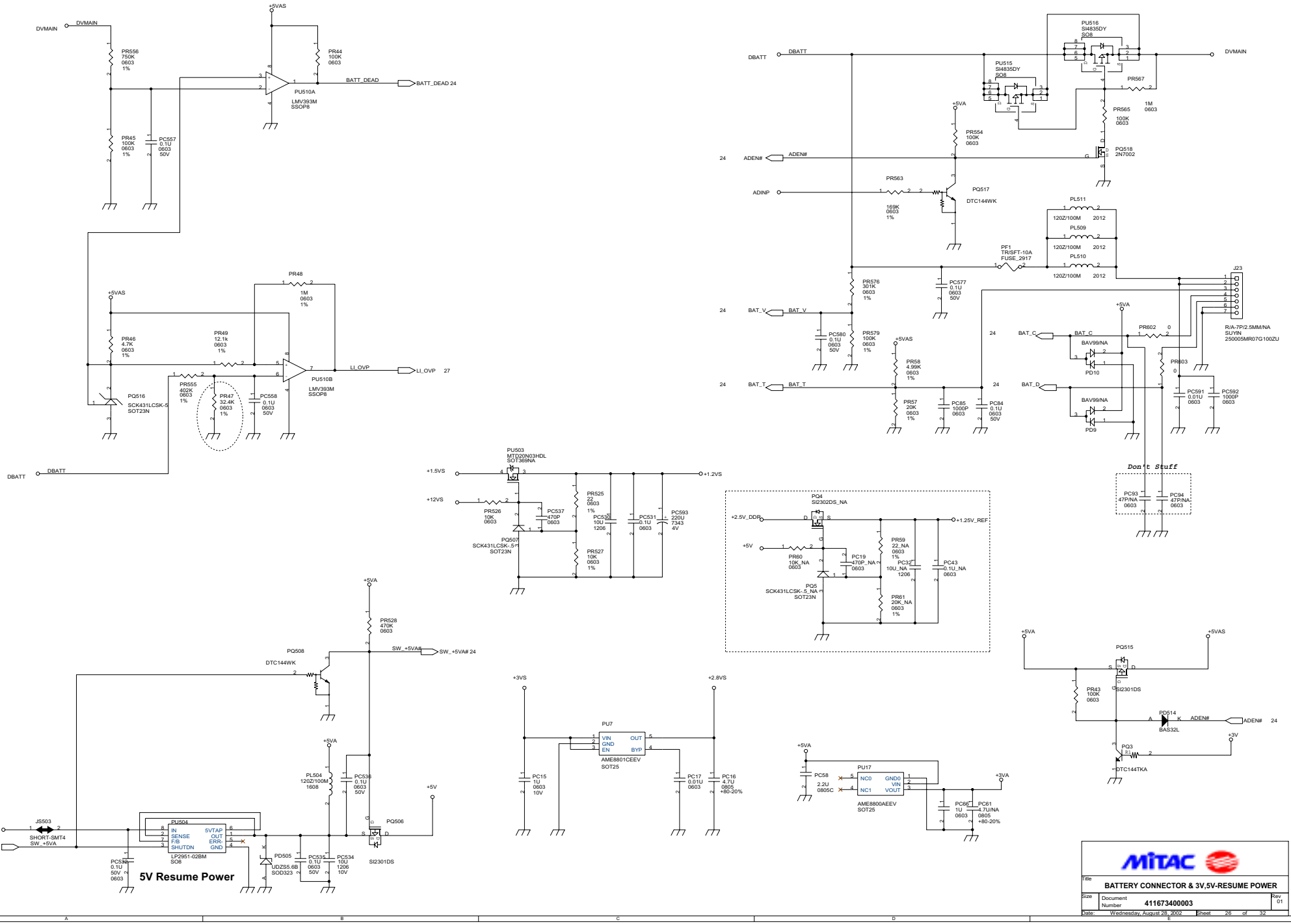


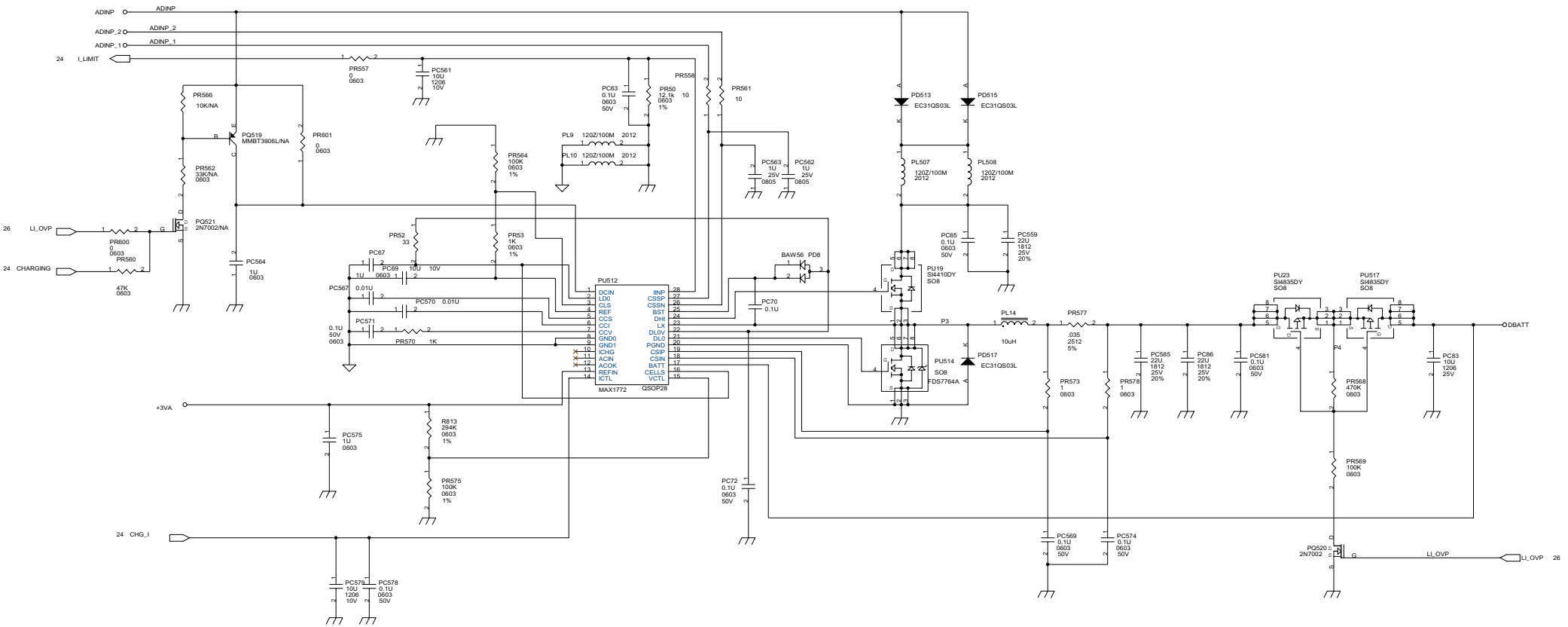
MINI-PCI











MiTAC

Title	DC-DC CONNECTOR ,CHARGER	
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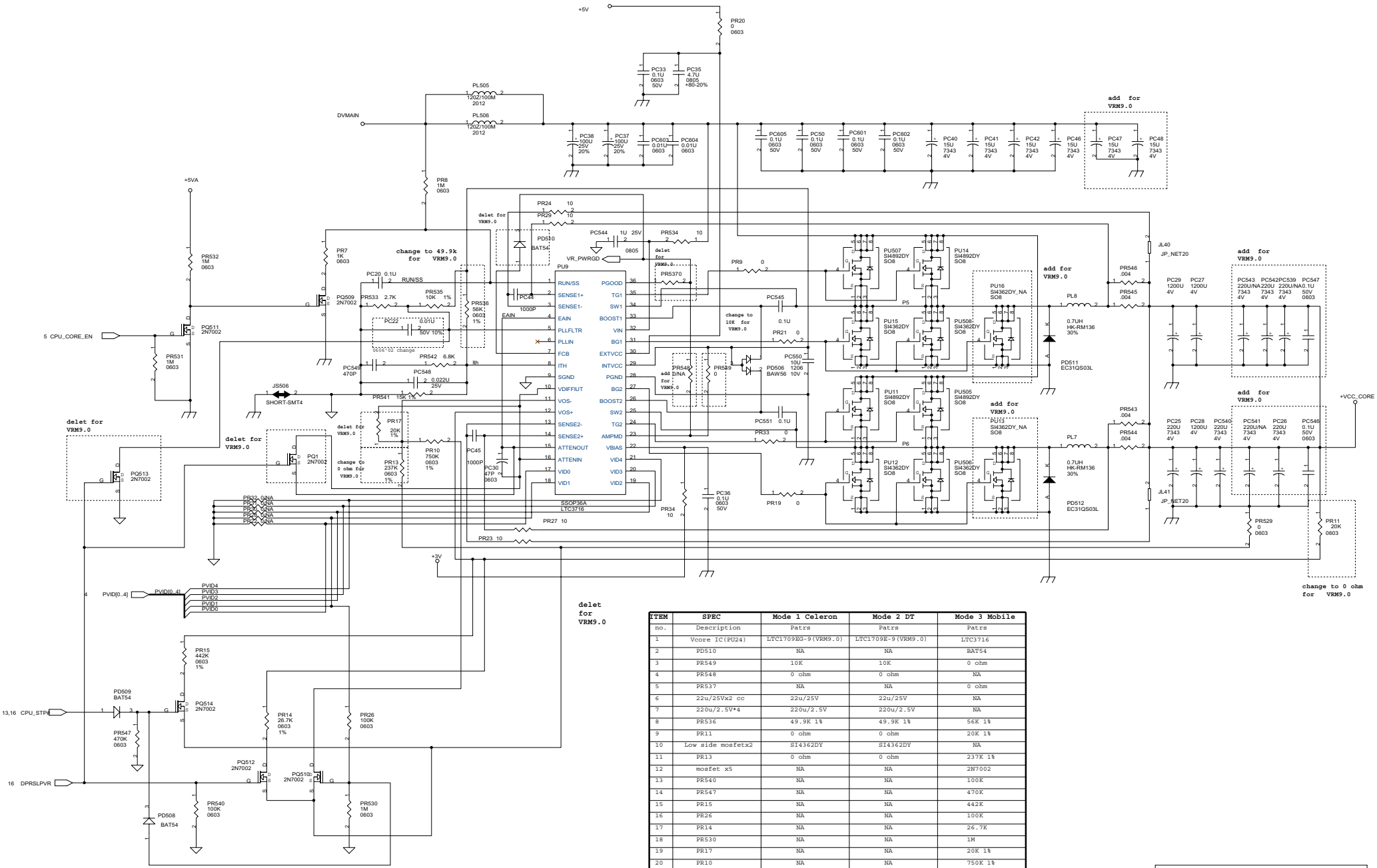

delet for VRM9.0

ITEM	SPEC	Mode 1 Celeron	Mode 2 DT	Mode 3 Mobile
no.	Description	Patrs	Patrs	Patrs
1	Vcore IC(PU24)	LTC1709EG-9(VRM9.0)	LTC1709E-9(VRM9.0)	LTC3716
2	PD510	NA	NA	BAT54
3	PR549	10K	10K	0 ohm
4	PR548	0 ohm	0 ohm	NA
5	PR537	NA	NA	0 ohm
6	22u/25Vx2 cc	22u/25V	22u/25V	NA
7	220u/2.5V*4	220u/2.5V	220u/2.5V	NA
8	PR536	49.9K 1%	49.9K 1%	56K 1%
9	PR11	0 ohm	0 ohm	20K 1%
10	Low side mosfetx2	SI4362DY	SI4362DY	NA
11	PR13	0 ohm	0 ohm	237K 1%
12	mosfet x5	NA	NA	2N7002
13	PR540	NA	NA	100K
14	PR547	NA	NA	470K
15	PR15	NA	NA	442K
16	PR26	NA	NA	100K
17	PR14	NA	NA	26.7K
18	PR530	NA	NA	1M
19	PR17	NA	NA	20K 1%
20	PR10	NA	NA	750K 1%
21	Diode	NA	NA	BAT54

MiTAC

Title: CPU CORE VOLTAGE (LTC3716)

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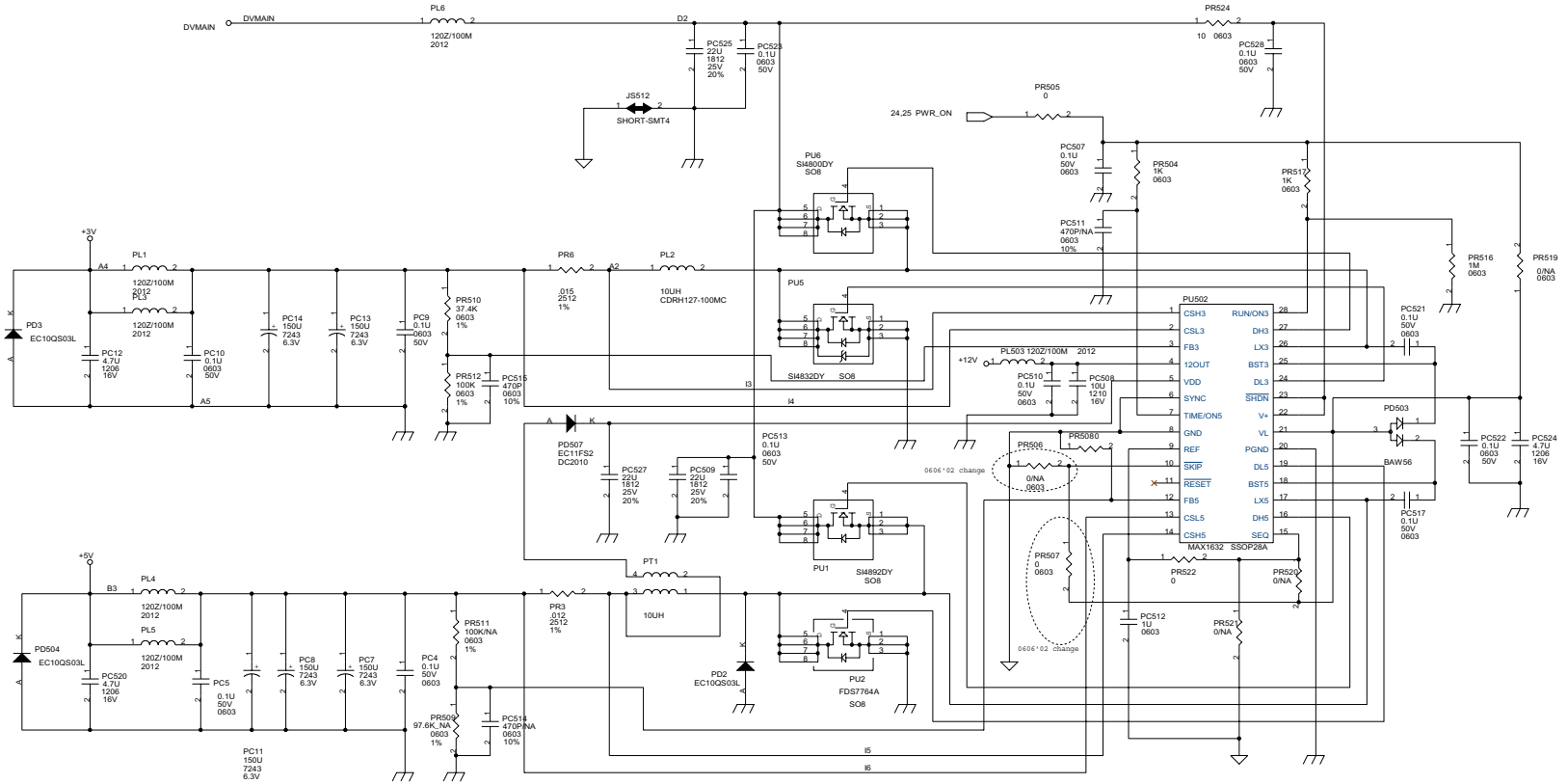
SYSTEM POWER (5V 3V 12V)



Title	SYSTEM POWER		
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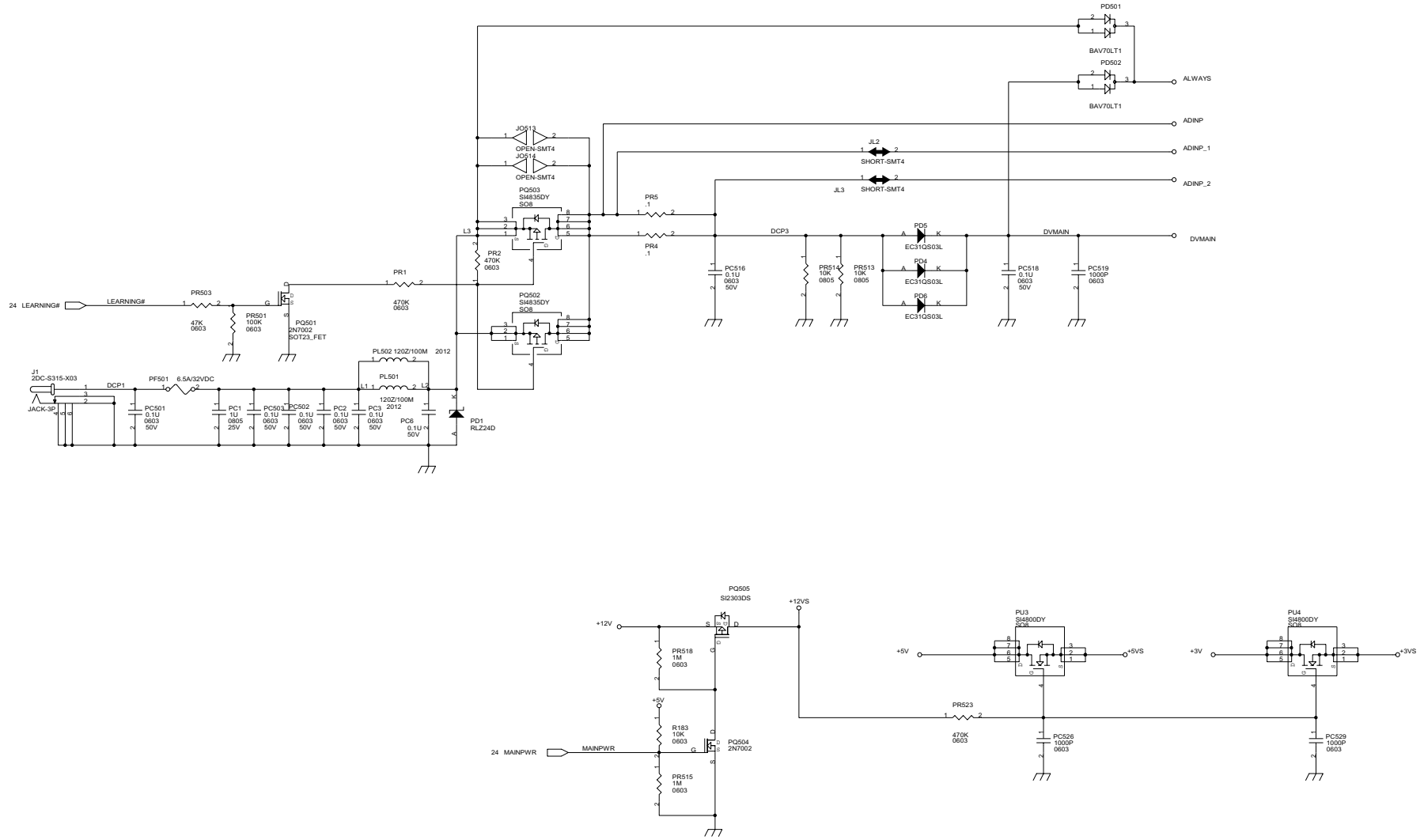

MiTAC

Title: DC POWER

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History:

REV. Layout

1.Changed FootPrint from 0603B to 0603D for easy layout.(all parts) 4/4/2002
2.Change DDR socket from stand to rev at location J5 for easy layout. 4/4/2002
3.Mirror 8P4C capacitors at location CP1,CP2,CP3,CP4,CP5,CP6 for easy layout. 4/4/2002
4.Mirror array bead at location FA1,FA2,FA3,FA4,FA5,FA6 for easy layout. 4/9/2002
5.Creat display ID for auto detect panel. 4/10/2002
6.Change CPURST# pullup from 51ohm/NA to 51ohm at location R28 that the signal don't have on-die termination and must be terminated on the system board. 4/10/2002
7.Change R44 value from 200 ohm to NA. 4/11/2002
8.Change net name AGPVREF to AGP_VREF connect to MAP17 pin AC30 for AGP 4X mode. 4/11/2002 by Jim
9.Change R43 from 200ohm to 301ohm and chang R45 from 301ohm to 200ohm for 0.4*VDDQ at AGP 2X mode. 4/11/2002
10.Change R200 and R203 from 10K to NA tor set default NTSC (MAP17)in TVMODE. 4/12/2002
11.Change R220 and R222 from 10K to NA for MAP17 default parallel ROM type. 4/12/2002
12.Change R209 from 10K to NA to enable AGP faster write.4/12/2002
13.Change R212,R213,R215,R218 from 10K to NA to enable the default device of MAP17.4/12/2002
14.Mirror 8P4R resistors at location RP58 for easy layout. 4/12/2002
15.Update Hardware Trap table for SIS692 in page 17. 4/12/2002
16.Change net from +3VCC to VDDQ at loctation C161,C162,C163,C164,C165 for add VDDQ bypass.4/12/2002
17.Change net of DDR damping resistors at loctation RP11,RP13,RP15,RP17,RP19,RP21,RP23,RP25,RP27,RP29,RP31,RP33,RP35 for easy layout.4/12/2002
18.Change net of AGP pull up resistors at loctation RP48 foreasy layout .4/12/2002
19.Add AGP pull up resistors at loctation R520~R528 and delete RP49 for easy layout .4/12/2002
20.Update Hardware Trap table for SIS645DX/650 in page 7. 4/15/2002
21.Change net of DDR thermination resistors at loctation RP12,RP14,RP16,RP18,RP20,RP22,RP24,RP26,RP28,RP30,RP32,RP34,RP36 for easy layout.4/15/2002
22.Change resistors value from 10K to NA for MAP17 default 2M X 32 DDR SDRAM support at loctation R187,R191,R192,R194. 4/12/2002
23.Change resistors value from 1K 5% to 1K 1% at loctation R172. 4/15/2002
24.Correct the LVDS signals of channel 2 (page 11) . 4/15/2002
25.Change LAN PHY from ICS1839 to ICS 1839AF. 4/16/2002
26.Change net H8_PWROK from H8 pin A4 to P51 for Jimmy request . 4/16/2002
27.Update B TO B connector from 50 pin to 70 pin at location PJ1. 4/16/2002
28.Update Quick Key board connector from 10 pin to 20 pin at location J22. 4/16/2002
29.Add THERM_ADM# net from ADM1032 to H8(add R533,R532,Q29) . 4/16/2002
30.Add NET of WIRE_LED# from MINI PCI to J22. 4/16/2002
31.Change CRT_DDA,CRT_DDCK pull up voltage from +5VS to +3VS . 4/16/2002
32.Change capacitors value from 100P to 22P at location C483,C486,C487,C494,C503 for USB. 4/16/2002
33.Disconnect USB_OC#5 to R359 pull up to +3V and delete unuse parts of R361,R362 for USB5 pair pull low 15K . 4/16/2002
35.Correct the signals name from AD[0..31] to PCI_AD[0..31] . 4/16/2002
36.Delete unuse parts of Q18,R482 . 4/16/2002
37.Add AC-Link signals in Mini-PCI (For MDC) . 4/16/2002
38.Connector MINI PCI pin 21 to PCI_REQ3# ,pin22 to PCI_GNT3#, pin43 to IDSEL AD22 and pin121 to RI for costumer request. 4/16/2002
39.Mirror chock at location 157,158 for easy layout. 4/16/2002
40.Correct the PCI_DEVID3 from MAP17 pin AC3 to pin AB3 . 4/17/2002
41.Change MD_PD pull up voltage from +3V to +3VS at location R229 . 4/17/2002
42.Change DIRECT pull up voltage from +3VS to 1394VCC3 at location R455 . 4/17/2002
43.Add by pass 10U capicator for 1394VCC3 at location C661 . 4/17/2002
44.Change PCI1410 CORE and PCI voltage from +3VS to CBVCC3. 4/17/2002
45.Add by pass 10U capicator for PCI1410 CBVCC3 at location C662 . 4/17/2002
46.Change MAP17 VDDAGP netname from +1.5VS to VDDQ at pin AG14,AK14,AG17,AK17,AG20,AK20,AK23,AK26,AK29,AF30. 4/17/2002
47.Remove Side Band bus from NB and MAP17.4/17/2002
48.Add THRMTRIP# pull up resistor to VCCPVID at location R539 . 4/17/2002
49.Change X2 value from NA to 27MHZ and change X3,C311,C312 to NA. 4/17/2002
50.Remove unuse resistor at location R148.4/17/2002
51.Add net COVER_SW# to B to B connector . 4/17/2002
50.Remove dumping resistors of LAN MII TX signals at location R299,R301,R303,R307.4/18/2002
52.Change turn on main power net from SUSB# to MAINPWR(H8 P40 pin49) and delete unuse part of Q26. 4/18/2002
53.Update Hardware Trap table for M650 Panel ID in page 17. 4/17/2002
54.Add pull up resistor for MAINPWR at location R540 . 4/17/2002
55.Rename USB0VCC5 to USB2VCC5 at USB2 pair voltage net name . 4/17/2002
56.Add by pass 10U capicator for AGP VDDQ at location C663 . 4/17/2002
57.Delete R147 and connect VDDFBIO to VDD_MEM2.5 . 4/22/2002
58.Change AGP bus pull up voltage from +1.5VS to VDDQ at location RP48,RP50,525~R528 . 4/22/2002
59.Creat TV_COMP net to support AV output.(Add C554,C665,C666,D29,L83 and delete R113) . 4/22/2002
60.Connect AGP VDDQ net to +1.5VS for easy layout. 4/22/2002
61.Change R533 pull up voltage from +5V to +3V.4/22/2002
62.Delete duplicate capicator of CARS_RI# signa at location C555 . 4/22/2002
63.Connect +12VS,+3VS,+3v,+5V,DVMAIN to PJ1 BTB connector. 4/22/2002
64.Remove unuse net USB_OC#5 at BTB connector . 4/22/2002
65.Add +5VS connect to BTB connector (pin44) . 4/23/2002
66.Change ISA pull up resistors from 4.7K to 10K at location RP40~RP46.4/23/2002
67.Delete R470,R474 and connect CLKRUN# to PC83793 pin6.4/23/2002
67.Delete R473 and disconnect SUS_STAT# to PC87393.4/23/2002
68.Add pull up 10K resistor for ROMCS# signal at location R451. 4/23/2002
69.Connect +5VS to PJ1 pin34. 4/24/2002
70.Connect DVMAIN to PJ1 pin32. 4/24/2002
71.Mirror L69,L71,L73,L75 for easy layout. 4/24/2002
72.Change CRT_IN# pull up voltage from +3VS to +3V at location R233.4/24/2002
73.Add 10U capacitors for +2.5V_DDR at location C667~C671. 4/24/2002
74.Change PCI_REQ1# pull up resistor from RP37 to R542. 4/24/2002
75.Change R334 from 4.7K to NA. 4/24/2002
76.Delete R326 and change the connect pin of MPCIACT# from SIS962 pine E5 to T8.4/24/2002
77.Delete R325 and change the connect pin of SPK_OFF from SIS962 pine C4 to U4.4/24/2002
78.Change AGP_STOP# and AGP_BUSY# vpull up voltage from +3VS to +1.5VS .4/25/2002
79.Add MIC connector in M/B at location J30 . 4/25/2002
80.Connect the net of AGP_STOP# to SIS962 pin E5 through series diode at location D30.4/24/2002
81.Change the net of CPUPERF# through series diode at location D31 to SIS962 pin A16.4/24/2002
82.Add reserve resistor R544 to connect SUSC# and H8_SUSU for debug only. 4/24/2002
83.Change R359 value from 10K to NA .4/24/2002
84.Updata Hardware strap table in sheet 17 to change USB_OC#5(South bridge debug mode) disable status from Hi to Low .4/28/2002
85.Add pull up resistor for the net of ROMCS# at location R541. 4/24/2002
86.Delete the unuse parts at location R475 and TP48. 4/24/2002
87.Delete R473 and disconnect the net of SUS_STAT# to SIO pin 7. 4/24/2002
88.Delete R474 and connect CLKRUN# to SIO pin6. 4/24/2002
89.Change the connection of MINI PCI RI from WAKE_UP# to H8 RI(pin48). 4/24/2002
90.Add pull up resistor for USB_OC#5 at location R577. 4/28/2002
91.Change R261 value from 33 ohm to NA .4/28/2002
91.Change pull up voltage of MPCIACT# from +3V to +3VS.4/28/2002
92.Change the connection of C567 from LAN_GND to GND for easy layout.4/28/2002
93.Connect the net of GPIO11 to X8 through series resistor at location R543.4/24/2002
94.Change the net name of J11(1394 Connector) GND from 1394GND to 1394CAS_GND for easy layout.4/28/2002
95.Add pull up resistor for the net of LPS at location R558. 4/28/2002
96.Delete unuse bypass capacitors at location C13,C14,C15,C16,C44,C59,C41,C58,C63,C57,C56,C55,C54,C53,C51,C221,C359,C358,C259,C262,C253,C274,C228,C237,C236,C247,C266,C130. 4/24/2002
97.Change R328 value from 0 ohm to NA .4/29/2002
98.Change R296 value from 0 ohm to NA and R305 from NA to 0 ohm .4/29/2002
99.Change R367 value from NA to 432 1% ohm .4/29/2002
100.Change R395 value from 0 ohm to NA and R394 from NA to 0 ohm .4/29/2002
101.Delete Q3 and connect WIR_LED# to MINI PCI pin 13 through a series resistor R559.4/29/2002
102.Add Q32,Q33 to switch SMBUS and spreat SB (SMBUS signals) at S3 status.4/29/2002
103.Change G gate voltage from +3VS to +5VS at location Q19 .4/29/2002
104.Add JO37~JO40 at 1394 output signals for ESD.4/29/2002
105.Add JO41 at MIC signals for ESD.4/29/2002
106.Change the connection of C638 from H8 RI#(pin 48) to PCI1410 MF2(pin 64) .4/29/2002
107.Correct the Foot Print of RJ45 connector .4/29/2002
108.Correct the Foot Print of PS2 connector .4/29/2002
109.Change AGP_DEVSEL# pull up from RP48 pin 3 to pin 7 for easy layout.4/29/2002
110.Change AGP_RBF# pull up from RP48 pin 2 to pin 6 for easy layout.4/29/2002
111.Add Q34,R560,R561 to shift level and connect the new net of PSON#_H8 to H8 pin21 .4/29/2002

Rename reference. 4/30/2002

112.Change Resistors value from 51ohm 5% to 49.9 ohm 1% at location R89,R611,R667,R673,R674,R679,R680,R681.5/2/2002
113.Change R106,C112,OSC501,C706 value to N/A.5/2/2002
114.Change C128,c126 from NA to 10P.5/2/2002
115.Change X2 value to NA.5/2/2002
116.Change L11,C554,C557,C556 value to NA.5/2/2002
117.Change F501value from NA to SMDC110 ,D503 from NA to EC11FS2 and C501 from NA to 10U.5/2/2002
118.Change R614 from 147 ohm 5% to 150 ohm 1%.5/3/2002
119.Change R731 from 5.6K ohm to 4.7K ohm.5/3/2002
120.Change R639~R642 from 56.2 ohm to 56 ohm.5/3/2002
121.Correct Footprint from 0603D_DFS to 0603D at location R761,R736,R740,R742 .5/3/2002
122.Change C853~C872 value from 1000P to 0.1U 5/6/2002
123.Change C877,C891~C893 value from 0.015U to 0.1U 5/6/2002
124.Change the value from 49.9 ohm 1% to 51 ohm 1% at location R611,R645,R648,R650,R653,R663,R667,R670,R673,R674,R679,R680,R681,R89. 5/6/2002
125.Change the value from NA to 27P at location C674,C675. 5/6/2002
126.Change the value from NA to 25MHZ at location X505. 5/6/2002
127.Change the value from 0 ohm to NA at location R697. 5/8/2002
128.Change the value from 10K ohm to NA at location RP507. 5/9/2002
129.Change the value from NA to 10K ohm at location R170. 5/9/2002
130.Change the value from 8.2K to NA at location R150, R147. 5/9/2002
131.Change the value from 10K 5% to 10K 1% at location R77,R72. 5/9/2002
132.Change the value from NA to 10K at location R174. 5/9/2002
132.Change the value from NA to 0 at location R184. 5/9/2002
132.Change the value from 0 to NA at location R185. 5/9/2002
132.Change the value from 22P to NA at location CP503,CP504,CP505,CP506. 5/9/2002

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R00 TO R0A

1.Delete the necessary pull up resistor of ADM1032 at location RP507.
2.Install R94 to pull up Test_Hi12(DPSLP#) at DT mode.
3.Change the PCB Footprint from 1812 to 1210 at location C693,C696.
4.Support 300mA VCCPVID output to add parts of U520,R850,C904,C905,L359,C903.
5.Changed the resistance from 150ohm 1% to 49.9ohm 1% for DDRVREFA/B at location R98,R108,R750,R745.
6.Reserved +1.25V_REF to provid DDRVREF at location R823,R248,R825.
7.Changed the resistance from 1Kohm 1% to 49.9ohm 1% for +DDRVREF at location R807,R812.
8.Change the PCB Footprint from 0603D_DFS to 0603D for M650 LCD_ID at location R736,R740,R742.
9.Change the PCB Footprint from 0603D to 0603D_DFS at location R578.
10.Add 10K resistors R838~R845 and delete R615,R60,R75,R634,R618,R58,R71,R635 for modify MAP17 RAM_CFG strap circuit (refer page 10.11).
11.Change the pull up voltage of AGP_BUSY# signal from +1.5VS to +3VS.
12.Disconnect U6 pinAG10 and pull up to +3VS.(R591,N_AGP_STOP#)
13.Changed the voltage of MAP17 IFP0IOAVDD from +2.8VS to A3V.(L16 pin1)
14.Change resistors value to NA at location R38,R568 that no connect SM530 REFOUT.
15.Change resistors value from NA to 10K at location R636,R62 for correctly MAP17 ROM TYPE.
16.Change resistors value from 10K to NA at location R637,R83 for correctly MAP17 ROM TYPE.
17.Correct S-VIDEO pin connection that pin5 connect to TV_LUMA and pin7 connect to TV_CRMA.
18.Change resistors value from 100K to 10K at location R501 for CRT_IN# signal.
19.Correct FSB SELECT circuit .(refer page13)
20.Correct DDR CLOCK buffer BF_OUT layout.
21.Changed capacitor value from 10P to NA at location C829.(BF_OUT)
22.Delete the necessary pull up resistor of S3AUXSW# at location R115.
23.Add R115,R192 0ohm/NA to disconnect pull up to +3VS of P_INIT#,P_STB#.
24.Change resistors value from NA to 8.2K to meet AGP specification at location R150,R147 for AGP_ADSTB0#,AGP_ADSTB1#.
25.Changed capacitor value from 22U to 10U at location C132 and add 10U capacitor at location C254 for ME issue.(AUXOK)

27.Changed the USB pair signal to J10 from USB2 to USB4 to support USB boot function.
28.Connect unused USB pair pull low(10K) of USB2 at location R127,R130 and pull up USB_OC#2 to +3V at location R153.
29.Change resistor value from NA to 10K to disable debug mode of USB_OC#4.
30.Changed the BEAD value from NA to 120ohm at location L29 for USBPVDD.
31.Changed the resistor value to 0ohm for IDE busd.(refer page18)
32.ADD SIORDY pull up +5VS(R196),IRQ15 pull low (R197) and SDDREQ pull low (R198).
33.Connect PJ1 pin 28 to +5VS for power team requist.
34.Add DFS parts for EMI request at location JS510,JS511.
35.Changed LAN transformer from LF-H80P to LF_H41S.
36.Reserved pull up resistor for 1394 LPS signal at location R152.
37.Changed USB connector for ME request.
38.Add Q5,R60,R109 to correct WIR_LED# circuit.(refer page 23)
39.Add R193 that pin1 connect to J503 pin 116(MINI PCI socket)and pin 2 connect to MODEM_SPK.
40.Connect J503 to GND for CODEC ID0#.(R194)
41.Add R75 for WIRE_LED.
42.Add R170 for WIRE_LED#.
43.Add J24,D3,Q12 for system second FAN.
44.Add R161,Q512 and changed resistors value from 10K to 470 ohm at location R169,R170 to correct ADM1089 THERM function.
45.Add R831,R169,Q510 to correct CPU THERMTRIP function.
46.Changed capacitor from 10U 1210 to 10U 1206 at location C241,C242,C243,C245,C244,C213,C216,C847.
47.Changed C92 from 22U 1210 to 10U 1206 and add C902 10U 1206 for clock generator +3VS for ME issue.
48.Add 10U 1206 capicators for MAP17 +1.2VS at location C896,C897,C898.
49.Add 100K pull low resistor for PWROK signal at location R826.
50.Change part from RSL4148 to EC10QS03L at location D515.
51.Delete necessary parts of Q12,Q13(2N7002).
52.Changed USB signal damp resistors from 22 ohm to 0 ohm.(refer page 17)
53.Changed USB signal by pass capacitors value from 22P to NA.(refer page 17)
54.Delete USB signal pull low resistors value from 15K to NA.(refer page 21,23)
55.Add 0.1U capatitor at location C252 that pin 1 connect to U12 pin62(CB1410 SPKR_OUT#) and pin2 connect to CARDSPK#.
56.Rename R799 to RT1.
57.Delete MIC connector from M/B.(J12)
58.Correct MINIPCI_RI circuit.(refer page24)

R0A -> R0B(Only modified artwork from PCB vendor)

1. Change +1.25V power source from +3V to +3VS. for saving S3 power consumption (refer page25)

R0B -> R01

1.Change Fan lie to stand(refer page24)
2.It disabled the I2C function and can also reduce the S3 resume time,add 4 2.2k ohm to +5vs(refer page11)
3.Change Diode D507,D515 footprint(refer page16)
4.Reserve 0.1uF in Q503 B, E, it will avoid H8 reset when Power off.(refer page24)
5.Change C252 from 0.1uF to 0ohm in BOM (Page 19)
6.Change R192 (Page 23) from 0ohm to 0ohm/NA [In BOM],Add R403 (Page 23) 0ohm connect to PJ1 (Page 18) Pin 54.
7.Add three 0.1uF Cap.(C901,C902,C913) for Mini-PCI +5VS.
8. PJ1,J19 change PCB Footprint
9.It will avoid LED blinking.(refer page12)

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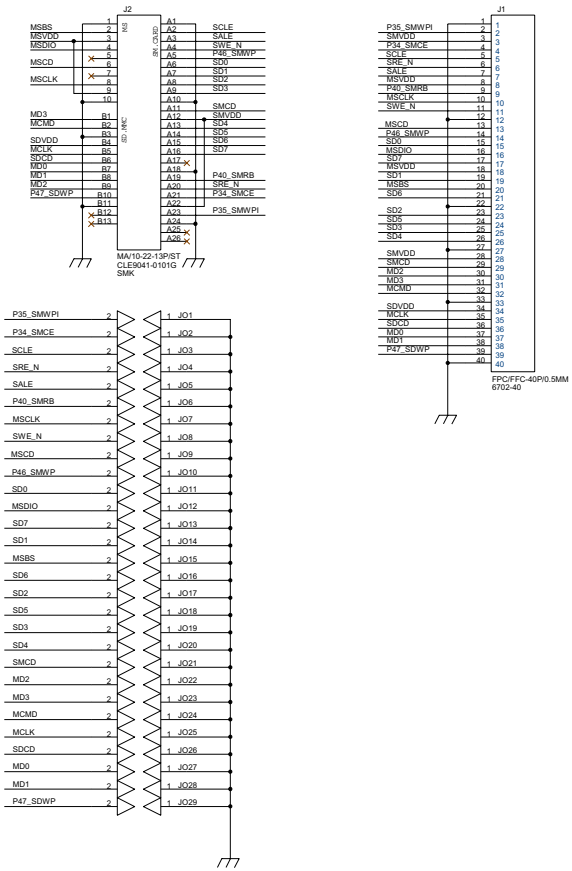
8640 FPC R01



Title	8640 FPC
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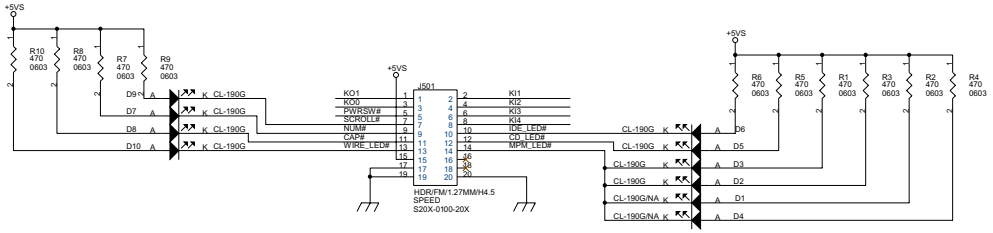
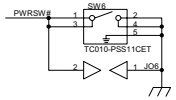
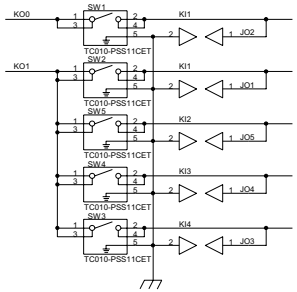
8640 EASY BUTTON BOARD



PWR BUTTON



MPM BUTTON



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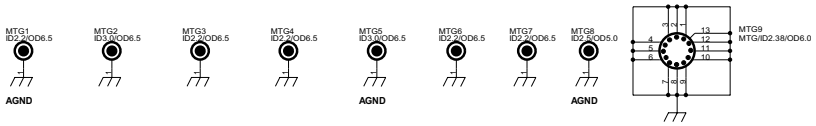
Title: 8640 EASY START BOARD

Size | Document Number | Rev 00

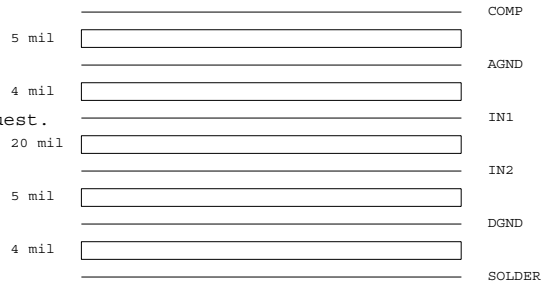
Date: Thursday, June 27, 2002 Sheet 1 of 1

MODEL : 8640 Card Reader/Audio/Touch Pad Board Revision 00

Contexts



1.Correct SM/MS pull up voltage to +3V.
2.Correct W27C512 VCC from +5VS to +5V.
3.Change th connection of 24C02 pin8 from +3V to GND to disable write portec.
4.Change the pin assigment of J1 for ESD solution.
5.Delete SW1 and SW4.
6.Change the TOUCH PAD connect from 6 pin to 12 pin at location J501.
7.Add damping resistors for Card Reader signals at location R513~R516.
8.Add Audio Code clock select function at location R70,R71.
9.Add 10K/NA resistor connect to GND of 14.318MHZ_AUDIO net at location R517for EMI request.
10.Delete capicators for ALC2002 at location C36,C39,C55.
11.Change resistance from 200K to 200K/NA at location R54,R55 to disable BEEP function.
12.Change bead to DFS type at location L5o1~L504.
13.Change the connection of Q2 poin2 from Q504 pin3 to +3VS
14.Delete R57.
15.Add 0 ohm resistor at location R72.
16.Change the part of VR501.



DRAW	DESIGN	CHECK	ISSUED

MiTAC

Title: COVER SHEET & HISTORY

Size | Document Number: 411673400002 | Rev: 00

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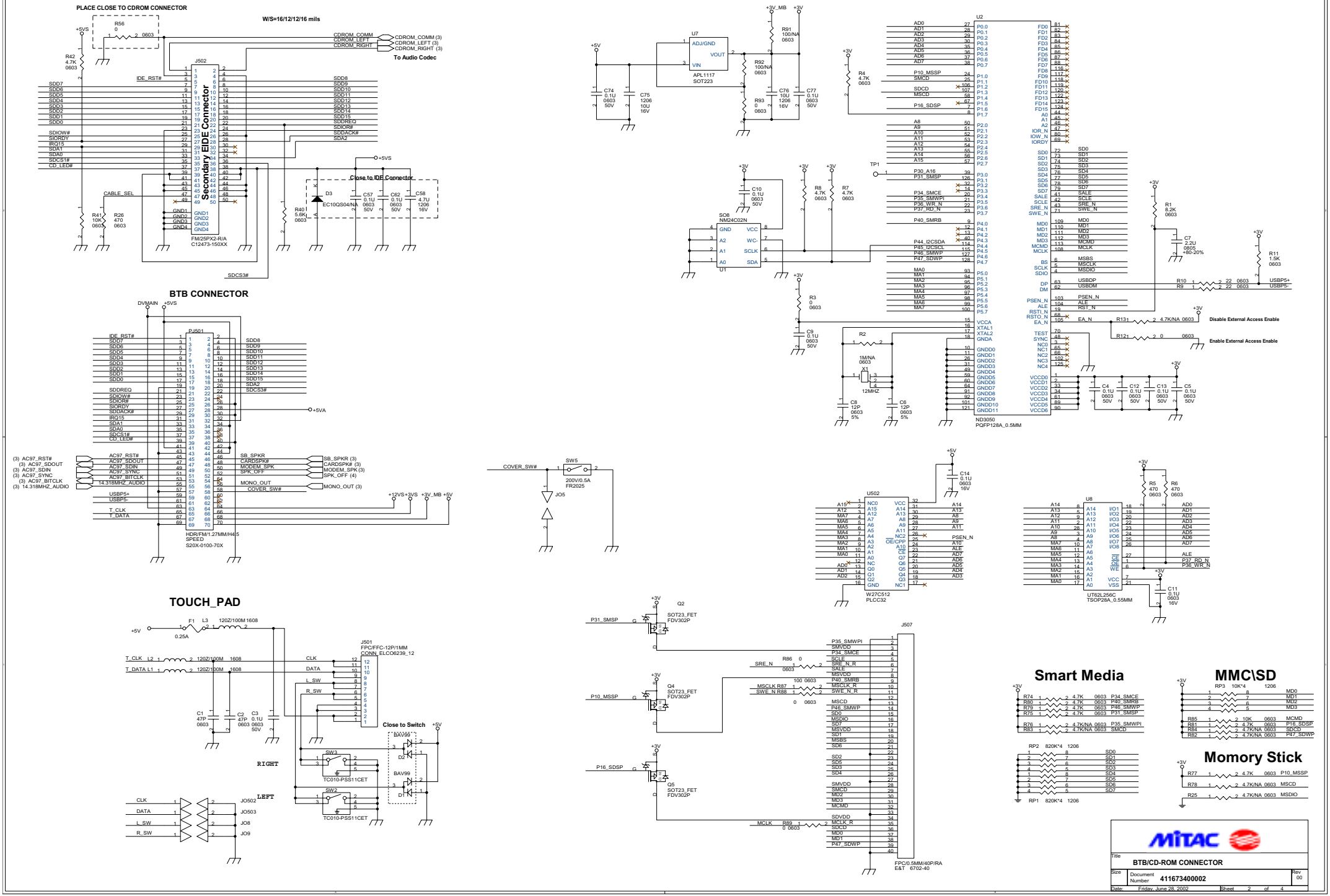
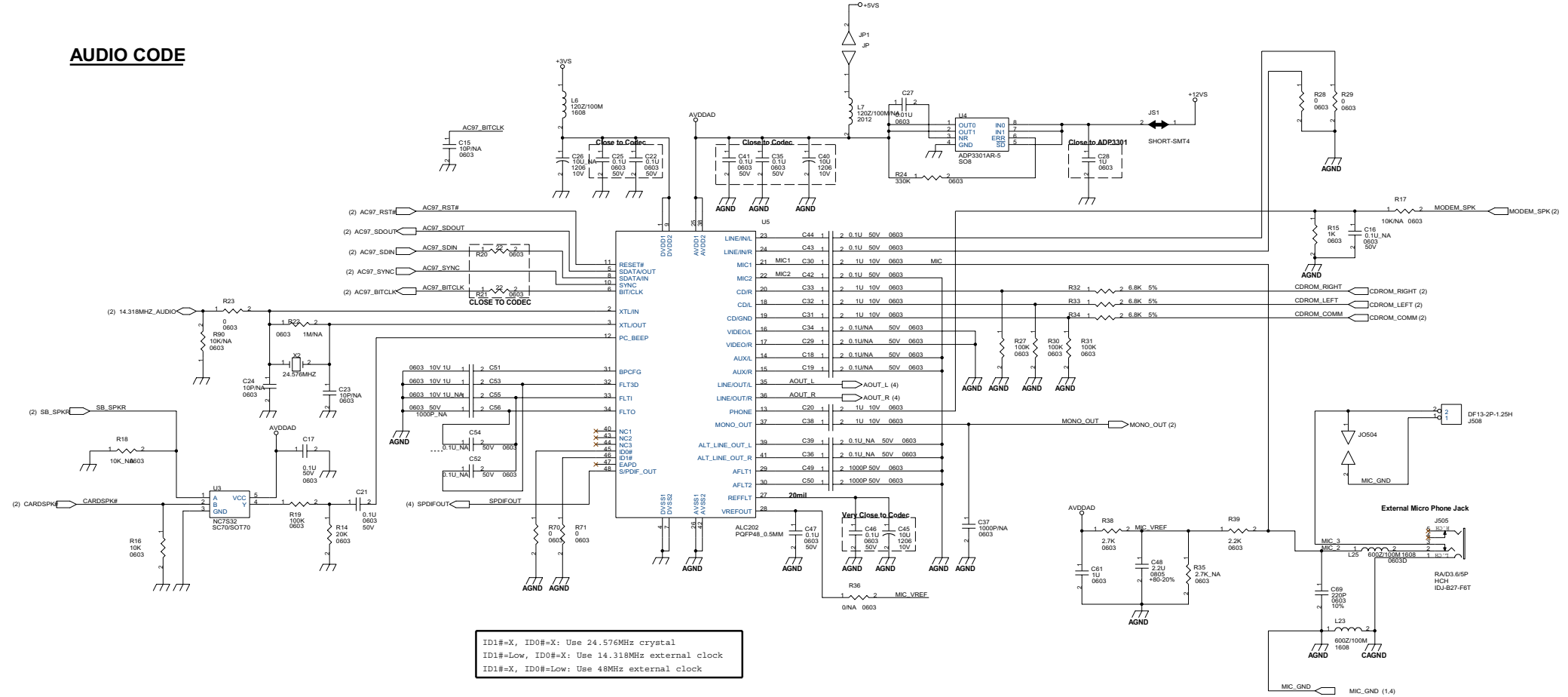


AUDIO CODE



ID1#=X, ID0#=X: Use 24.576MHz crystal
ID1#=Low, ID0#=X: Use 14.318MHz external clock
ID1#=X, ID0#=Low: Use 48MHz external clock

Title	AUDIO CODEC		
Size: Custom	Document Number: 411673400002		Rev: 00
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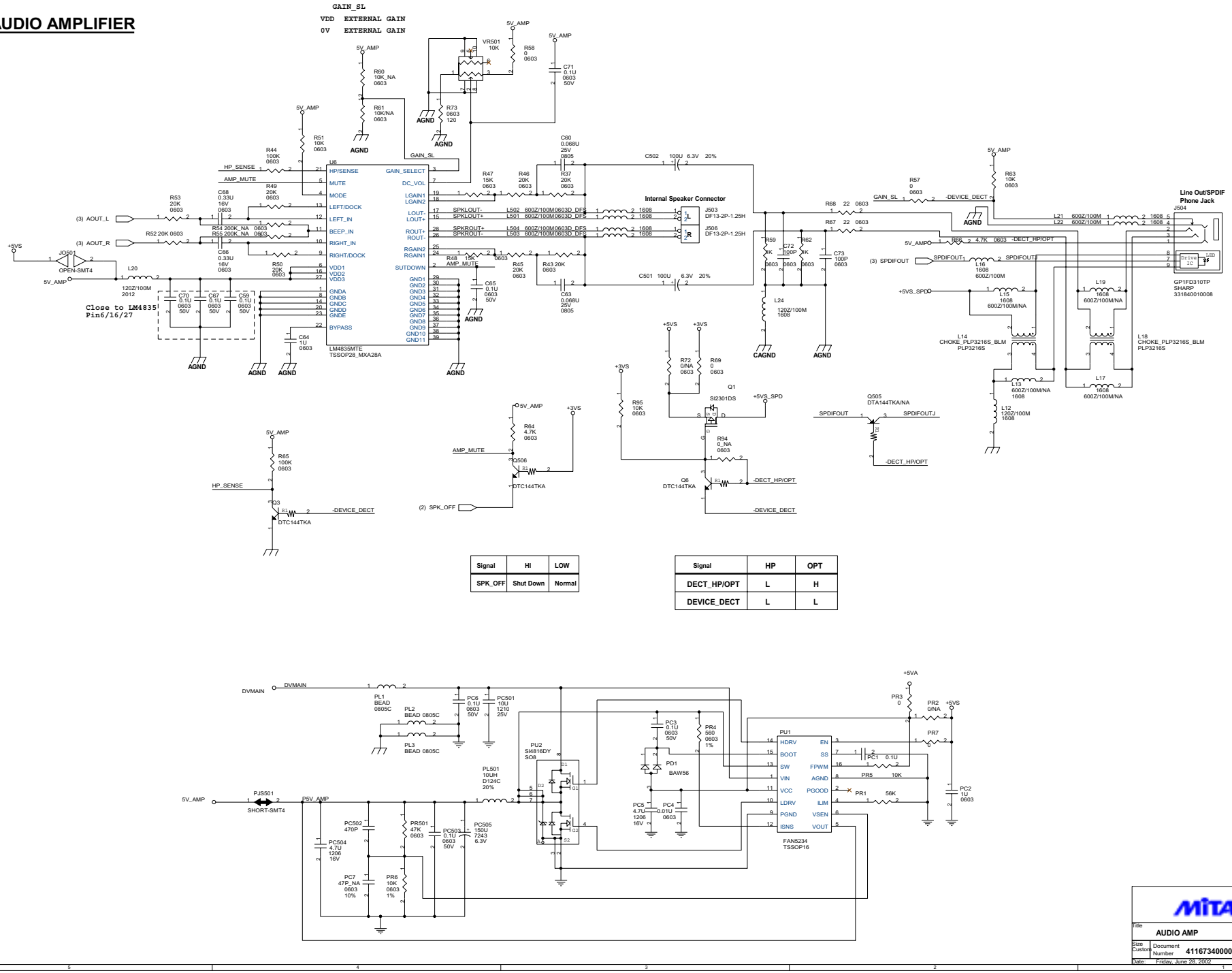
AUDIO AMPLIFIER



Signal	HI	LOW
SPK_OFF	Shut Down	Normal

Signal	HP	OPT
DECT_HP/OPT	L	H
DEVICE_DECT	L	L

Title	AUDIO AMP	
Size: Custom	Document Number: 411673400002	Rev: 00
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