Chapter 17

Winding Capacitance and Leakage Inductance

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Introduction

Operation of transformers at high frequencies presents unique design problems due to the increased importance of core loss, leakage inductance, and winding capacitance. The design of high frequency power converters is far less stringent than designing high frequency, wide-band audio transformers. Operating at a single frequency requires fewer turns, and consequently, there is less leakage inductance and less capacitance with which to deal. The equivalent circuit for a two-winding transformer is shown in Figure 17-1.

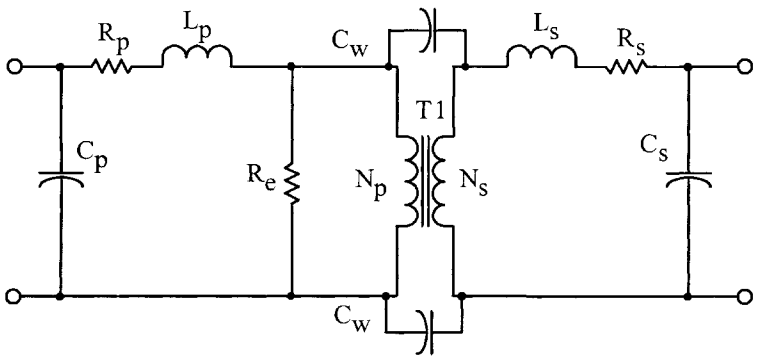

Figure 17-1. Equivalent Transformer Circuit.

High frequency designs require considerably more care in specifying the winding specification. This is because physical orientation and spacing of the windings determine leakage inductance and winding capacitance. Leakage inductance and capacitance are actually distributed throughout the winding in the transformer. However, for simplicity, they are shown as lumped constants, in Figure 17-1. The leakage inductance is represented by, L_p for the primary and, L_s for the secondary. The equivalent lumped capacitance is represented by, C_p and C_s for the primary and secondary windings. The dc winding resistance is, R_p, and R_s is for the equivalent resistance for the primary and secondary windings. C_w is the equivalent lumped, winding-to-winding capacitance. R_e is the equivalent core-loss shunt resistance.

Parasitic Effects

The effects of leakage inductance on switching power supplies' circuits are shown in Figure 17-2. The voltage spikes, shown in Figure 17-2, are caused by the stored energy in the leakage flux and will increase with load. These spikes will always appear on the leading edge of the voltage switching waveform.

$$Energy = \frac{L_{(Leakage)}\left(I_{(pk)}\right)^2}{2}, \quad \text{[watt-seconds]} \quad [17\text{-}1]$$

Transformers designed for switching applications are normally designed to have minimum leakage inductance, in order to minimize the voltage spikes, as shown in Figure 17-2. Also, leakage inductance can be observed by the leading edge slope of the trapezoidal current waveform.

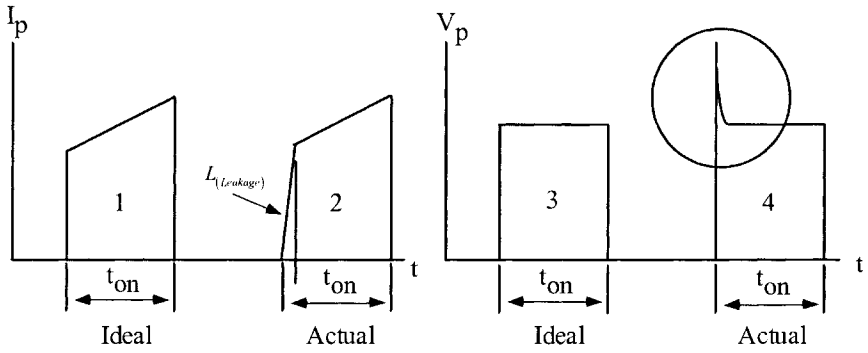

Figure 17-2. Switching Transistor Voltage and Current Waveforms.

Transformers designed for power conversion are normally being driven with a square wave, characterized by fast rise and fall times. This fast transition will generate high current spikes in the primary winding, due to the parasitic capacitance in the transformer. These current spikes, shown in Figure 17-3, are caused by the capacitance in the transformer; they will always appear on the lead edge of the current waveform and always with the same amplitude, regardless of the load. This parasitic capacitance will be charged and discharged every half cycle. Transformer leakage inductance and capacitance have an inverse relationship: if you decrease the leakage inductance, you will increase the capacitance; if you decrease the capacitance, you increase the leakage inductance. These are trade-offs that the power conversion engineer must make to design the best transformer for the application.

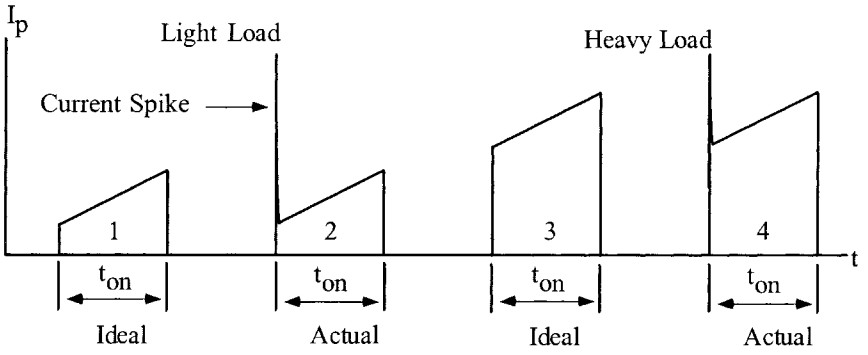

Figure 17-3. Transformer Capacitance Induced Current spike.

Leakage Flux

Leakage inductance is actually distributed throughout the windings of a transformer because of the flux set-up by the primary winding, which does not link the secondary, thus giving rise to leakage inductance in each winding without contributing to the mutual flux, as shown in Figure 17-4.

However, for simplicity, leakage inductance is shown as a lumped constant in Figure 17-1, where the leakage inductance is represented by L_p.

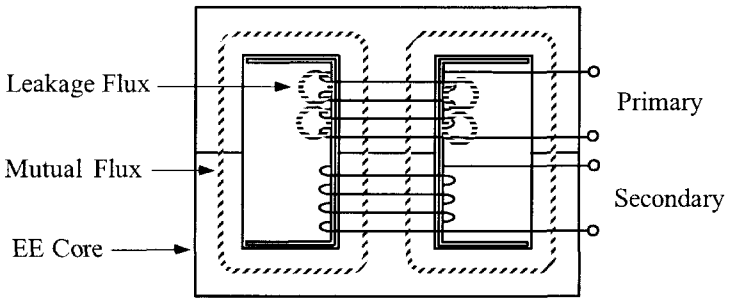

Figure 17-4. Leakage Flux.

In the layer-wound coil, a substantial reduction in leakage inductance, L_p and L_s, is obtained by interweaving the primary and secondary windings. The standard transformer, with a single primary and secondary winding, is shown in Figure 17-5, along with its leakage inductance, Equation [17-2]. Taking the same transformer and splitting the secondary on either side of the primary will reduce the leakage inductance, as shown in Figure 17-6, along with its leakage inductance, Equation [17-3]. The leakage inductance can be reduced even more, by interleaving the primary and secondary, as shown in Figure 17-7, along with its leakage inductance, Equation [17-4]. Transformers can also be constructed using the side-by-side, sectionalized bobbin as shown in Figure 17-8, along with its leakage inductance, Equation [17-5]. The modified three section, side-by-side bobbin is shown in Figure 17-9, along with its leakage inductance Equation [17-6].

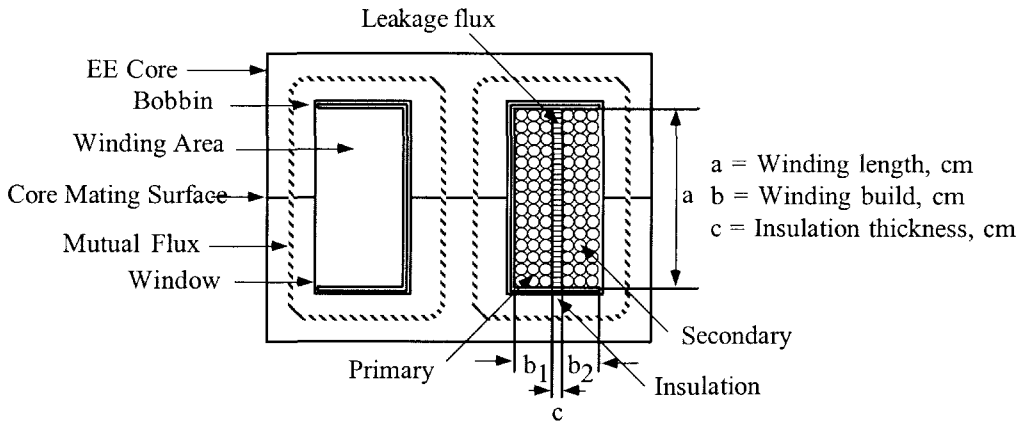

Figure 17-5. Conventional Transformer Configuration.

$$L_p = \frac{4\pi (MLT) N_p^2}{a}\left(c + \frac{b_1 + b_2}{3}\right)\left(10^{-9}\right), \quad \text{[henrys]} \quad [17\text{-}2]$$

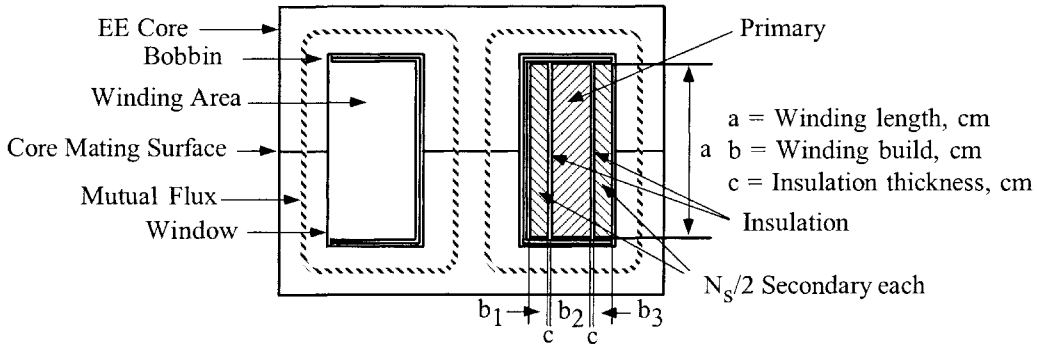

Figure 17-6. Conventional, Transformer Configuration with Simple Interleave.

$$L_p = \frac{\pi (MLT) N_p^2}{a}\left(\Sigma c + \frac{\Sigma b}{3}\right)\left(10^{-9}\right), \quad \text{[henrys]} \quad \text{[17-3]}$$

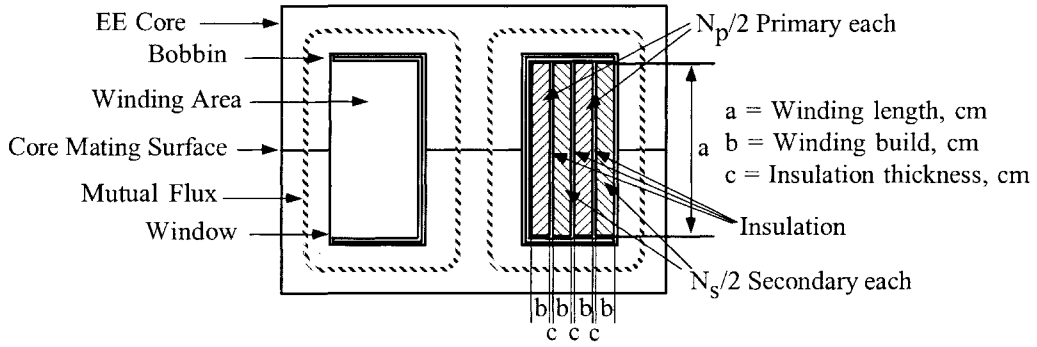

Figure 17-7. Sectionalized, Transformer Configuration Primary and Secondary Interleave.

$$L_p = \frac{\pi (MLT) N_p^2}{a}\left(\Sigma c + \frac{\Sigma b}{3}\right)\left(10^{-9}\right), \quad \text{[henrys]} \quad \text{[17-4]}$$

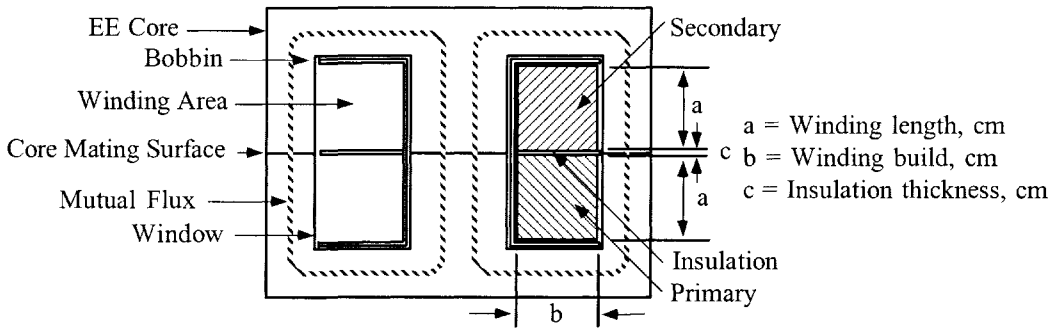

Figure 17-8. Pot Core, Sectionalized Transformer Configuration.

$$L_p = \frac{4\pi (MLT) N_p^2}{b}\left(c + \frac{\Sigma a}{3}\right)\left(10^{-9}\right), \quad \text{[henrys]} \quad \text{[17-5]}$$

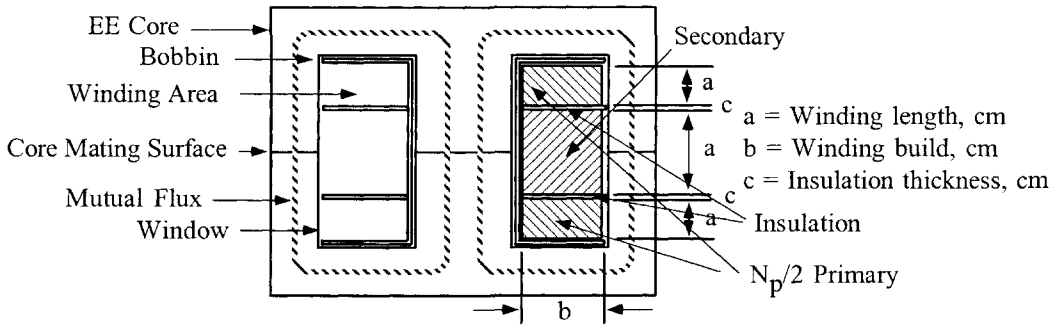

Figure 17-9. Modified, Pot Core Sectionalized, Transformer Configuration.

$$L_p = \frac{\pi (MLT) N_p^2}{b} \left(\Sigma c + \frac{\Sigma a}{3} \right) \left(10^{-9} \right), \quad \text{[henrys]} \quad [17\text{-}6]$$

Minimizing Leakage Inductance

Magnetic core geometry has a big influence on leakage inductance. To minimize leakage inductance, the primary winding should be wound on a long bobbin, or tube, with the secondary wound as close as possible, using a minimum of insulation. Magnetic cores can have identical rating, but one core will provide a lower leakage inductance than the other. A simple comparison would be two cores with the same window area, but one core has twice the winding length. Only half the winding build is shown in Figure 17-10.

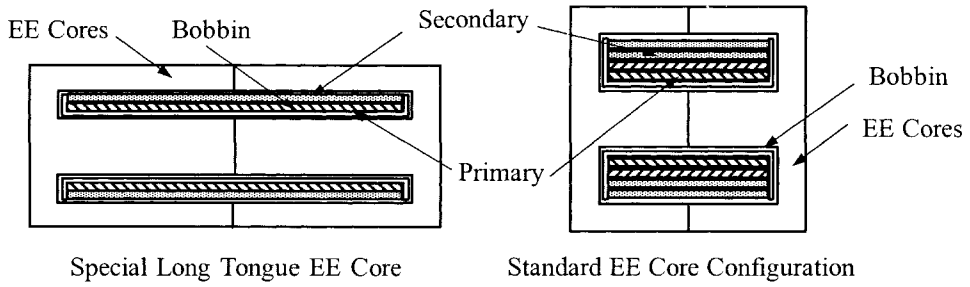

Figure 17-10. Comparing a Standard EE Core and a Special Long Tongue Core.

If layers must be used, the only way to reduce the leakage inductance is to divide the primary winding into sections, and then to sandwich the secondary winding between them, as shown in Figure 17-7. This can pose a real problem when designing around the European VDE specification, because of the required creepage distance and the minimum insulation requirements between the primary and secondary. Minimizing the leakage inductance on a push-pull converter design could be a big problem. A special consideration is required symmetry in both the leakage inductance and dc resistance; this is in order to get a balanced winding for the primary switching circuit to function properly.

The best way to minimize the leakage inductance, and to have a balanced dc resistance in a push-pull or center-tapped winding, is to wind bifilar. Bifilar windings will drastically reduce leakage inductance. This condition also exists on the secondary, when the secondary is a full-wave, center-tapped circuit. A bifilar winding is a pair of insulated wires, wound simultaneously and contiguously, (i.e., close enough to touch each other); Warning: do not use bifilar wire or the capacitance will go out of sight. Each wire constitutes a winding; their proximity reduces leakage inductance by several orders of magnitude, more than ordinary interleaving. This arrangement can be applied to the primary, to the secondary, or, it can be applied to the primary and secondary together. This arrangement will provide the minimum leakage inductance.

Winding Capacitance

Operating at high frequency presents unique problems in the design of transformers to minimize the effect of winding capacitance. Transformer winding capacitance is detrimental in three ways: (1) winding capacitance can drive the transformer into premature resonance; (2) winding capacitance can produce large primary current spikes when operating from a square wave source, (3) winding capacitance can produce electrostatic coupling to other circuits.

When a transformer is operating, different voltage gradients arise almost everywhere. These voltage gradients are caused by a large variety of capacitance throughout the transformer, due to the turns and how they are placed throughout the transformer. When designing high frequency converters, there are several factors that have a control over the turns: (1) the operating flux density or core loss; (2) the operating voltage levels in the primary and secondary; (3) the primary inductance.

Keeping turns to a minimum will keep the capacitance to a minimum. This capacitance can be separated into four categories: (1) capacitance between turns; (2) capacitance between layers; (3) capacitance between windings; and (4) stray capacitance. The net effect of the capacitance is normally seen by the lumped capacitance, C_p, on the primary, as shown in Figure 17-1. The lumped capacitance is very difficult to calculate by itself. It is much easier to measure the primary inductance and the resonant frequency of the transformer or inductor, as shown in Figure 17-11. Then, calculate the capacitance using Equation [17-7]. The test circuit, in Figure 17-11 functions as follows: The input voltage, V1, is held constant while monitoring the voltage, V2, sweep through the frequency with the power oscillator. When the voltage, V2, rises to a peak, and starts to decay at this peak voltage, the transformer or inductor is in resonance. At this point the phase angle is also 0 degrees at resonance when looking at both the curves of V1 and V2.

$$C_p = \left(\frac{1}{(\omega_r)^2 L} \right) = \frac{1}{4\pi^2 f_r^2 L}, \quad \text{[farads]} \quad [17\text{-}7]$$

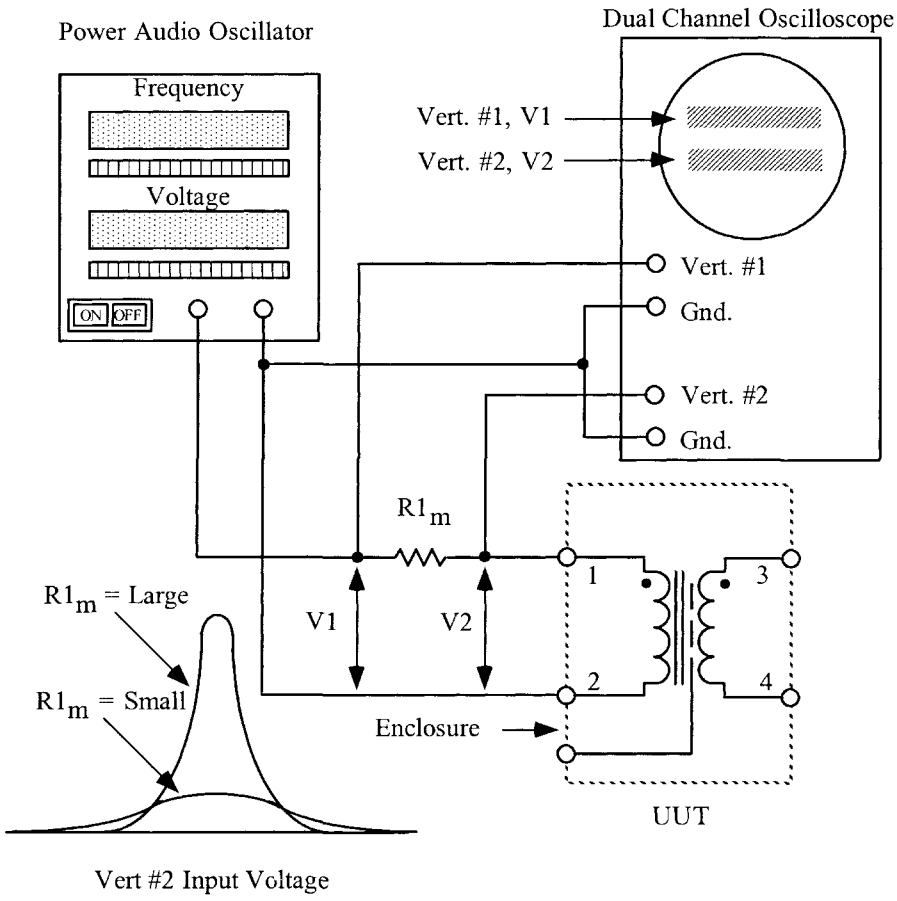

Figure 17-11. Circuit for Measuring either a Transformer or Inductor Self Resonates.

For transformers designed to operate with a square wave, such as dc-to-dc converter, leakage inductance, L_p, and the lumped capacitance, C_p, should be kept to a minimum. This is because they cause overshoot and oscillate, or ring, as shown in Figure 17-12. The overshoot oscillation, seen in Figure 17-12A, has a resonant frequency, f, that is controlled by, L_p and C_p. This resonant frequency could change and change drastically after potting, depending on the material and its dielectric constant, as shown Figure 17-12B.

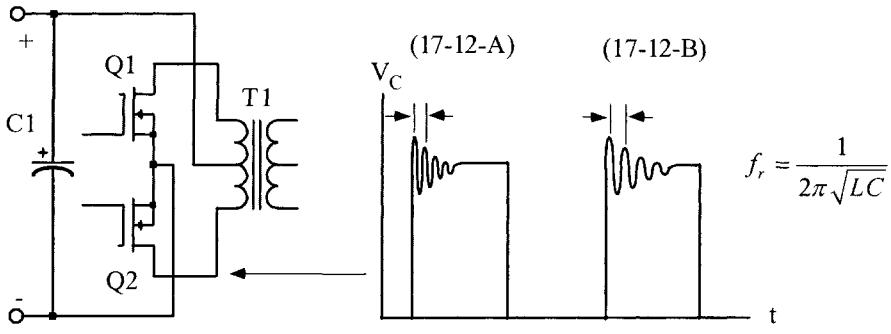

Figure 17-12. Primary Voltage with Leading Edge Ringing.

Winding Capacitance Turn-to-Turn

The turn-to-turn capacitance, C_t,, shown in Figure 17-13, should not be a problem if you are operating at high frequency, low voltage power converters, due to the low number of turns. If the turn-to-turn capacitance is important, then change the magnet wire insulation to one with a lower dielectric constant. See Chapter 4.

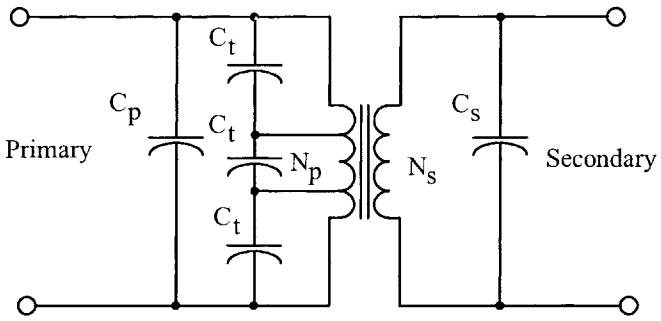

Figure 17-13. Capacitance Turn-to-Turn.

Winding Capacitance Layer-to-Layer

The capacitance between layers on the primary or secondary is the best contributor to the overall, lumped capacitance, C_p. There are three ways to minimize the layer capacitance: (1) Divide the primary and secondary windings into sections, and then sandwich the other winding between them, as shown in Figure 17-7; (2) The foldback winding technique, shown in Figure 17-14, is preferred to the normal U type winding, even though it takes an extra step before starting the next layer. The foldback winding technique will also reduce the voltage gradient between the end of the windings; (3) Increasing the amount of insulation between windings will decrease the amount of capacitance. But remember, this will increase the leakage inductance. If the capacitance is reduced, then the leakage inductance will go up. There is one exception to this rule, and that is, if the windings are sandwiched or interleaved, it will reduce the winding capacitance, but, it will increase the winding-to-winding capacitance.

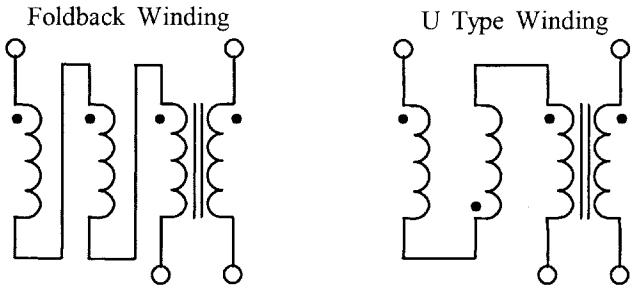

Figure 17-14. Comparing the Foldback to the U Type Winding.

Transformers and inductors wound on toroidal cores can have capacitance problems, just as much if care is not taken in the design at the beginning. It is difficult to control the winding capacitance on a toroidal core because of its odd configuration, but there are ways to control the windings and capacitance. The use of tape barriers to mark a zone for windings, as shown in Figure 17-15, offers a good way to control this capacitance.

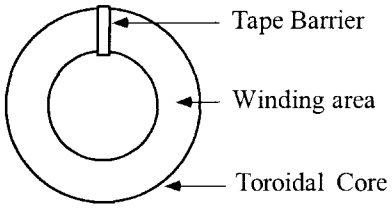

Figure 17-15. Tape Barrier for Winding Toroidal Core.

Another way to help reduce the capacitance effect on toroids is to use the progressive winding technique. The progressive winding technique example is shown in Figure 17-16 and 17-17: Wind 5 turns forward and wind 4 turns back, then wind 10 turns forward and keep repeating this procedure until the winding is complete.

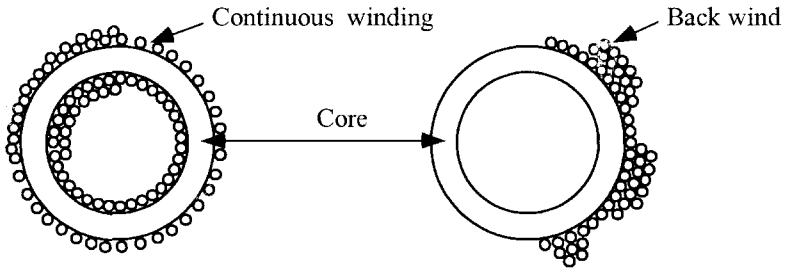

Figure 17-16. Progress Winding Top View.

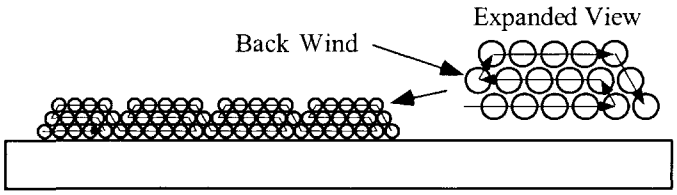

Figure 17-17. Progress Winding Side View.

Capacitance Winding-to-Winding

Balanced windings are very important in keeping down noise and common mode signals that could lead to in-circuit noise and instability problems later on. The capacitance, from winding-to-winding, shown in Figure 17-18, can be reduced, by increasing the amount of insulation between windings. This will decrease the amount of capacitance, but again, this will increase the leakage inductance. The capacitance effect

between windings can be reduced, without increasing the leakage inductance noticeably. This can be done, by adding a Faraday Shield or screen, as shown in Figure 17-19, between primary and secondary windings.

A Faraday Shield is an electrostatic shield, usually made of copper foil. The Faraday Shield is normally added along with the insulation between primary and secondary. In some designs, the Faraday Shield can consist of three independent insulated shields or just one. It all depends on the required noise rejection.

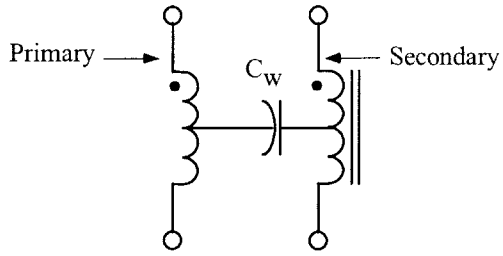

Figure 17-18. Capacitance, C_w, Winding-to-Winding.

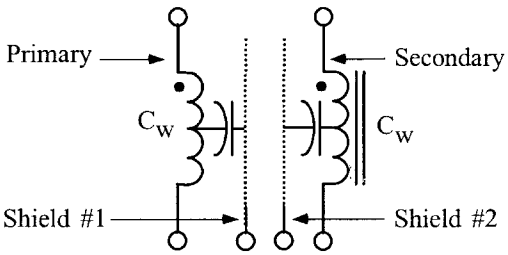

Figure 17-19. Transformer with a Primary and Secondary Shield.

Stray Capacitance

Stray capacitance is very important to minimize because it too, can generate asymmetry currents and could lead to high common mode noise. Stray capacitance is similar to winding-to-winding capacitance except that the capacitance is between the winding next to the core, C_c, and the outer winding next to the surrounding circuitry, C_s, as shown in Figure 17-20. Stray capacitance can be minimized by using a balanced winding, or using a copper shield over the entire winding. A means for measuring leakage current is shown in Figure 17-21. The winding-to-winding capacitance can be calculated, using Equations [17-8] and [17-9].

$$X_c = R1\sqrt{\left(\frac{V_{in}}{V_o}\right)-1}, \quad \text{[ohms]} \quad \text{[17-8]}$$

$$C_x = \frac{1}{2\pi f X_c}, \quad \text{[farads]} \quad \text{[17-9]}$$

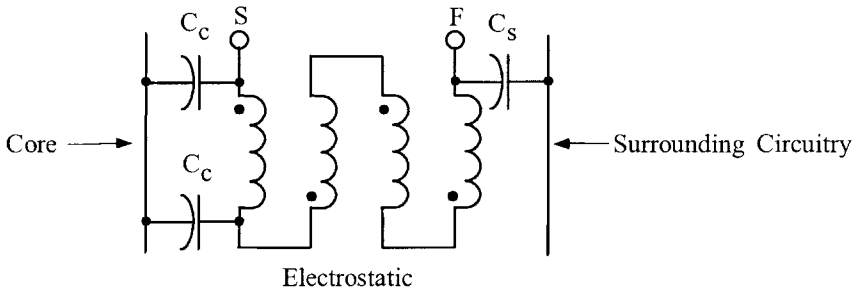

Figure 17-20. Transformer Winding with Stray Capacitance.

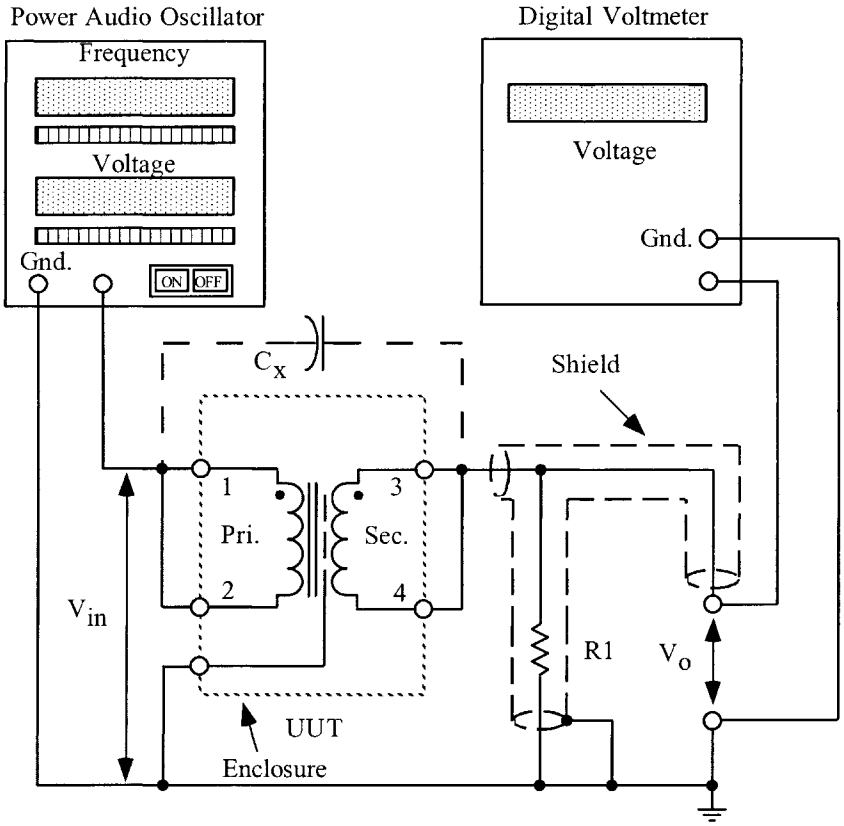

Figure 17-21. Test Circuit for Measuring Primary and Secondary, ac Leakage Current.

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