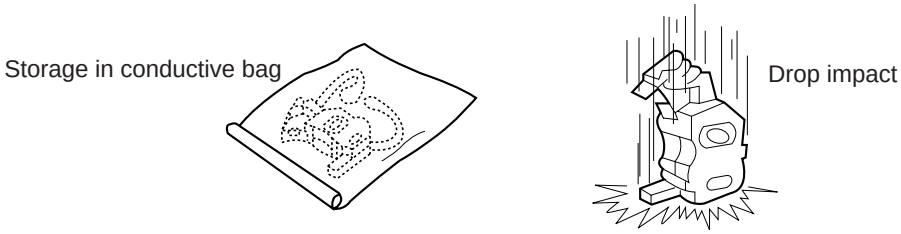
SERVICING PRECAUTIONS

NOTES REGARDING HANDLING OF THE PICK-UP

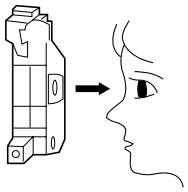
1. Notes for transport and storage

1) The pick-up should always be left in its conductive bag until immediately prior to use.
2) The pick-up should never be subjected to external pressure or impact.



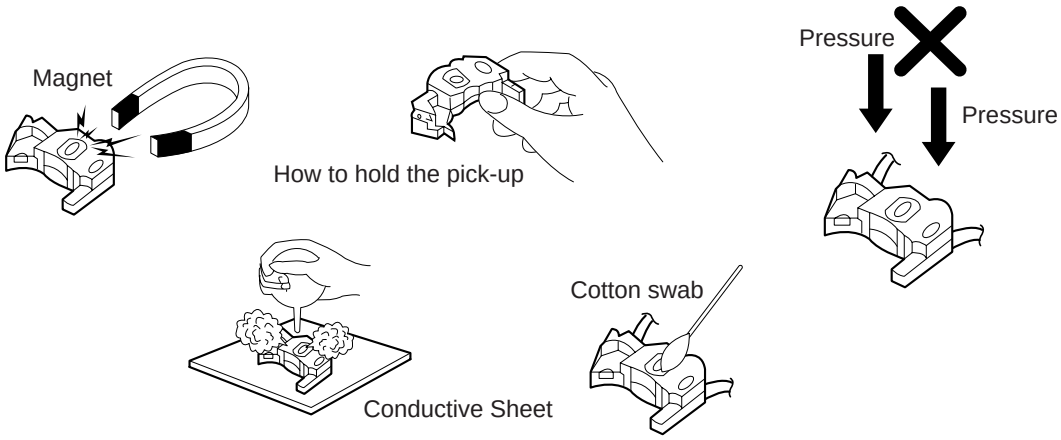
2. Repair notes

1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation screws should absolutely never be touched.
4) Laser beams may damage the eyes!
   Absolutely never permit laser beams to enter the eyes!
   Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.



NEVER look directly at the laser beam, and don¡t˙let contact fingers or other exposed skin.

5) Cleaning the lens surface
   If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.



6) Never attempt to disassemble the pick-up.
   Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

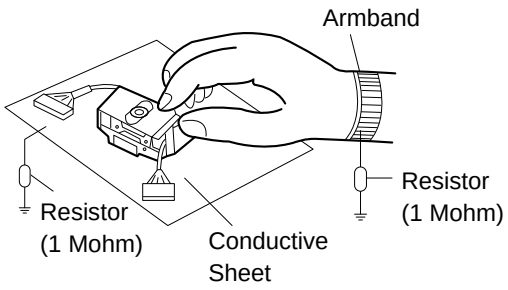
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

1) Before replacing a component part, first disconnect the power supply lead wire from the unit
2) All equipment, measuring instruments and tools must be grounded.
3) The workbench should be covered with a conductive sheet and grounded.
   When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
5) Workers should be grounded by an armband (1MΩ)
6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

ADJUSTMENTS

This set has been aligned at the factory and normally will not require further adjustment. As a result, it is not recommended that any attempt is made to modificate any circuit. If any parts are replaced or if anyone tampers with the adjustment, realignment may be necessary.

1.IMPORTANT

1. Check Power-source voltage.
2. Set the function switch to band being aligned.
3. Turn volume control to minimum unless otherwise noted.
4. Connect low side of signal source and output indicator to chassis ground unless otherwise specified.
5. Keep the signal input as low as possible to avoid AGC and AC action.

2.TUNER ADJUSTMENT

1. Test & Adjustment Points

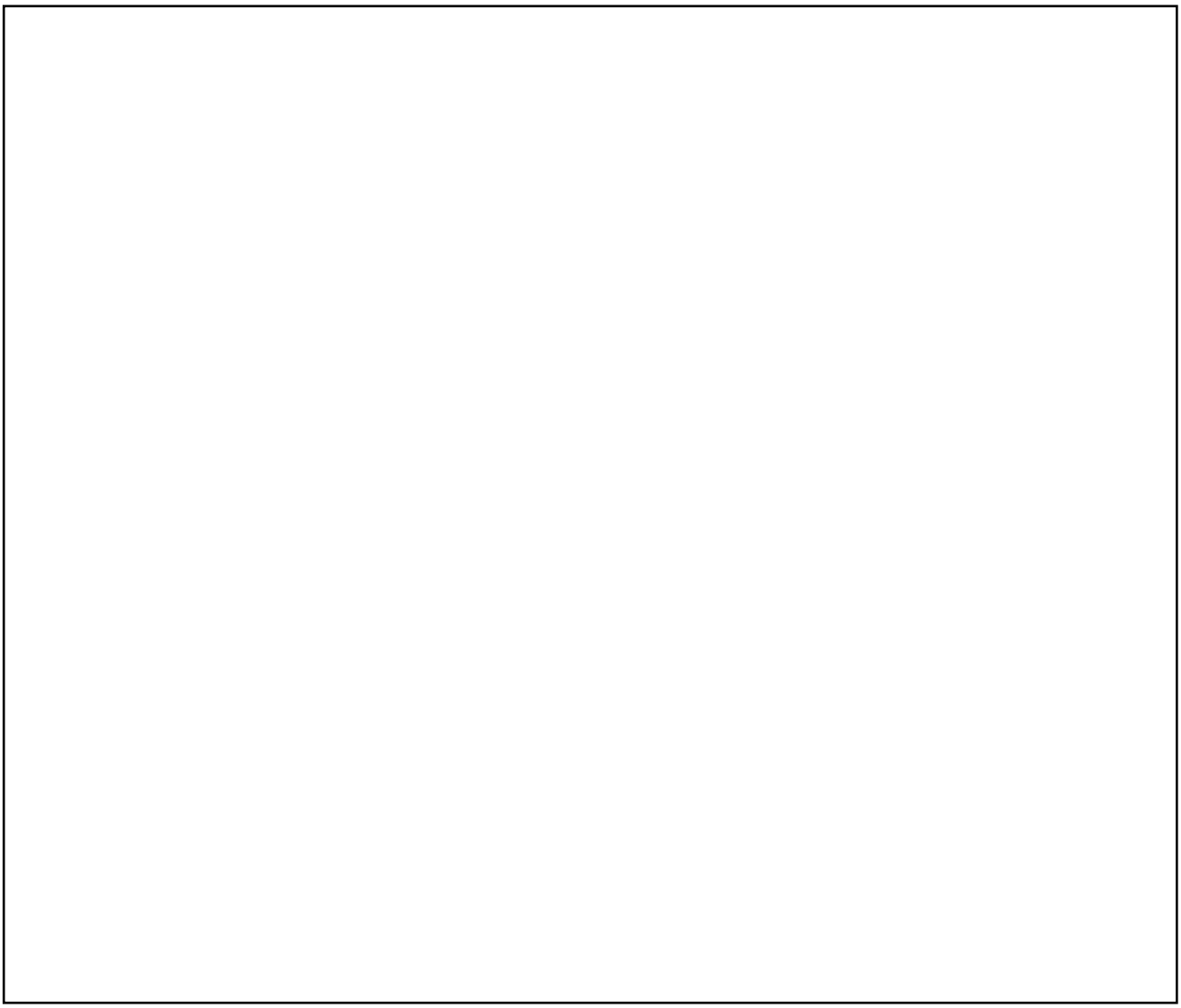


Figure 1. Main P.C. Board

2. AM (MW) IF Adjustment

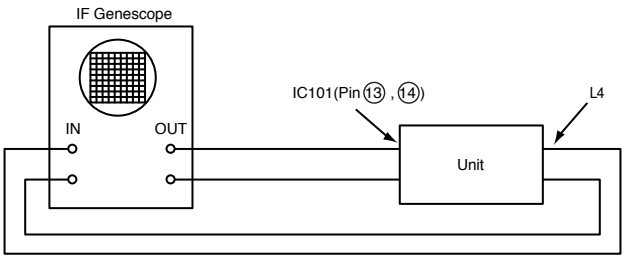


Figure 2.AM(MW) IF Adjustment Connection Diagam

IF	Adjust for	Adjustment
455kHz	Maximum	L7(See figure 3)

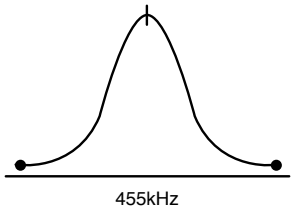


Figure 3.AM(MW) IF Curve

3. AM(MW) RF(Coverage & Tracking) Adjustment

NO	ITem	SG Output	Adjust for	Adjustment
1	Coverage	515kHz	Maximum	L5
2		1,650kHz or 1,710kHz(U.S.A)	Maximum	VC1-3
3		Repeat steps 1 and 2 several times.		
4	Tracking	600kHz	Maximum	L1
5		1,400kHz	Maximum	VC1-4
6		Repeat step 4 and 5 several times.		

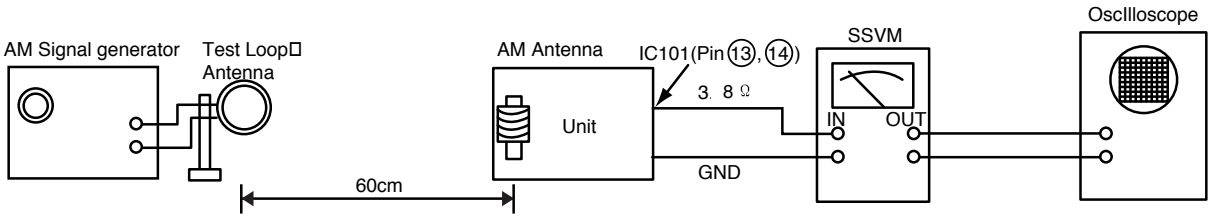


Figure 4.AM(MW) RF Adjustment Connection Diagram

4. FM RF(Coverage & Tracking) Adjustment

NO	ITem	SG Output	Adjust for	Adjustment
1	Coverage	87.35MHz(AX Band:64MHz)	Maximum	L4
2		108.25MHz(AX Band:109MHz)	Maximum	VC1-1
3		Repeat steps 1 and 2 several times.		
4	Tracking	90MHz(AX Band:68MHz)	Maximum	L3
5		106MHz	Maximum	VC1-2
6		Repeat step 4 and 5 several times.		

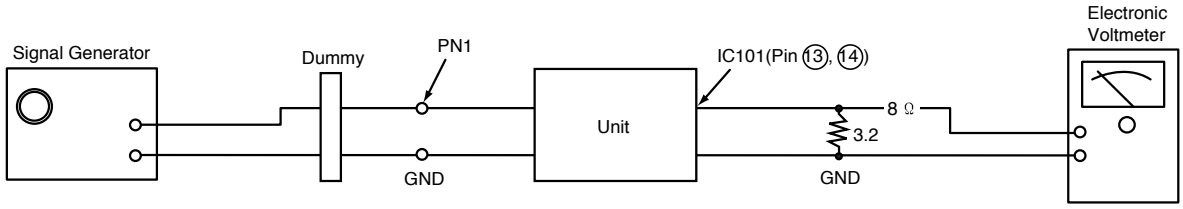


Figure 5. FM RF Adjustment Connection Diagram

3.TAPE DECK ADJUSTMENT

1. AZIMUTH ADJUSTMENT

Deck Mode	Test Tape	Test Point	Adjust for	Adjustment
Playback	MTT-114	L/R Output	R/L Maximum	Azimuth adjusting screw

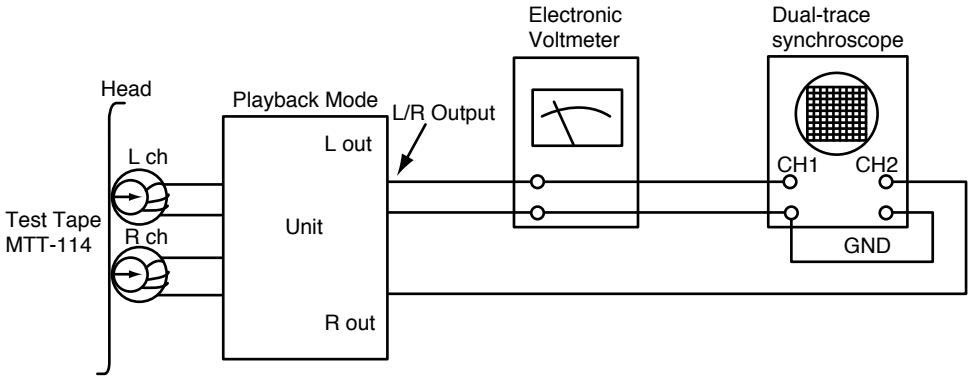


Figure 6. Azimuth Adjustment Connection Diagram

3. RECORD BIAS ADJUSTMENT

Deck Mode	Test Tape	Test Point	Adjust for	Adjustment
Rec/Pause	MTT-5511	Q140 EMITTER	71kHz±0.2kHz	L140

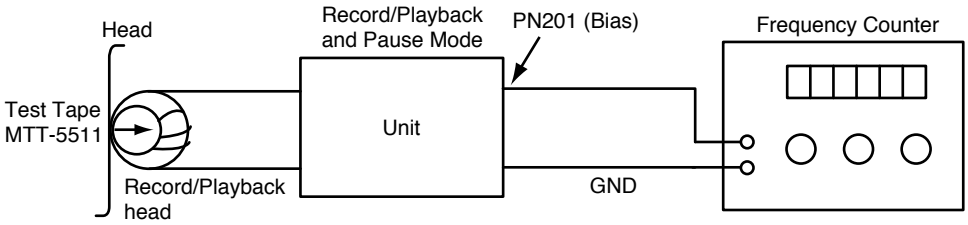


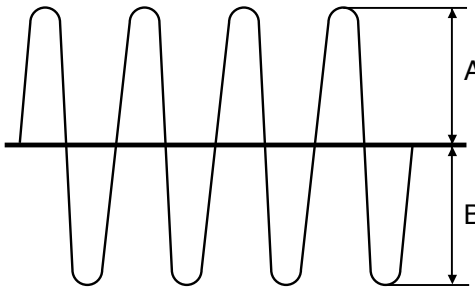
Figure 7. Record Bias Adjustment Connection Diagram

CDP ADJUSTMENTS

※ When change the pick-up must be confirm as follow

1. TRACKING BALANCE CONFIRMATION

1. Connect the oscilloscope to TP501(TEO and REF)
2. Access from 1 st selection to last section of test disc (YEDS-18)
3. Confirm the normal state of tracking error signal (T.B deviation : less than ±3%)



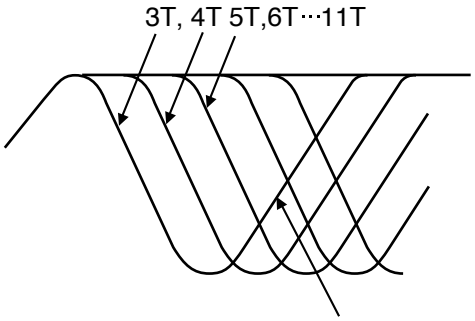
A=B

T.B deviation(%)

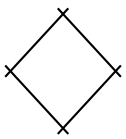
$$= \frac{A-B}{A+B} \times \frac{100}{2} \%$$

2. RF WAVEFORM CONFIRMATION

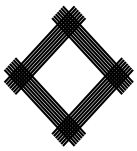
1. Connect the oscilloscope to TP 501(RF and REF)
2. Put a test disc (SONY YEDS-18) into unit and playback the 18th selection of the test disc.
3. Confirm the normal state of RF waveform.
4. Confirm the less than 30nS of Jitter Meter reading.



EYE-PATTERN



OK

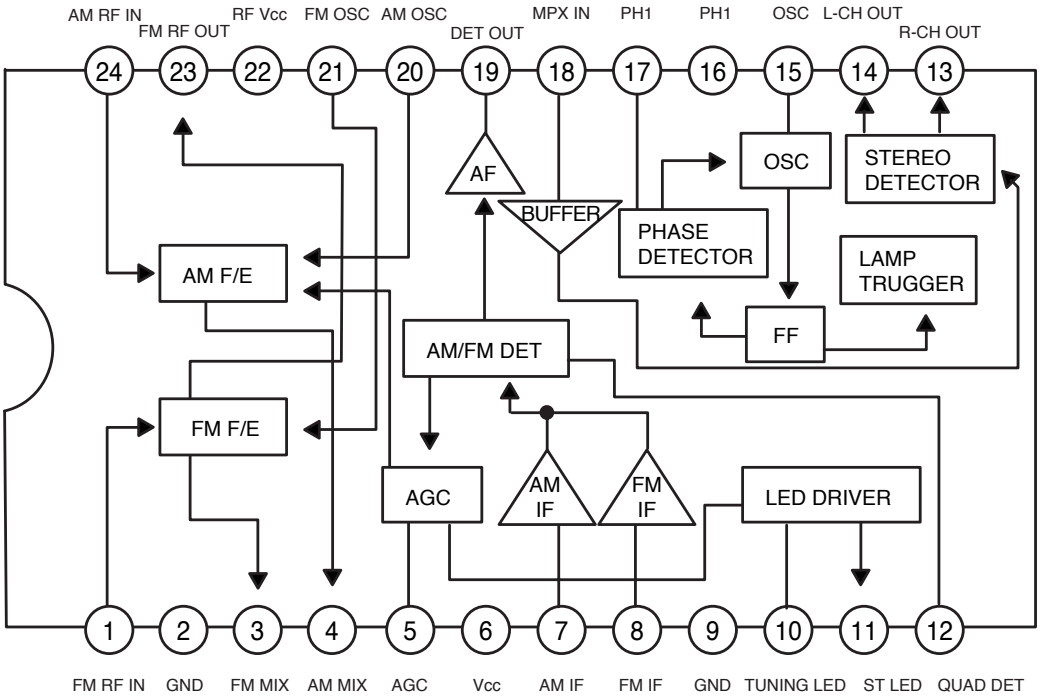


NG

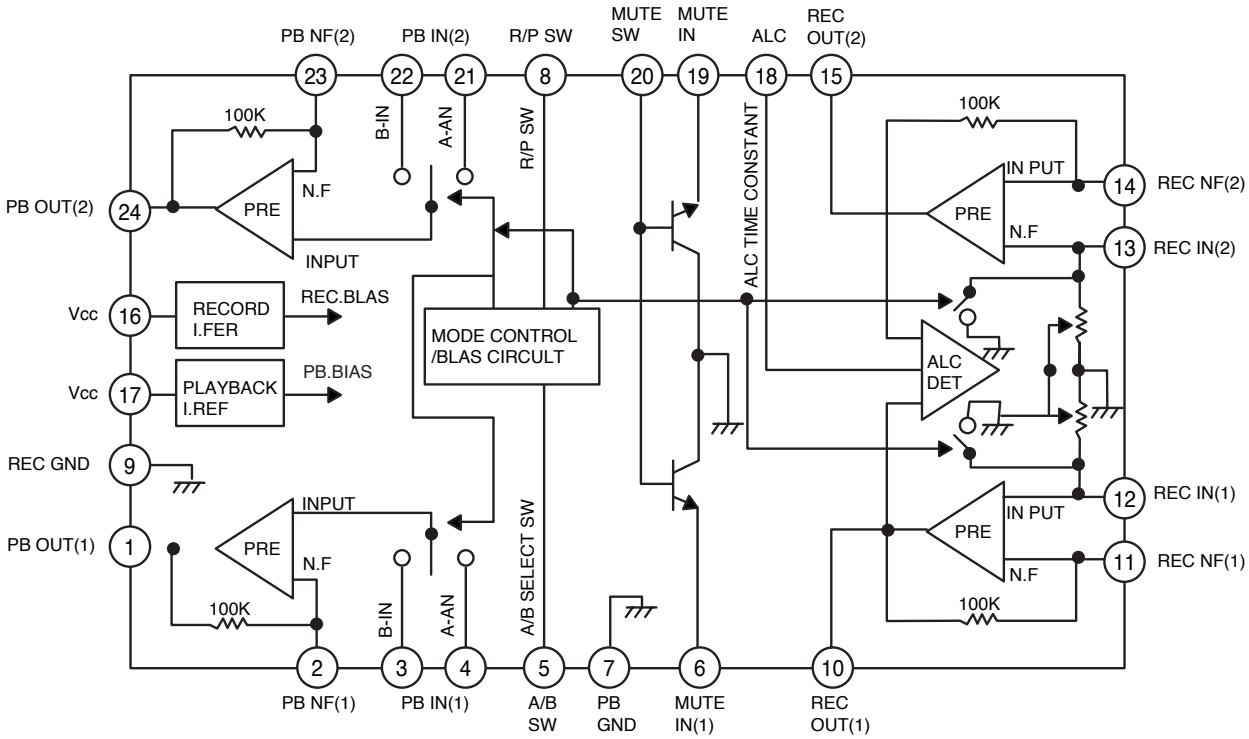
EYE-PATTERN

CIRCUIT DESCRIPTIONS

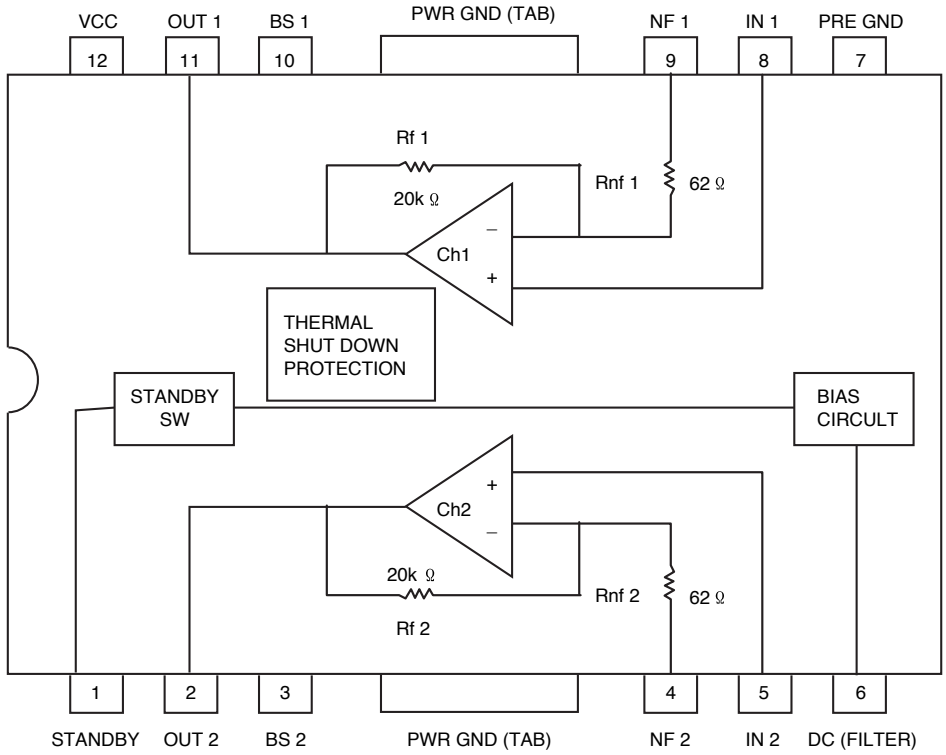
1. IC1(KA22901)



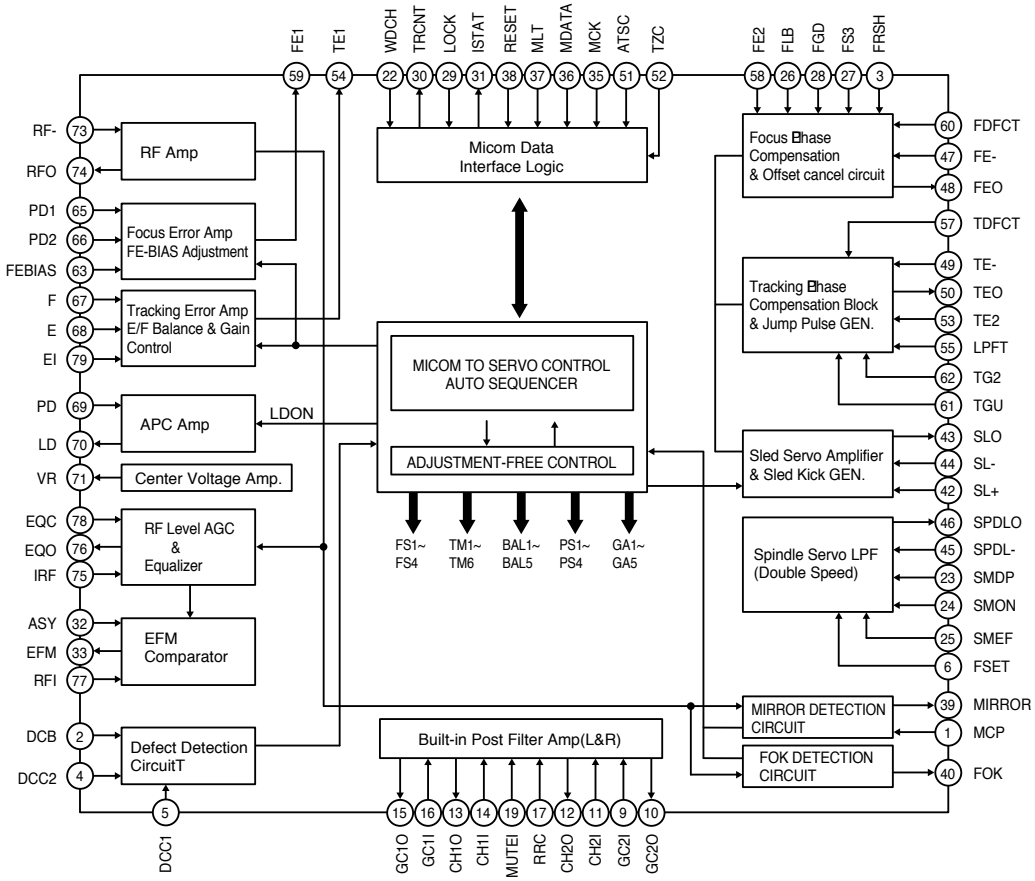
2. IC101(KA22291)



3. IC300(LA4227)



4. IC501(KB9223)

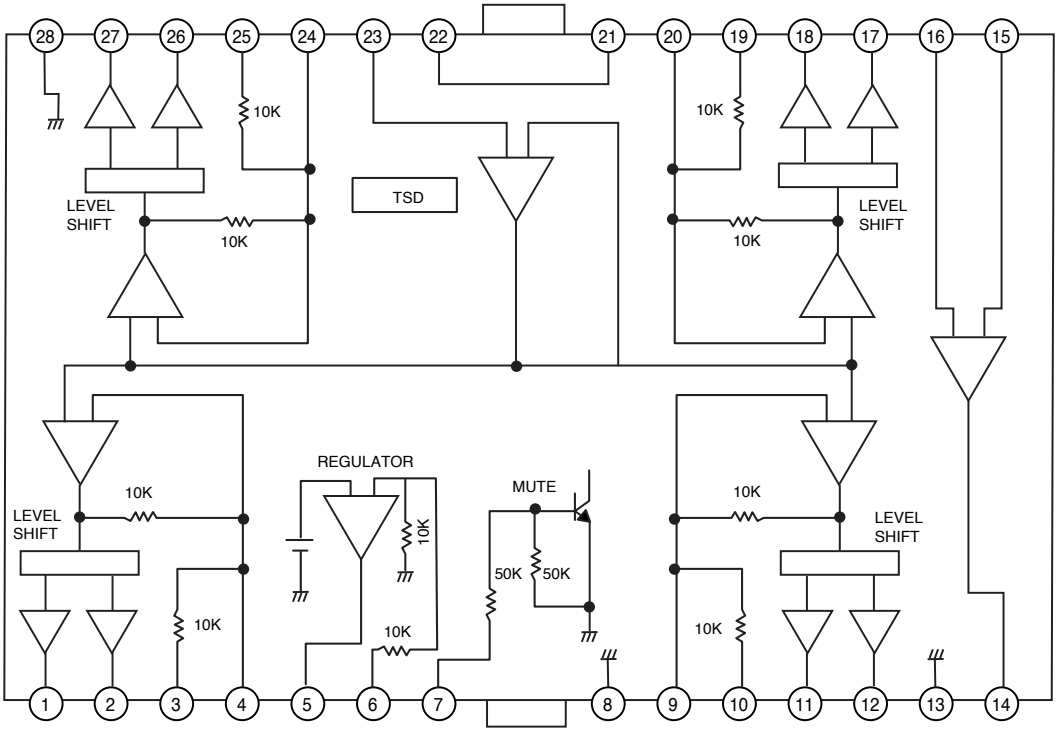


■ PIN DESCRIPTION (continued)KB9223

PIN NO	SYMBOL	DESCRIPTION
1	MCP	Capacitor connection pin for mirror hold
2	DCB	Capacitor connection pin for defect Bottom hold
3	FRSH	Capacitor connection pin for time constant to generate focus search waveform
4	DCC2	The input pin through capacitor of defect bottom hold output
5	DCC1	The output pin of defect bottom hold
6	FSET	The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF
7	VDDA	Analog VCC for servo part
8	VCCP	VCC for post filter
9	GC2I	Amplifier negative input pin for gain and low pass filtering of DAC output CH2
10	GC2O	Amplifier output pin for gain and low pass filtering of DAC output CH2
11	CH2I	The input pin for post filter channel2
12	CH2O	The output pin for post filter channel2
13	CHIO	The output pin for post filter channel1
14	CH1I	The input pin for post filter channel1
15	GC1O	Amplifier output pin for gain and low pass filtering of DAC output CH1
16	GC1I	Amplifier negative input pin for gain and low pass filtering of DAC output CH1
17	RRC	The pin for noise reduction of post filter bias
18	VSSP	VSS for post filter
19	MUTEI	The input pin for post filter muting control
20	ISET	The input pin for current setting of focus search, track jump and sled kick voltage
21	VREG	The output pin of regulator
22	WDCK	The clock input pin for auto sequence
23	SMDP	The input pin of CLV control output pin SMDP of DSP
24	SMON	The input pin for spindle servo ON through SMON of DSP
25	SMEF	The input pin of provide for an external LPF time constant
26	FLB	Capacitor connection pin to perform rising low bandwidth of focus loop
27	FS3	The pin for high frequencygain change of focus loop with internal FS3 switch
28	FGD	Reducing high frequency gain with capacitor between FS3 pin
29	LOCK	Sled runaway prevention pin
30	TRCNT	Track count output pin
31	ISTAT	Internal status output pin
32	ASY	The input pin for asymmetry control
33	EFM	EFM comparator output pin
34	VSSA	Analog VSS for servo part

PIN NO	SYMBOL	DESCRIPTION
35	MCK	MICOM clock input pin
36	MDATA	MICOM data input pin
37	MLT	MICOM data latch input pin
38	RESET	Reset input pin
39	MIRROR	The mirror output for test
40	FOK	The output pin of focus OK comparator
61	TGU	The capacitor connection pin for high frequency tracking gain switch
62	TG2	The pin for high frequency gain change of tracking servo loop with internal TG2 switch
63	FEBIAS	Focus error bias voltage control pin
64	DVEE	The DVEE pin for logic circuit
65	PD1	The negative input pin of RF I/V amplifierl(A+C signal)
66	PD2	The negative input pin of RF I/V amplifier2(B+D signal)
67	F	The negative input pin of F I/V amplifier (F signal)
68	E	The negative input pin of E I/V amplifier (E signal)
69	PD	The input pin for APC
70	LD	The output pin for APC
71	VR	The output pin of (AVEE+AVCC)/2 voltage
72	VCC	VCC for RF part
73	RF-	RF summing amplifier inverting input pin
74	RFO	RF summing amplifier output pin
75	IRF	The input pin for AGC
76	EQO	The output pin for AGC
77	RFI	The input pin for EFM comparison
78	EQC	The capacitor connection pin for AGC
79	EI	Feedback input pin of E I/V amplifier for EF Balance control
80	GND	GND for RF part

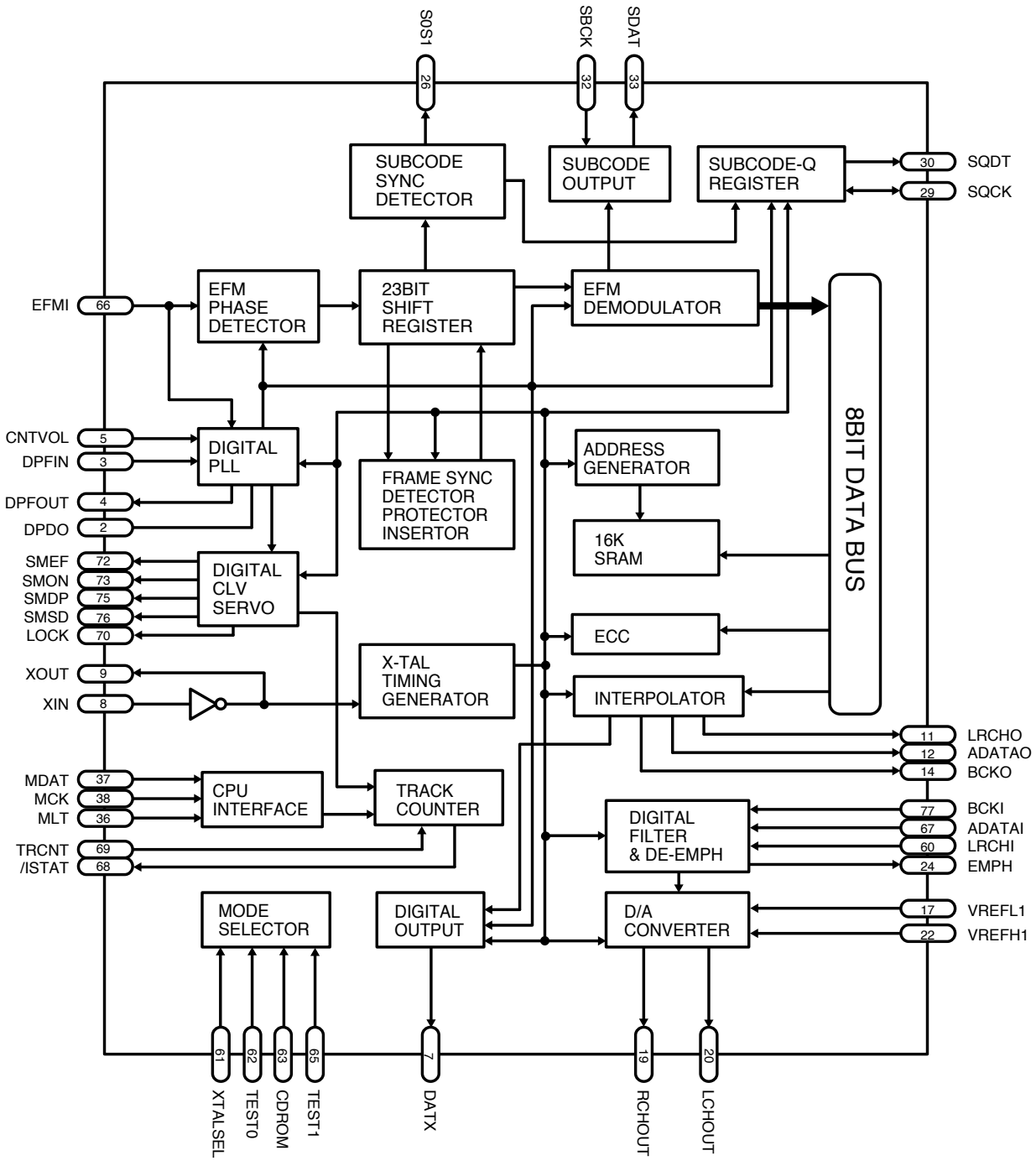
5. (IC502)KA9258BD



■ PIN DESCRIPTION KA9258BD

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	DO1-1	O	Drive Output	15	OPIN(-)	I	OPamp Input(-)
2	DO1-2	O	Drive Output	16	OPIN(+)	I	OPamp output(+)
3	DI1-1	I	Drive Input	17	DO3-1	O	Drive Output(-)
4	DI1-2	I	Drive Input	18	DO3-2	O	Drive Output(+)
5	REG		Regulator	19	DI3-I	I	Drive Input
6	REO	O	Regulator Output	20	DI3-2	I	Drive Input
7	MUTE	I	Mute	21	VCC1	-	Supply Voltage
8	GND1	-	Ground	22	VCC2	-	Supply voltage
9	DI2.1	I	Drive Input	23	VREF	I	2.5V Bias Voltage
10	DI2.2	I	Drive Input	24	DI4.1	I	Drive Input
11	DO2.1	O	Drive Output	25	DI4.2	I	Drive Input
12	DO2.2	O	Drive Output	26	DO4.1	O	Drive Output(+)
13	GND2	-	Ground	27	DO4.2	O	Drive Output(-)
14	OPOUT	O	OPamp Output	28	GND3	-	Ground

6. IC503(KA9286B)



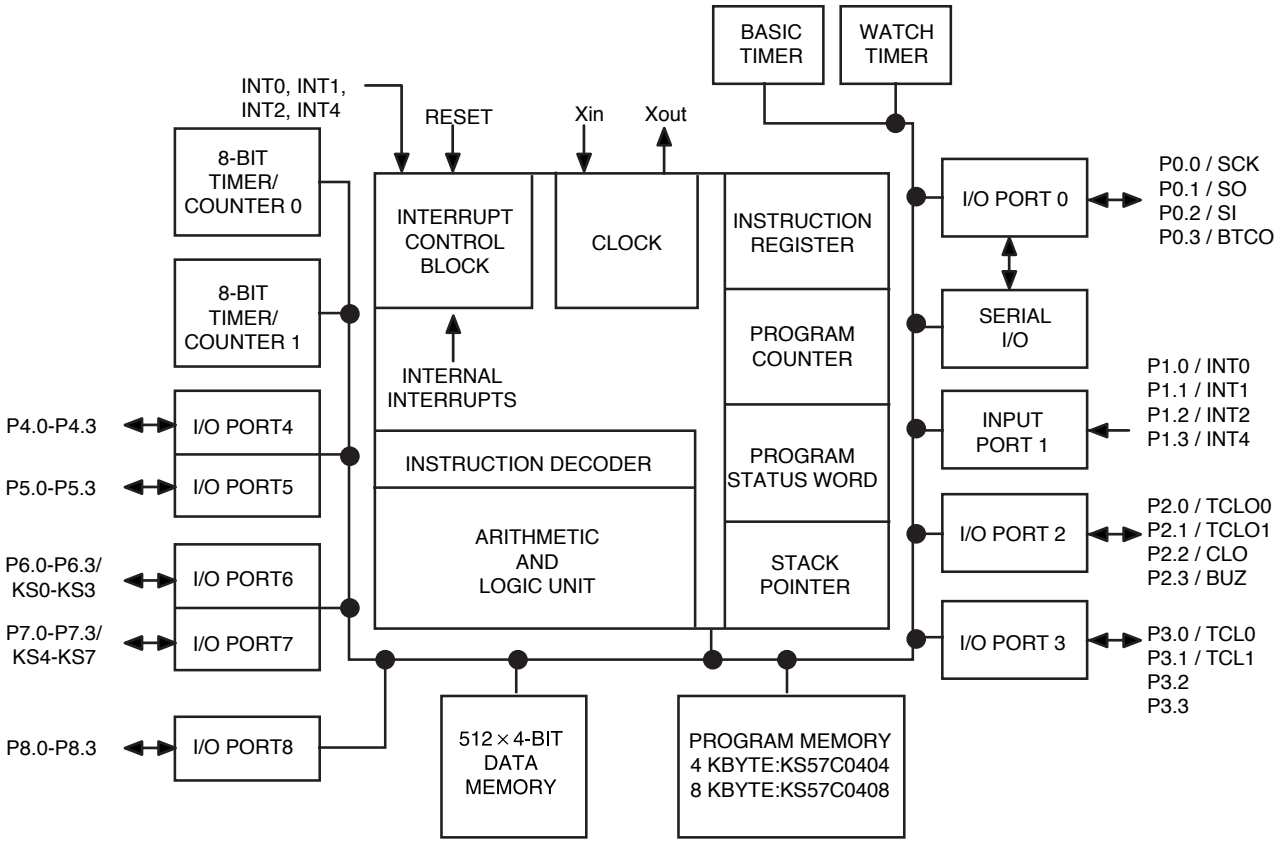
■ PIN DESCRIPTION KS9286B

PIN NO	SYMBOL	I/O	DESCRIPTION
1	AVDD1	-	Analog VCC1
2	DPDO	O	Charge pump output for Digital PLL
3	DPFIN	I	Filter input for Digital PLL
4	DPFOUT	O	Filter output for Digital PLL
5	CNTVOL	I	VCO control voltage for Digital PLL
6	AVSS1	-	Analog Ground 1
7	DATX	O	Digital Audio output data
8	XIN	I	X'tal oscillator input
9	XOUT	O	X'tal oscillator Output
10	WDCHO	O	Word clock output of 48bit/Slot (88.2KHz)
11	LRCHO	O	Channel clock output of 48 bit/Slot (44.1 KHz),88.2KHz when ESP ON
12	ADATAO	O	Serial audio data output of 48 bit/Slot(MSB first), double speed output when ESP ON
13	Dvss1	-	Digital Ground1
14	BCKO	O	Audio data bit clock output of 48 bit/Slot (2.1168MHz),4.2336MHz when ESP ON
15	C2PO	O	C2 Pointer for output audio data
16	VREFL2	I	Input terminal2 of reference voltage "L" (Floating)
17	VREFL1	I	Input terminal1 of reference voltage "L" (GND connection)
18	AVDD2	-	Analog VCC2
19	RCHOUT	O	Right-Channel audio output through D/A converter
20	LCHOUT	O	Left-Channel audio output through D/A converter
21	AVSS2	-	Analog ground2
22	VREFH1	I	Input terminal1 of reference voltage "H" (VDD connection)
23	VREFH2	I	Input terminal2 of reference voltage "H" (Floating)
24	EMPH	O	Emphasis/Non-Emphasis output, H: Emphasis ON, L: Emphasis OFF
25	LKFS	O	The Lock Status output of frame sync
26	S0S1	O	Output of subcode sync signal(SO+S1)
27	RESET	I	System reset at "L"
28	/ESP	I	ESP function ON/OFF control ("L": ESP function ON, "H": ESP function OFF)
29	SQCK	I	Clock for output Subcode-Q data
30	SQDT	O	Serial output of Subcode-Q data
31	SQOK	O	The CRC (Cycle Redundancy Check) check rssult signal output of Subcode-Q

PIN NO	SYMBOL	I/O	DESCRIPTION
32	SBCK	I	Clock for output subcode data
33	SDAT	O	Subcode serial dsta output
34	DVDD1	-	Digital VDD1
35	MUTE	I	Mute control input ("H": Mute ON)
36	MLT	I	Latch Signal Input from Micom (Schmit Trigger)
37	MDAT	I	Serial data input from Micom (Schmit Trigger)
38	MCK	I	Serial clock input from Micom (Schmit Trigger)
39	DB8	I/O	SRAM data I/O port 8 (MSB)
40	DB7	I/O	SRAM data I/O port 7
41	DB6	I/O	SRAM data I/O port 6
42	DBS	I/O	SRAM data I/O port 5
43	DB4	I/O	SRAM data I/O port 4
44	DB3	I/O	SRAM data I/O port 3
45	DB2	I/O	SRAM data I/O port 2
46	DB1	I/O	SRAM data I/O port 4 (LSB)
47	C1F1	I/O	Monitoring output for C1 error correction (RA1)
48	C1F2	I/O	Monitoring output for C1 error correction (RA2)
49	C2F1	I/O	Monitoring output for C2 error correction (RA3)
50	C2F2	I/O	Monitoring output for C2 error correction (RA4)
51	C2FL	I/O	C2 decoder flag (RA5, "H": When the processing C2 code is impossible correction status)
52	/PBCK	I/O	Output of VCO/2 (4.3218MHz) (RA6)
53	DVSS2	I/O	Digital ground 2
54	FSDW	I/O	Window or unprotected frame sync (RA7)
55	ULKFS	I/O	Frame sync protection state (RA8)
56	/JIT	I/O	Display of either RAM overflow or under flow for ± 4 frame jitter margin (RA9)
57	C4M	I/O	Only monitoring signal (4.2336MHz) (RA10)
58	C16M	I/O	16.9344MHz signal output(RA11)
59	/WE	I/O	Terminal for test
60	/CS	I/O	Tsrminal for test
61	XTALSEL	I	Mode Selectiona1(H: 33.8688MHz, L: 16.9344MHz)
62	TEST0	I	TEST input terminal (GND connection)
63	CDROM	I	Mode Selection2 (H: CD-ROM, L: CDP)
64	SRAM	I	TEST input tsrminal (GND connection)
65	TEST1	I	TEST input terminal (GND connection)

PIN NO	SYMBOL	I/O	DESCRIPTION
66	EFMI	I	EFM signal input
67	ADATAI	I	Serial audio data input of 48 bit/Slot (MSB first)
68	/ISTAT	O	The internal status output
69	TRCNT	I	Tracking counter input signal
70	LOCK	O	Output signal of LKFS condition sampled PBFR/16 (if LKFS is “H”, LOCK is “H”, if LKFS is sampled “L” at least 8 timss by PSFR/16, LOCK is “L”.)
71	PBFR	O	Write frame clock (LDck: 7.35KHz)
72	SMEF	O	LPF time constant control of the spindle servo error signal
73	SMON	O	ON/OFF control signal for spiNdle servo
74	DVDD2	-	Digital VDD2
75	SMDP	O	Spindle Motor drive (Rough control in the SPEED mode, Phase control in the PHASE mode)
76	SMSD	O	Spindle Motor drive (Velocity control in the PHASE mode)
77	BCKI	I	Audio data bit clock input of 48 bit/slot (2.1168MHz)
78	TESTV	I	TEST input terminal (GND connection)
79	DSPEED	I	TEST input terminal (VDD connection)
80	LRCHI	I	Channel clock input of 48 bit/Slot (44.1 KHz)

7. IC601(KS57C0408B)



■ PIN DESCRIPTIONS (KS57C0408B)

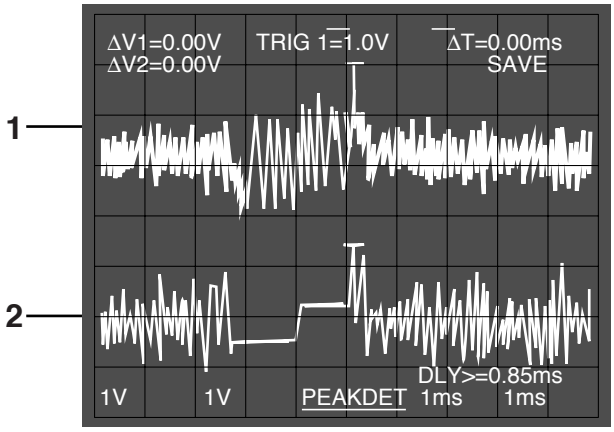
Pin Name	Pin Type	Description	Number	Share Pin
P0.0	I/O	4-bit I/O port.	12 (28)	SCK
P0.1		1-bit or 4-bit read/write and test is possible.	11(27)	SO
P0.2		Individual pins are software configurable as input or output.	10(26)	SI
P0.3		4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	9(25)	BTCO
P1.0	I	4-bit input port.	4 (20)	INT0
P1.1		1 -bit and 4-bit read and test is possible.	3 (19)	INT1
P1.2		3-bit pull-up resistors are assignable by software to	2 (18)	INT2
P1.3		pins P1.0, P1.1, and P1.2	1(17)	INT4
P2.0	I/O	Same as port 0.	8 (24)	TCLO0
P2.1			7 (23)	TCLO1
P2.2			6 (22)	CLO
P2.3			5 (21)	BUZ
P3.0	I/O	Same as port 0.	20 (38)	TCL0
P3.1			19 (37)	TCL1
P3.2			18 (36)	
P3.3			17 (35)	
P4.0-P4.3	I/O	4-bit I/O ports.	26-23	
		N-channel open-drain output up to 9 volts.	(44-41)	
P5.0-P5.3		1 -bit rind 4-bit read/write and test is possible.	30-27	
		Port 4 and 5 can be paired to support 8-bit data transfer.	(4-1)	
		8-bit unit pull-up resistors are assignable by mask option.		
P6.0-P6.3	I/O	4-bit I/O ports.	37-34	KS0-KS3
		1 -bit or 4-bit read/write and test is possible.	(11-8)	
P7.0-P7.3		Port 6 pins are individually software configurable as input or output	41-38 (15-12)	KS4-457
		4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins(port 6 only).		
		Ports 6 and 7 can be paired to enable 8-bit data transfer.		
P8.0-P8.3	I/O	4-bit I/O ports.	16-13	
		1 -bit and 4-bit read/write and test is possible.	(32-29)	
		Pins are individually software configurable as input or output.		
		4-bit pull-down resistors are software assignable;pull-down resistors are automatically disabled for output pins		

■ PIN DESCRIPTIONS (KS57C0408B)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	12 (28)	P0.0
SO	I/O	Serial data output	11(27)	P0.1
SI	I/O	Serial dots input	10 (26)	P0.2
BTCO	I/O	Basic timer clock output (2 Hz, 16 Hz,64 Hz, or 256 Hz at 4.19 MHz)	9 (25)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INTO and INT1 is selectable. INT0 is synchronized to system clock.	4,3 (20, 19)	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	2 (18)	P .2
INT4	I	External interrupt with detection of rising and falling edges.	1 (17)	P1.3
TCLO0	I/O	Timer/counter 0 clock output	8 (24)	P2.0
TCLO1	I/O	Timer/counter 1 clock output	7 (23)	P2.1
CLO	I/O	Clock Output	6 (22)	P2.2
BUZ	I/O	2 kHz,4 kHz,8 kHz, or 16 kHzfrequency output at 4.19 MHz for buzzer sound	5 (21)	P2.3
TCL0	I/O	External clock input for timer/counter 0	20 (38)	P3.0
TCLI	I/O	External clock input for timer/counter 1	19 (37)	P3.1
KS0-KS3 KS4-KS7	I/O	Quasi-interrupt inputs with falling edge detection	37-34 (11-8) 41-38 (5-12)	P6.0-P6.3 P7.0-P7.3
V_{DD}	-	Power supply	21 (39)	
V_{SS}	-	Ground	42 (16)	
RESET	I	Reset signal	31 (5)	
X_{in}, X_{out}	-	Crystal, ceramic, or RC oscillator signal for system clock (For external clock input, use X_{in} and input X_{in}' s reverse phase to X_{out})	33,32 (7,6)	
TEST	-	Test signal input (must be connected to V_{SS})	22 (40)	
NC	-	No connection (must be connected to V_{SS})	(33,34)	

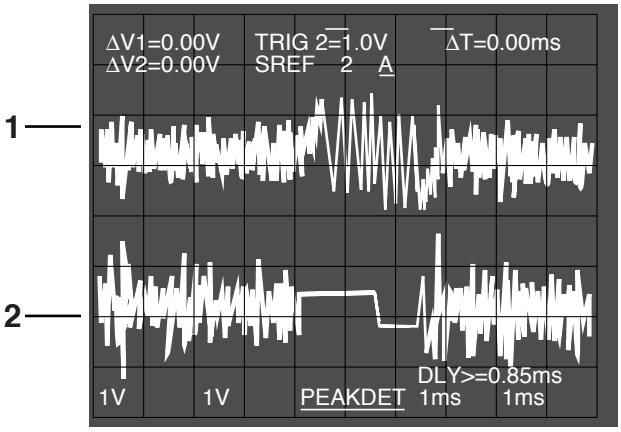
MAJOR WAVEFORM

TRACKING ERROR(REW)



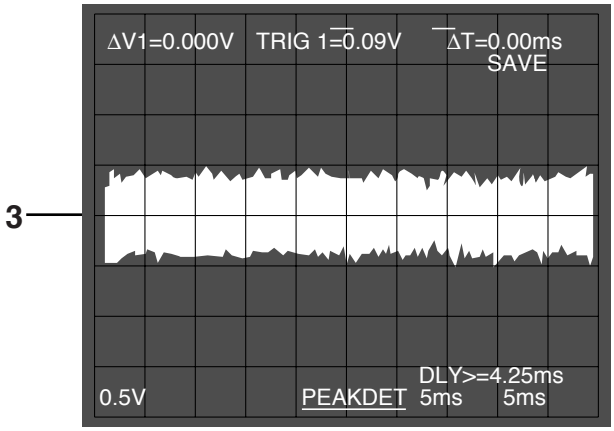
- **Connection** : 1. IC501 pin (54).(TEO)
  2. IC501 pin (50)
- **Inspection** : Check tracking servo circuit.(RWD)

TRACKING ERROR(FWD)



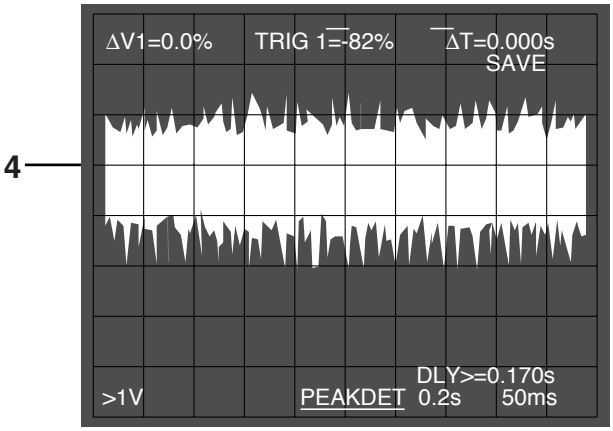
- **Connection** : 1. IC501 pin (54).(TEO)
  2. IC501 pin (50)
- **Inspection** : Check tracking servo circuit.(FWD)

FOCUS GAIN



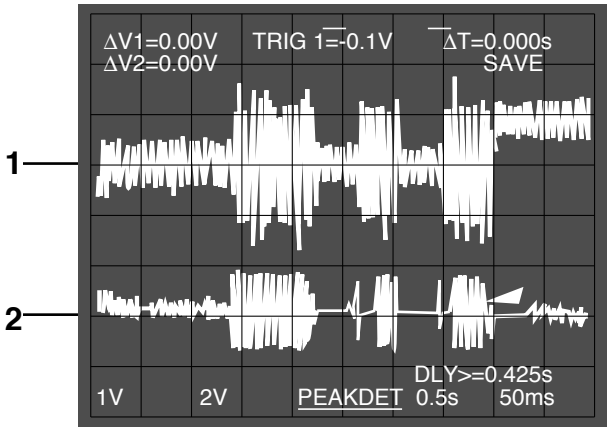
- **Connection** : 3. IC502 pin (1) and (2).
  ※ Test disc : YEDS-43
- **Inspection** : Check focus servo circuit.

TRACKING GAIN



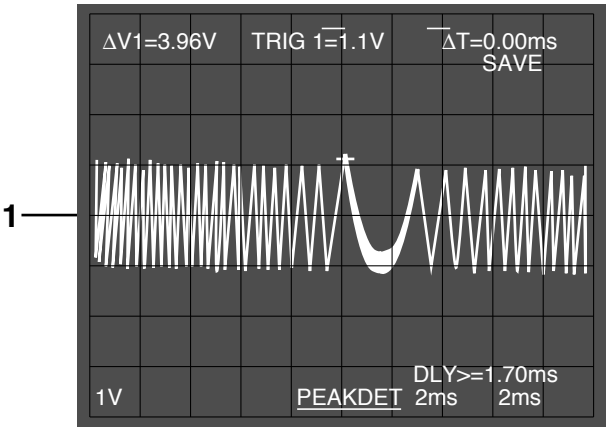
- **Connection** : 3. IC502 pin (26) and (27)
  ※Test disc: YEDS-43
- **Inspection** : Check tracking servo circuit.

TRACKING COIL DRIVE



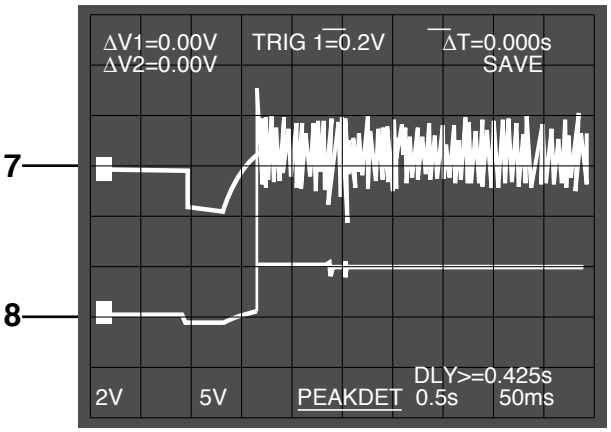
- **Connection** : 1. IC501 pin (54). (TEO)
  2. IC501 pin (50)
- **Inspection** : - Confirm tracking servo circuit.
  - Check IC501 (Cold solder joint or short circuit)

E.F. BALANCE



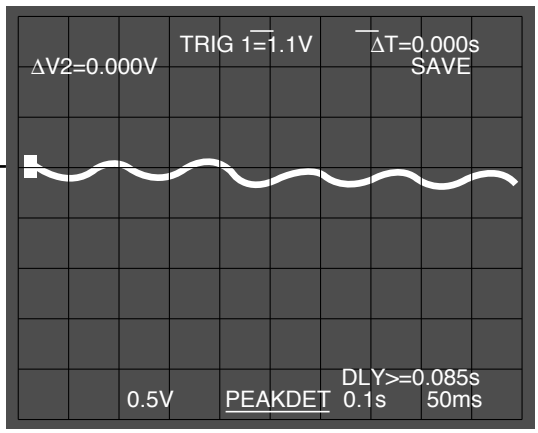
- **Connection** : 1. IC501 pin (54).
- **Inspection** : Confirm tacking servo balance deviation rate

READING



- **Connection** : 7. IC501 pin (48).
  8. IC501 pin (40) (FOK)
- **Inspection** : Check IC502 pin (4) to IC501 pin (48) (Pattern defective)

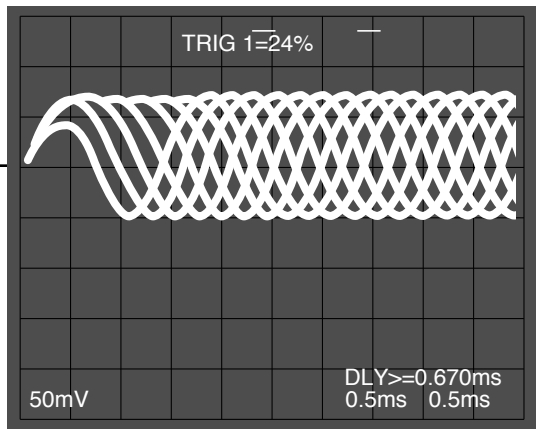
9



• **Connection** : 9. IC502 pin (17) and (18)

• **Inspection** : - Check IC501 pin (43) to IC502 pin (20) (Pattern defective)
- Check voltage. (IC502 pin (20))

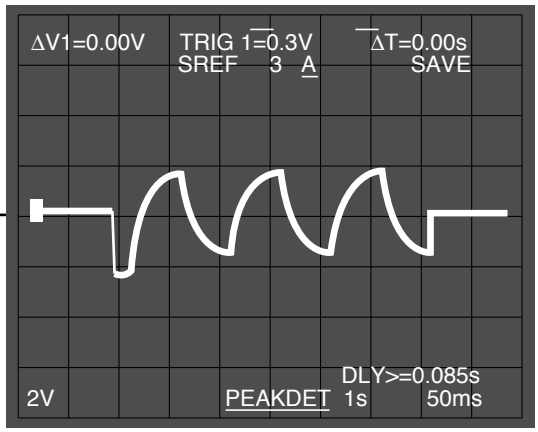
10



• **Connection** : 10. IC501 pin (74).

• **Inspection** : Check objective Lens of Pickup clear or not

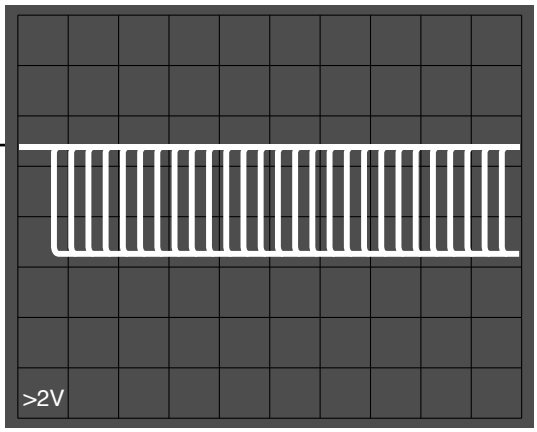
11



• **Connection** : 11. IC502 pin (1) and (2).

• **Inspection** : - Is focus search signal output to IC501 pin (48)?

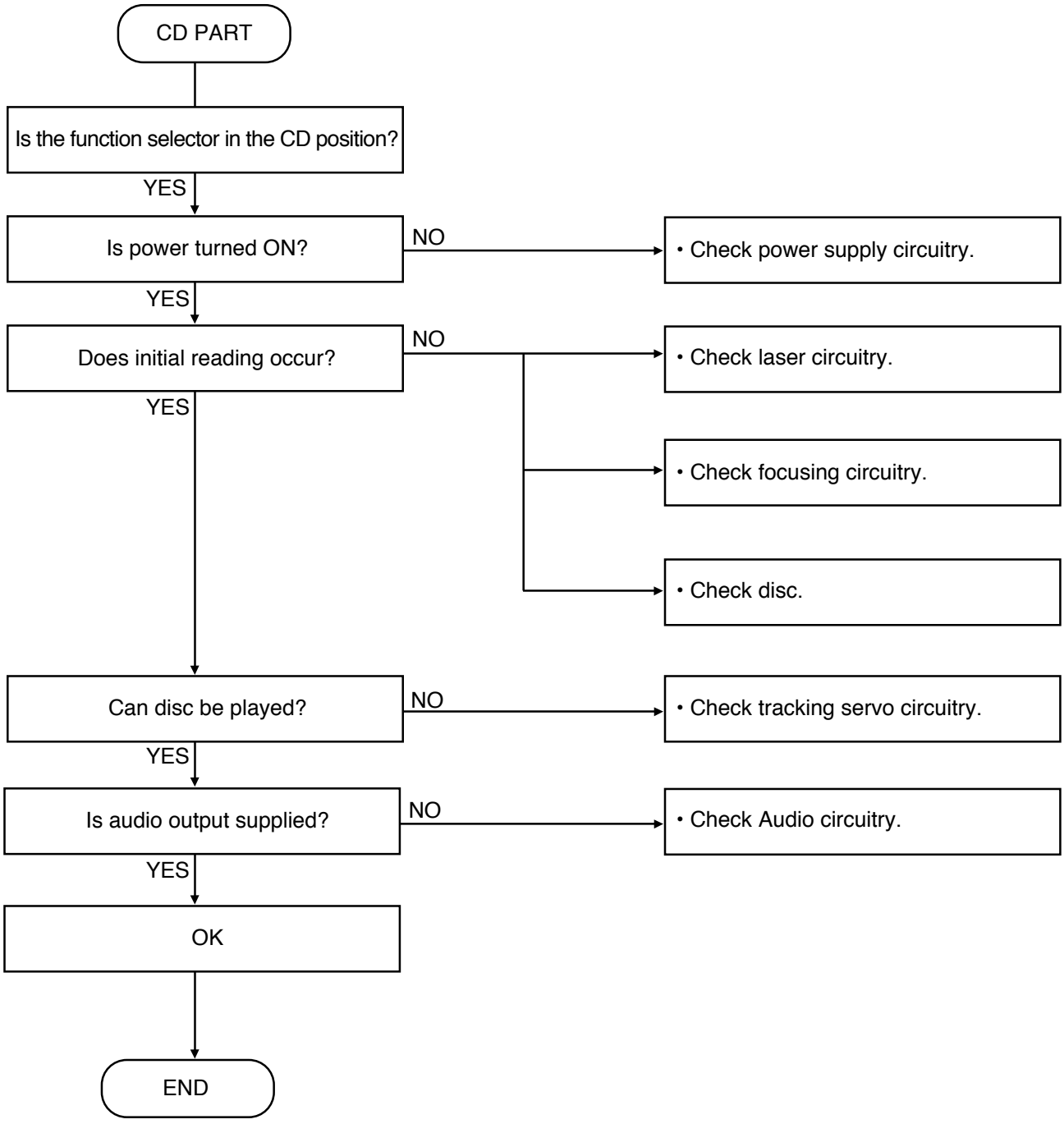
12



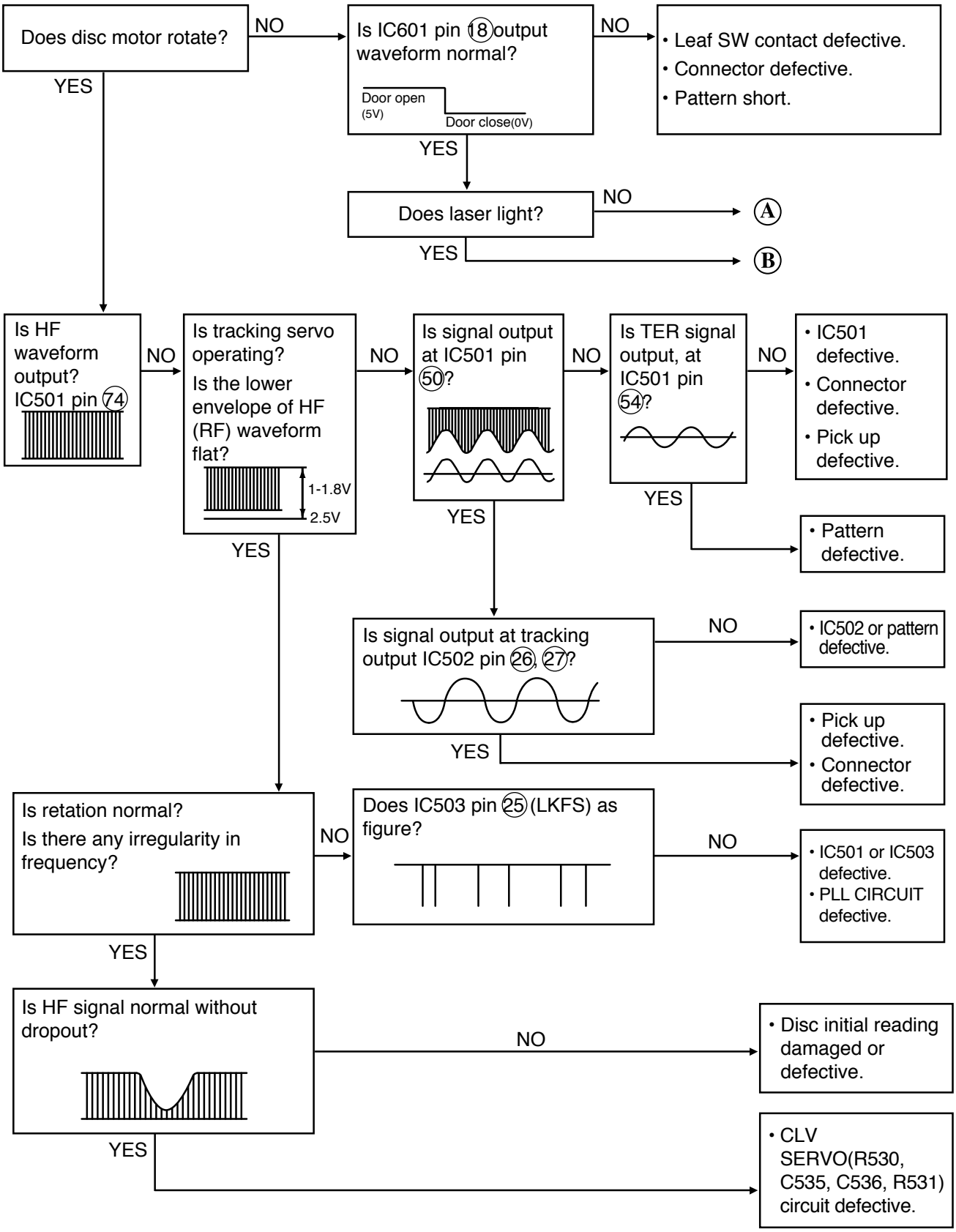
• **Connection** : 12. IC501 pin (33).

• **Inspection** : Check IC503 and surrounding circuit (Cold solder joint or short circuit)

TROUBLESHOOTING GUIDE



1. If initial reading is not carried out (with disc)



Ⓐ When laser does not light

Is below signal “H” at IC501 pin ㊳ (RESET)?

YES

NO

Has Pick-up returned to the innermost position?

NO

Are data transferred from IC601?

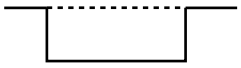
NO

• IC601 defective.

YES

YES

Is below signal output at IC502 pin ⑰, ⑱?



NO

• IC501, 502 defective.

YES

• Slide motor defective.
• Connector defective.

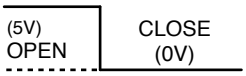
Does pick-up stop after having moved to the innermost position?

NO

• IC502 defective.

YES

Are detect output input at IC601 pin ⑰?



NO

• LMT SW defective.
• Connector defective.

YES

• IC502 defective.

Does generate about 3.3V at IC501 pin ㊵ (LD)?

NO

• IC501 defective.
• Surrounding Circuitry defective.

YES

Has Laser Power source returned to the Q501?

(Q501 Collector Voltage about 1.8V)

NO

• Connector defective.
• Pick-up defective.

YES

Flow Laser Current?

Both voltage of R507 is about 1.0V

R507 ≫ 1.0V

YES

• Q501 defective, connector defective.
• Laser defective.

NO

R507 ≪ 1.0V

YES

• Laser defective.
• Connector defective. short etc.

Ⓑ When laser light

Do lenses move up and down?

NO → Is signal output at focus search terminal?

IC 501 pin 48 (FEO)

NO → • IC501 defective.
• C527 defective.

YES → Is signal output at IC502 pin 1, 2?

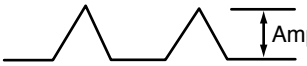
NO → • IC 502 defective.

YES → • Actuator short.
• Connector short.

YES → Is IC501 pin 74 (HF) signal waveform output?

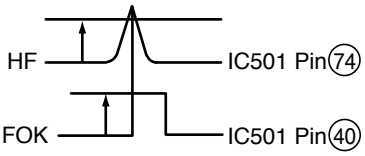
NO → • Connector short.
• IC501 defective.
• Pick-up defective.

YES → The waveform of IC501 pin 74 (HF) is below figure?



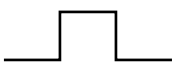
NO → • Turntable height error
• Laser diode degraded.

YES → Is Fok signal output?
(HF and REF) 0.4 over OK.



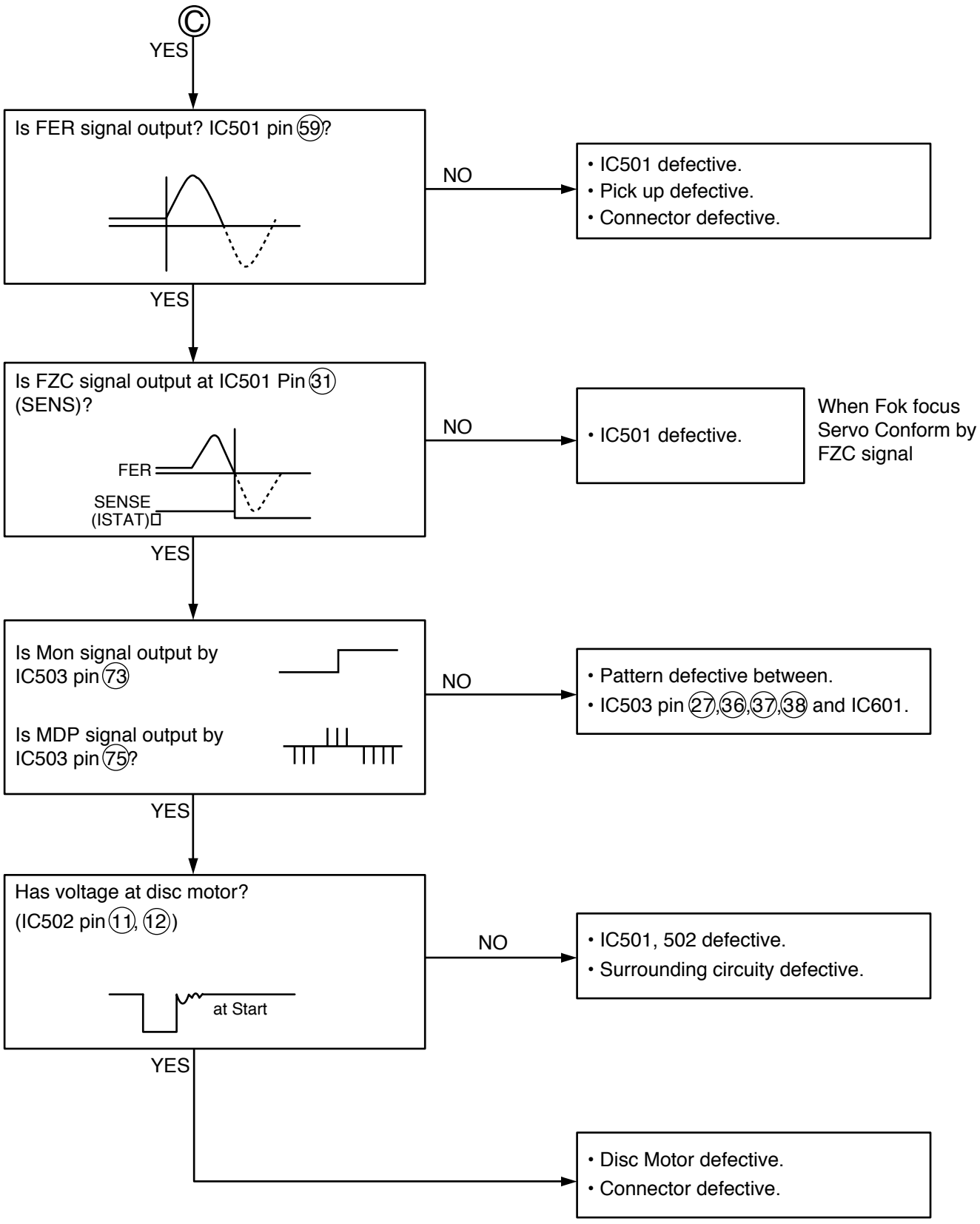
NO → • IC501 defective.

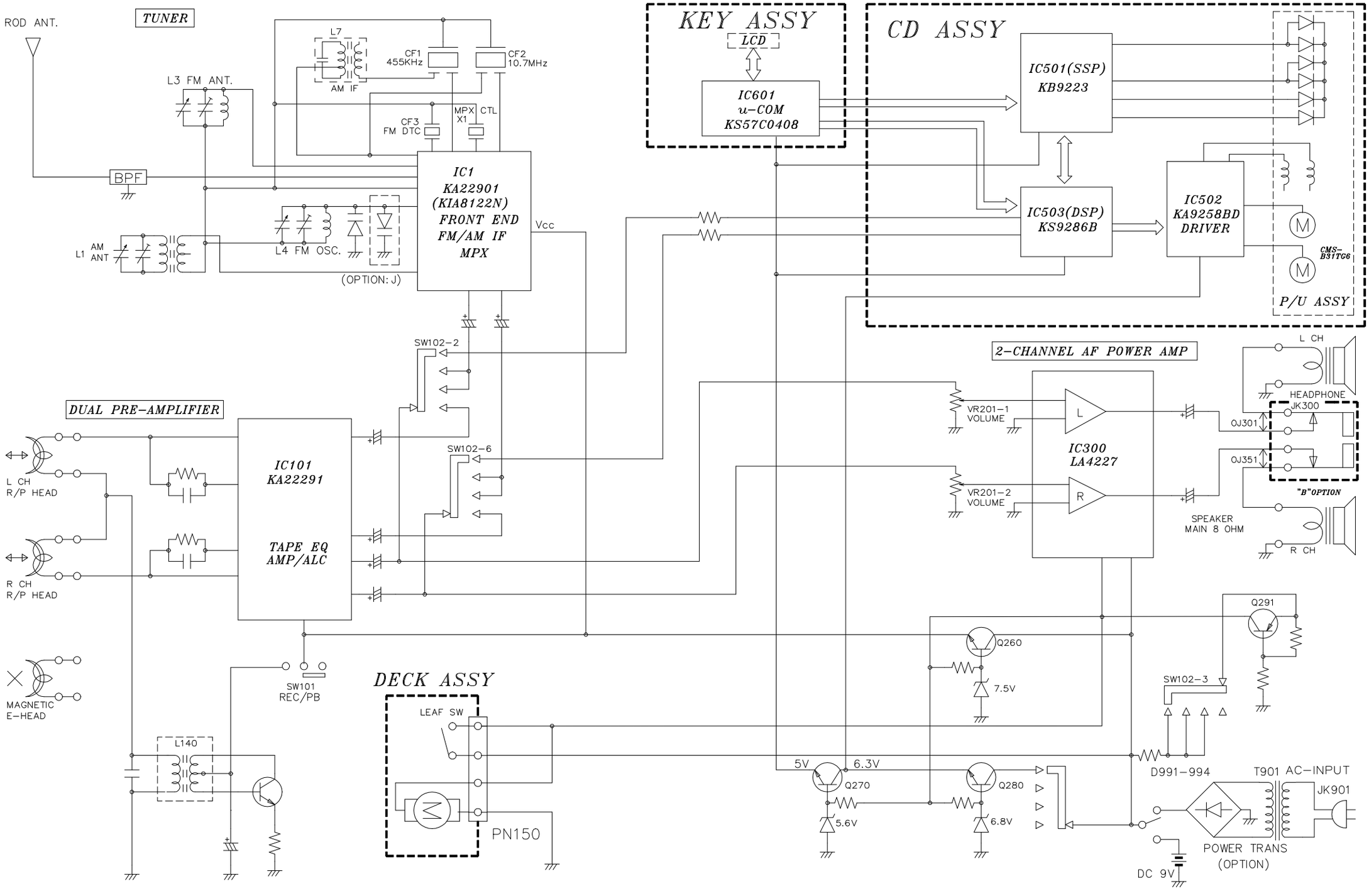
YES → Is Fok signal intput to IC601 pin 25 ?



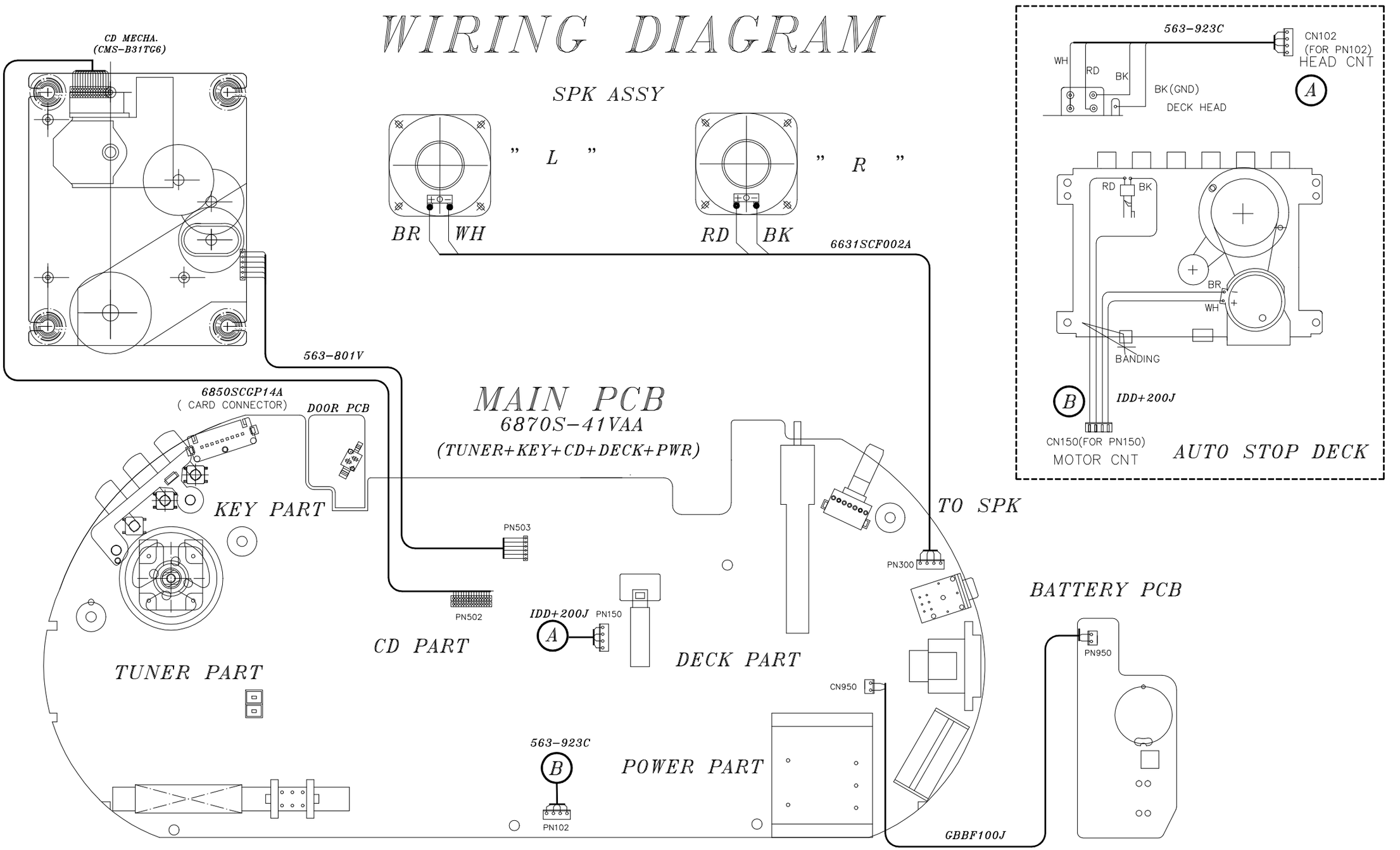
NO → • Pattern defective.

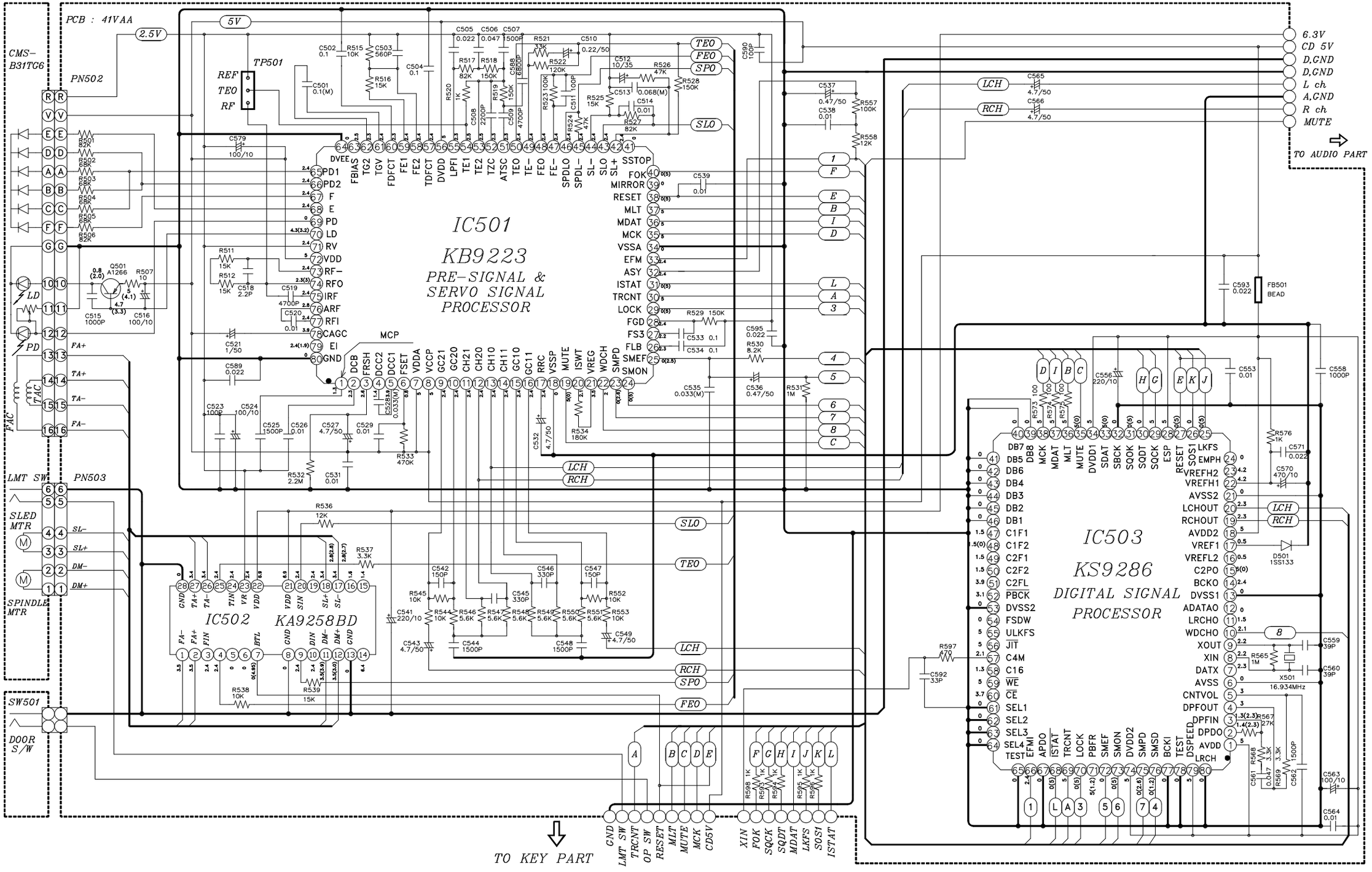
YES → Ⓒ

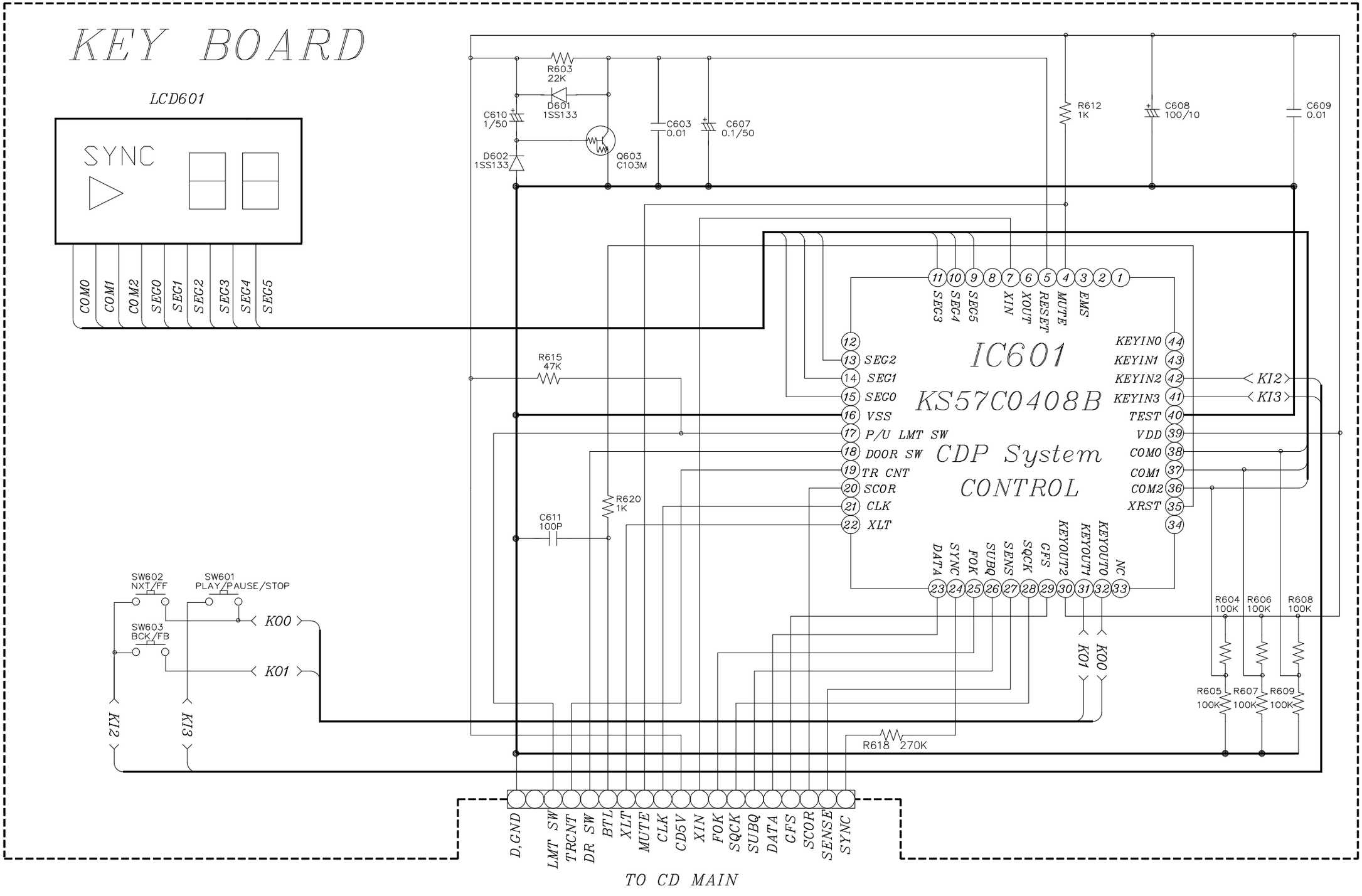

Ⓒ
YES
Is FER signal output? IC501 pin 59?
NO
• IC501 defective.
• Pick up defective.
• Connector defective.
YES
Is FZC signal output at IC501 Pin 31 (SENS)?
FER
SENSE (ISTAT)
NO
• IC501 defective.
When Fok focus Servo Conform by FZC signal
YES
Is Mon signal output by IC503 pin 73
Is MDP signal output by IC503 pin 75?
NO
• Pattern defective between.
• IC503 pin 27,36,37,38 and IC601.
YES
Has voltage at disc motor? (IC502 pin 11, 12)
at Start
NO
• IC501, 502 defective.
• Surrounding circuity defective.
YES
• Disc Motor defective.
• Connector defective.

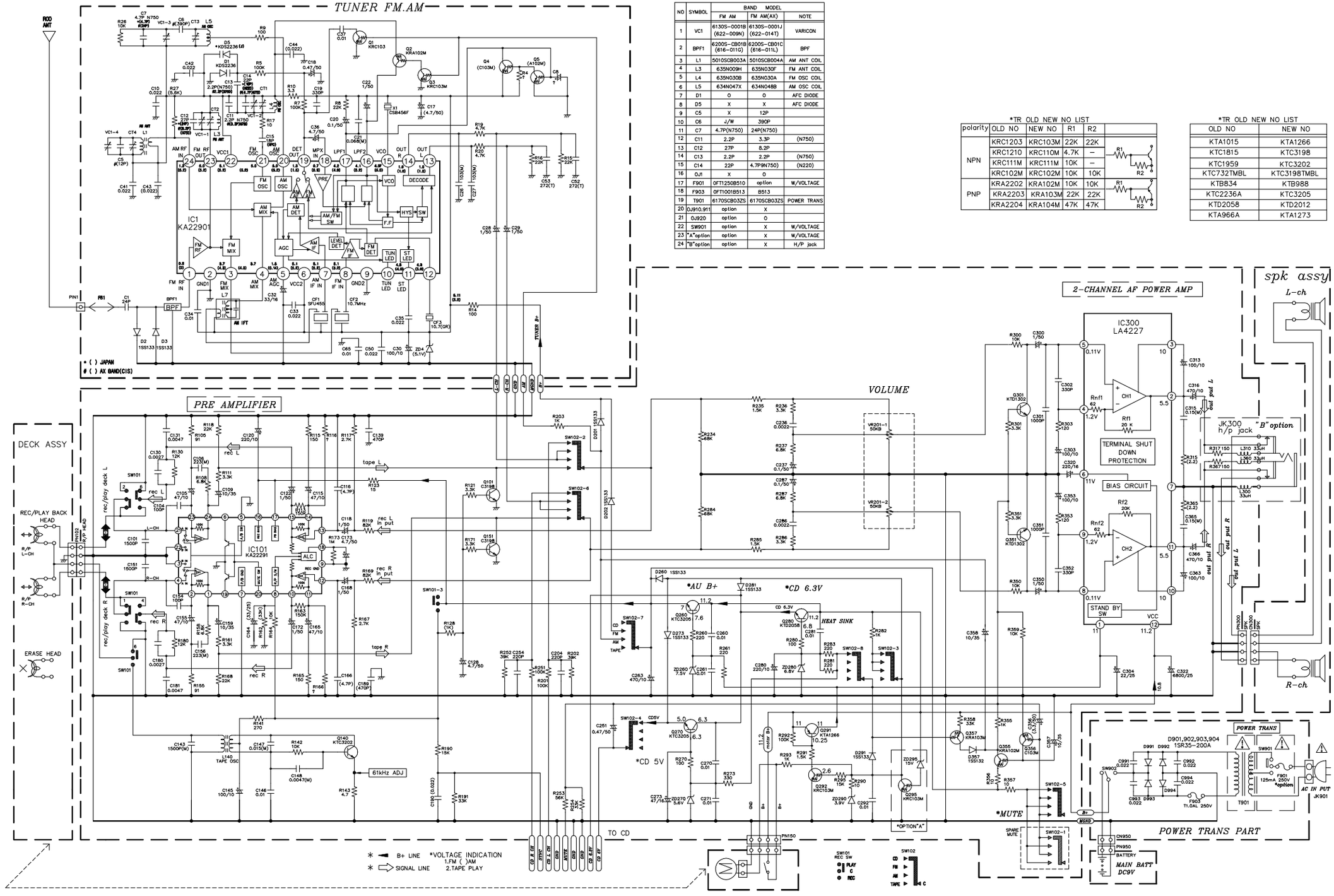

TUNER
ROD ANT.
L3 FM ANT.
L7
AM IF
CF1
455KHz
CF2
10.7MHz
CF3
FM DTC
MPX
X1
CTL
BPF
IC1
KA22901
(KIA8122N)
FRONT END
FM/AM IF
MPX
Vcc
L1 AM ANT
L4 FM OSC.
(OPTION: J)
KEY ASSY
LCD
IC601
u-COM
KS57C0408
CD ASSY
IC501(SSP)
KB9223
IC503(DSP)
KS9286B
IC502
KA9258BD
DRIVER
CMS-B31TG6
P/U ASSY
SW102-2
SW102-6
DUAL PRE-AMPLIFIER
IC101
KA22291
TAPE EQ
AMP/ALC
L CH
R/P HEAD
R CH
R/P HEAD
MAGNETIC
E-HEAD
SW101
REC/PB
L140
2-CHANNEL AF POWER AMP
VR201-1
VOLUME
VR201-2
VOLUME
IC300
LA4227
L
R
L CH
HEADPHONE
JK300
OJ301
OJ351
"B"OPTION
SPEAKER
MAIN 8 OHM
R CH
Q291
Q260
7.5V
SW102-3
DECK ASSY
LEAF SW
PN150
5V
6.3V
Q270
5.6V
Q280
6.8V
D991-994
T901 AC-INPUT
JK901
POWER TRANS
(OPTION)
DC 9V

WIRING DIAGRAM




PCB : 41VAA
CMS-B31TG6
PN502
PN503
TP501
REF
TEO
RF
IC501
KB9223
PRE-SIGNAL & SERVO SIGNAL PROCESSOR
IC502
KA9258BD
IC503
KS9286
DIGITAL SIGNAL PROCESSOR
MCP
LMT SW
SLED MTR
SPINDLE MTR
SW501
DOOR S/W
FAC
TAC
LD
PD
X501
16.934MHz
D501
1SS133
FB501
BEAD
TO AUDIO PART
TO KEY PART
6.3V
CD 5V
D.GND
D.GND
L ch
A.GND
R ch
MUTE
GND
LMT SW
TRCNT
OP SW
RESET
MLT
MUTE
MCK
CD5V
XIN
FOK
SQCK
SQDT
MDAT
LKFS
SOS1
ISTAT


KEY BOARD
LCD601
SYNC
COM0
COM1
COM2
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
R603 22K
D601 1SS133
C610 1/50
D602 1SS133
Q603 C103M
C603 0.01
C607 0.1/50
R612 1K
C608 100/10
C609 0.01
IC601
KS57C0408B
CDP System CONTROL
SEC3
SEC4
SEC5
XIN
XOUT
RESET
MUTE
EMS
SEG2
SEC1
SEG0
VSS
P/U LMT SW
DOOR SW
TR CNT
SCOR
CLK
XLT
KEYIN0
KEYIN1
KEYIN2
KEYIN3
TEST
VDD
COM0
COM1
COM2
XRST
KI2
KI3
R615 47K
R620 1K
C611 100P
DATA
SYNC
FOK
SUBQ
SENS
SQCK
GFS
KEYOUT2
KEYOUT1
KEYOUT0
NC
KO1
KO0
SW602 NXT/FF
SW601 PLAY/PAUSE/STOP
SW603 BCK/FB
R604 100K
R606 100K
R608 100K
R605 100K
R607 100K
R609 100K
R618 270K
D.GND
LMT SW
TRCNT
DR SW
BTL
XLT
MUTE
CLK
CD5V
XIN
FOK
SQCK
SUBQ
DATA
GFS
SCOR
SENSE
SYNC
TO CD MAIN



NO	SYMBOL	BAND MODEL		NOTE
		FM AM	FM AM(AX)	
1	VC1	6130S-0001B (622-009N)	6130S-0001J (622-014T)	VARICON
2	BPF1	6200S-CB01B (616-011G)	6200S-CB01C (616-011L)	BPF
3	L1	5010SCB003A	5010SCB004A	AM ANT COIL
4	L3	635N009H	635N030F	FM ANT COIL
5	L4	635N030B	635N030A	FM OSC COIL
6	L5	634N047X	634N048B	AM OSC COIL
7	D1	0	0	AFC DIODE
8	D5	X	X	AFC DIODE
9	C5	X	12P	
10	C6	J/W	390P	
11	C7	4.7P(N750)	24P(N750)	
12	C11	2.2P	3.3P	(N750)
13	C12	27P	8.2P	
14	C13	2.2P	2.2P	(N750)
15	C14	22P	4.7P9N750)	(N220)
16	OJ1	X	0	
17	F901	0FT1250B510	option	W/VOLTAGE
18	F903	0FT1001B513	B513	
19	T901	6170SCB03ZS	6170SCB03ZS	POWER TRANS
20	0J910.911	option	X	
21	0J920	option	0	
22	SW901	option	X	W/VOLTAGE
23	"A"option	option	X	W/VOLTAGE
24	"B"option	option	X	H/P jack

*TR OLD NEW NO LIST

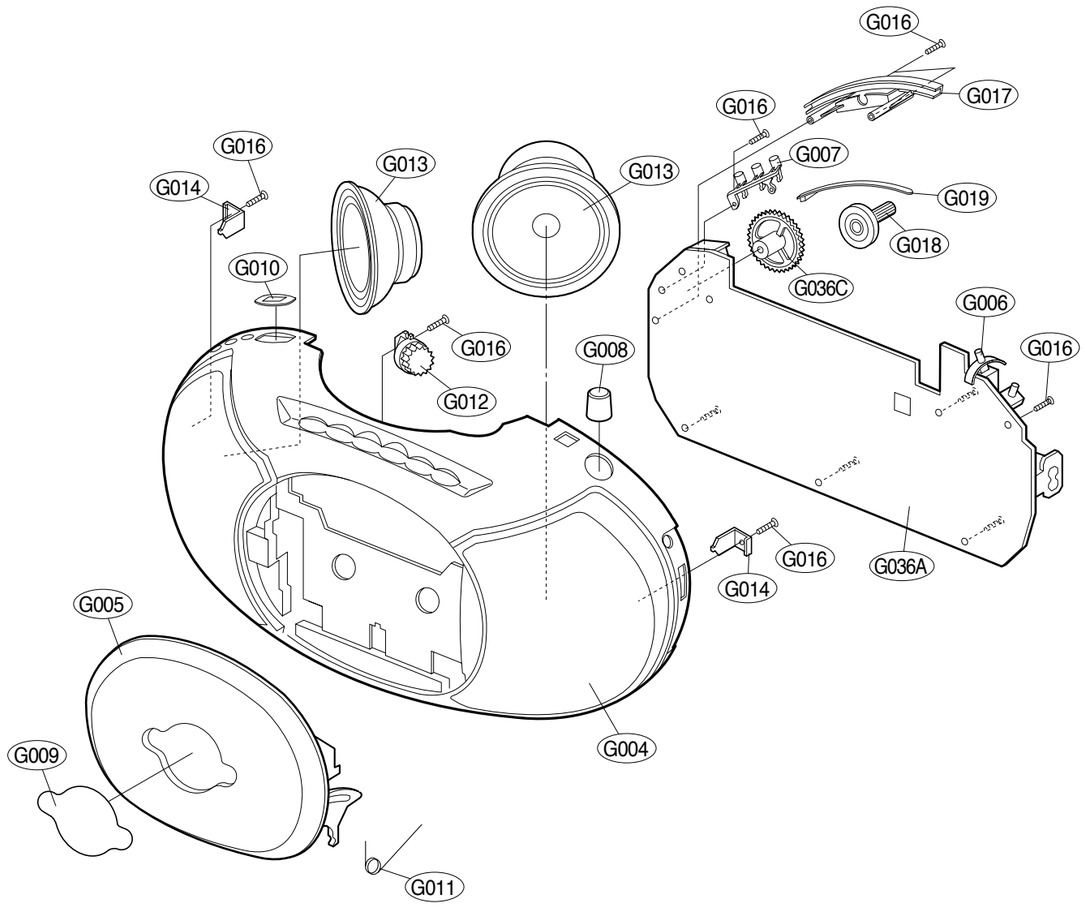
polarity	OLD NO	NEW NO	R1	R2	
NPN	KRC1203	KRC103M	22K	22K	
	KRC1210	KRC110M	4.7K	–	
	KRC111M	KRC111M	10K	–	
	KRC102M	KRC102M	10K	10K	
PNP	KRA2202	KRA102M	10K	10K	
	KRA2203	KRA103M	22K	22K	
	KRA2204	KRA104M	47K	47K	

*TR OLD NEW NO LIST

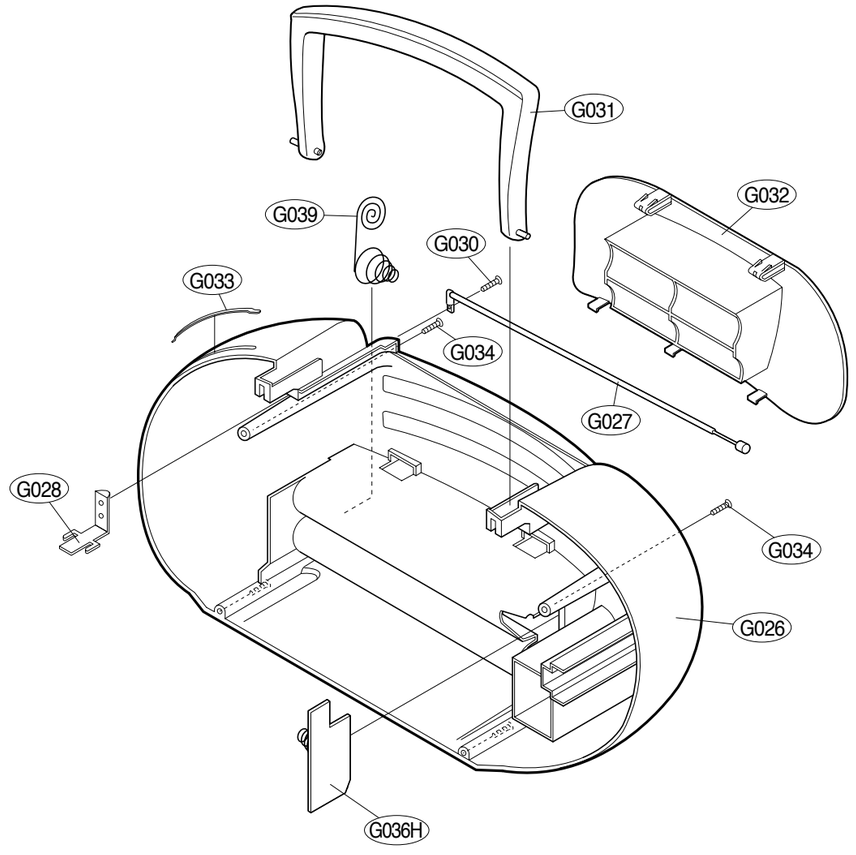
OLD NO	NEW NO
KTA1015	KTA1266
KTC1815	KTC3198
KTC1959	KTC3202
KTC732TMBL	KTC3198TMBL
KTB834	KTB988
KTC2236A	KTC3205
KTD2058	KTD2012
KTA966A	KTA1273

EXPLODED VIEW & PARTS LIST

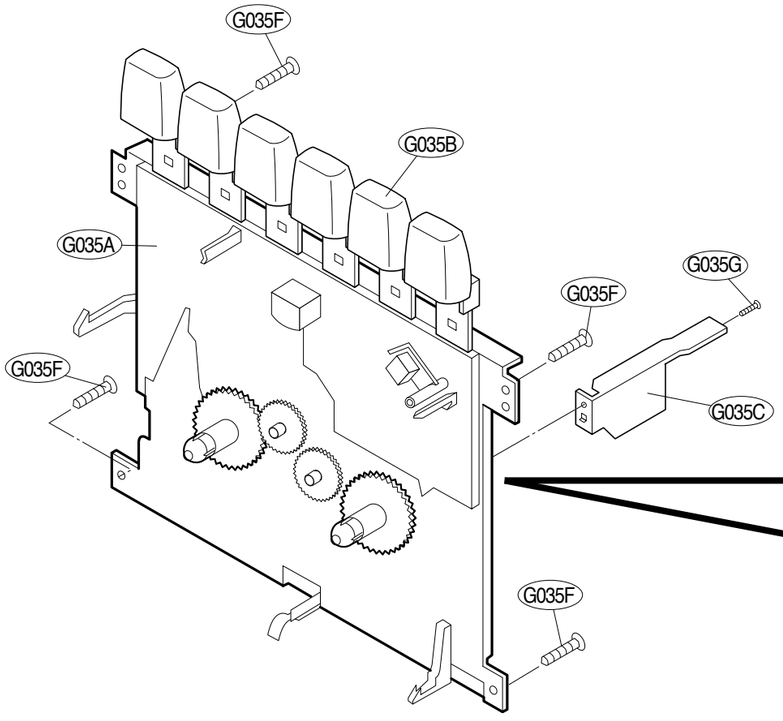
• FRONT SECTION

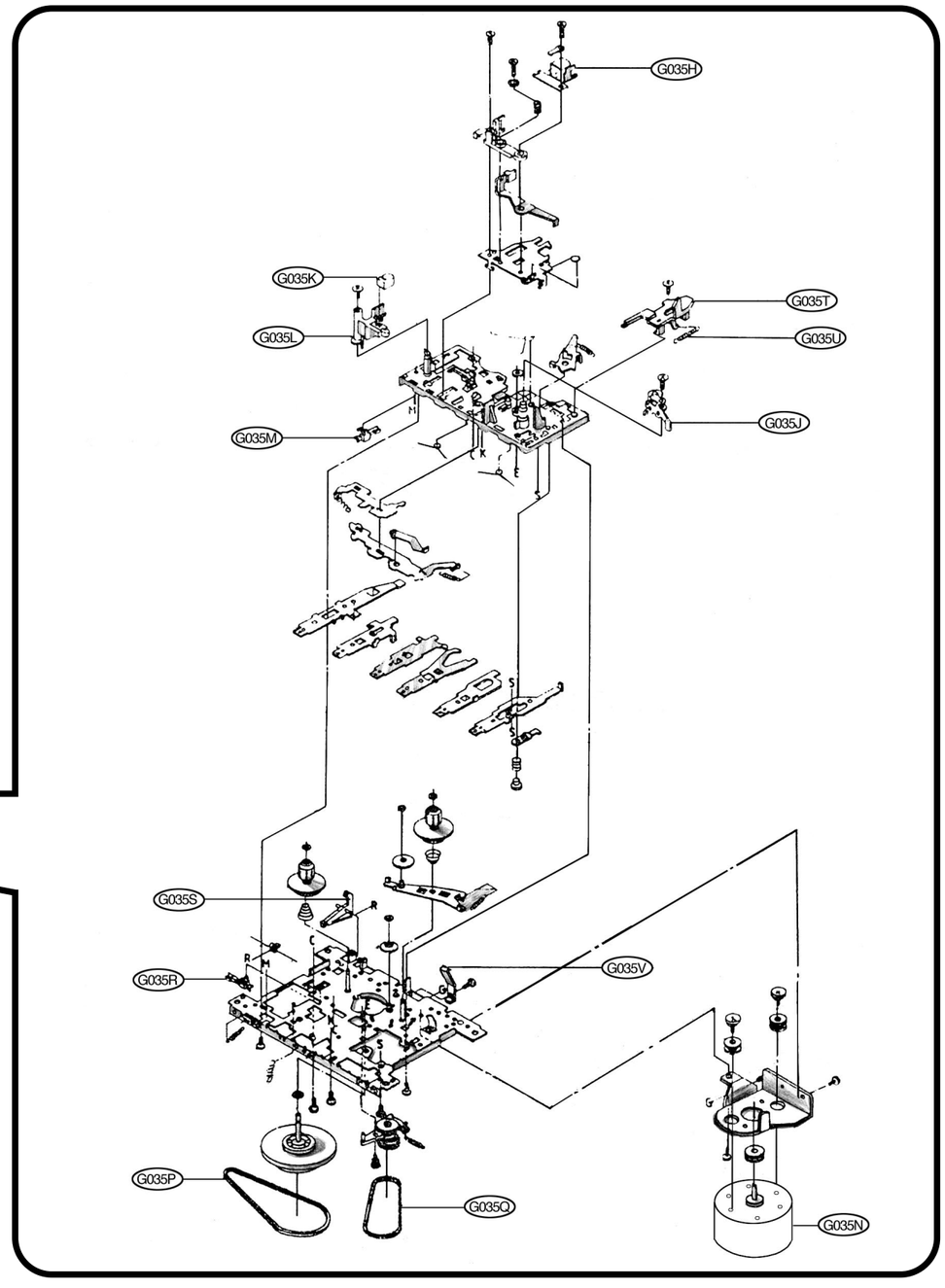


• REAR SECTION



• CASSETTE DECK SECTION





• CD PLAYER SECTION