Pin Description

PIN	NAME	FUNCTION
1	DCIN	DC Supply Voltage Input. Bypass DCIN with a 1µF capacitor to power ground.
2	LDO	Device Power Supply. Output of the 5.4V linear regulator supplied from DCIN. Bypass with a 1µF capacitor.
3	ACIN	AC Detect Input. This uncommitted comparator input can be used to detect the presence of the charger's power source. The comparator's open-drain output is the ACOK signal.
4	REF	4.2235V Voltage Reference. Bypass with a 1µF capacitor to GND.
5	GND	MAX1909: Ground this pin
	$\overline{\text{PKPRES}}$	MAX8725: Pull $\overline{\text{PKPRES}}$ high to disable charging. Used for detecting presence of battery pack.
6	ACOK	AC Detect Output. High-voltage open-drain output is high impedance when ACIN is greater than 2.048V. The ACOK output remains a high impedance when the MAX1909/MAX8725 are powered down.
7	MODE	Trilevel Input for Setting Number of Cells and Asserting the Conditioning Mode: MODE = GND; asserts conditioning mode. MODE = float; charge with 3 times the cell voltage programmed at VCTL. MODE = LDO; charge with 4 times the cell voltage programmed at VCTL.
8	IINP	Input Current Monitor Output. The current delivered at the IINP output is a scaled-down replica of the system load current plus the input-referred charge current sensed across CSSP and CSSN inputs. The transconductance of (CSSP - CSSN) to IINP is 3mA/V.
9	CLS	Source Current-Limit Input. Voltage input for setting the current limit of the input source.
10	ICTL	Input for Setting Maximum Output Current
11	VCTL	Input for Setting Maximum Output Voltage
12	CCI	Output Current-Regulation Loop-Compensation Point. Connect 0.01µF to GND.
13	CCV	Voltage-Regulation Loop-Compensation Point. Connect 10kΩ in series with 0.1µF to GND.
14	CCS	Input Current-Regulation Loop-Compensation Point. Use 0.01µF to GND.
15	GND	Analog Ground
16	BATT	Battery Voltage Feedback Input
17	CSIN	Output Current-Sense Negative Input
18	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
19	PGND	Power Ground
20	DLO	Low-Side Power-MOSFET Driver Output. Connect to low-side NMOS gate. When the MAX1909/MAX8725 are shut down, the DLO output is LOW.
21	DLOV	Low-Side Driver Supply. Bypass with a 1µF capacitor to ground.
22	DHIV	High-Side Driver Supply. Bypass with a 0.1µF capacitor to SRC.
23	DHI	High-Side Power-MOSFET Driver Output. Connect to high-side PMOS gate. When the MAX1909/MAX8725 are shut down, the DHI output is HIGH.
24	SRC	Source Connection for Driver for PDS/PDL Switches. Bypass SRC to power ground with a 1µF capacitor.
25	CSSN	Input Current Sense for Charger (Negative Input)
26	CSSP	Input Current Sense for Charger (Positive Input). Connect a current-sense resistor from CSSP to CSSN.
27	PDS	Power-Source PMOS Switch Driver Output. When the MAX1909/MAX8725 are powered down, the PDS output is pulled to SRC through an internal 1MΩ resistor.
28	PDL	System-Load PMOS Switch Driver Output. When the MAX1909/MAX8725 are powered down, the PDL output is pulled to ground through an internal 100kΩ resistor.