

FAN8045G3

4-CH Motor Driver (5 Input & 4 Output)

Features

- 4-CH Balanced Transformerless (BTL) Driver
- Optional Input (CH4,5) For Output CH4
- Operating Supply Voltage : 4.5 V ~ 14V
- Built-in Thermal Shut Down Circuit (TSD)
- Built-in Channel Mute Circuit
- Built-in 1-OP AMP
- TSD Monitoring Function

Description

The FAN8045G3 is a monolithic integrated circuit suitable for a 4-CH motor driver which drives a tracking actuator, a focus actuator, a sled motor, a spindle motor, and a tray motor of the CDP/CAR-CD/DVDP systems.

28-SSOPH-375SG2



Typical Application

- Compact Disk Player
- Video Compact Disk Player
- Car Compact Disk Player
- Digital Video Disk Player

Ordering Information

Device	Package	Operating Temp.
FAN8045G3	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8045G3X ^{note1}	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8045G3_NL ^{note2}	28-SSOPH-375-SG2	-35°C ~ +85°C
FAN8045G3X_NL	28-SSOPH-375-SG2	-35°C ~ +85°C

Notes:

1. X : Tape&Reel
2. NL : Lead free

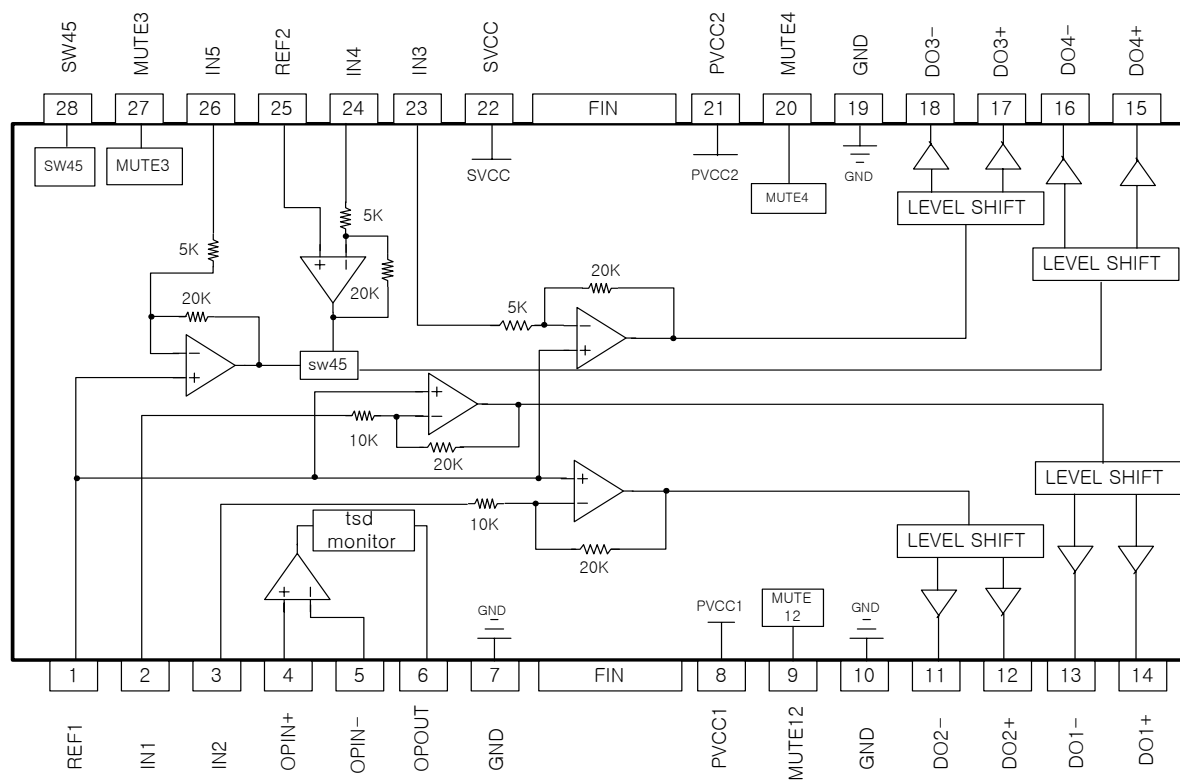
Pin Assignments



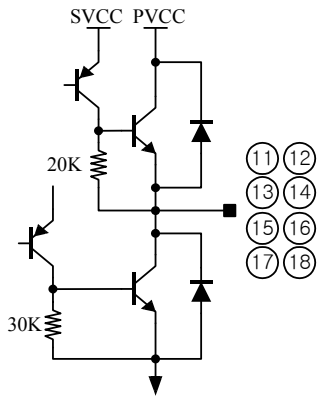
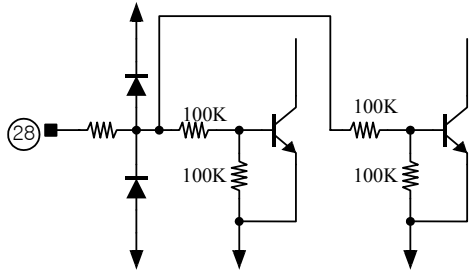
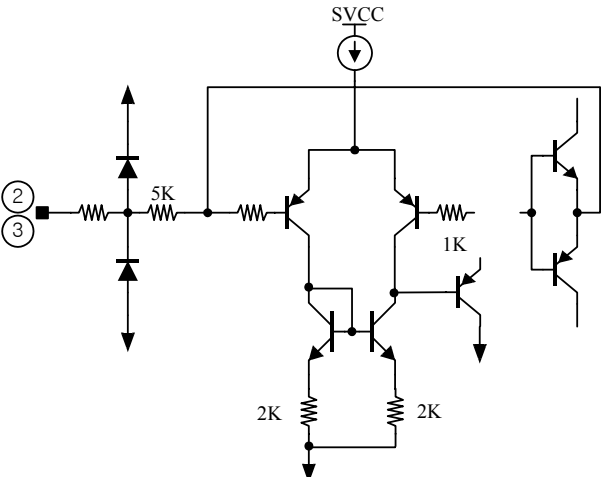
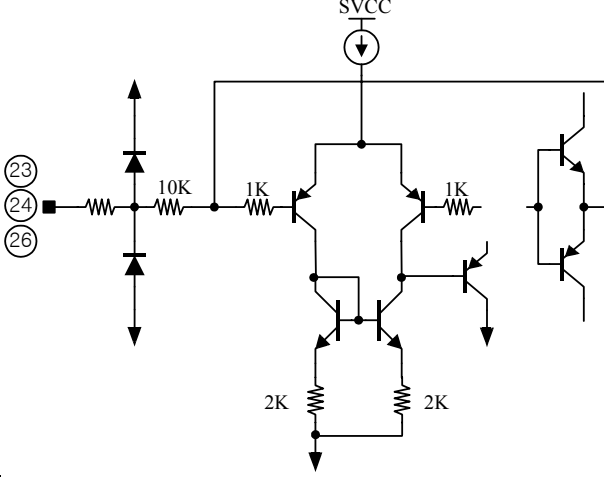
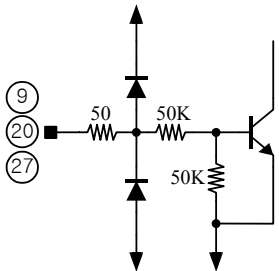
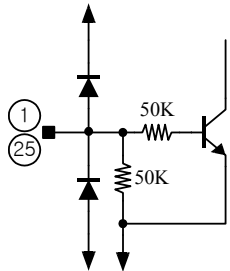
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	REF1	I	Bias Voltage Input
2	IN1	I	CH1 Input
3	IN2	I	CH2 Input
4	OPIN+	I	Nomal OP-AMP Input(+)
5	OPIN-	I	Nomal OP-AMP Input(-)
6	OPOUT	O	Nomal OP-AMP Output
7	GND	-	Signal Ground
8	PVcc1	-	Power Vcc (CH1,CH2)
9	MUTE12	I	Mute 1,2
10	GND	-	Power GND(CH1,CH2)
11	DO2-	O	CH2 Drive Output (-)
12	DO2+	O	CH2 Drive Output (+)
13	DO1-	O	CH1 Drive Output (-)
14	DO1+	O	CH1 Drive Output (+)
15	DO4+	O	CH4 Drive Output (+)
16	DO4-	O	CH4 Drive Output (-)
17	DO3+	O	CH3 Drive Output (+)
18	DO3-	O	CH3 Drive Output (-)
19	GND	-	Power GND(CH3,CH4)
20	MUTE4	I	Mute 4
21	PVcc2	-	Power Vcc (CH3,CH4)
22	SVcc	-	Signal Vcc
23	IN3	I	CH3 Input
24	IN4	I	CH4 Input
25	REF2	I	REF2
26	IN5	I	CH5 Input
27	MUTE3	I	Mute 3
28	SW45	I	Select Switch For 4,5CH

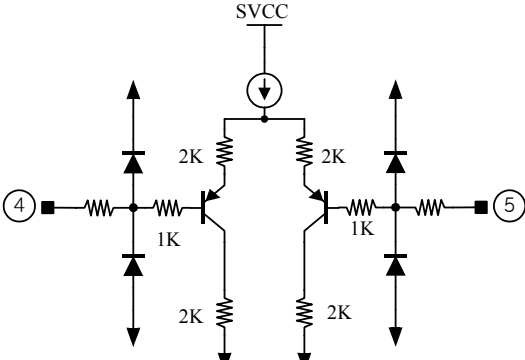
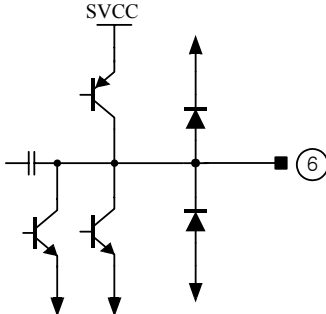
Internal Block Diagram



Equivalent Circuits

BTL Driver Output	SW45
	
BTL Input(CH1,2)	BTL Input(CH3,4)
	
Mute	Reference
	

Equivalent Circuits (Continued)

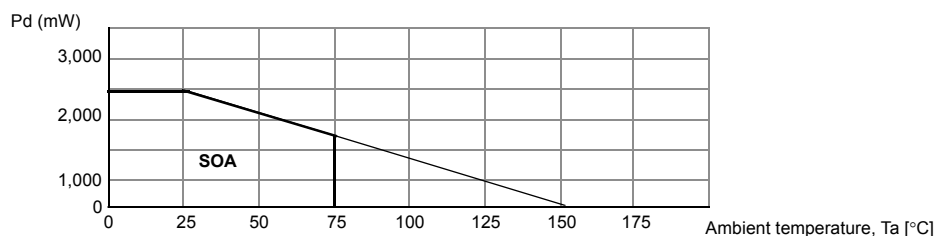
OP-AMP Input	OP-AMP Output
 The diagram shows the input equivalent circuit of the OP-AMP. It features a differential input stage with two NPN transistors. The bases are connected to input nodes 4 and 5 through 1K resistors. Each base is also connected to a 2K resistor leading to a diode stack (two diodes in series) and a 2K resistor leading to ground. The emitters are connected to a common emitter node, which is biased by a current source (represented by a circle with a downward arrow) connected to an SVCC supply. The collector nodes are connected to 2K resistors leading to another diode stack and a 2K resistor leading to ground.	 The diagram shows the output equivalent circuit of the OP-AMP. It features a common-emitter output stage with an NPN transistor. The base is connected to a diode stack (two diodes in series) and a 2K resistor leading to ground. The emitter is connected to a common emitter node, which is biased by a current source (represented by a circle with a downward arrow) connected to an SVCC supply. The collector is connected to a 2K resistor leading to another diode stack and a 2K resistor leading to ground. The output node 6 is connected to the collector through a 1K resistor.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	SVCCMAX	18	V
	PVCC1MAX	18	V
	PVCC2MAX	18	V
Power Dissipation	PD	2.5 ^{note1,2,3}	W
Operating Temperature	TOPR	−35 ~ +85	°C
Storage Temperature	TSTG	−55 ~ +150	°C
Maximum Output Current	IOMAX	1	A

Notes:

1. When it is mounted on 70mm × 70mm × 1.6mm PCB.
2. Power dissipation decreases at the rate of 20mW/°C in T_A >25°C.
3. Do not exceed P_D and SOA.



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	SVCC	4.5	-	14	V
	PVCC1	4.5	-	SVCC	V
	PVCC2	4.5	-	SVCC	V

Electrical Characteristics

(SVCC = PVCC2 = 12V, TA = 25°C, PVCC1 = 5V, Ref1 = 1.65V, Ref2 = 2.5V, RL = 8Ω)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent Circuit Current	ICC	Under no-load	-	17	25	mA
BTL DRIVER CIRCUIT (RL=8Ω)						
Output Offset Voltage(CH12)	VOOF1	VIN=1.65V	-50	-	+50	mV
Output Offset Voltage(CH34)	VOOF2	VIN=1.65V	-100	-	+100	mV
Output Offset Voltage(CH5)	VOOF3	VIN=2.5V	-100	-	+100	mV
Maximum Output Voltage(CH12)	VOM1	PVcc1=5V, RL=8Ω	3.6	4.0	-	V
Maximum Output Voltage(CH34)	VOM2	PVcc2=12V, RL=24Ω	9.6	10.5	-	V
Close-loop Voltage Gain(CH12)	AvF	VIN= 0.3V	15.5	17.5	19.5	dB
Close-loop Voltage Gain(CH34)	AvF	VIN= 0.3V	21.5	23.5	25.5	dB
NORMAL OPAMP CIRCUIT(SVCC,PVCC2=12V)						
Input Offset Voltage	VOF	-	-10	-	+10	mV
Input Bias Current	IB1	-	-	-	300	nA
High Level Output Voltage	VOH1	-	11	-	-	V
Low Level Output Voltage	VOL1	-	-	-	0.1	V
Output Sink Current	ISINK	-	5	8	-	mA
Output Source Current	ISOU1	-	1	5	-	mA
Open Loop Voltage Gain	GVO1	f=1kHz, VIN= -75dB	-	75	-	dB
Ripple Rejection Ratio ^{note1}	RR1	f=120Hz, VIN= -20dB	-	65	-	dB
Slew Rate ^{note1}	SR1	f=120Hz, 2Vp-p	-	1	-	V/us
Common Mode Rejection Ratio ^{note1}	CMRR1	f=1kHz, VIN= -20dB	-	80	-	dB
TSD ON Voltage ^{note1}	Vtsdon	-	-	-	0.5	V
MUTE AND OTHER FUNCTION CIRCUIT						
Mute On Voltage	VMON	Pin9,20,27=Variation	-	-	0.5	V
Mute Off Voltage	VMOFF	Pin9,20,27=Variation	2	-	-	V
SW On Voltage	VSWL	Pin28=Variation	-	-	0.5	V
SW Off Voltage	VSWH	Pin28=Variation	2	-	-	V
Mute Low Level Sink Current	IMTL	VMUTE = 0V	-15	0	15	uA
Mute High Level Sink Current	IMTH	VMUTE = 5V	-	85	170	uA
SW45 Low Level Sink Current	ISWL45	SW45 = 0V	-15	0	15	uA
SW45 High Level Sink Current	ISWH45	SW45 = 5V	-	85	170	uA
REF1 Sink Current	IRL	REF1 = 1.65V	-	52	104	uA
REF2 Sink Current	IRH	REF2 = 2.5V	-	85	170	uA

Note:

1.Guaranteed field. (No EDS/ Final test .)

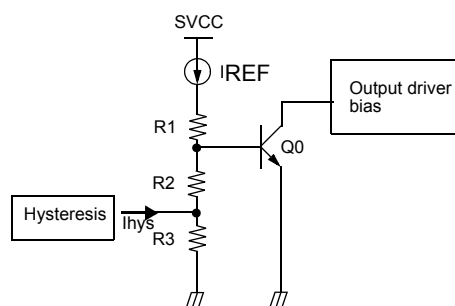
Application Information

1. MUTE, REF & SW45 Function

INPUT						OUTPUT					
SW45	MUTE12	MUTE3	MUTE4	REF1	REF2	BTL			PRE-AMP		OP
						CH12	CH3	CH4	CH4	CH5	
H	H	H	-	H	-	ON	ON	IN5	ON	ON	ON
H	H	L	-	H	-	ON	OFF	IN5	ON	ON	ON
H	H	H	-	L	-	OFF	OFF	OFF	OFF	ON	OFF
H	L	H	-	H	-	OFF	ON	OFF	ON	ON	ON
H	L	L	-	H	-	OFF	OFF	OFF	ON	ON	ON
L	-	-	L	-	-	OFF	OFF	OFF	OFF	ON	OFF
L	-	-	H	-	H	OFF	OFF	IN4	OFF	ON	OFF
L	-	-	H	-	L	OFF	OFF	OFF	OFF	ON	OFF

2. TSD Function

- When the chip temperature reaches to 167°C by abnormal condition, the TSD circuit is activated
- During TSD Function is activated, OP-AMP Output (pin 6) remains below 0.5V. (TSD monitoring function).
- This makes the bias current of the output drivers shut down, and all the output drivers are on cut-off state. Therefore the chip temperature begins to decrease.
- When the chip temperature falls to 63°C, the TSD circuit is deactivated and the output drivers start to operate normally.

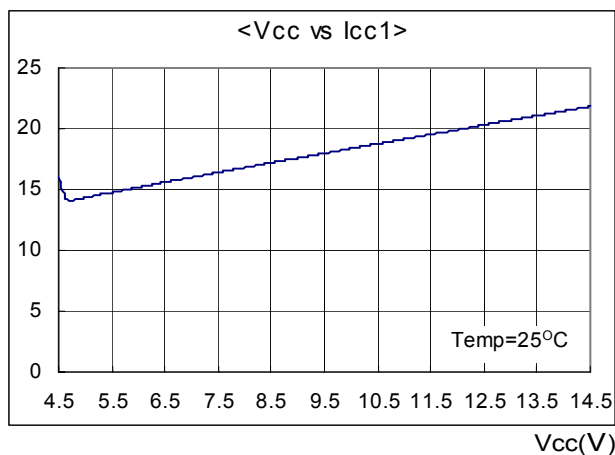
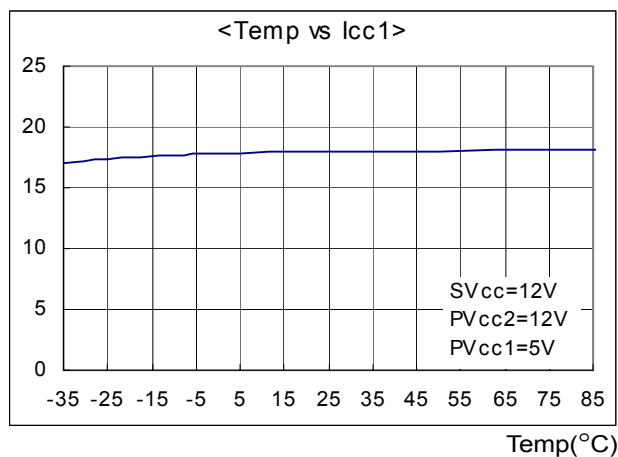


3. Notice

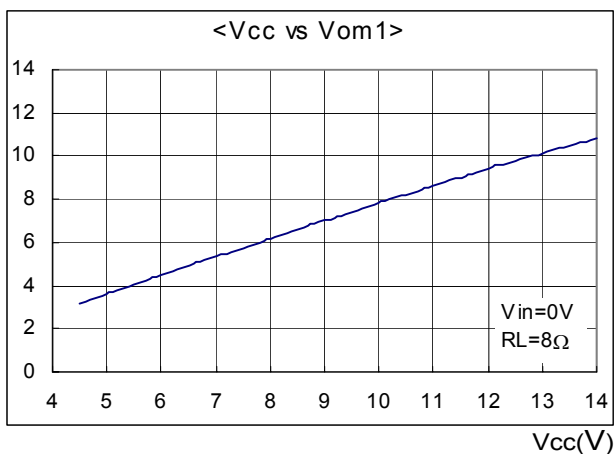
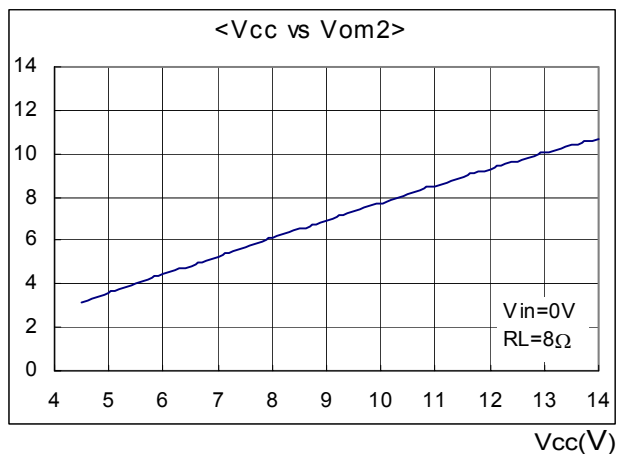
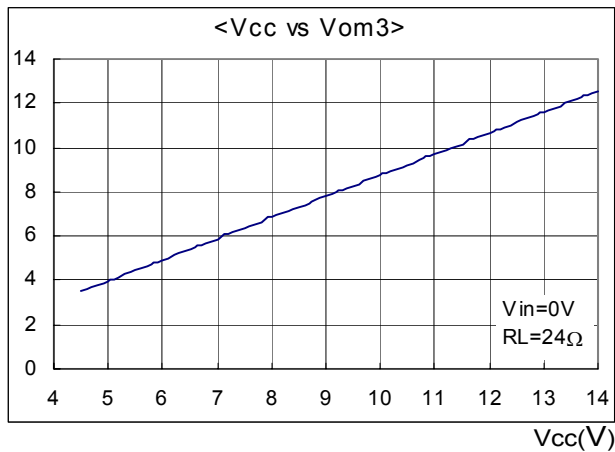
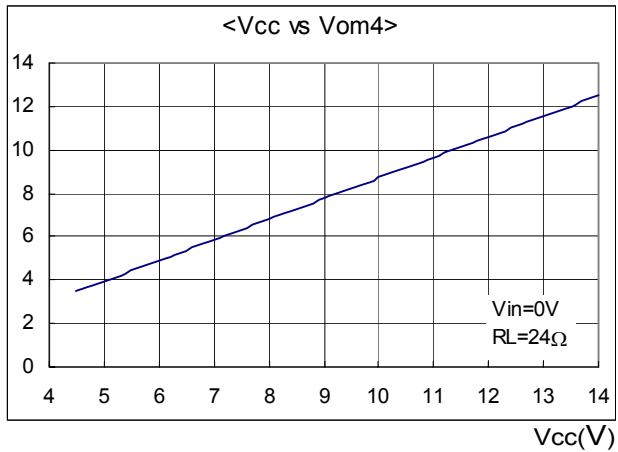
- If REF1(pin1) or REF2(pin25) is lower than 0.7V, BTL Output is off.
- Under Voltage Protection Function. (If SVcc is lower than 3.8V, Chip is disable. Hysteresis is 0.2V)
- Mute ON BTL OutPut Voltage is as followed:
 - Mute ON BTL Output (CH1,2) = (PVcc1) / 2
 - Mute ON BTL Output (CH3,4) = ((PVcc2-0.6) / 2
- Each output to output and output to GND short should be kept away.

Typical Performance Characteristics

Total Circuit

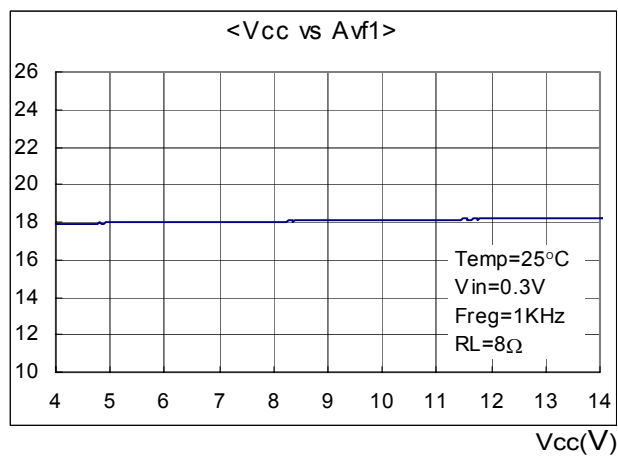
I_{cc}(mA)I_{cc}(mA)

BTL Drive Part

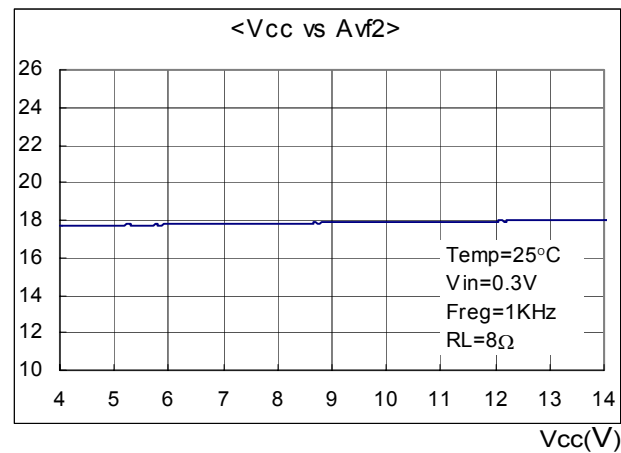
V_{om}(V)V_{om}(V)V_{om}(V)V_{om}(V)

Typical Performance Characteristics (Continued)

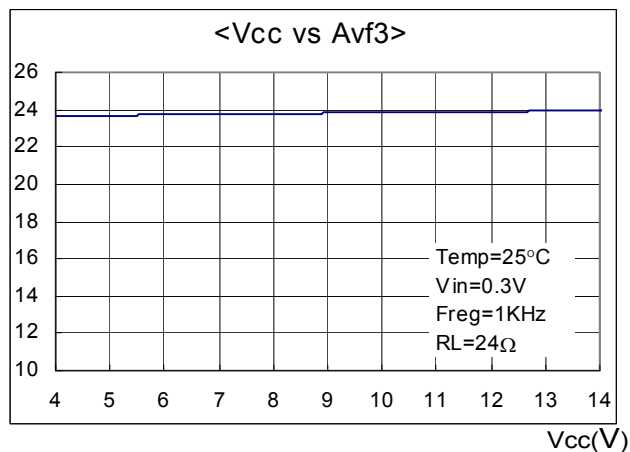
Avf(dB)



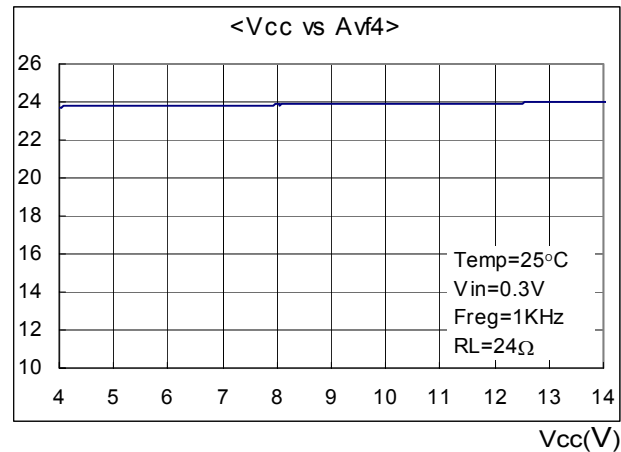
Avf(dB)



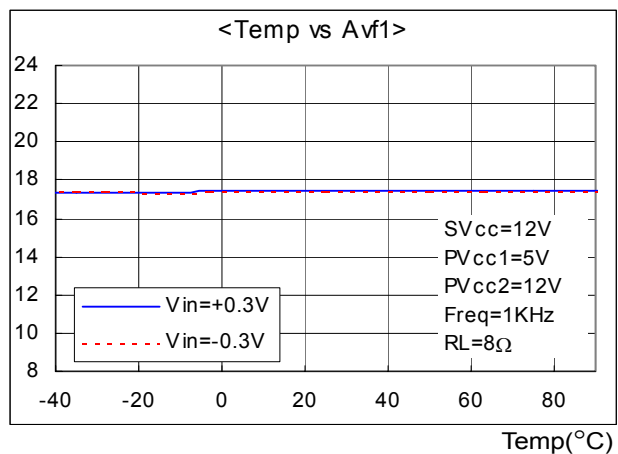
Avf(dB)



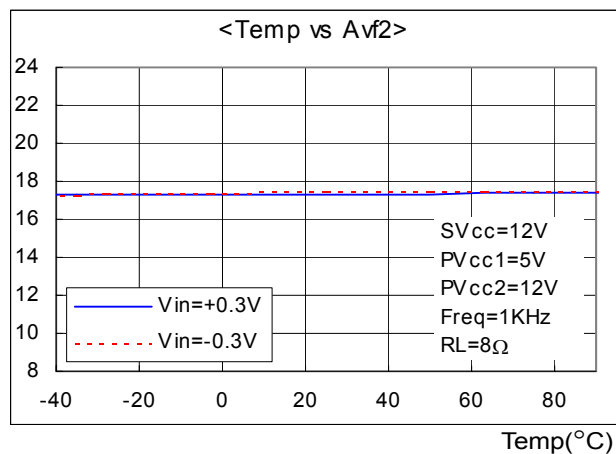
Avf(dB)



Avf(dB)

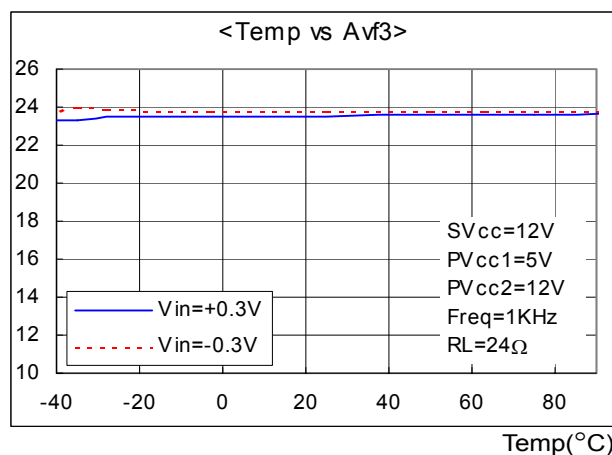


Avf(dB)

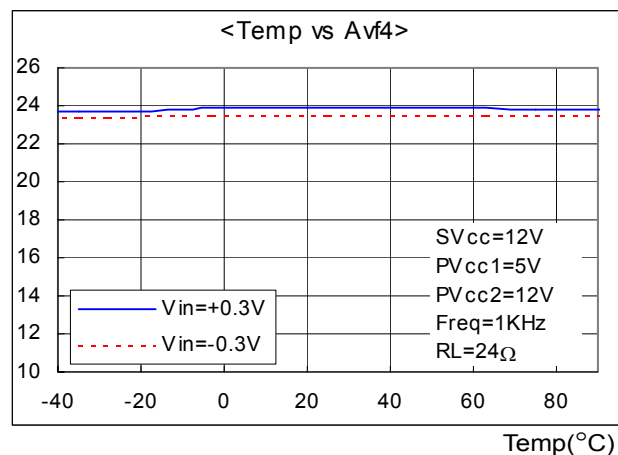


Typical Performance Characteristics (Continued)

Avf(dB)

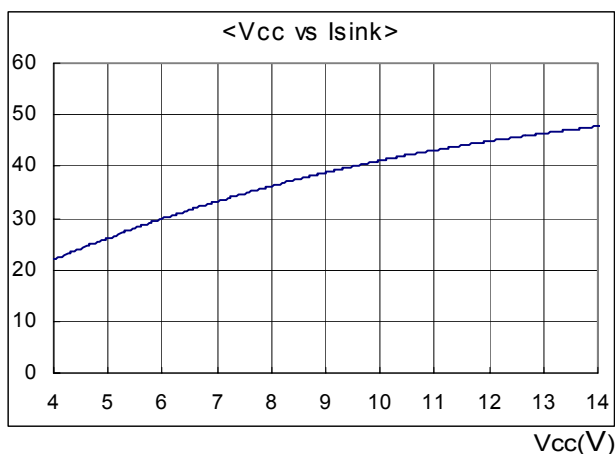


Avf(dB)

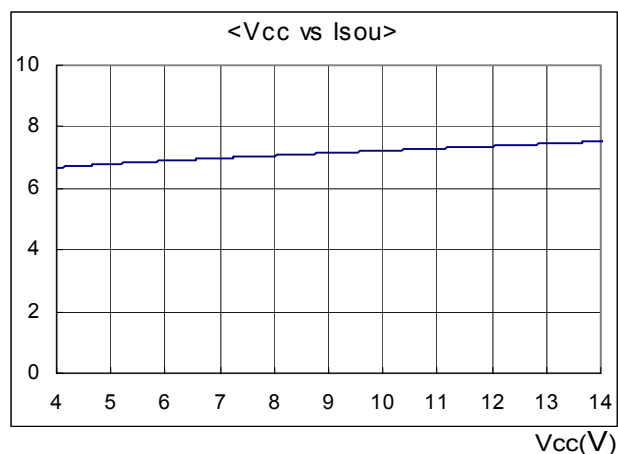


OP-AMP Part

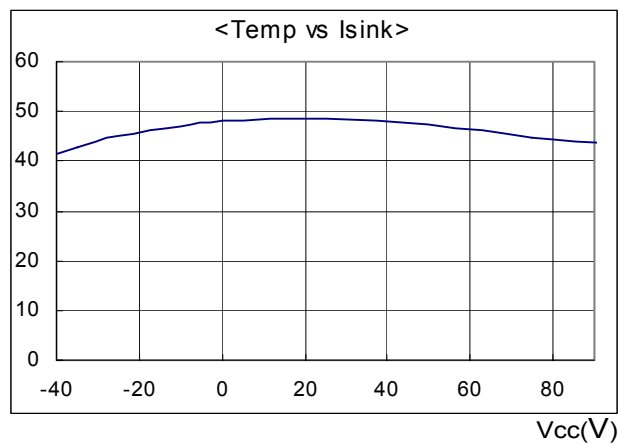
Isink(mA)



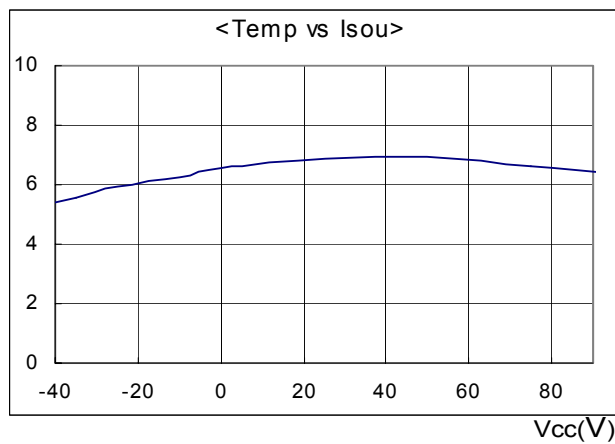
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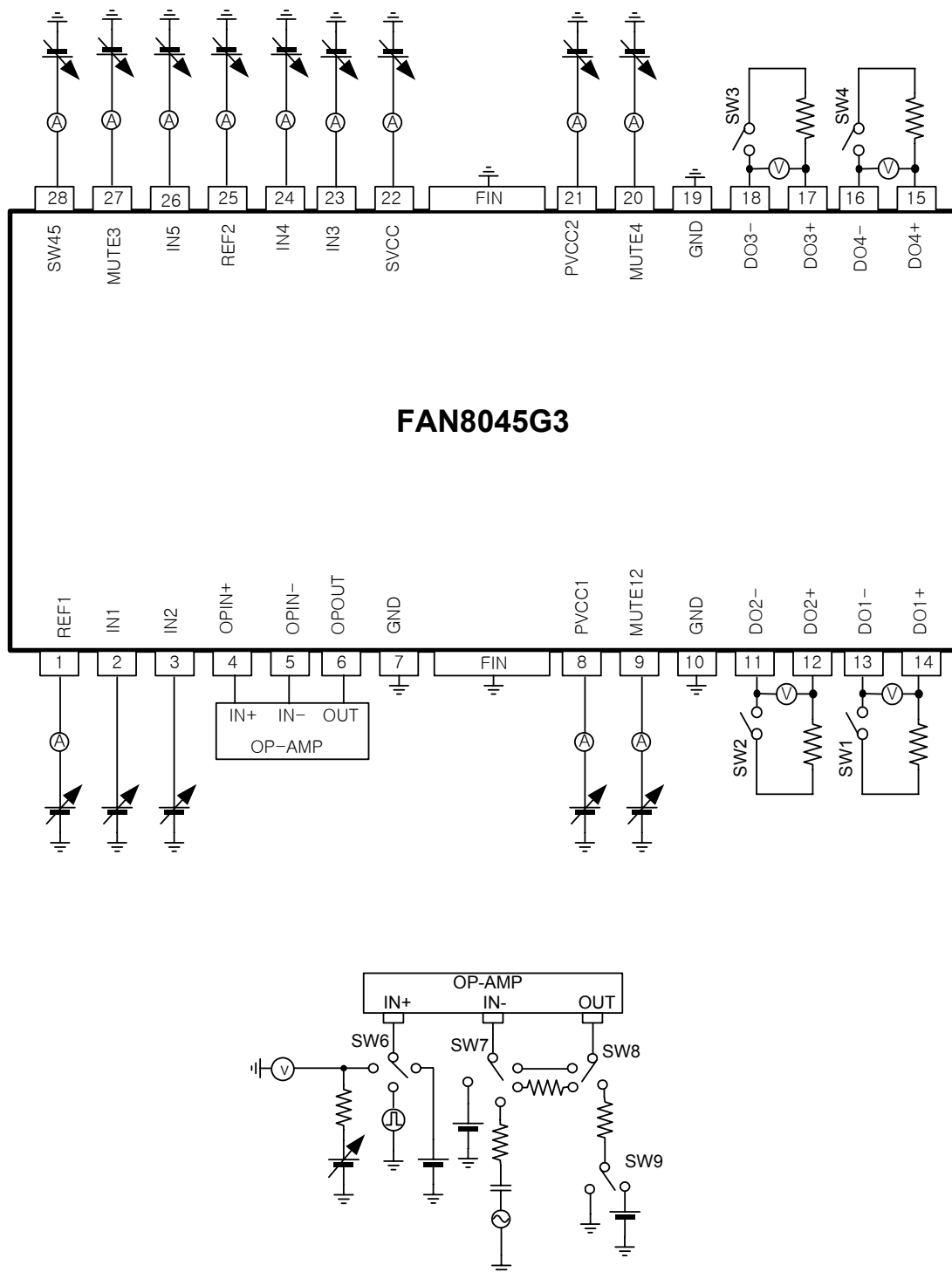
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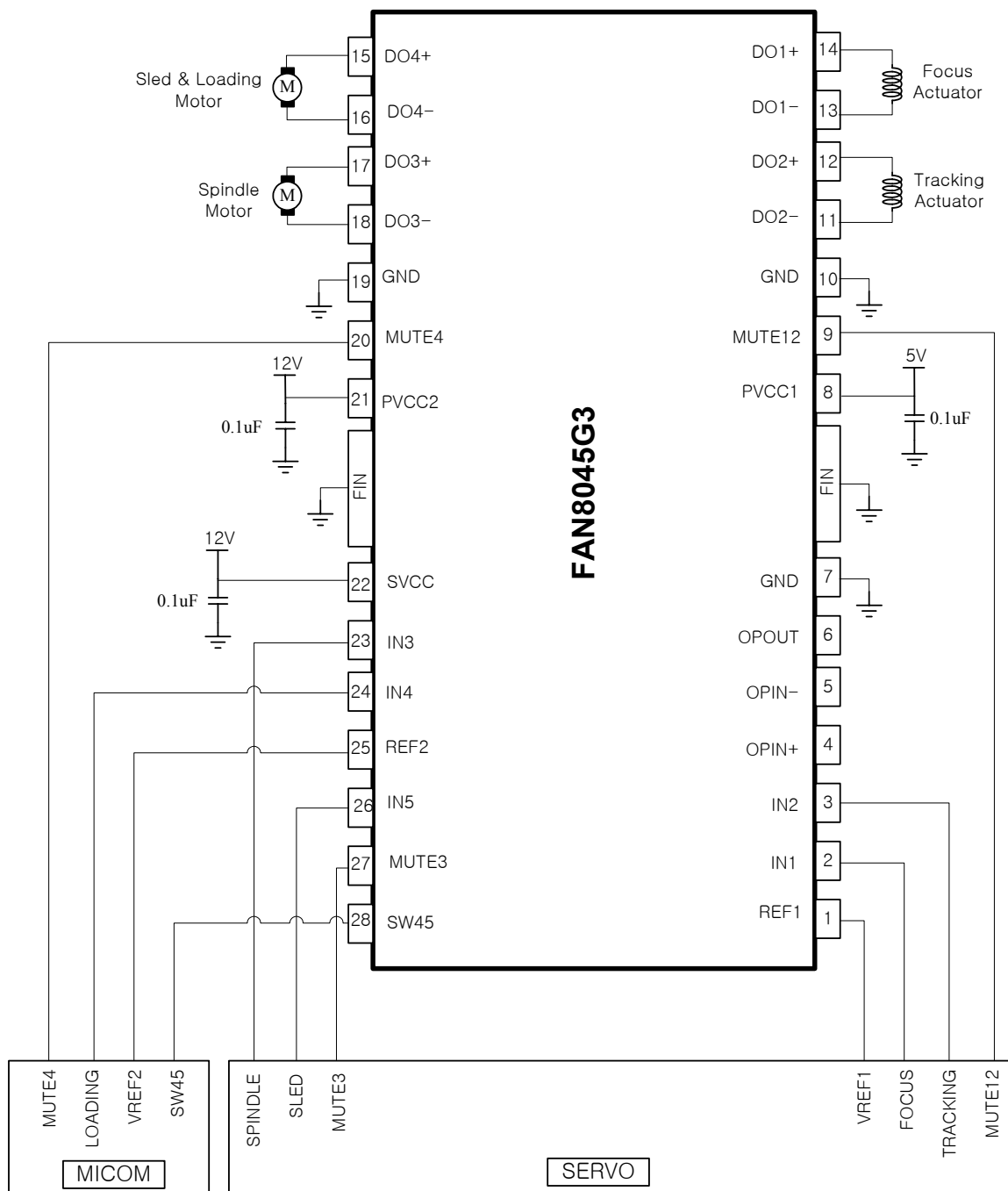
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Test Circuits

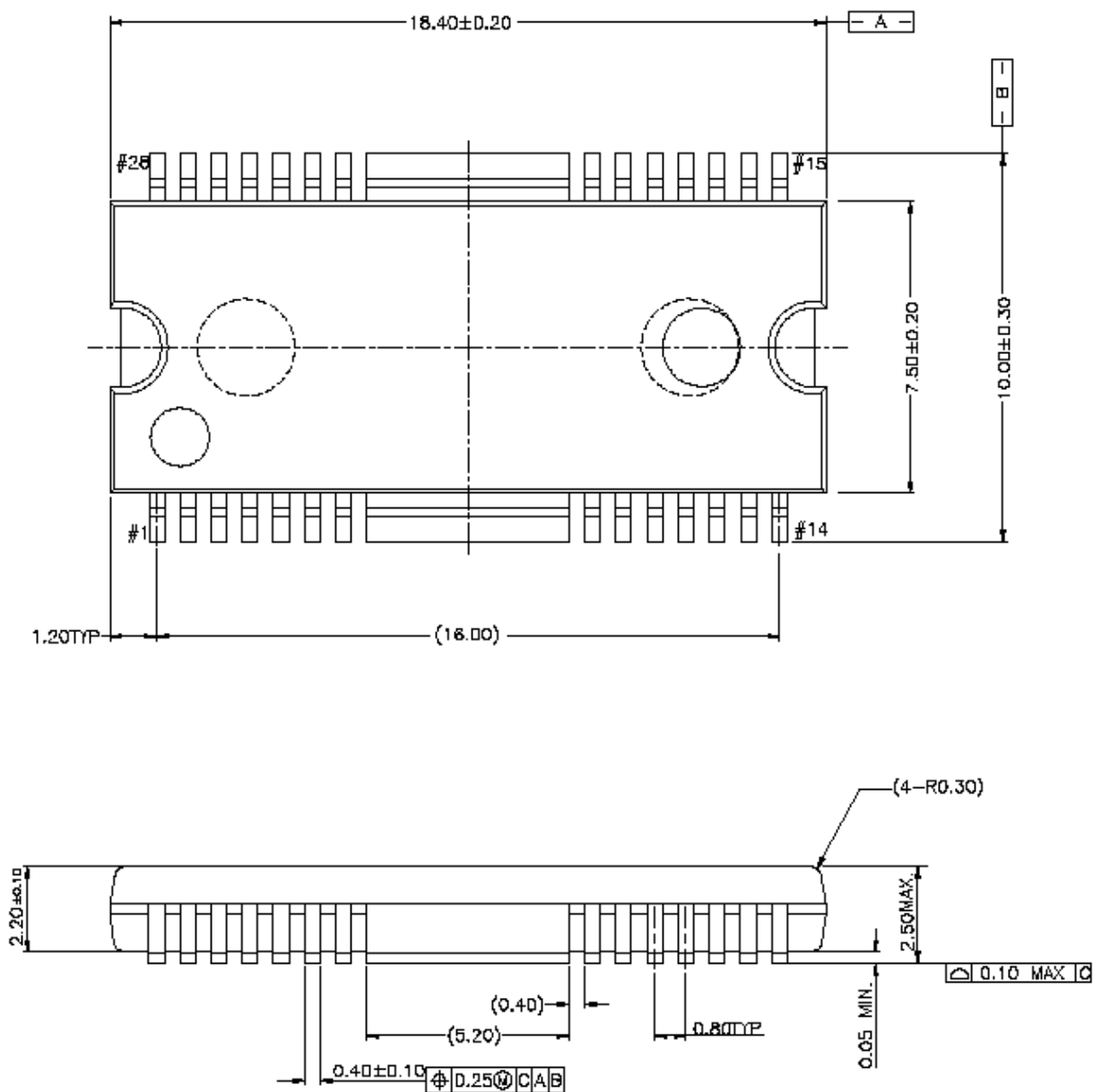


Typical Application Circuit



Package Dimension

28-SSOPH-375-SG2



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