Description of Demodulator IC U501 (SAA7011)
(See Figs. 8.1.14 — 8.1.16.)

Pin Description of Demodulator IC:

Pin No.	Signal Name	In/ Out	Description
1	VBB	In	—2.5 V. Back bias supply.
2	SDATA	Out	Push-pull output for subcoding data. An 8 bit burst of data (including a 1 bit subcoding frame sync) is output serially once per frame coincident with SBCL.
3	SBCL	Out	Push-pull output for subcoding bit clock. An 8 bit burst clock at nominally 2.1609 MHz which is used to synchronize the subcoding data.
4	SWCL	Out	Push-pull output for subcoding word clock. A square wave signal at data frame rate (7.35 kHz) used to synchronize the subcoding words and the pause (P) bit.
5	P	Out	Push-pull output for the subcoding pause bit. This signal is derived from the encoded subcoding word and is used to indicate a music pause. A debounce circuit is incorporated to eliminate erroneous data.
6	HFD	In	Input from external high frequency detector. When this signal is high the frequency detector output (FD) and phase detector are enabled. (This input is kept High.)
7	HFI	In	Non-inverting input to the level detector. A differential signal of between 0.5 V and 2.5 V peak-peak is required between pins 7 and 8 to drive the level detector correctly.
8	$\overline{\text{HFI}}$	In	Inverting input to the level detector.
9	$\overline{\text{FB}}$	Out	Inverted feedback output from the level detector. These outputs ($\overline{\text{FB}}$ and FB) have a nominal impedance of 10 kΩ and will default to 1/2 VDD1 when a dropout is sensed.
10	FB	Out	Non-inverted feedback output from the level detector (see $\overline{\text{FB}}$).
11	DEFM	Out	Push-pull output for EFM (Eight-to-Fourteen Modulation) data after it has passed through the level detector. (This pin is not used.)
12	PD2	Out	Phase detector output signal. These outputs (PD1 and PD2) have a nominal impedance of 10 kΩ and the differential DC content of the signals is a measure of the phase difference between the data and the internal 4.3218 MHz clock.
13	PD1	Out	Phase detector reference signal. (see PD2.)
14	VSSD	—	Digital ground. Main ground terminal.
15	VDD2	In	+12 V supply.
16	OA1	In	Non-inverting input to the operational amplifier.
17	OA2	In	Inverting input to the operational amplifier.
18	OA3	Out	Source follower output of the operational amplifier.
19	VSSA	—	Analog ground. Ground terminal for operational amplifier only. Connected internally to VSSD via a nominal 25 Ω resistor.
20	VCO1	In	Input to voltage controlled oscillator amplifier. The amplifier is a simple inverter designed for up to 10 MHz operation. The frequency control is achieved via an external "Varicap" tuned circuit.
21	VCO2	Out	Output from voltage controlled oscillator amplifier. The load for the inverting transistor may be turned off for test purposes by reducing VDD2 to 0 V.
22	$\overline{\text{CEFM}}$	Out	A push-pull output from the internal 4.3218 MHz clock generator. (This pin is not used.)
23	FD	Out	Three state push-pull output from the frequency detector. This output has a nominal 1 kΩ impedance when active but assumes a high impedance state once the system is in lock.
24	FSDE	Out	Push-pull output for frame sync signal to the Error Corrector IC U504. A positive going pulse occurring at the end of each data frame (nominal frequency 7.35 kHz).
25	$\overline{\text{SSDE}}$	Out	Push-pull output for symbol sync signal to the Error Corrector IC U504. A negative going pulse occurring during the last bit of each data symbol (nominal frequency 254 kHz).
26	$\overline{\text{CLDE}}$	Out	Push-pull output for data bit clock to the Error Corrector IC U504. An 8 bit burst clock at nominally 2.1609 MHz which is used to synchronize the data to U504.
27	DADE	Out	Push-pull output for data to the Error Corrector IC U504. Serial data consisting of 32 x 8 bit symbols per frame which is synchronized to $\overline{\text{CLDE}}$.
28	VDD1	In	+5 V supply.

General Description of Demodulator IC:

The SAA7011 Demodulator IC forms the front-end of the compact disc digital audio decoding system, supplying demodulated data and timing signals to the Error Corrector SAA7020 and the subcoding microprocessor.

The detected signal from the disc is amplified and filtered externally and then converted to a digital signal via the level detector. This is an adaptive data slicer which relies on the nature of the modulation system to determine the optimum slicing level.

A frequency detector and a phase detector provide the coarse and fine control signals for the phase locked loop (PLL) system. The gain is supplied by an internal operational amplifier which drives a voltage controlled oscillator (VCO) running at twice the input data rate which is nominally 4.3218 MHz. The oscillator output is divided by 2 within the main clock generator which then clocks the input shift register and the timing chain. This clock signal completes the PLL loop when it is compared with the incoming data in the phase detector.
After the phase detector the data is clocked into the 23 bit input shift register to enable the frame sync pattern to be detected. Also, a minimum and maximum data length detector provides frequency limit signals (Tmin and Tmax) for the frequency detector.

The frame sync signal is used to reset the ÷588 slave-counter which, together with a ÷17 symbol rate counter, supplies timing signals for clocking the Eight-to-Fourteen Modulation (EFM) decoder and the subcoding outputs. The data is read from the input shift register in symbols of 14 bits which are latched and then decoded into 8 bit data words. The subcoding part consists of only one word per frame (see Fig. 8.1.15), therefore the output (SDATA) is a burst of 8 bits of data accompanied by a 2.1609 MHz burst clock signal (SBCL) (see Fig. 8.1.16). One bit of this subcoding output data is replaced by a subcoding frame sync bit (SF) which is decoded from either of two special EFM codes. The displaced bit is known as the Pause or P bit and is latched to its own output via a debounce circuit to remove erroneous changes.

The ÷588 slave counter also provides a sync coincidence pulse which occurs when two detected sync pulses are precisely one frame length apart (588 clock cycles). This is used by the lock indication counter as an "in-lock" signal to reset the counter and disable the frequency detector output (FD). If the system goes out of lock for any reason and the sync pulses cease then the lock indication counter will count frame periods and after 63 frames will enable the frequency detector output.

The sync coincidence pulse is also used via a delay line to reset the protected ÷588 master counter. The counter is prevented from accidental reset by erroneous sync patterns by accepting only coincident sync pulses or sync pulses which occur during a predetermined "window" at the beginning of each frame. This window is wide enough to allow for PLL bit slips, but narrow enough to avoid false sync signals generated by corrupt data.

The ÷588 master counter, together with a second ÷17 symbol rate counter, is used to time the data and clock signals to the Error Corrector SAA7020 (see Fig. 8.1.16). In this way, even if the data has been corrupted, the timing signals are correct and only re-synchronized after a complete frame has been sent to the Error Corrector.

The data to the Error Corrector (DADE) consists of 32 x 8-bit symbols per frame with half bit gaps between each symbol and a much longer gap during the frame sync period. It is this longer gap that will change in length when corrupt data upsets the timing system.

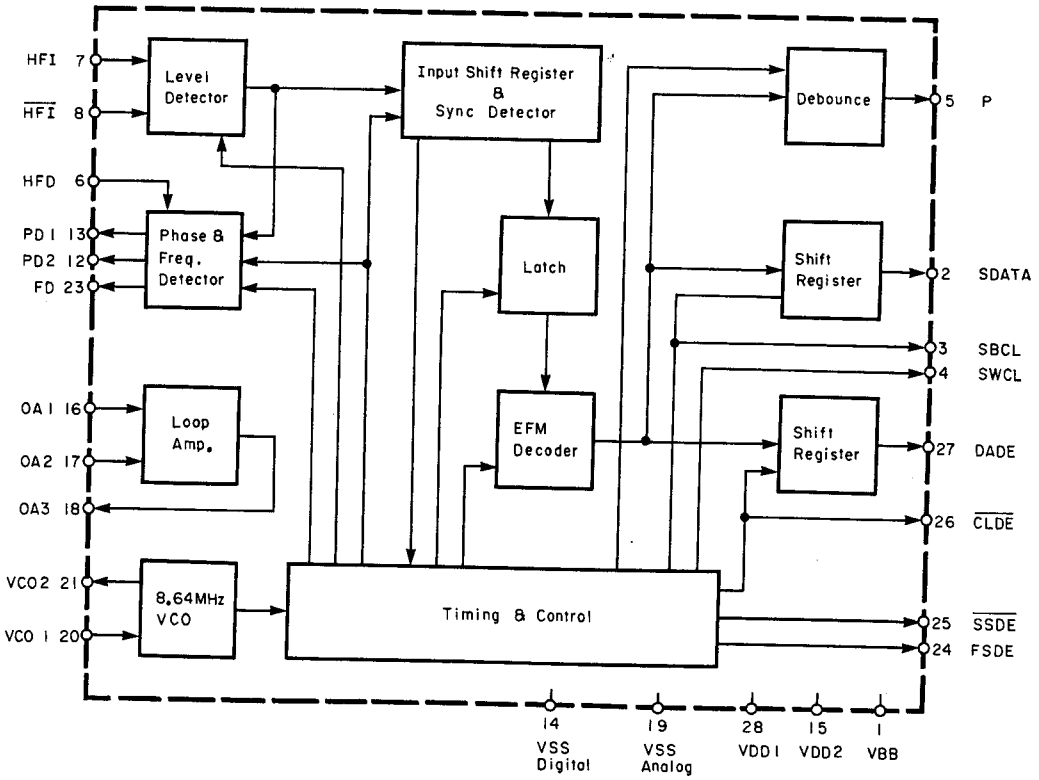

Fig. 8.1.14 Demodulator IC SAA7011

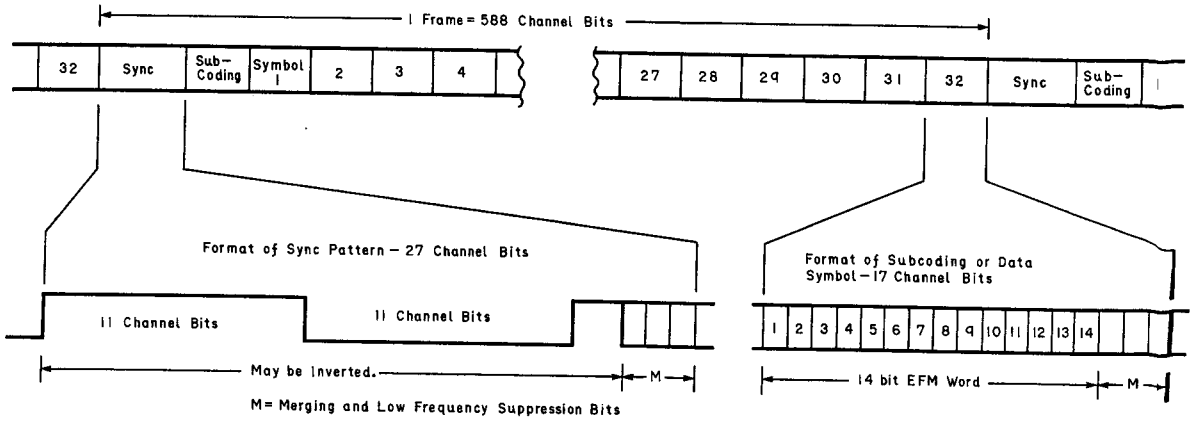

Fig. 8.1.15 Input Waveform to HF Pin (SAA7011)

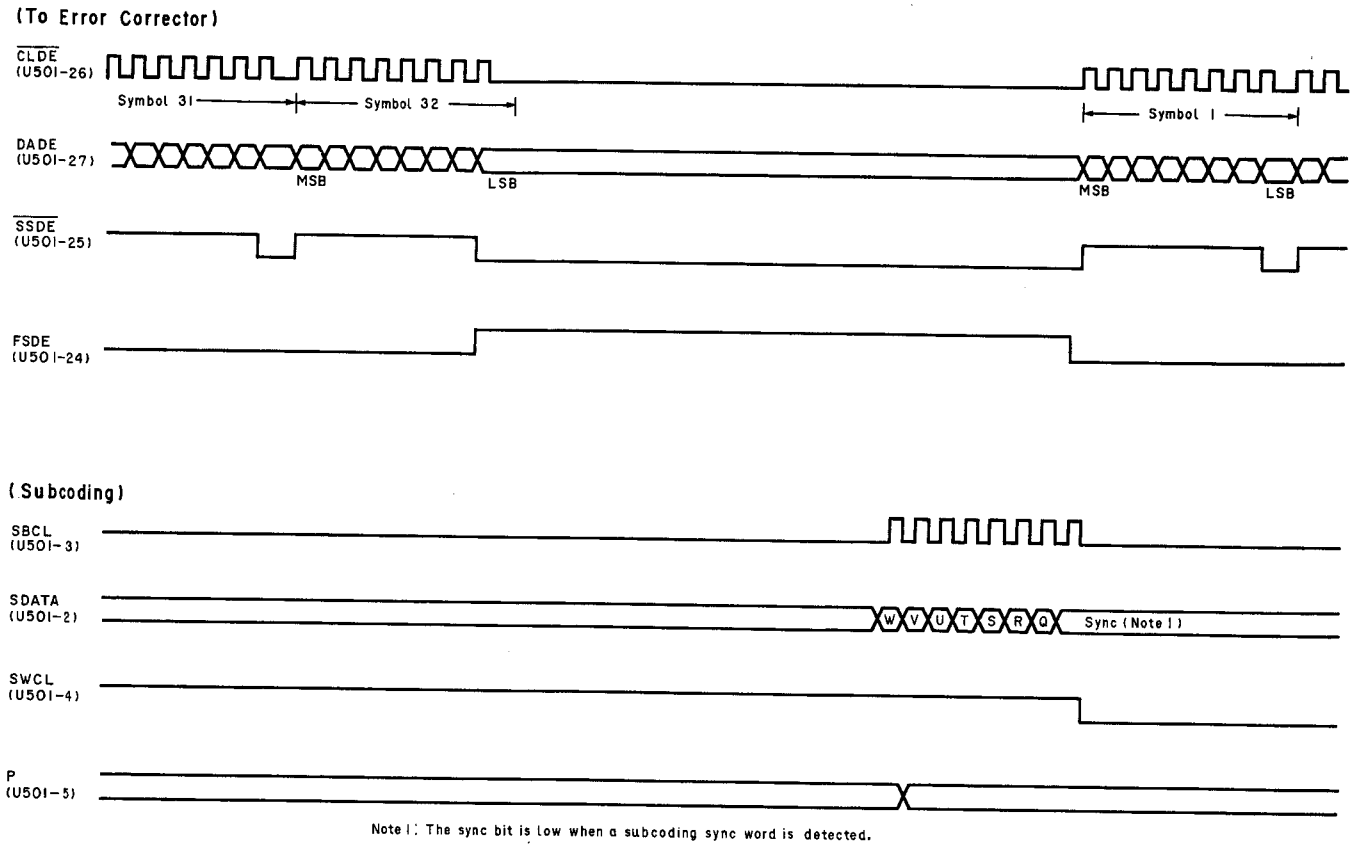

Fig. 8.1.16 Output Waveforms (SAA7011)

Description of Error Corrector IC U504 (SAA7020)
(See Figs. 8.1.17 and 8.1.18.)

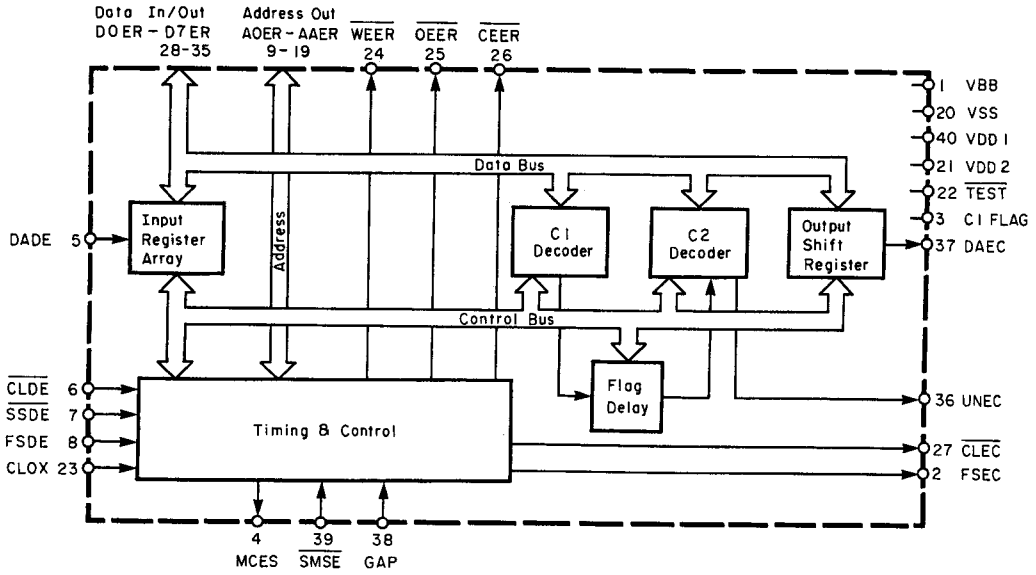

Fig. 8.1.17 Error Corrector IC SAA7020