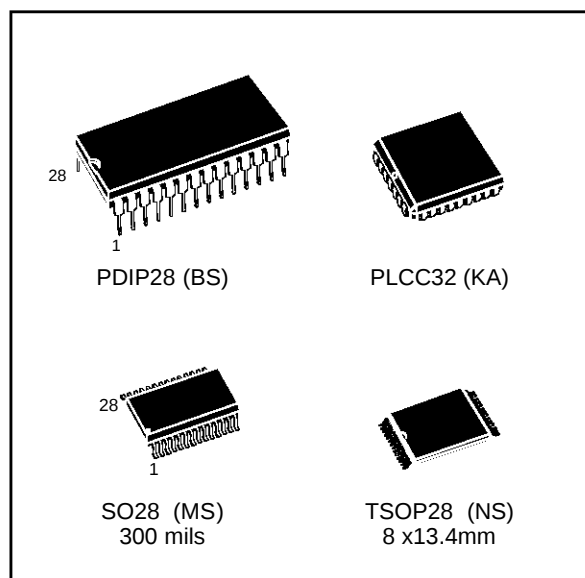


PARALLEL 256K (32K x 8) EEPROM WITH SOFTWARE DATA PROTECTION

PRELIMINARY DATA

- FAST ACCESS TIME: 90ns
- SINGLE 5V $\pm$ 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE:
 - 64 Bytes Page Write Operation
 - Byte or Page Write Cycle
- ENHANCED END OF WRITE DETECTION:
 - Data Polling
 - Toggle Bit
- STATUS REGISTER
- HIGH RELIABILITY SINGLE POLYSILICON, CMOS TECHNOLOGY:
 - Endurance >100,000 Erase/Write Cycles
 - Data Retention >10 Years
- JEDEC APPROVED BYTEWISE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP
- SOFTWARE DATA PROTECTION



DESCRIPTION

The M28256 is a 32K x 8 low power Parallel EEPROM fabricated with SGS-THOMSON proprietary double polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a single 5V power supply. The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Data Polling and Toggle Bit and access to a status register. The M28256 supports 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

Table 1. Signal Names

A0 - A14	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V _{CC}	Supply Voltage
V _{SS}	Ground

Figure 1. Logic Diagram

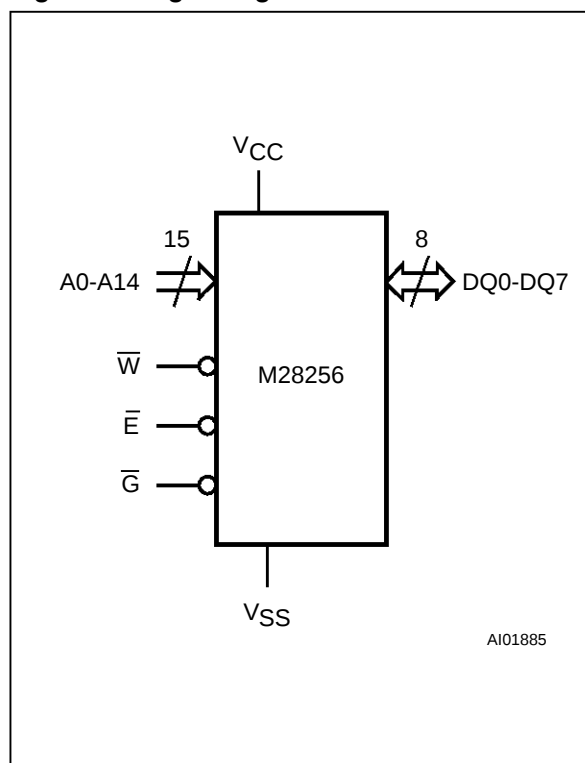


Figure 2A. DIP Pin Connections

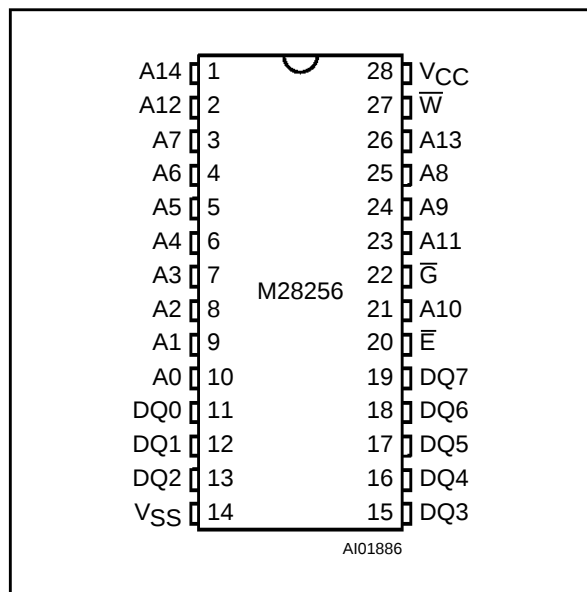
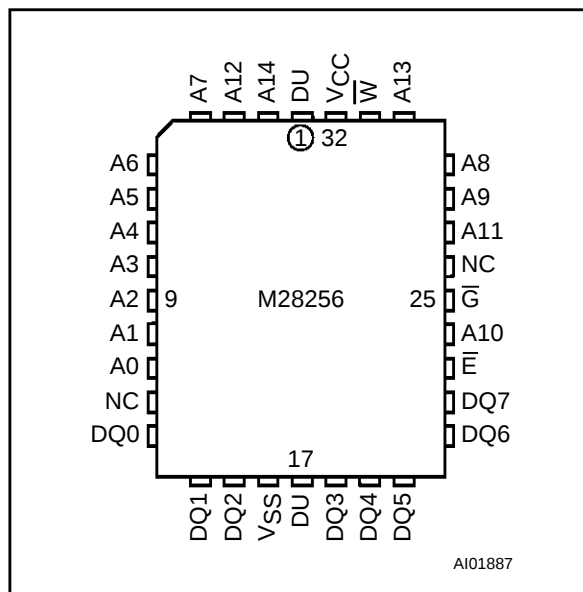


Figure 2B. LCC Pin Connections



Warning: NC = Not Connected, DU = Don't Use.

Figure 2C. SO Pin Connections

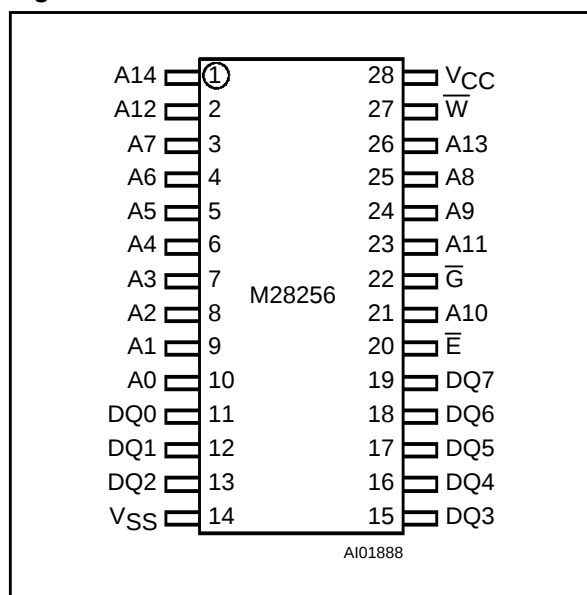
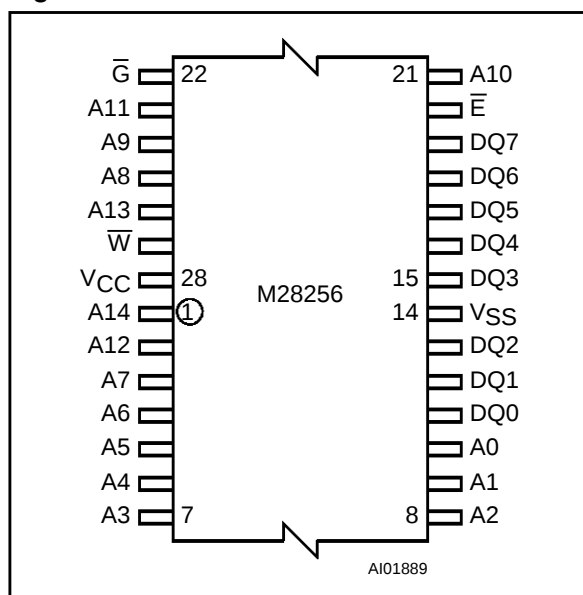


Figure 2D. TSOP Pin Connections



PIN DESCRIPTION

Addresses (A0-A14). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0- DQ7). Data is written to or read from the memory through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the memory.

Table 2. Absolute Maximum Ratings ⁽¹⁾

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	– 40 to 85	°C
T _{STG}	Storage Temperature Range	– 65 to 150	°C
V _{CC}	Supply Voltage	– 0.3 to 6.5	V
V _{IO}	Input/Output Voltage	– 0.3 to V _{CC} +0.6	V
V _I	Input Voltage	– 0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ⁽²⁾	4000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents

2. 100pF through 1500Ω; MIL-STD-883C, 3015.7

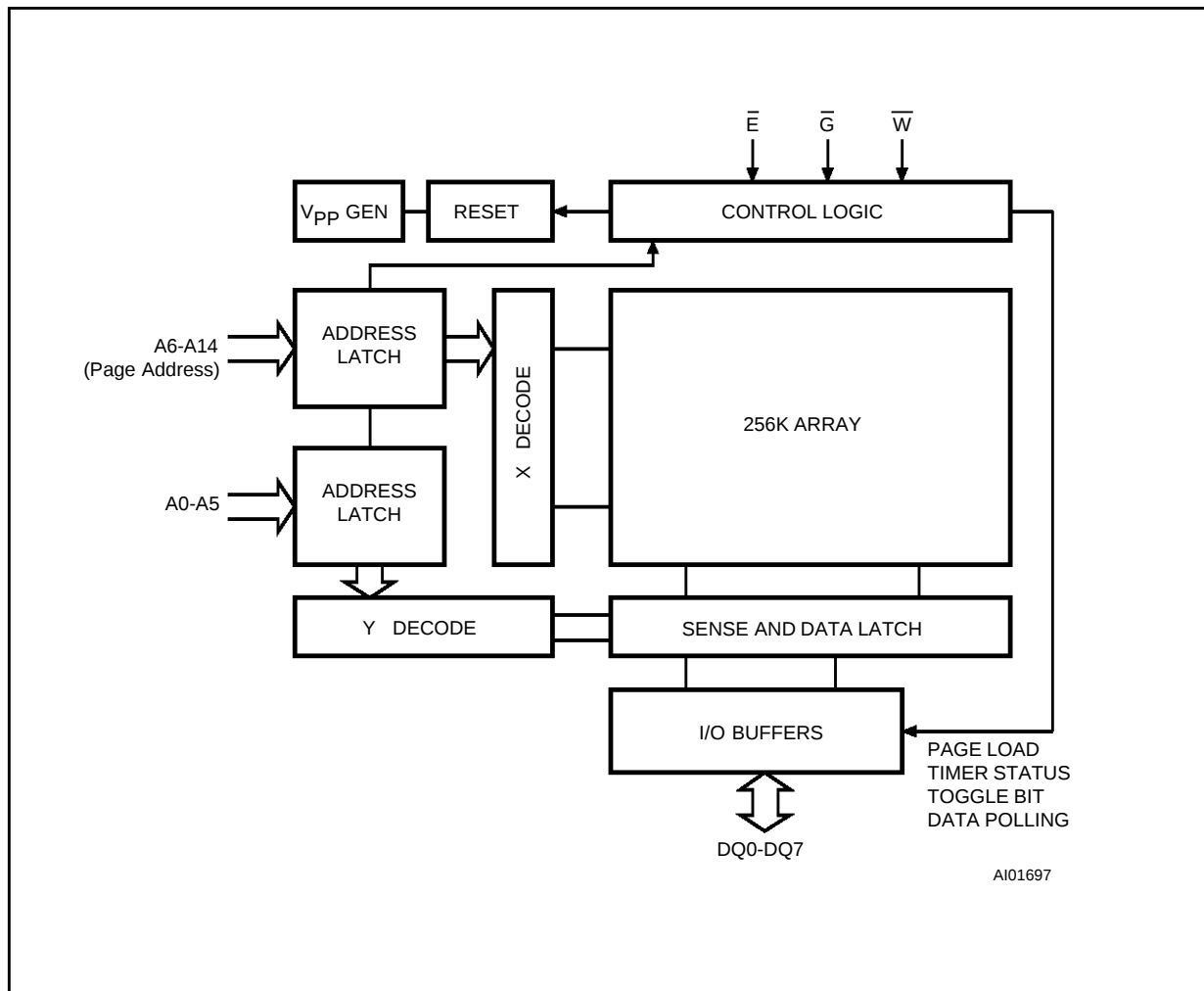
Figure 3. Block Diagram

Table 3. Operating Modes ⁽¹⁾

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V _{IL}	V _{IL}	V _{IH}	Data Out
Write	V _{IL}	V _{IH}	V _{IL}	Data In
Standby / Write Inhibit	V _{IH}	X	X	Hi-Z
Write Inhibit	X	X	V _{IH}	Data Out or Hi-Z
Write Inhibit	X	V _{IL}	X	Data Out or Hi-Z
Output Disable	X	V _{IH}	X	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}.

OPERATIONS

Write Protection

In order to prevent data corruption and inadvertent write operations; an internal VCC comparator inhibits Write operations if VCC is below VWI (see Table 6). Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The device is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The device supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion and the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6 is controlled accordingly.

Page Write

Page write allows up to 64 bytes within the same page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is

A14-A6 must be the same for all bytes; if not, the Page Write instruction is not executed. The page write can be initiated by any byte write operation.

A page write is composed of successive Write instructions which have to be sequenced with a specific period of time between two consecutive Write instructions, period of time which has to be smaller than the t_{WHWH} value (see Table 8).

If this period of time exceeds the t_{WHWH} value, the internal programming cycle will start. The completion of a Write operation triggers the Data Polling and the Toggle bit functions on DQ6 and DQ7.

Status Register

The M28256 provides several Write operation status flags that can be used to minimize the application write time. These signals are available on the I/O port bits during programming cycle only.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	X	X	X	X	X

DP = Data Polling
 TB = Toggle Bit
 PLTS = Page Load Timer Status

Data Polling flag (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle flag (DQ6). The M28256 offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any byte of the memory. When the internal cycle is completed the toggling will stop and the data read on DQ7-DQ0 is the addressed memory byte. The device is now accessible for a new Read or Write operation.

Page Load Timer Status flag (DQ5). During a Page Write instruction, the M28256 expects to receive the stream of data with a minimum period of time between each data byte. This period of time (t_{WHWH}) is defined by the on-chip Page Load timer which running/overflow status is available on DQ5. DQ5 Low indicates that the timer is running, DQ5 High indicates the time-out after which the internal write cycle will start.

Software Data Protection

The M28256 offers a software controlled write protection facility that allows the user to inhibit all write modes to the device. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The M28256 is shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents.

The device remains in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences. To enable the Software Data Protection (SDP) the device requires the user to

write (with a Page Write addressing three specific data bytes to three specific memory locations, each location in a different page) as per Figure 6. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 5 (with a Page Write addressing different bytes in different pages).

This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

Figure 5. Software Data Protection Disable Algorithm

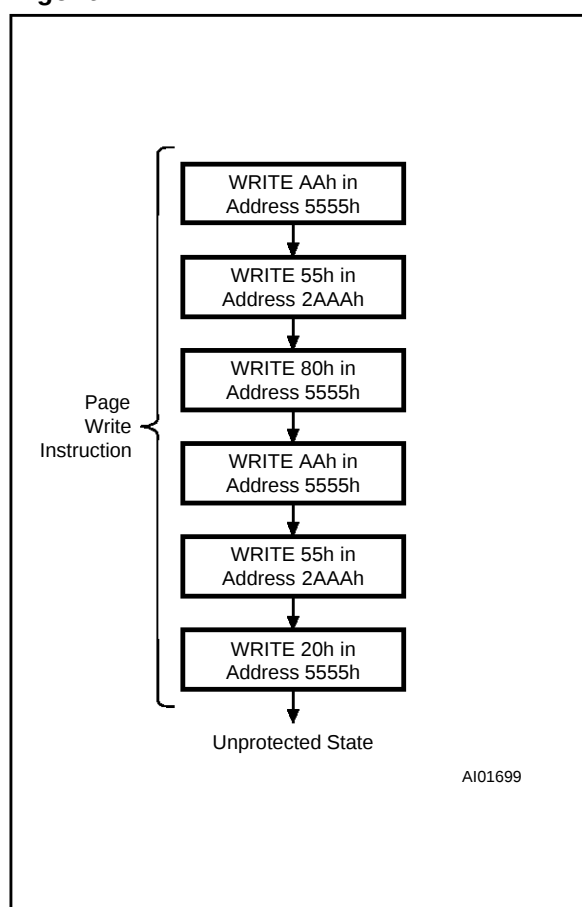
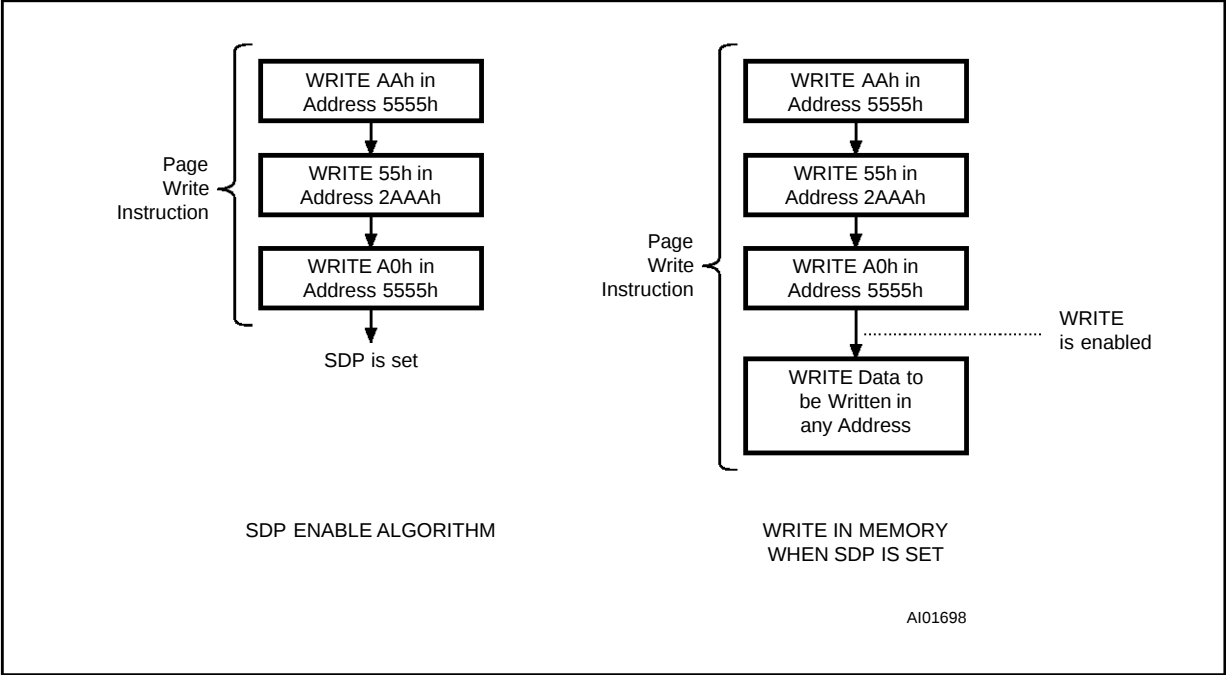


Figure 6. Software Data Protection Enable Algorithm and Memory Write



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Input Output Waveforms

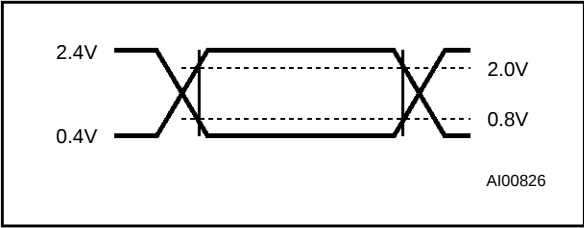


Figure 8. AC Testing Equivalent Load Circuit

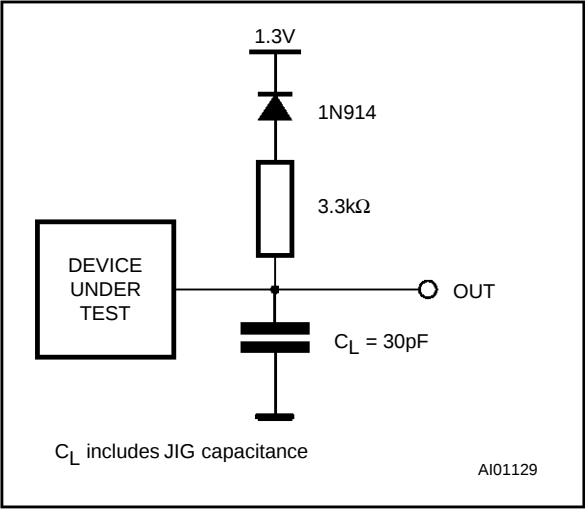


Table 4. Capacitance⁽¹⁾ ($T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Note: 1. Sampled only, not 100% tested.

Table 5. Read Mode DC Characteristics
($T_A = 0\text{ to }70^{\circ}\text{C}$ or $-40\text{ to }85^{\circ}\text{C}$; $V_{CC} = 4.5V\text{ to }5.5V$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	μA
$I_{CC}^{(1)}$	Supply Current (TTL inputs)	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, f = 5\text{ MHz}$		30	mA
	Supply Current (CMOS inputs)	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, f = 5\text{ MHz}$		25	mA
$I_{CC1}^{(1)}$	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		1	mA
$I_{CC2}^{(1)}$	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.3V$		100	μA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{ mA}$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400\text{ }\mu A$	2.4		V

Note: 1. All I/O's open circuit.

Table 6. V_{CC} Voltage Monitoring⁽¹⁾ ($T_A = 0\text{ to }70^{\circ}\text{C}$ or $-40\text{ to }85^{\circ}\text{C}$)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation (once $V_{CC} \geq V_{WI}$)	100		μs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)	5		ms
V_{WI}	V_{CC} Write Inhibit	3	3.9	V

Note: 1. Sampled only, not 100% tested.

Table 7. Read Mode AC Characteristics(T_A = 0 to 70°C or -40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28256								Unit
				-90		-120		-150		-200		
				min	max	min	max	min	max	min	max	
t _{AVQV}	t _{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$		90		120		150		200	ns
t _{ELQV}	t _{CE}	Chip Enable Low to Output Valid	G = V _{IL}		90		120		150		200	ns
t _{GLQV}	t _{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		40		45		50		50	ns
t _{EHQZ} ⁽¹⁾	t _{DF}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	40	0	45	0	50	0	50	ns
t _{GHQZ} ⁽¹⁾	t _{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	40	0	45	0	50	0	50	ns
t _{AXQX}	t _{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}, \overline{G} = V_{IL}$	0		0		0		0		ns

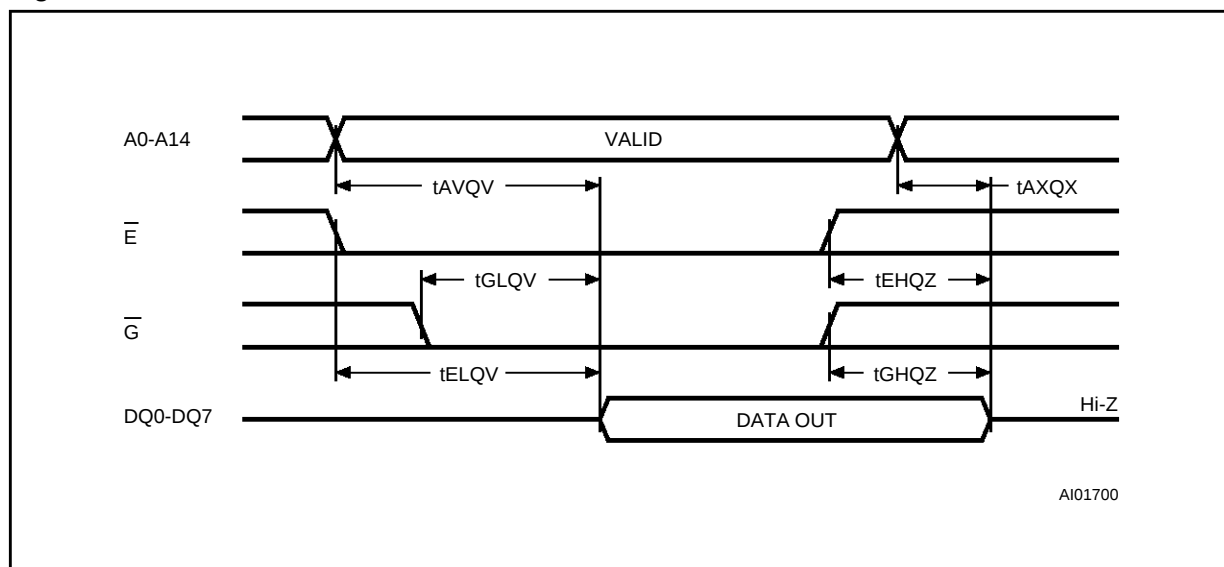
Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.**Figure 9. Read Mode AC Waveforms****Note:** Write Enable ($\bar{W}$) = High.

Table 8. Write Mode AC Characteristics(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t _{AVWL}	t _{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}, \overline{G} = V_{IH}$	0		ns
t _{AVEL}	t _{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}, \overline{W} = V_{IL}$	0		ns
t _{ELWL}	t _{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t _{GHWL}	t _{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t _{GHEL}	t _{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t _{WLLEL}	t _{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t _{WLAX}	t _{AH}	Write Enable Low to Address Transition		50		ns
t _{ELAX}	t _{AH}	Chip Enable Low to Address Transition		50		ns
t _{WLDV}	t _{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}, \overline{G} = V_{IH}$		1	μs
t _{ELDV}	t _{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}, \overline{W} = V_{IL}$		1	μs
t _{ELEH}	t _{WP}	Chip Enable Low to Chip Enable High		50		ns
t _{WHEH}	t _{CEH}	Write Enable High to Chip Enable High		0		ns
t _{WHGL}	t _{OEH}	Write Enable High to Output Enable Low		0		ns
t _{EHGL}	t _{OEH}	Chip Enable High to Output Enable Low		0		ns
t _{EHWH}	t _{WEH}	Chip Enable High to Write Enable High		0		ns
t _{WHDX}	t _{DH}	Write Enable High to Input Transition		0		ns
t _{EHDX}	t _{DH}	Chip Enable High to Input Transition		0		ns
t _{WHWL}	t _{WPH}	Write Enable High to Write Enable Low		100		ns
t _{WLWH}	t _{WP}	Write Enable Low to Write Enable High		50		ns
t _{WHWH}	t _{BLC}	Byte Load Repeat Cycle Time		0.15	150	μs
t _{WHRH}	t _{WC}	Write Cycle Time			3	ms
t _{EL} , t _{WL}		$\overline{E}$ or $\overline{W}$ Input Filter Pulse Width	Note 1	15		ns
t _{DVWH}	t _{DS}	Data Valid before Write Enable High		50		ns
t _{DVEH}	t _{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. Sampled only, not 100% tested.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

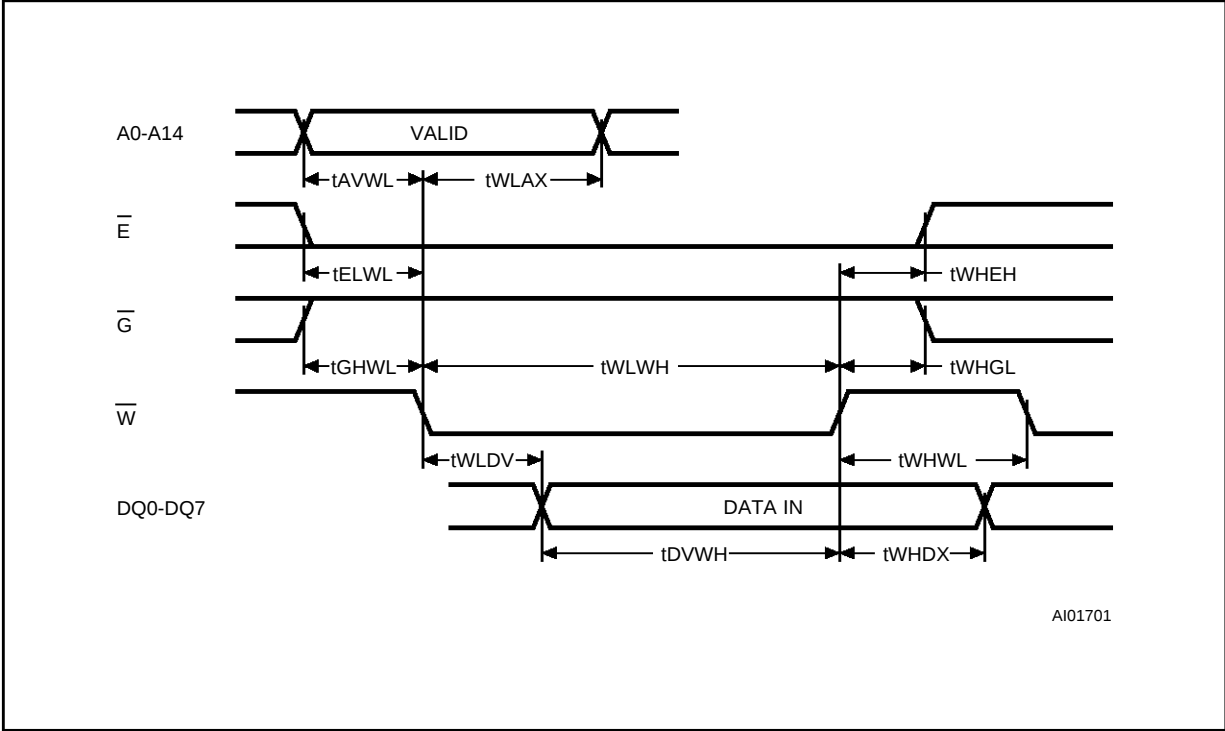


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

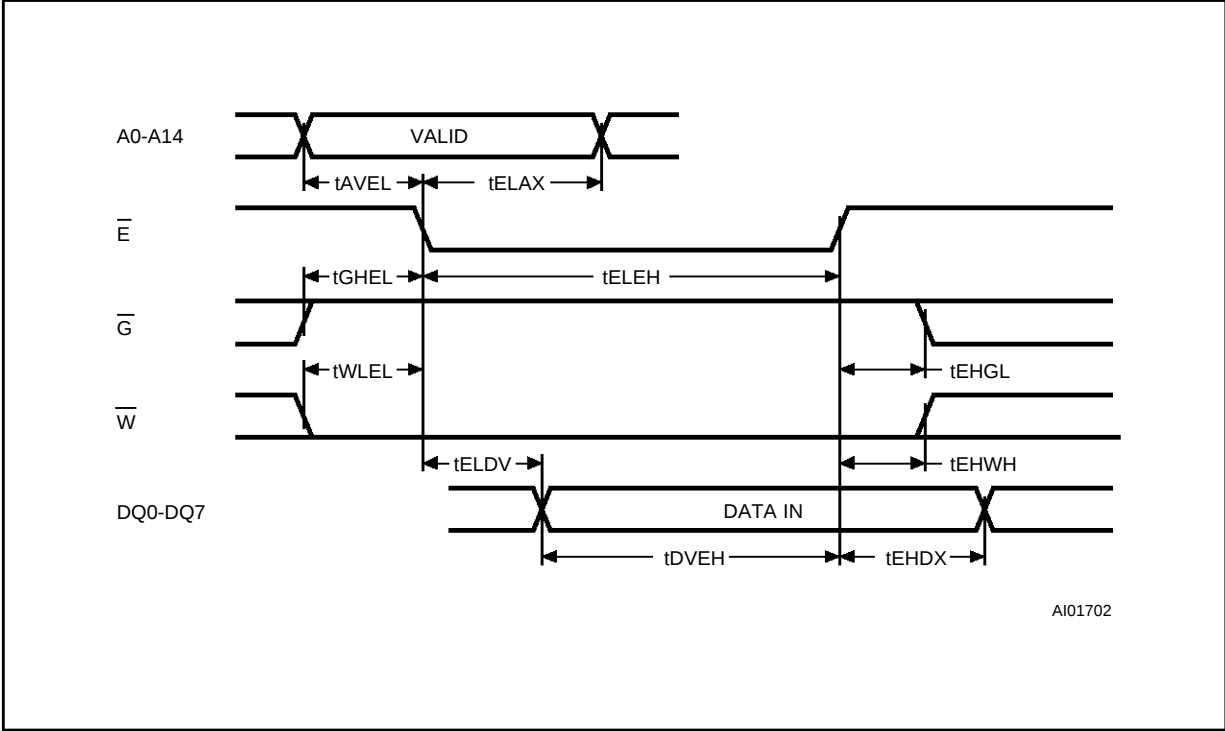


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

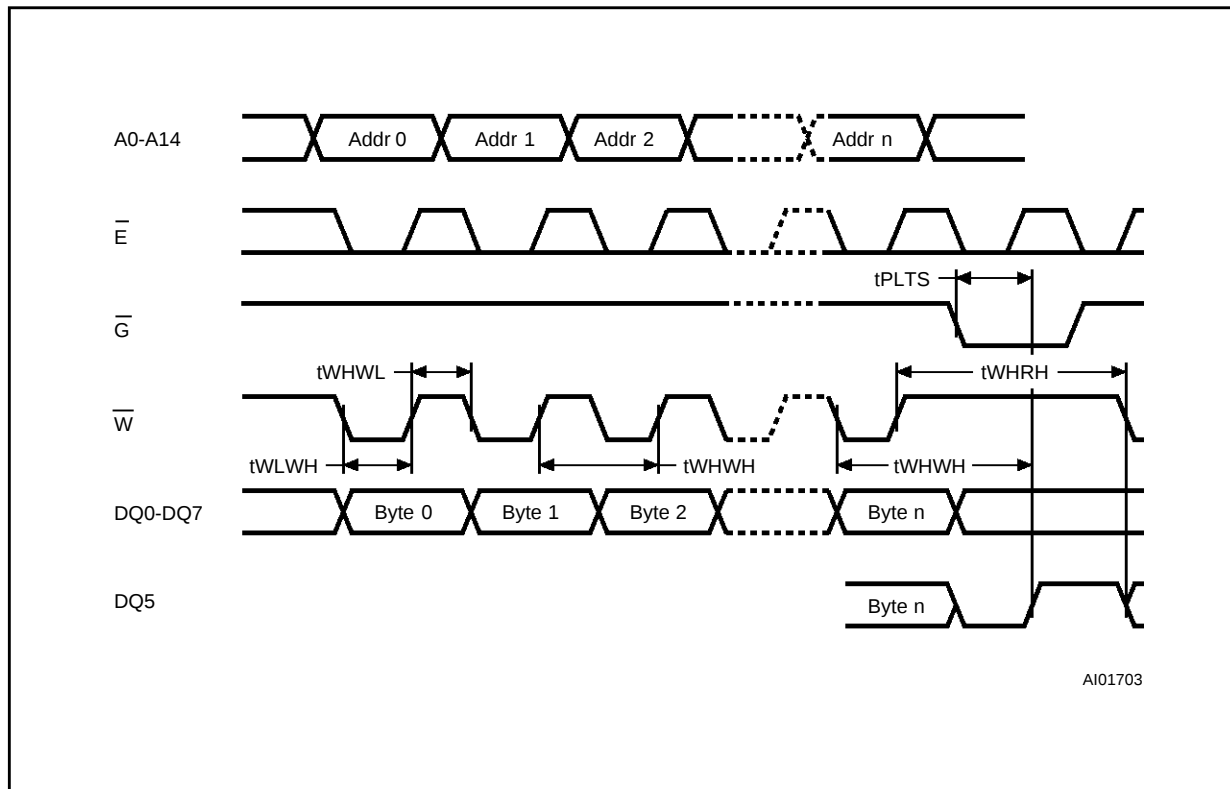
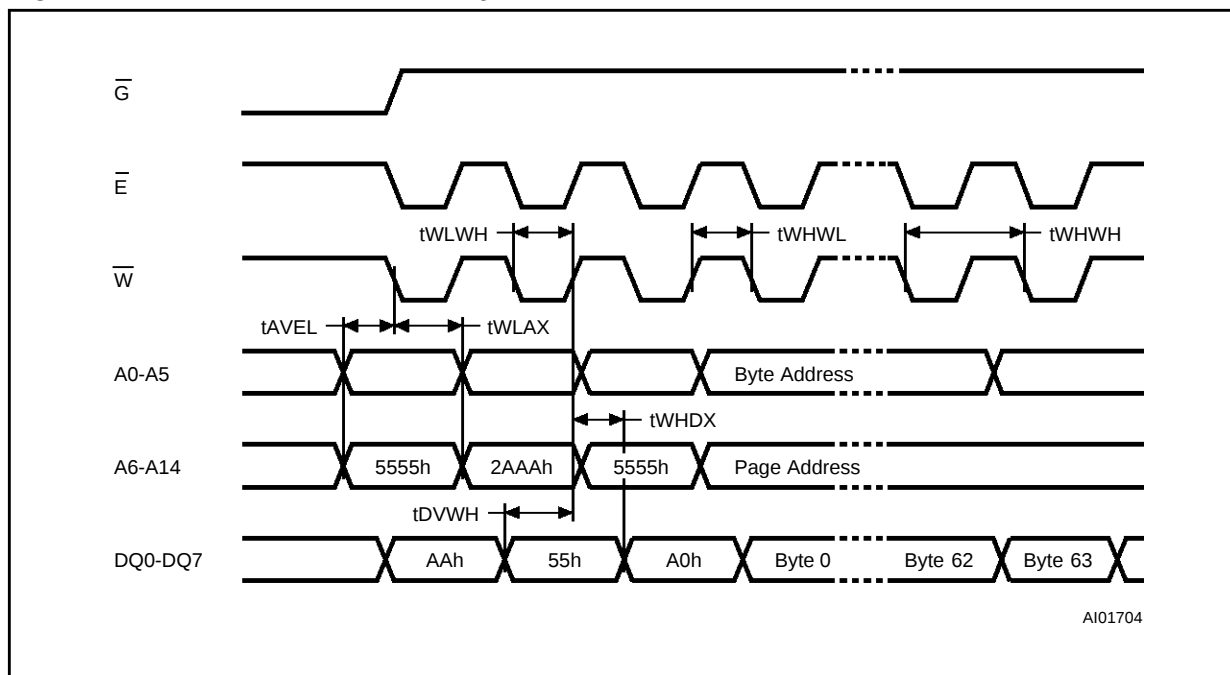


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A14 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. G must be high only when W and E are both low.

Figure 14. Data Polling Waveform Sequence

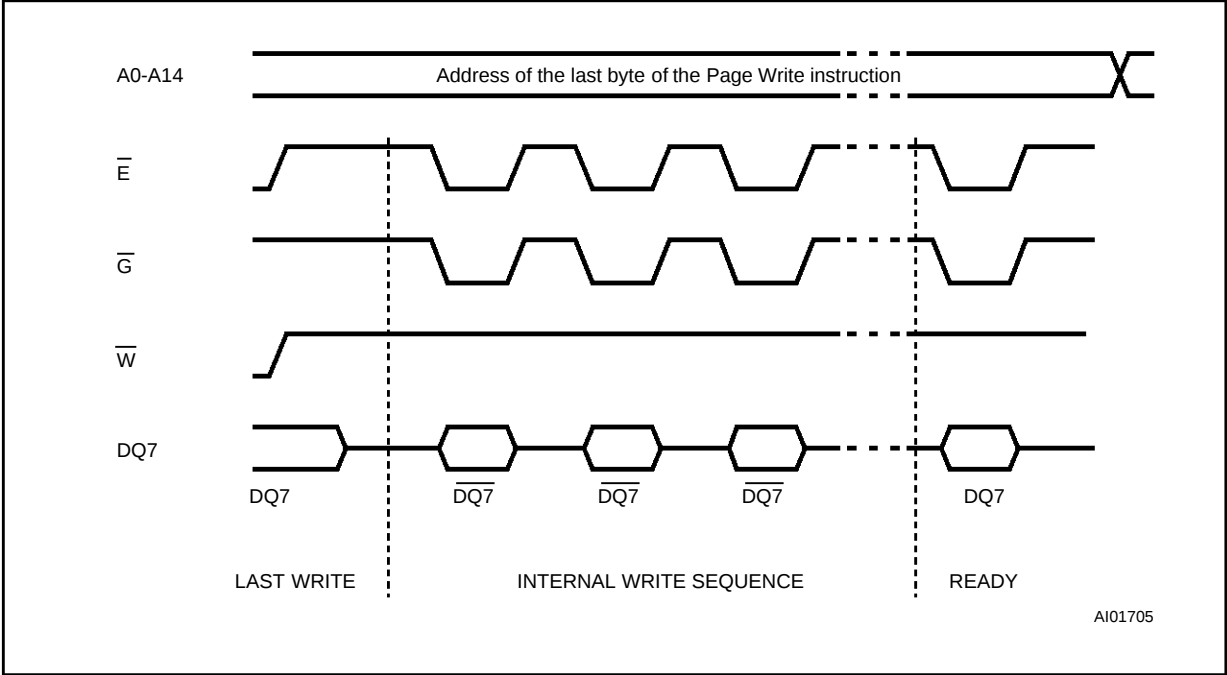
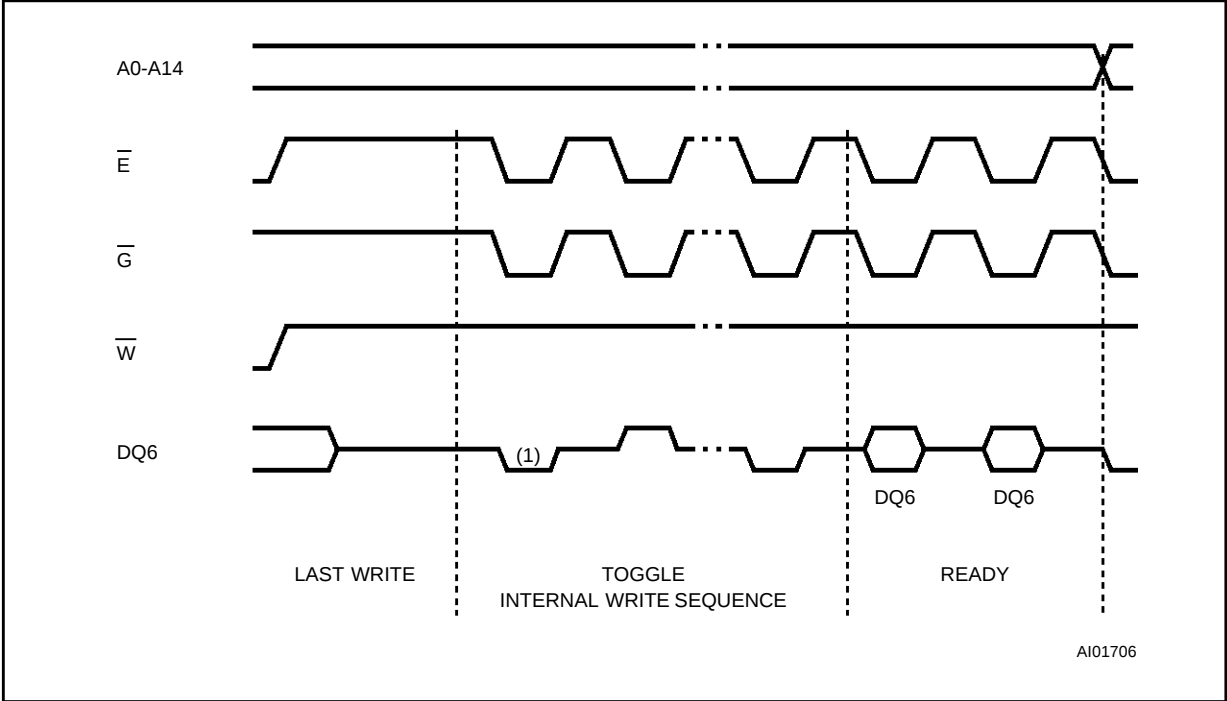
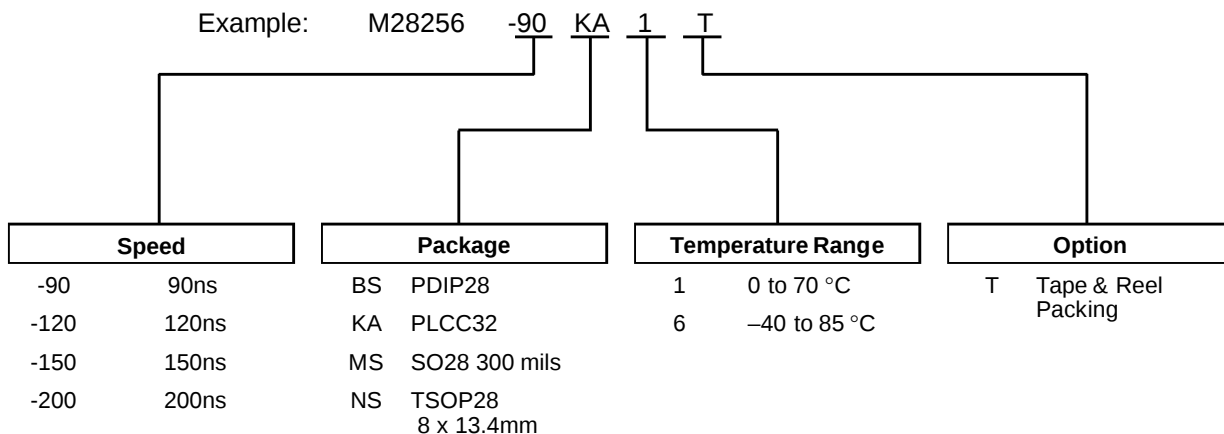


Figure 15. Toggle Bit Waveform Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME



Parts are shipped with the memory content set at all "1's" (FFh).

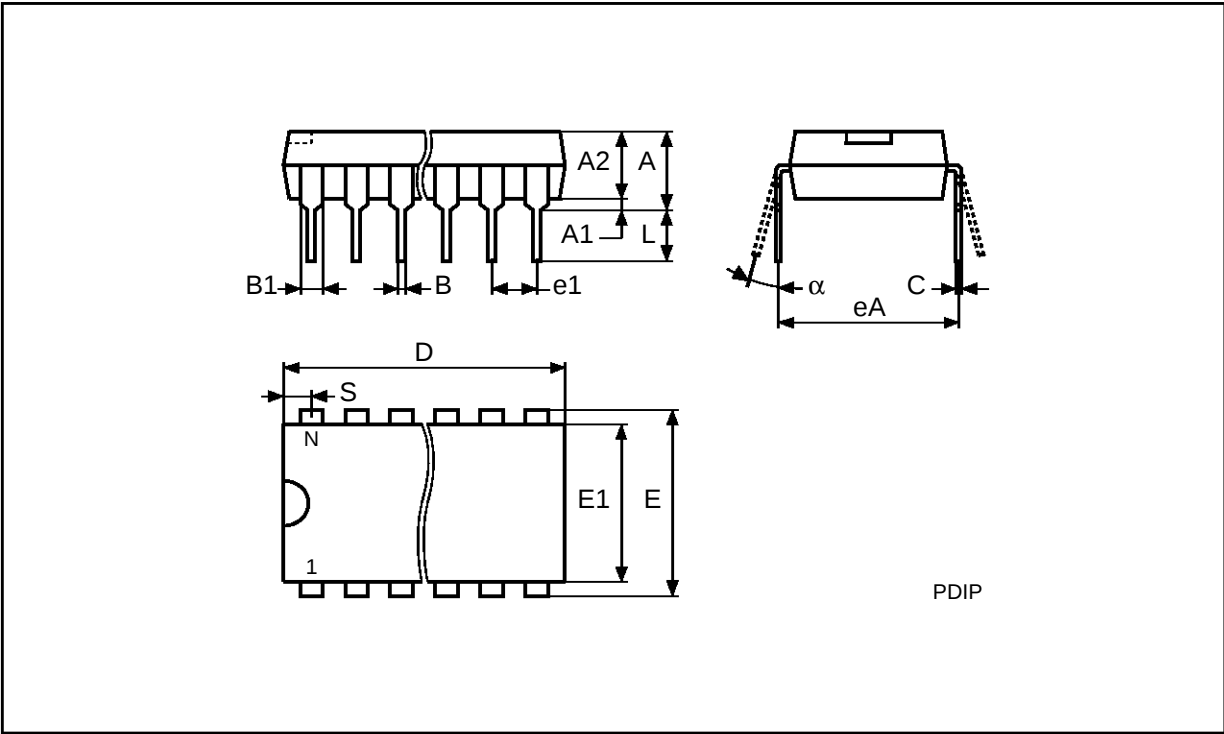
For a list of available options (Speed, Package, Temperature Range, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	—	—	0.100	—	—
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

PDIP28

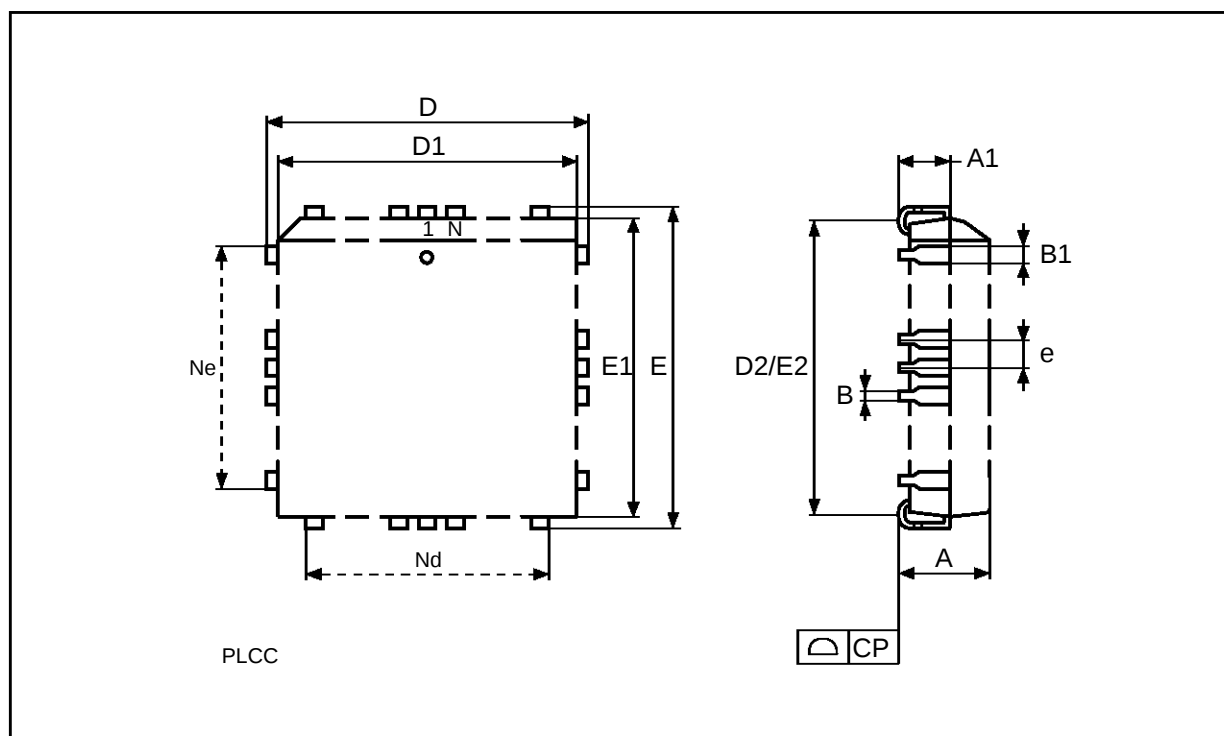


Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

PLCC32

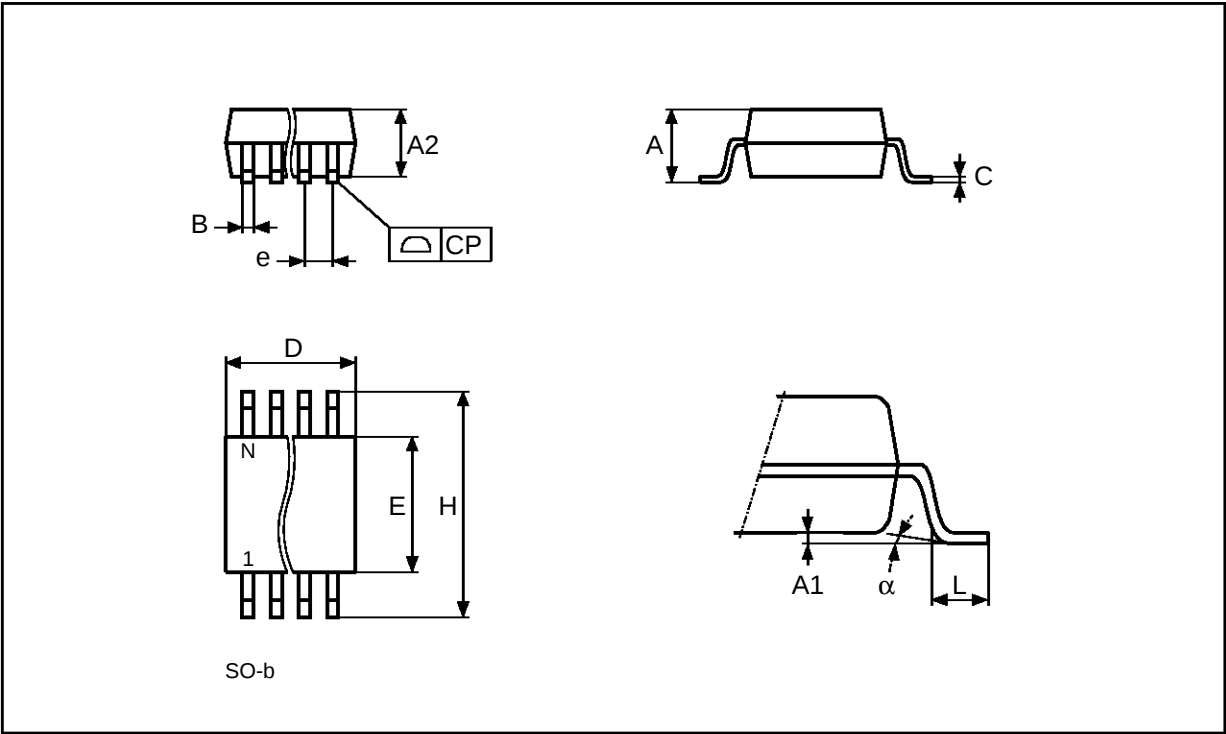


Drawing is not to scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	—	—	0.050	—	—
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SO28

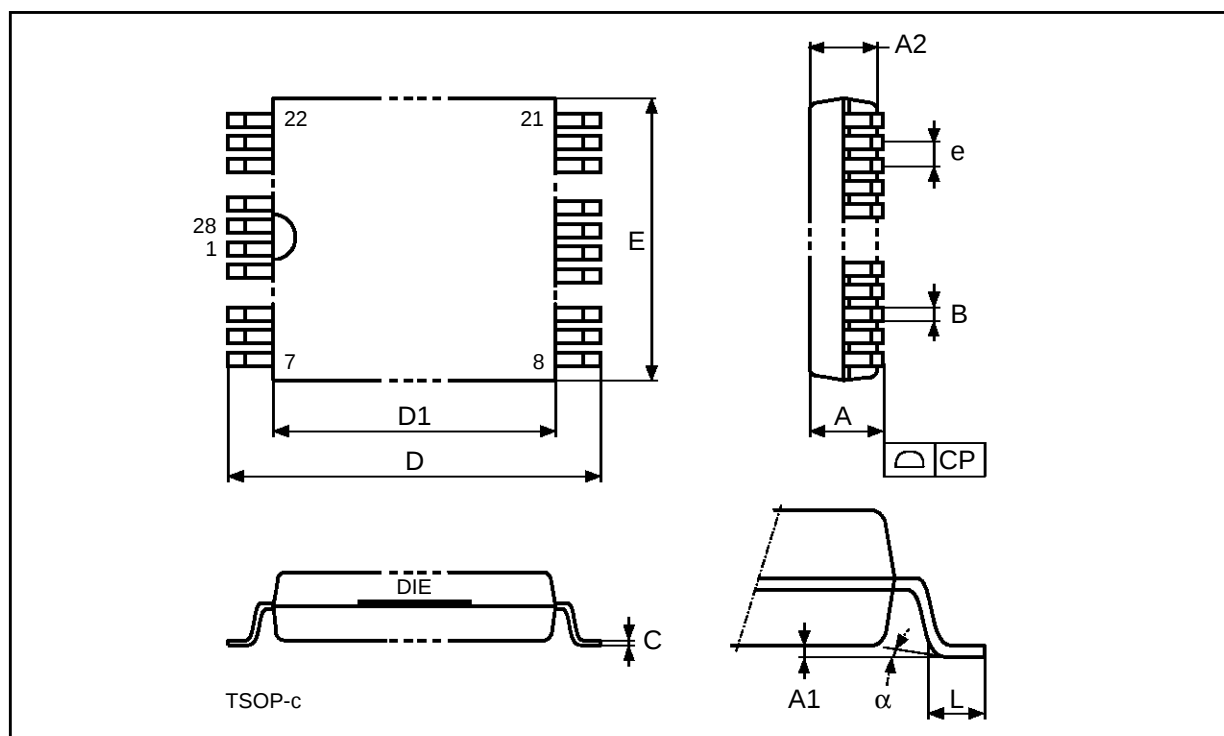


Drawing is not to scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

TSOP28



Drawing is not to scale

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