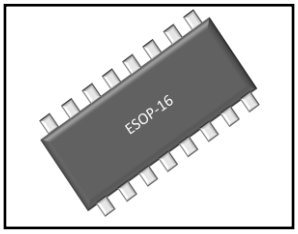
Data Sheet

UR4205C

SmartPower Enabled Non-Flickering APFC Controller For LED Lighting

Overview:



UR4205C is a high-voltage Integrated Circuit(IC) for driving LED lamps in general mains lighting applications. It is a single stage of boost or non-isolated flyback controller with Active Power Factor Correction (APFC) feature.

With several unique technologies, the main benefits of this IC include:

1. High power factor, Low THD with Zero LED output current ripple, allow a wide LED power range
2. Single stage of Switching Power topology for small PCB footprint
3. Integrated high voltage SmartPower allows fast startup
4. Single winding inductor for low cost, No bias winding needed
5. Rich protection provides high reliability
6. Low electronic Bill of Material (BOM)

The IC works as boundary conduction mode converters, typically in boost or flyback configuration. High-efficiency switch mode boost controller drives an external power FET with Quasi-Resonant operation.

The IC can apply to compact mains connected, LED lamps for single or universal mains voltages, including 100V (AC), 120V (AC), 230V (AC) and 90~305V (AC). External components determine the power level. The power level ranges from 2W to over 40W.

Features:

1. PF>0.95, THD<10%
2. Ultra-high conversion efficiency up to 96%
3. Flickering Free, Zero ripple
4. Tight mass production current tolerance at ±3% in mass production
5. Quick startup <500ms
6. Excellent line/load regulation
7. Rich Built-in Protections:
   - VDD UnderVoltage Lockout (UVLO)
   - Leading-Edge Blanking (LEB)
   - PowerFET's cycle by cycle Current limit
   - Internal Over Temperature Protection (OTP)
   - LED short/open protection
   - LDO over power limit
   - LED over current protection
   - Boost output over voltage protection
   - Easy external temperature protection with a single NTC resistor

Typical Application:

1. LED lighting.
2. Down light, Tube lamp, PAR lamp, Bulb etc.

A small size, THD<10%, 18W input (420V/40mA load) T8 tube's performance is as below.

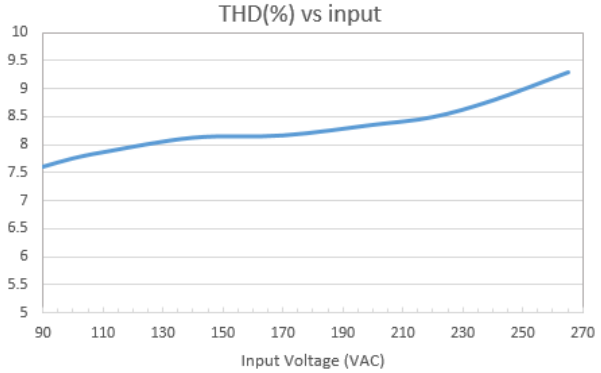


Fig.1 THD(%) vs. input voltage

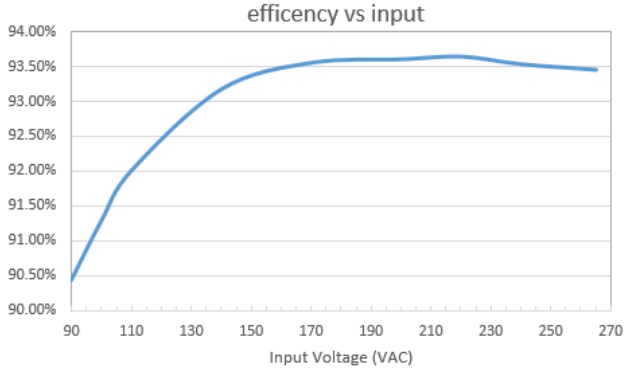
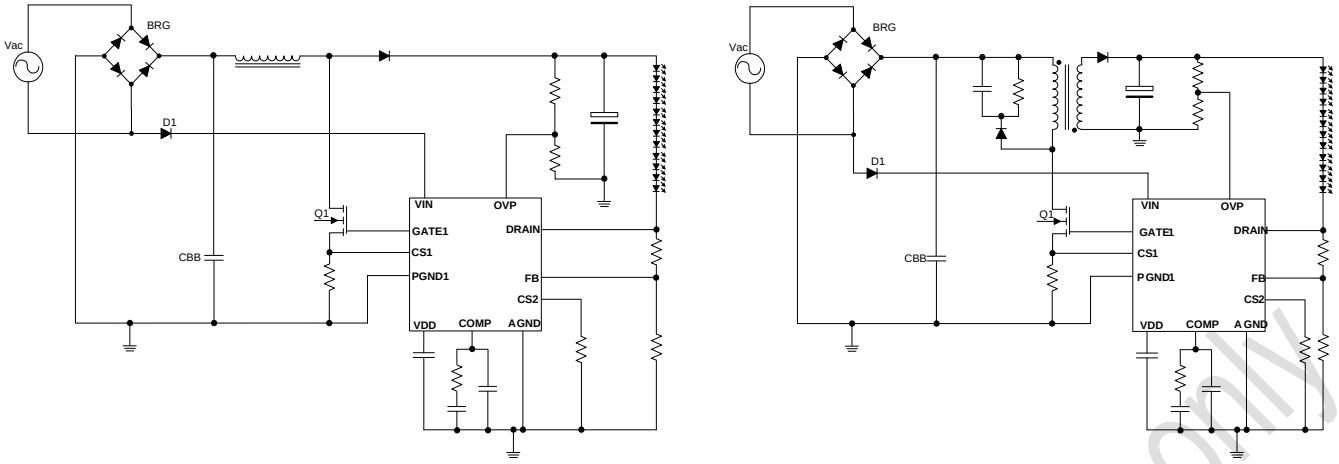


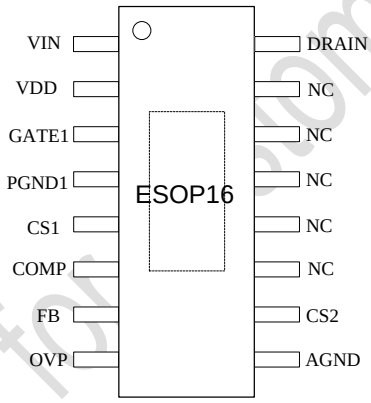
Fig.2 Efficiency vs. input voltage



(a) Simplified Boost application (b) Simplified NON-isolated Flyback application

Fig.3 UR4205C's typical application diagrams used as BOOST and Flyback topology

Pin Description:



UR4205C

Device	Pin Count	Package	Junction Temperature
UR4205C	16	ESOP-16	-40°C - +150°C

Pin	Symbol	Description
1	VIN	Power input, connected to main AC source through a diode.
2	VDD	Power, this pin provides bias power for the IC during startup and steady state operation.
3	GATE1	Gate switch for boost transistor, connected to a MOSFET's gate.
4	PGND1	Power ground for boost stage.
5	CS1	Current sense for boost transistor, used for cycle-by-cycle peak current limit.
6	COMP	Compensation network, Output of the error amplifier. Connect TYPEII compensation network to this pin t to make the converter's loop stable.
7	FB	Boost stage output voltage feedback, used to set boost output voltage.
8	OVP	Boost output over voltage protection pin, programmed by resistor divider.
9	AGND	Analog ground.

…continued above

10	CS2	A resistor between CS2 and GND sets the LDO's current regulation.
11	NC	Not connected.
12	NC	Not connected.
13	NC	Not connected.
14	NC	Not connected.
15	NC	Not connected.
16	DRAIN	Connect to LED string's cathode pole.
17	EP	Exposed Pad, internally electrically connected to AGND.

Block Diagram:

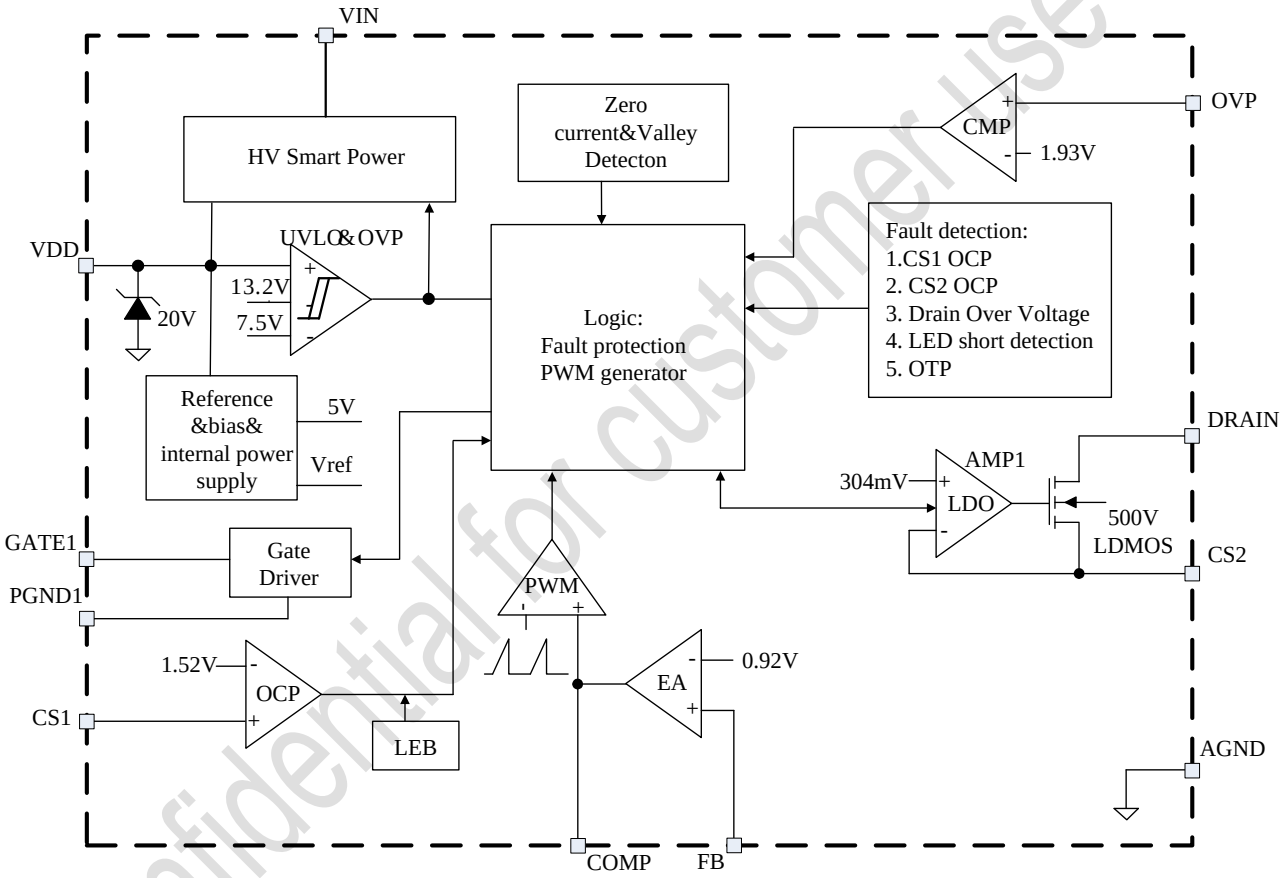


Fig.4 Block diagram

Operation:

The UR4205C's typical application is a single stage boost (or non-isolated flyback) converter with an integrated 500V high voltage low dropout regulator (LDO) inside who is series with LED load. With the constant on time and Boundary Current Mode (BCM), high power factor correction can be achieved. Unlike the transitional boost converter to regulate the boost's output directly, the IC controls the loop to regulate the LDO drain's average voltage to be sable at certain low level which will keep the LDO always regulate LED at constant current state.

Figure 3 shows the basic application diagram. Figure 5 shows the waveforms. Energy is stored in inductor Lm each period that the switch is on. The inductor current I_{Lm} is zero when the external power FET switch is switched on. Thereafter, the amplitude of the current build-up in Lm is proportional to VIN and the time that the power FET switch is on. When the power FET switch is switched off, the current continues to flow through the freewheel diode and the output capacitor. The current then falls at a rate proportional to the value of Vout-VIN. The Power FET's turn on time is determined by COMP's voltage which is the internal error amplifier's output. And COMP's voltage will be set by FB's regulation. LED's current is always equal to the 304mV/Rcs2.

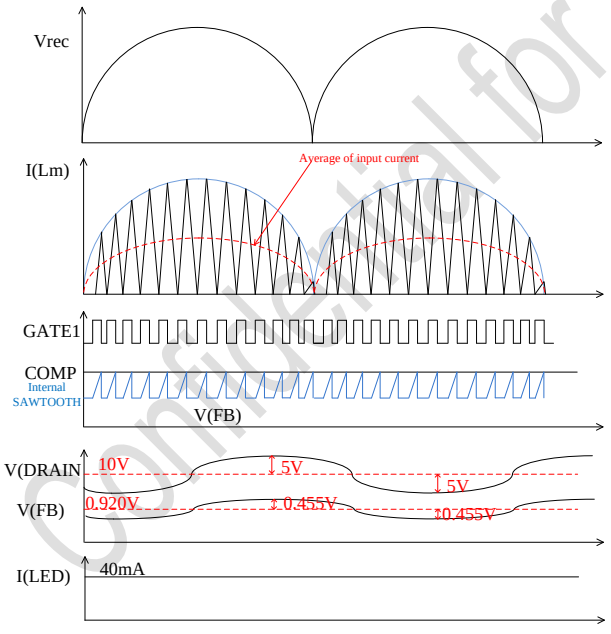


Fig.5 boost operation waveforms

Smart Power supply:

The UR4205C is supplied by Bps's patented high voltage smart power supply method:

- At start-up, there is an internal current source powered by VIN pin. The current source fast charge up VDD to exceeds VDD_TH. The IC starts to output PWM driving signal.
- Under normal operation, the Smart Power supply provides the IC's operation current. The unique supply method makes the IC's power consumption limit to couple tens of mW.
- The transitional auxiliary winding supply method also is available if the user wants.

The IC starts up when the voltage at VDD pin exceeds VDD_TH. The IC locks out (stops switching) when the voltage at the VDD pin is <VDD_UVLO. An internal active Zener limits the maximum voltage on the supply VDD pin.

Valley detection:

A special feature, called valley detection is an integrated part of the UR4205C circuitry. Dedicated built-in circuitry senses when the voltage on the drain of the power FET has reached its lowest value. The next cycle is then started and as a result the capacitive switching losses are reduced. If a valid valley is not detected, the secondary stroke is continued until the maximum off-time (T_{MAX_OFF}) is reached. Then the next cycle is started.

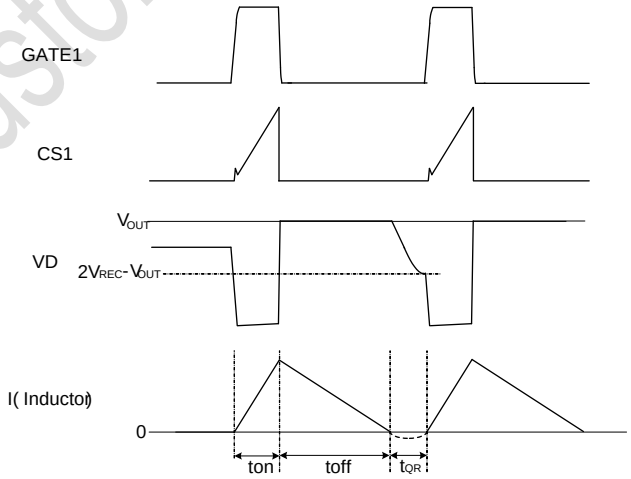


Fig.6 valley detection (Quasi Resonant) operation

Protective features:

The IC has the following protective features:

- VDD Under Voltage LockOut (UVLO)
- Leading-Edge Blanking (LEB)
- Power FET switch Over Current Limit (OCL)
- Internal Over Temperature Protection (OTP)
- LDO Over Power Limit (OPL)
- LED Short Protection (LSP)
- LED Over Current Protection (LOCP)
- Output capacitor/LED open over voltage protection (OVP)
- LED over temperature control and protection

The LSP, LOCP and OVP are latched protections. It causes the IC to halt until a reset (a result of power

cycling) is executed. When VDD drops to below VDD_UVLO, the IC resets the latch protection mode. The switching starts only when a no fault condition exists.

VDD Under Voltage LockOut (UVLO)
When the voltage on VDD pin drops to below VDD_UVLO, the IC stops switching. An attempt is made to restart by supplying VDD from VIN pin voltage.

Leading-Edge Blanking (LEB)
To prevent false detection of the powerFET over current, a blanking time following switch-on is implemented. When the power FET switch switches on, there can be a short current spike due to capacitive discharge of voltage over the drain and source and the charging of the gate to source capacitance. During the LEB time (T_{LIM_BLK}), the spike is disregarded.

Power FET switch Over Current Limit (OCL)
The UR4205C contains an accurate built-in peak current detector. It triggers when the voltage at the source pin reaches the peak-level V_{CS1_LIM}. The current through the switch is sensed using a resistor connected to the CS1 pin. The sense circuit is activated following LEB time. When the OCL state is detected, the IC turn off the switch immediately for the rest of the cycle. This current limit is a cycle by cycle behavior.

Internal Over Temperature Protection (OTP)
When the internal OTP function is triggered at certain IC temperature (T_{OTP}), the converter stops operating. The safe-restart protection is triggered and IC restarts with switching resuming when the IC temperature drops lower than T_{OTP_HYS}.

LDO Over Power Limit (OPL)
OPL protection is designed to limit the power consumption of the internal HV LDO. The detection is through FB pin. When abnormal fault happened (like Vrec goes too high to boost normally), Drain will increase and make LDO power consumption increased. To limit drain's voltage, OPL will be triggered. When OPL is triggered, the GATE1 stops to output and COMP will be pulled low with extra current sink. The OPL detection is given by following equation:
V_{DRAIN_OPL}=20uA*Rfb1+1.93V*(Rfb1+Rfb2)/Rfb2

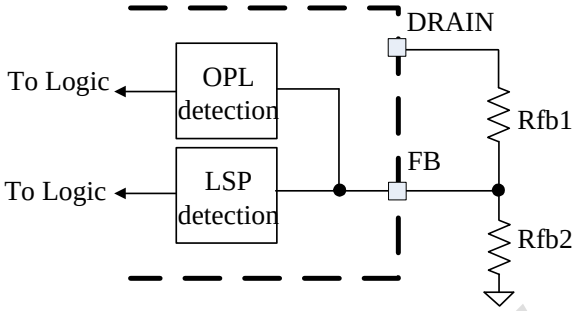


Fig.7 OPL and LSP detection

LED Short Protection (LSP)
When LED is short or Vrec rises to an extreme high level, Drain will be pulled to a very high level, then LSP protection is triggered and latch the IC immediately. The LSP will be triggered when the Drain's voltage reaches the following value:
V_{DRAIN_LSP}=50uA*Rfb1+1.93V*(Rfb1+Rfb2)/Rfb2

LED Over Current Protection (LOCP)
LOCP is triggered when CS2's voltage exceeds 410mV. This will keep the LED always meet no over shoot current. When LOCP is triggered, the IC will latch off until IC is reseted.

Output capacitor/LED open over voltage protection (OVP)
When the LED is open or the boost feedback loop is opened, the converter will keep to charge up Cout. The OVP will limit the voltage of Cout to avoid damage. Cout's voltage is sensed by resistor divider and through OVP pin to compare with V_{OVP_TH}.

Soft-Start function:
The IC naturally has the soft-start function with proper compensation network at COMP pin.

Heat Sinking:
The exposed pad of the Esop16 package is internally electrically tied to AGND. For single layer PCB, to increase the effective heat sinking area, the NC pins should be soldered onto AGND copper as shown in fig.8. For two layers PCB, top and bottom side areas connected with vias can also be used to further increase the heat sinking area.

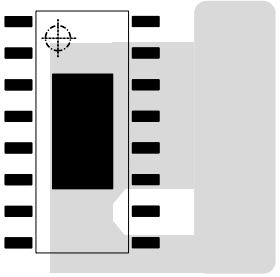


Fig.8 Layout consideration for heat sinking

Absolute Maximum Ratings:

Parameters	Value	Unit
VIN	-0.3 to +650	V
DRAIN	-0.3 to +550	V
VDD, CS1, GATE1	-0.3 to 22	V
NTC, FB, OVP, COMP, CS2	-0.3 to +6.0	V
ESD Susceptibility (HBM, JESD22-A114-F)	2	KV
Store temperature Range	-55 to 150	°C
Operating Junction Temperature	-40 to 150	°C
Maximum Power Dissipation (SOP14)	0.85	W
Maximum Power Dissipation (ESOP16)	1.5	W
Lead Temperature	260	°C

Electrical Characteristics:

T_A=+25°C, unless otherwise noted.

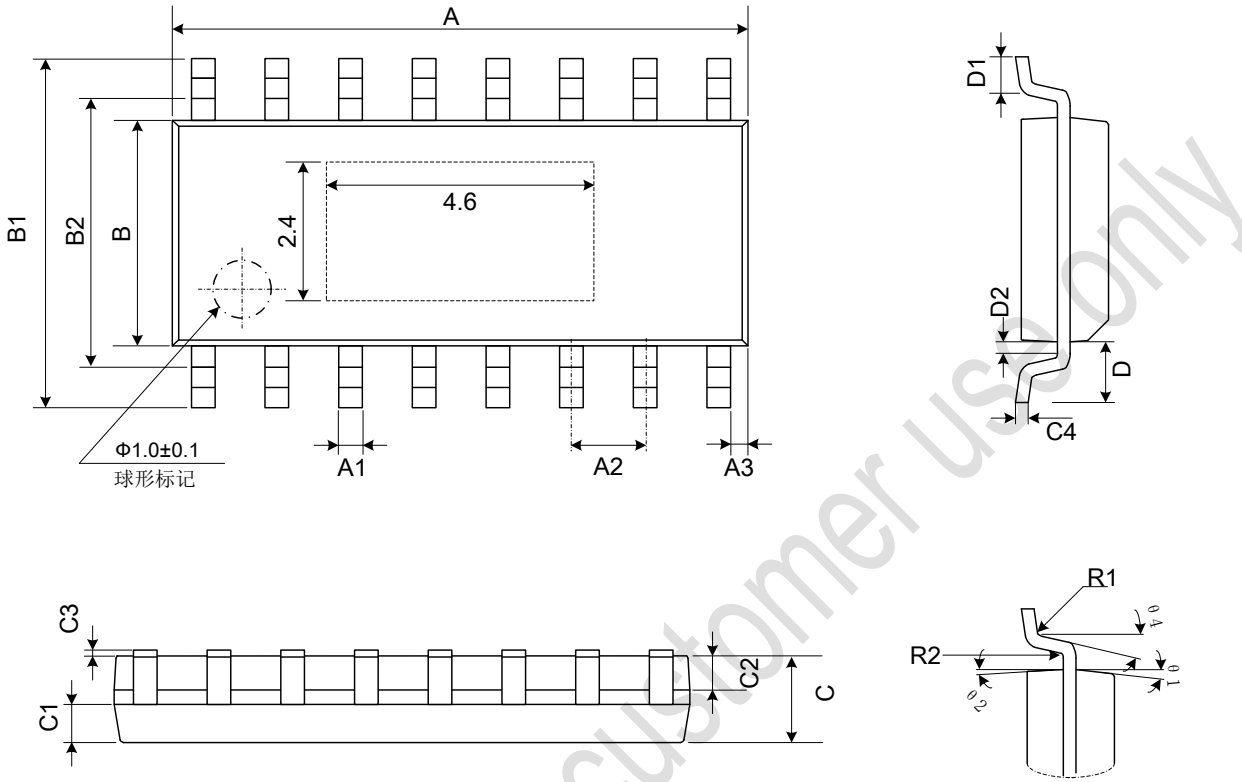
VDD Supply Section						
V_{DD_TH}	Startup Voltage			13.2	14	V
V_{DD_UVLO}	Under-voltage Lockout Threshold		7.0	7.5		V
$I_{VIN\_STARTUP}$	VIN current charge VDD at startup	VIN=100V, VDD=6V	2	3	4.5	mA
V_{DD_CLAMP}	VDD's clamp voltage	I(VDD)=2mA		20		V
$I_{DD\_QIESCENT\_MAX}$	Max Quiescent current after startup	VDD=17.5V, GATE1=1nF, fsw=22kHz	400	700	1000	uA
VIN_{BV}	VIN breakdown voltage		600			V
I_{DSS_VIN}	VIN's leakage current	VDD=14.5V, VIN=600V	10	40	60	uA
EA Section						
V_{FB_REF}	FB regulation voltage		862	917	972	mV
V_{COMP_CLAMP}	Comp lower clamp voltage after startup	FB=1.2V		800		mV
$V_{FB\_CLAMP\_REF}$	FB clamp voltage reference	IFB=50uA	1.75	1.93	2.19	V
$I_{DRAIN\_OPL\_REF}$	Drain OPL reference current through FB pin			20		uA
$I_{LED\_SHORT\_REF}$	LED short protection through FB pin			50		uA
BOOST (or FLYBACK) Section						
T_{MAX_OFF}	Max off time		30	45	60	us
T_{MIN_OFF}	Min off time			2		us
T_{DET_BLK}	Valley detection blanking time			750		ns
F_{MAX_SW}	Max switching frequency			250		kHz
V_{CS1_LIM}	CS1 current limit voltage			1.52		V
T_{ON_MIN}	Minimum turn on time		300	400	550	ns
T_{LIM_BLK}	CS1 current limit blanking time			280		ns
V_{OVP_TH}	Boost output over voltage protection threshold voltage		1.83	1.93	2.03	V
LDO Section						
V_{CS2_REF}	CS2 regulation current reference		292	306	320	mV
V_{CS2_IIM}	CS2 over current detection			410		mV

R_{DSON}	PowerFET's Rdson	I(DRAIN)=30mA	20	30	35	ohm
V_{BV}	PowerFET's breakdown voltage		500			V
I_{DSS}	PowerFET's leakage	V(DRAIN)=500V, VDD=6V			20	uA
TEMPERATURE Protection Section						
T_{OTP}	Over temperature shutdown threshold			150		°C
T_{OTP_HYS}	Over temperature protection hysteresis			30		°C

NOTE: 1. the upper and lower limitation is guaranteed by ATE testing.

Physical Dimensions:

ESOP16



\尺寸 标注\	最小(mm)	最大 (mm)	\尺寸 标注\	最小(mm)	最大(mm)
A	9.80	10.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05 TYP	
A2	1.27 TYP		D1	0.40	0.70
A3	0.302 TYP		D2	0.15	0.25
B	3.85	3.95	R1	0.20 TYP	
B1	5.84	6.24	R2	0.20 TYP	
B2	5.00 TYP		θ1	8^0 ～ 12^0 TYP	
C	1.40	1.60	θ2	8^0 ～ 12^0 TYP	
C1	0.61	0.71	θ3	0^0 ～ 8^0	
C2	0.54	0.64	θ4	4^0 ～ 12^0	
C3	0.05	0.15			

Notes:

All dimensions are in millimeters.

Environment Protection and RoHS Compliant：

To protect our environment, the devices in these pacakges are designed to be green. It is RoHS compatible for all 6 substances, free of Halogen, Bromine/BFR.

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