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Plating pulse switching power based on a CPLD

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ABSTRACT

This paper presents a method of using a CPLD to generate a PWM trigger pulse to a full bridge inverter and a chopper circuit. This method results in a very good high power and low voltage large current pulse plating power supply. A single-chip microcomputer is the core of the feedback control system. A fuzzy PID algorithm with SCM and CPLD complexes precisely controls the output voltage, allowing it to maintain a constant value. The system contains a protection circuit that detects output current and output voltage and can correct the system if it enters an over-current abnormal state, ensuring that the driving circuit can effectively drive the IGBT. The circuit is also protected by setting the inverter frequency and dead time of a digital PWM chip. This method for bidirectional pulse plating power supply digital control was verified to be correct and practicable by a Matlab software simulation.

1. Introduction

Traditional DC plating uses the action of DC around the cathode in an electroplating solution of metal ion under continuous precipitation to destroy the uniformity of the solution concentration in the electroplating bath and produce certain concentration differences [1]. This approach leads to an increase in the plating on the hydrogen evolution volume, resulting in bad quality of the plating layer, pinholes, pits, roughness and foaming problems. 'Reverse current pulse with timing mode', a bidirectional pulse electroplating method, can solve the problems caused by the direct plating well. In fact, pulse electroplating can be regarded as switching DC plating. The forward pulse equivalent DC plating process starts by applying the inverting pulse peak current (a 2–3 times larger positive value). The transient current of the metal ion is in the high overpotential reduction state. After the negative current turn-off, the solution near the cathode metal concentration returns to the initial state and concentration polarization is eliminated. This greatly optimizes the next positive cycle of pulse plating process. Pulse inversion can simultaneously produce favorable recrystallization of the deposited layer and adsorption phenomena. Practice has proven that bidirectional pulse plating refines the crystal layer, improves the coating quality, and saves precious metals. These are incomparable advantages over traditional DC plating. This paper describes a CPLD control plating pulse switch power supply.

2. Experimental

2.1. Overall system design

Our bidirectional pulse power supply is mainly composed of an inverter main circuit, a control circuit, a drive circuit and a protection circuit. The overall structure diagram is shown in Fig. 1 [2–6]. The main circuit is responsible for power conversion. The control circuit is responsible for power supply constant voltage control and IGBT switching control. The drive circuit is responsible for driving IGBT. The protection circuit is used to control the primary circuit with over-current, over-voltage protection.

The main circuit is composed of a full bridge inverter using IGBT, 50 Hz, 380 V alternating current after rectification, a capacitance–resistance filter (formed after approximately 520 V direct current), and the IGBT full bridge inverter circuit. The inverter generates a high frequency alternating current (20KHZ), which passes through a DC blocking capacitor and transformer. It is transformed into a low voltage and high current AC. It passes through a full wave rectifier bridge into the low voltage DC power, the reactor and the capacitor filter. Finally, it passes through the H-bridge chopper, formation pressure and negative pulse.

Beyond the main circuit, the rest can be characterized as a bidirectional pulse power control system and an auxiliary power supply control system. This consists of the main control system, the protection circuit, the voltage sampling circuit, the driving circuit and other components. The process of this circuit is as follows: (1) the main circuit operates normally, (2) the main control system uses the sampling circuit to obtain certain signal, (3) the system performs a comparison operation between the main control system and the digital PWM, (4) the drive circuit sends a control signal, so

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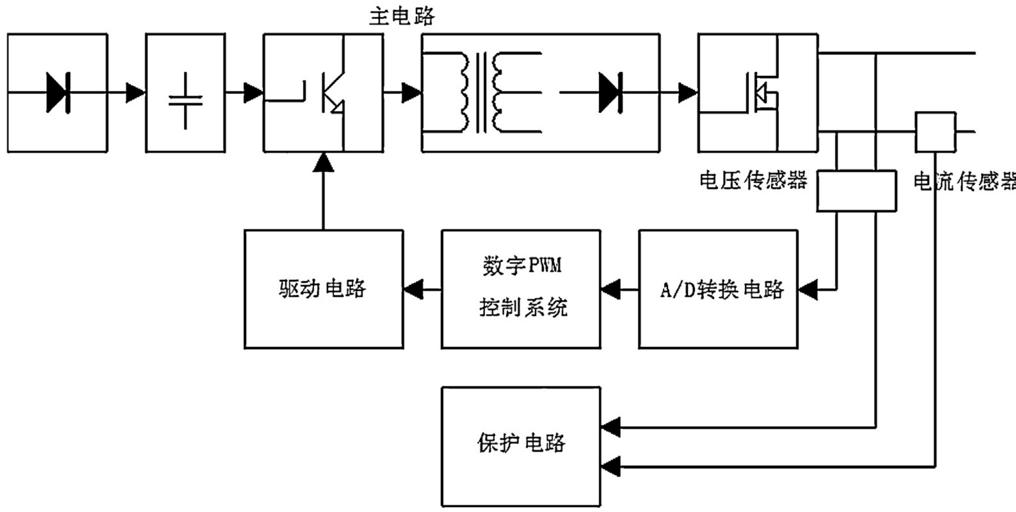

Fig. 1. Overall block diagram of the pulse power system.

that the main circuit and H-bridge quickly break-over and (5) the output end obtains positive and negative pulse voltage requirements.

2.2. The main circuit of the bidirectional pulse power supply

To achieve a new high power, low voltage and high current, high frequency, bidirectional pulse power supply circuit, we selected a full-bridge PWM converter. It is suitable for applications that require low voltage output (5–20 V), high power, and larger ranges of power supply voltage and load current. The use of a PWM full bridge converter does not require an extra auxiliary device. It has the advantage of simple structure and is therefore very suitable (see Fig. 2).

Using the filter circuit and the rectification circuit, the 380 V AC current becomes a stable DC power source. Then, the transformer step-down and IGBT chopper circuit convert the DC to AC. The AC current is obtained by step-down transformer and passed through the diode to satisfy the LC filtering electroplating needs of the adjustable DC power. An H-bridge chopper circuit is added to obtain a bidirectional pulse.

The full bridge inverter circuit for a voltage-type inverter circuit is composed of two bridge arms. Each bridge arm is composed of two controllable devices and two anti-parallel diodes. If the DC side is connected with a sufficiently large capacitance, the output voltage is the midpoint of the two bridge arms. The PWM signal is designed such that two phase differences of 180° in the pulse signal produce V1 and V4 in one cycle and then turn-on and turn-off the forward voltage. The upper end of the full bridge circuit is called the forward full bridge. The lower end of the full bridge circuit is called negative full bridge, producing V2 and V3 in one cycle and then turn-on and turn-off the output voltage. When the load is sensitive, the output voltage of the rectangular wave (i.e., amplitude for the DC side voltage) and output current varies with load. In some time ago V1, V4 for conducting state, this time to the V1, V4 off signal to V2, V3, V1, V4 turn-on signal, shutdown, but not immediately change the current D8, D9 continuous current conduction, current to the DC side capacitor charging, until the current will be zero, V2, the V3 opened, voltage. Reverse full bridge and forward full bridge similar to. However, in the positive and negative pulse output state, pulse output shall be set between the dead zones, preventing the positive and negative output from passing to the full bridge through conduction. During the dead time, the switch tube ends at an anti-parallel diode for continuous flow. The forward full bridge has stopped working, and the negative full bridge has not begun work time. The current passes through diodes 8 and 9 for continuous flow, and the feedback of energy stored temporarily in the DC side capacitor, which plays the role of a buffer.

The output voltage square wave passing through a transformer to change the amplitude meets the amplitude requirement. Then, passing the signal through a full wave rectifier, converting the output voltage into a DC amplitude, and finally passing it through the H-bridge chopper circuit meets the positive and negative pulse power requirements.

The H-bridge chopper circuit working principle is similar to the inverter bridge. The H-bridge chopper circuits outputs in four modes: DC, single pulse, pulse and reverse DC. The pulse amplitude, frequency, and duty ratio (in a certain range) are continuous and adjustable. It has two arms; each bridge arm is composed of two controllable devices and two anti-parallel diodes. With a full bridge output and a filter capacitor, we control 1, 4 at the same time as the turn-on and turn-off of the forward voltage and we control 2, 3 at the same time as the turn-on and turn-off of the output voltage.

2.3. Control circuit

At present, the inverter power supply often uses special chips such as TL494 and SG3525. The PWM waveforms are generated by the feedback signal and the PWM waveform width adjustment is used to obtain stable output. After the design is completed, the control circuit is a relatively independent system. The control mode cannot be changed, and the overall function is system coordination.

A single chip microcomputer and CPLD with programming is used to achieve a PWM waveform. This method requires only one chip to complete the task, due to the use of VHDL programming with PWM signal output. Changing the CPLD external crystal oscillator frequency improves the duty ratio of the adjustable precision. The power switch tube of the dead time can also be conveniently adjusted with high precision and control.

The system design [7] is shown in Fig. 3. Note the digital PWM chip, its external pin, *oc*, for over-current protection control, and *uv*, for under-voltage protection control. The *pwm_en* label indicates the PWM pulse output enable control terminal. The figure also shows the protection signal input end, a digital PWM control chip and some control signals. On the left of the figure are various protection signals and a control signal input control. The leads on

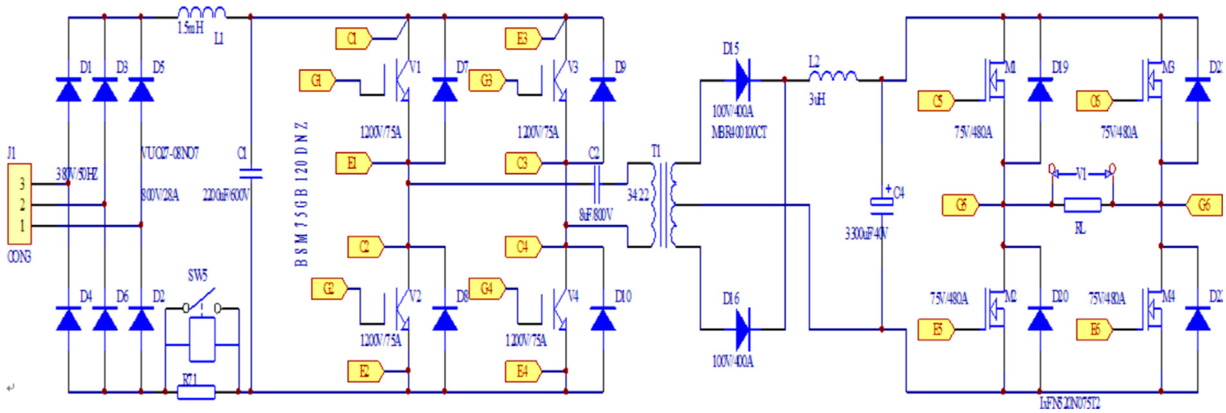

Fig. 2. Pulse power main circuit structure diagram.

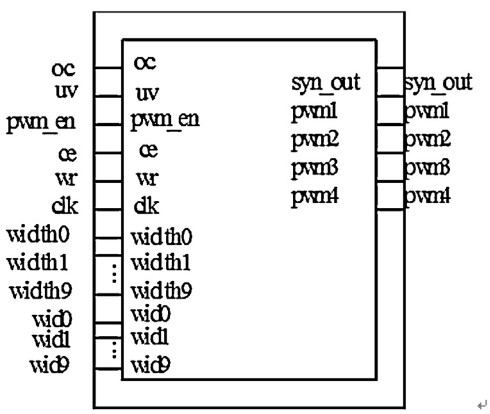

Fig. 3. Digital PWM chip control signal distribution diagram.

the right are for the signal output control terminal. The CLK lead is controlled by a clock signal input, which is the digital PWM chip count control baseline rhythm, and is the foundation of whole system. It has stable output and improves the accuracy of the role. The *ce* marks the chip select terminal. The *wr* marks the write signal control end. The *width*[*0*. . .*9*] and *wid*[*0*. . .*9*] leads set the pulse width of the data input end through a data bus connected to a control processor chip, and given by single pulse width value. These control signals, in coordination, determine the digital PWM chip strobe and write pulse width data. The *pwm1*, *pwm2*, *pwm3* and *pwm4* are tied to PWM pulse output. They are used to output two paths of the drive pulse signal with phase difference of 180 DEG. *Syn_out* is the output signal coordination control end. It is connected to the microcontroller to control the entire system.

Generally, a high frequency IGBT inverter main circuit working frequency is 20 kHz, so it has a working cycle of 50 μs. In the full bridge inverter circuit, the two output drive pulses must ensure that there is enough dead time. During the dead time, the two bridge arm four switching devices are not conducted. Only the diode is freewheeling to ensure that the power device is not burned and the circuit operates safely. This is due to the power switching device switching ends of an anti-parallel diode, resulting in a reverse recovery time. For the main circuit of the IGBT, considering these dead time requirements, the dual PWM pulse has a duty ratio of no more than 80%. The single PWM pulse duty ratio shall not exceed 40% (i.e., each bridge arm of the two IGBT has maximum conduction time of $50 \times 0.4 = 20$ μs, and the PWM pulse is generated for each dead time between $50 \times 0.1 = 5$ μs). If the CPLD/FPGA external crystal oscillator is set to 50 MHz (i.e., the clock period is 0.02 μs) and a 20 kHz IGBT full bridge inverter work period is 50 μs, then a total of 2500 clock cycles pass as each arm conducting a period of dual pulse width is changed twice. Therefore, for each single clock cycle, the dual pulse width changes in 2 clock cycles, and the duty ratio of the rate of change is 2/2500 = 0.08%. The duty ratio of precision can be achieved by conveniently changing the external crystal size. Finally, according to the above analysis, using a 50 MHz crystal and a full bridge converter frequency of 20 kHz, the system has a total of 2500 clock cycles and an IGBT dead time requirement of a single PWM maximum output duty ratio of 40%, accounting for 1000 clock cycles. Therefore, the actual system can be adjusted for

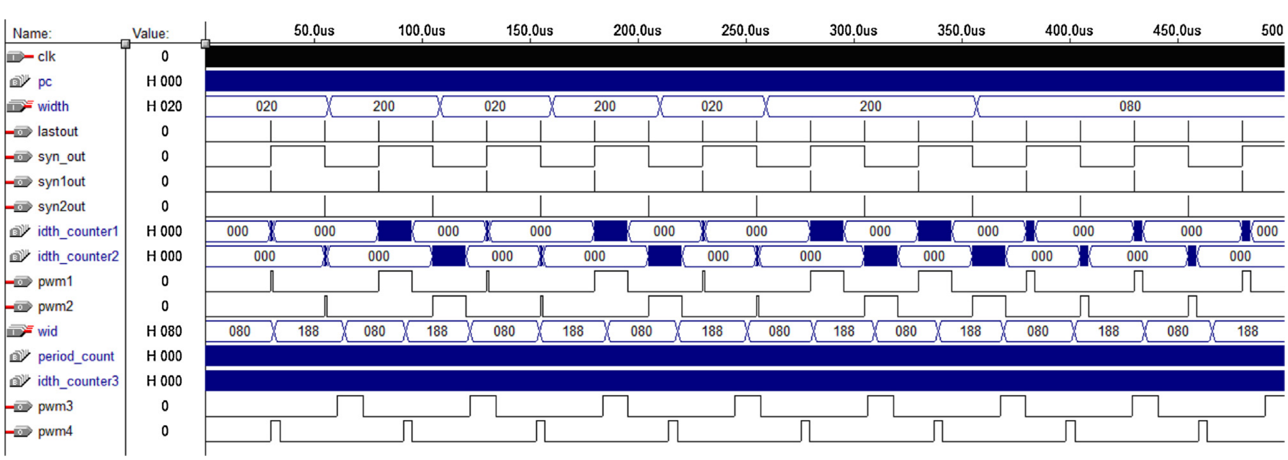

Fig. 4. The generation of the four-channel digital PWM.

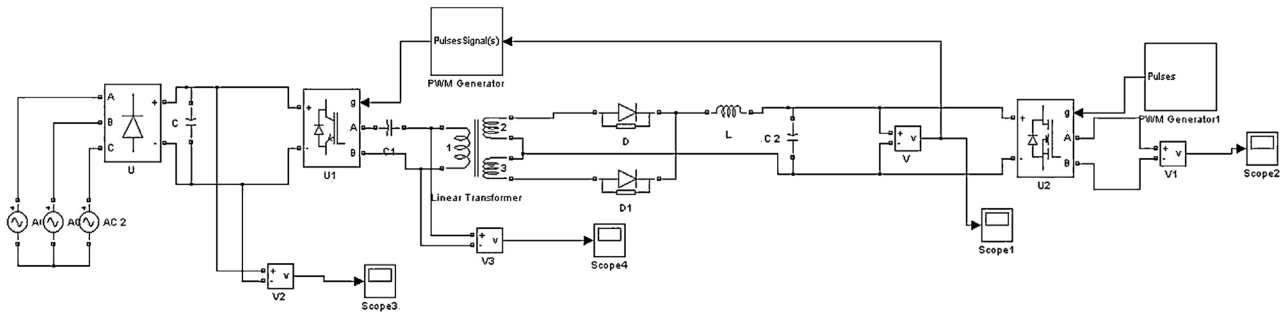

Fig. 5. Simulation diagram of the main circuit.

a pulse number range in 0–1000. The number of bits of the input pulse width is 10 ($2^{10} = 1024 > 1000$).

The design of a bidirectional switch used in the power supply of a MOSFET tube composed of an H bridge chopper circuit also needs a two phase difference of 180° output pulse. With the IGBT full bridge pulse driving only different frequencies, it is only required to cycle the register initial value set. The other part can refer to IGBT full bridge pulse driving. Program results from four pulse (PWM1, PWM2, PWM3, and PWM4) simulation waveforms are shown in Fig. 4.

Overall, the PWM pulse wave generated in the SYN1OUT is ‘1’, ‘0’. PWM1 goes from ‘1’ to ‘0’ in a jump at the falling edge of the output pulse count. The PWM wave occurred from a ‘1’ to ‘0’ jump. PWM is ‘1’. The time axis is the pulse count register count time. PWM2, PWM3, and PWM4 are similar. It can be observed from the figure that in producing two phase difference of 180° PWM trigger pulse, the pulse width is composed of a single chip microcomputer calculation of feedback voltage with the given value and the pulse width value. When the single chip computer CPLD value changes due to the WIDTH [9. . .0] input change from 20 to 200, the output of the PWM duty cycle is also changed accordingly, but the cycle is the same. Therefore, the duty ratio is determined by the WIDTH [9. . .0] input to the pulse count register count value.

3. Results and discussion

3.1. The main circuit simulation model

With pulse width modulation (PWM) for the control of the core, we used an IGBT full bridge topology. A MATLAB Simulink simulation result of the main circuit of the circuit diagram is shown in Fig. 5. The Pulse power main circuit has IGBT power switch full bridge topology. The inverter frequency is 20 kHz.

3.2. Simulation waveform

After the parameters are calculated and the element is selected and set, the main circuit operation under a bidirectional pulse switching power supply waveform is shown in Fig. 6.

It can be observed that the basic realization of the test requirements of bidirectional pulse power supply is voltage stability. However, we found there is a small amount of clutter. The reason may be that the rectification process includes a small amount of harmonic voltage fluctuation after the H bridge chopper circuit, at the end of the circuit output waveform display.

3.3. Experimental results

A prototype of the plating pulse switching power supply was built and tested in the laboratory. The experimental waveform is shown in Fig. 7. It may be observed that positive output voltage is 5 V, $t = 0.9$ s, and the negative output voltage is -10 V, $t = 0.25$ s.

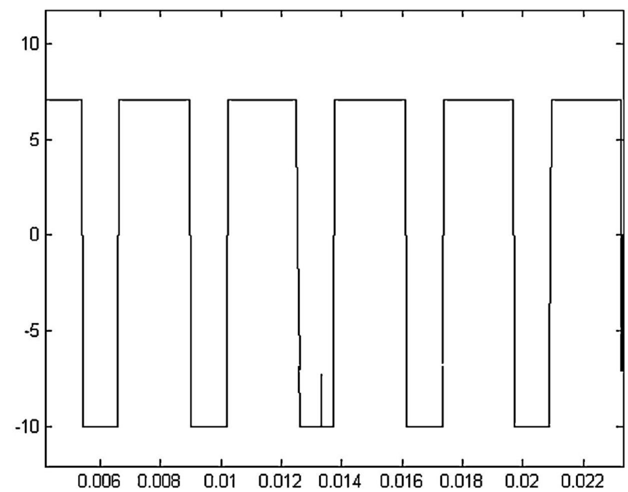

Fig. 6. Diagram of simulation results.

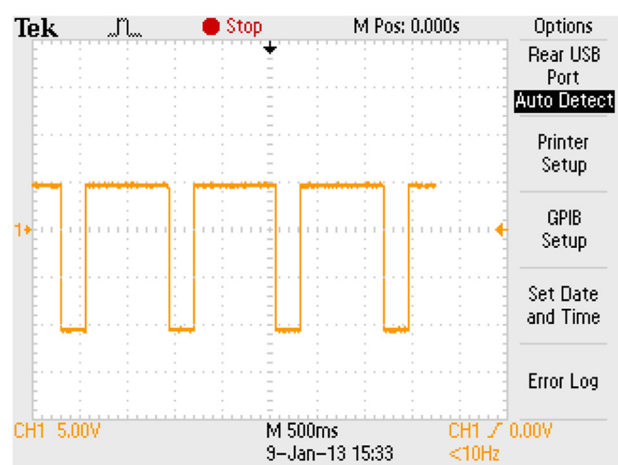

Fig. 7. Experimental results.

4. Conclusions

Based on the principle of full-bridge inverter circuit research, we describe a type of high power double pulse electroplating power supply. The model is used with a digital PWM pulse and a single chip with a CPLD control scheme. The design of the chip includes a two phase difference of 180° and adjustable pulse width control. The bidirectional pulse power main circuit, the control circuit and other parts of the structure were analyzed in detail. They were validated by a simulation and produced an ideal waveform.

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