Compensation of Dual Slope ADC Error Caused by Dielectric Absorption

L. Michaeli, J. Šaliga, P. Dolinský, I. András

Department of Electronics and Multimedia Telecommunications, Faculty of Electrical Engineering and Informatics, Technical University of Košice, Slovakia
Email: linus.michaeli @tuke.sk

Abstract. *Integrating Analog to Digital Converters (IADCs) are known for high resolution and continuous transfer characteristics. Nonlinearity of the transfer characteristics is influenced by dielectric absorption of the integrating capacitor, which is the only external element. The nonlinearity can be compensated if dielectric absorption elements are known. This article deals with such compensation by means of theoretical analysis, which is more feasible because of precision constraints of the instrumentation.*

Keywords: Dielectric Absorption, Dual Slope ADCs, ADC Nonlinearity Compensation

1. Introduction

Dielectric absorption (DA) of capacitors is a source of possible errors in the integrating analog to digital converters (IADC). Application manuals of IADCs recommend the use of polypropylene integrating capacitors with low dielectric absorption (DA < 0.5 %) [1], [2]. The physical reason - relaxation of dielectric dipoles in the capacitor's dielectric – is manifested by "memory" effects in capacitors utilized in the analog preprocessing blocks. Dielectric absorption modelled by RC dipoles in parallel with the main capacitance determines the residual charge from absorption capacitors.

Theoretical analysis of the converting procedure shows that in addition to the low dielectric absorption (DA) the time constants also influence nonlinearity of the dual slope IADC. Optimal adjustment of the time constants of dipoles representing dielectric absorption allows to compensate for the IADC nonlinearity. Requirements on instruments for practical testing are high with ADC resolutions typical for IADC. Such testing can be circumvented by using a mathematical model of dual slope IADC and analysing the impact of the capacitor dielectric constants on the resulting nonlinearity. Real parameters of the capacitor could be identified by measuring the discharging process [3]. The main novelty of this paper is the analysis of the essential absorption effects determining IADC nonlinearity and a method of compensation of these effects caused by the integration capacitor.

2. Dielectric Relaxation in Real Capacitors

Dielectric relaxation process of a capacitor can be modelled as shown in Fig.1. The capacity C_1 represents the behaviour of an ideal capacitor. Parallel RC branches represent the relaxation processes of the dielectric. In a real capacitor with significant dielectric absorption the charge on the capacity C_1 is being recovered from the parasitic capacitors (C_2,C_3,..C_i) for any change of its voltage.

The DA represents the percentage of the voltage, which is recovered on the capacitor C_1 when the previously charged capacitor is shorted for a short period. The testing procedure is standardized and described in [4]. DA coefficient gives no information about time constants of the parallel RC branches in the capacitor's model.

Authors published method based on the direct optimization method of the circuit parameters C_i, R_i in the set of linear differential equations describing circuit in Fig.1 during charging process [3].

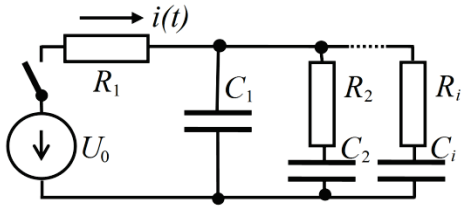

Fig. 1 Electrical model of the dielectric absorption in the capacitor and process of Isothermal Current Analysis.

3. IADC Nonlinearity Caused by the Dielectric Absorption

Let consider the simplified structure of dual slope IADC in Fig.2 Time interval of the first phase is constant T_0 and in the second phase T_x. The dielectric absorption of the integrating capacitor is modelled by three parallel absorption RC branches. Two branches R_2-C_2, R_3-C_3 represent absorption effects. R_4-C_4 branch is considered as relaxation branch suitable for nonlinearity compensation. The output voltage from the integrator is described by the system of linear differential equations.

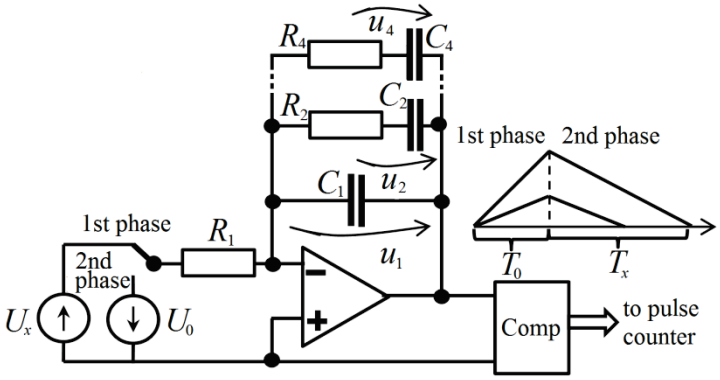

Fig. 2 Block scheme of dual slope ADC

$$\begin{bmatrix} u_1' \\ u_2' \\ u_3' \\ u_4' \end{bmatrix} = \begin{bmatrix} -\frac{G}{C_1} & \frac{1}{R_2C_1} & \frac{1}{R_3C_1} & \frac{1}{R_4C_1} \\ \frac{1}{R_2C_2} & -\frac{1}{R_2C_2} & 0 & 0 \\ \frac{1}{R_3C_3} & 0 & -\frac{1}{R_3C_3} & 0 \\ \frac{1}{R_4C_4} & 0 & 0 & \frac{1}{R_4C_4} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \end{bmatrix} + \begin{bmatrix} b \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{1}$$

The system of differential equations (1) can be solved analytically. Here conductivity $G = \left(R_2R_3 + R_3R_1 + R_2R_1\right)/R_1R_2R_3$, $b_1 = U_x/C_1R_1$ in the first phase and $b_2 = -U_{REF}/C_1R_1$ in the second phase. The output voltage of the integrator in the 1st and 2nd phase is described as

$$\begin{aligned} u_1(t) &= A_1t + A_2e^{-B_2t} + A_3e^{-B_3t} + A_4e^{-B_4t} \qquad \text{1. phase} \\ u_1(t) &= u(T_0) - (A_1t + A_2e^{-B_2t} + A_3e^{-B_3t} + A_4e^{-B_4t}) \text{ 2. phase} \end{aligned} \tag{2}$$

The nonlinearity $INL(k)$ of the ADC transfer characteristic was obtained as the difference between calculated time interval T_X and idealized time ${}^{i}T_X$. The ideal time interval was calculated as a linear interpolation between time $T_{X\min}$ for smallest input voltage $U_{X\min}$ and

$T_{X\max}$ for the voltage $U_{X\max}$ at the end of Full Scale Range (FSR). Proposed method is suppressing offset and gain error. The code value k is calculated as $k = round\left[2^N U_X / FSR\right]$. The resolution of IADC is N.

$$INL(k) = \frac{T_X - {}^iT_X}{{}^iT_X} 2^N \text{ where } {}^iT_X = \frac{T_{X\max} - T_{X\min}}{U_{X\max} - U_{X\min}}\left(U_X - U_{X\min}\right) + T_{X\min} \quad (3)$$

The proposed simulation allows predicting the influence of the dielectric absorption effects on the nonlinearity of IADC. Proposed software allows search for additional RC branch which can compensate nonlinearity caused by the two dominant relaxation absorption RC components.

4. Experimental Results

The functionality of studied dual slope IADC was modelled using time interval T_0=40 ms, input resistance R_1=50 kΩ and resolution N=12 bit. The first combination of absorption branches is represented by the resistance in R_2=20 MΩ (τ_1=100 ms) and R_3=10 MΩ (τ_1= 50 ms) Fig.3.a.

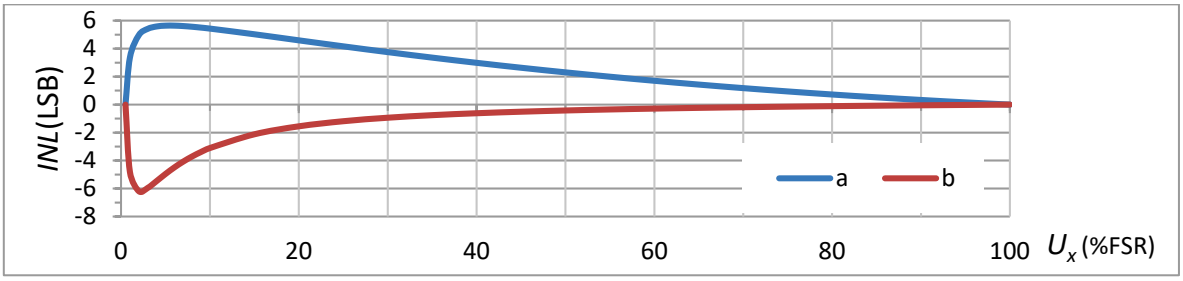

Fig. 3 Nonlinearity error of dual slope IADC with two time constants τ_1=100 ms, τ_2=50 ms (a), τ_1=1 ms, τ_2=2 ms (b)

The second combination of absorption RC braches is represented by R_2=500 kΩ (τ_1=1 ms) and R_3=2 MΩ (τ_1=2 ms) Fig.3.b. Modelled situations showed the high impact of time constants of dominant absorption RC branches on the linearity of the transfer characteristic after correction offset and the linearity error of dual slope IADC. Time constants of absorption branches change the integral nonlinearity from its convex to the concave shape. This provides an opportunity to minimize extremal nonlinearities along full voltage range by the additional RC branch.

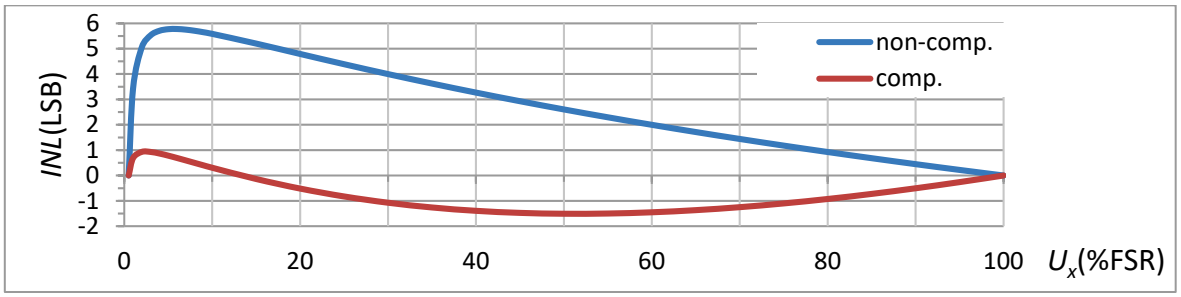

Fig. 4 Nonlinearity error of DS IADC with integrating capacitor Vishay MKP 470 nF

In the next experiment model of real Vishay MKP 470 nF capacitor was used. Its dominant absorption parameters were taken from [5]. Two dominant RC branches were represented by resistance R_2=7.2 MΩ, C_2=3 nF, R_3=16.7 MΩ and C_3=8.8 nF. Ideal capacity using the identification of the main exponential component was C_1= 458 nF. The dielectric absorption coefficient is DA= 2.5 %. Authors utilized third R_4-C_4 branch for the compensation of

nonlinearity shape. Fig. 4 shows the possibility to compensate nonlinearity by R_4=20 MΩ and C_4=1 nF.
Another tested component in IADC was the capacitor Arcotronic MKP 470 nF. Its parameters were characterized by C_1=478 nF, R_2=1.4 MΩ, C_2=23 nF, R_3=22.7 MΩ and C_3=4.7 nF [5]. The dielectric absorption coefficient is DA=5.7 %. Fig. 5 shows nonlinearity improvement by R_4=20 MΩ and C_4=6 nF.

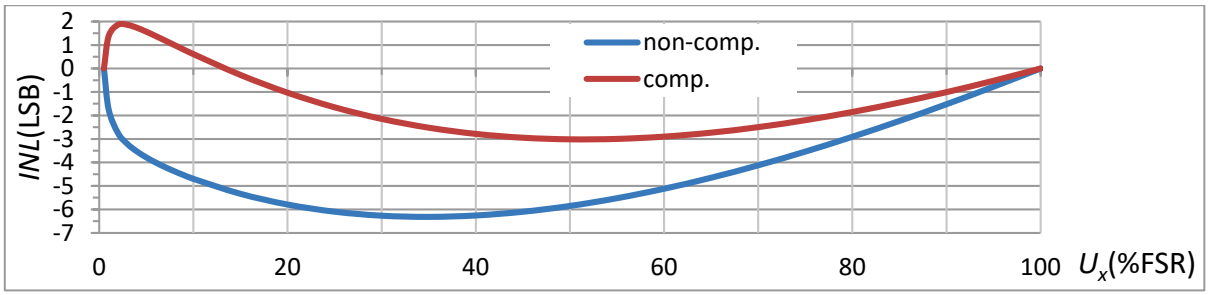

Fig. 5 Nonlinearity of DS IADC with integrating capacitor Arcotronic MKP 470 nF before (a) and after compensation by external RC branch (b).

5. Conclusions

Dielectric absorption of the integrating capacitor in the IADC has a considerable impact on the nonlinearity error. The maximal nonlinearity in Fig. 5 determined by (4) is INL_{max}=6 bits. It corresponds to the maximal value of the effective number of bits $ENOB$=7. This value is much smaller than the maximal resolution defined by ADC producers. The guaranteed resolution for ICL7109 is equal to 12 bit. Careful integrating capacitor selection is critical.
The software model of the dual slope IADC allows to compensate the integral nonlinearity by an external RC branch. The main advantage of the proposed approach is the possibility to estimate final nonlinearity without expensive testing equipment.
Another conclusion of the proposed simulation is that the information about the capacitor's absorption coefficient is not sufficient. The circuit designer has to know parameters of components representing dielectric absorption.

Acknowledgements

The work is a part of the projects supported by the Slovak Research and Development Agency (No. APVV-15-0692).

References

[1] Microchip Data sheet, Precision Analog Front Ends with Dual Slope ADC, TC500/A/510/514, www.microchip.com.

[2] ICL7109 Datasheet - Intersil Co., http://www.alldatasheet.com/datasheet-pdf/pdf/67426/INTERSIL/ICL7109.html.

[3] Michaeli L, Šaliga J, Godla M, Lipták J, Kollár I. Measurement of distorted exponential signal components using maximum likelihood estimation. Measurement, 58: 503-510, 2014.

[4] Kuenen JC, Meijer GCM. Measurement of dielectric absorption of capacitors and analysis of its effects on VCOs. IEEE Transactions on Instrumentation and Measurement, 45 (1): 89-97, 1996.

[5] András I, Dolinský P, Michaeli L, Šaliga J. Improvement of Multiexponential Signal Decomposition by the Preprocessing. Proc. of 26th Conf.Radioelektronika: 107-111, 2016.

[6] IEC/EN Standard 60384