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Digital Satellite Equipment Control (DiSEqC[™])

Applications Information For Using a "PIC" Microcontroller in $DiSEqC^{TM}$ And Simple Switcher Version 1.0

Reference Documents that define the DiSEqC System:

DiSEqC[™] Bus Specification Version 4.2 (February 25, 1998) DiSEqC[™] Slave Microcontroller Specification Version 1.0 (February 25, 1998) DiSEqC[™] Logos and Their Conditions of Use (February 25, 1998)

Associated Documents:

Update and Recommendations for Implementation Version 2.1 (February 25, 1998)

Application Information for using a "PIC" Microcontroller in DiSEqC[™] LNB and simple switcher Applications Version 1.0 (June 7, 1999)

Application Information for Tuner-Receiver/IRDs (April 12, 1996)

Application Information for LNBs and Switchers Version 2 (February 25, 1998)

Reset Circuits for the Slave Microcontroller (August 12, 1996)

Simple Tone Burst Detection Circuit (August 12, 1996)

Positioner Application Note Version 1.0 (March 15, 1998)



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1. Introduction

The Program Code of the original DiSEqCTM "Slave" microcontroller version 1.0 (using a Philips 8xC750) has now been adapted to a Microchip 'PIC' microcontroller for LNB and simple Switcher applications. The PICmicro has only 18 functional pins, compared with the 24 of the original Slave (and different hardware Input / Output configurations) so the new code is only suitable for applications requiring up to 6 switching control pins. The program code is typically just less than 512 words, so a PICmicro with $\frac{1}{2}$ kword of Program Memory (PROM) should be sufficient, although certain optional features may require a larger PROM.

Unlike the original Slave microcontroller, the new Program Code does not "scan" the controller pins to determine which functions are active externally. Instead, the Program Code must be adjusted for each specific application, so that the required switch outputs are available, and the correct DiSEqCTM "Level 2.0" Reply messages are returned. To define the requirements for each application, a "Fax-back" form (*Appendix A.*) has been prepared to indicate the main programming options. *See section 7.* for an explanation of the available options. It is assumed that LNBs use the standard 'Low' and 'High' Local Oscillator frequencies of 9.75 GHz and 10.6 GHz, but if not, the actual frequencies should be stated so that the correct DiSEqCTM Reply messages can be programmed.

2.

Choice of PICmicro Device

The program code is designed to use the PIC 16C620x microcontroller, although a 1 kword version (..621..) may be necessary if more complex requirements are requested. These microcontrollers include two analogue comparators on-chip, and thus eliminate many of the external components needed in the original DiSEqCTM Slave application. The 'x' in the above type number indicates that the device may optionally have a suffix 'A', which is a reduced-cost (smaller mask-geometry) version with similar electrical characteristics. The full type number includes other suffices to indicate the temperature range, maximum operating (clock) frequency and package style, as defined as follows:

For LNBs (and switchers used outdoors), an extended temperature range is required (- $40 \times to +85 \times C$), referred to as an "Industrial" type with the suffix 'I'. The software is designed to operate at a nominal clock frequency of 4 MHz and thus the standard 4 MHz PICmicro is suitable (i.e. with suffix '- 04').



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Three package styles are available: Plastic Dual in line (PDIP), Small Outline (SOIC) and Shrink Small Outline (SSOP), with suffices 'P', 'SO' and 'SS' respectively. Also, UV-erasable devices can be obtained for program development, in a windowed CERDIP package, with the suffix 'JW'.

Thus a complete type number is typically: 'PIC 16C620(A) - 04 I SO'

The "production" versions are One Time Programmable (OTP) devices and thus must be programmed with the appropriate data. This can be done on-site (sometimes in the actual target hardware), by a distributor, or for large volumes, in the Microchip factory. The latest Microchip "Product Line Guide" (October 1998) gives the possibility of a mask-ROM option for just the "..620A.." member of the family, but indications are that it only may be appropriate for volumes above 200k. Full data and contacts are on the Microchip Internet site (and also CDROM) at: http://www.microchip.com

3. Supply voltage and Reset circuit

The PICmicro can accept a wide range of supply voltages, but for this application a regulated supply rail of 5 volts $\pm 5\%$ (or closer) is recommended. This gives a minimum peripheral count when implementing "backwards compatible" detection of 13 / 18 Volt (Polarisation) signalling on the bus.

This particular PICmicro chip includes a "brown-out" (undervoltage protection) circuit, but it should only be enabled if certain limitations are understood. Firstly, the detection level (below which the PICmicro is held in a reset state) may be as high as 4.4 volts in the Industrial temperature-range version. Thus the "brown-out" detector must not be used unless the operational supply rail is always within the range 4.4 to 5.5 Volts.

A more serious limitation is that the "brown-out" detection can only be enabled if the on-chip "Power-up Timer" is also enabled. This "Power up Timer" has a nominal delay of 70ms, but a worst-case limit of 132 ms. However, it is recommended that DiSEqCTM Slaves which receive their power from the Bus should be fully operational within 100 ms of power being applied. This is because LNBs and "cascaded" Switchers may only receive power when they are "selected" by another Switch on the Bus.

Thus it is recommended that the 'brown-out' and / or 'Power-up Timer' should only be used with a local "mains" power supply which may rise (and/ or fall) rather slowly.

The PIC micro's internal "Oscillator Start-up Timer" gives a delay of 1024 oscillator cycles which is only approximately ¹/₄ ms in this application. Thus it is recommended that an external RC circuit is employed for the power-on



reset function. This could be typically a 39 k Ω resistor (the Microchip recommended maximum) and a capacitor of 100 nF, to give a delay of about 10 ms. Note that the Reset input to the PICmicro is the inverse polarity (i.e. "Active Low") compared with the original (8xC750) "Slave" microcontroller.

4. Pin Functions

This family of PICmicros has 18 functional pins (the SSOP package has 20 pins but Vss and VDD are duplicated) of which 5 pins have pre-defined functions (Vss, VDD, Clock-in, Clock-out and Reset). The remaining 13 pins are general purpose Input / Output with 5 pins grouped as "Port A" and 8 pins as "Port B". In this DiSEqCTM application, the 5 "Port A" pins are normally used for the Comparator inputs and outputs (analogue inputs and digital outputs), and "Port B" is used for digital (program control) Input / Output signals. The detailed pin allocations are shown in the table following.

Pin Number (DIP/SOIC)	Pin Number (SSOP)	PICmicro Function Name	DiSEqC™ Function Name	Function Description		
1	1	AN2	REF	V _{DD} / ₂ Reference Voltage out (or in)		
2	2	AN3	DOM	d.c. Detector Output <u>or</u> Mode Input		
3	3	AN4	CRD	Comparator Received Data output		
4	4	MCLR	RESET	Reset (active low) input		
5	5,6	Vss	Vss	EARTH (ground)		
6	7	RB0 / INT	DRX	DiSEqC™ Receive Data input		
7	8	RB1	OP 1	Output 1 (e.g. Hi / Lo Frequency)		
8	9	RB2	OP 2	Output 2 (e.g. H / V Polarisation)		
9	10	RB3	OP 3	Output 3 (e.g. Satellite B / A)		
10	11	RB4	OP 4	Output 4 (e.g. Lo / Hi Frequency)		
11	12	RB5	OP 5	Output 5 (e.g. V / H Polarisation)		
12	13	RB6	OP 6	Output 6 (e.g. Satellite A / B)		
13	14	RB7	DTX	DiSEqC [™] Transmit Data output		
14	15, 16	Vdd	Vdd	Power Supply (+5 volts)		
15	17	OSC2	X 2	Resonator (clock out)		



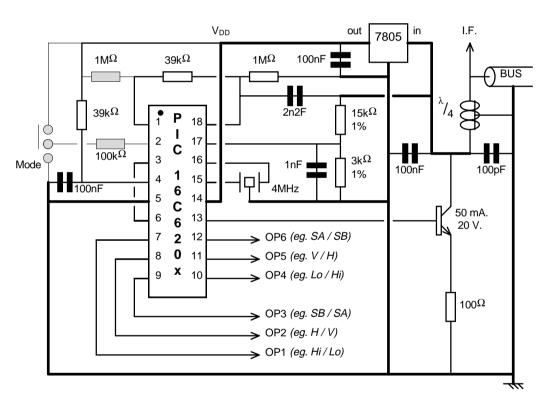
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Pin Number (DIP/SOIC)	Pin Number (SSOP)	PICmicro Function Name	DiSEqC™ Function Name	Function Description
16	18	OSC1	X 1	Resonator (clock in)
17	19	AN0	DDB	Divided d.c. Bus Signal input
18	20	AN1	ACB	a.c. Coupled Bus Signal input

5.

Typical Application Circuit Diagram



The figure above shows a typical peripheral circuit for the PICmicro application. Components which are shown faint shaded are not generally necessary, but may be required in certain applications. Their purpose is outlined in the following description. All pin numbers refer to the DIP and SOIC packages, and the equivalent SSOP pin numbers are shown in the table above. For clarity, all circuit 'nodes' are shown with only 3 lines meeting. 4 lines meeting always represents crossing connections (also shown with a slight 'break' in one path.



6. Circuit Description

The supply rail for the microcontroller is derived from the DiSEqCTM Bus (cable) via a three-terminal regulator such as a 7805 (which can also provide a regulated supply for the rest of the LNB or switcher). Such regulators normally require input and output decoupling capacitors, but the capacitance, particularly on the input, should be as small as practicable (certainly less than 400 nF) because it appears as a direct load across the DiSEqCTM Bus. Any deviation from the nominal 5.0 Volts regulated value will contribute directly to a proportional error in the 15.0 Volt "backwards compatible" H / V detection threshold.

The two internal analogue comparators are configured with their positive inputs commoned to pin 1, but with separate negative inputs to pins 17 and 18. In the normally programmed configuration, their outputs are available externally on pins 2 and 3 respectively. An internal resistive divider chain from VDD to VSS is available and is programmed with its mid point connected to the common input (pin 1). The upper and lower resistive arms are nominally 24 k Ω and thus the source impedance is about 12 k Ω . The specified precision seems to be about $\pm 1\%$, but note that even an external load resistance of 1 M Ω will offset the 'Reference Voltage' by slightly more than 1%.

The d.c. voltage on the DiSEqCTM Bus is externally divided to exactly 1/6 so that at the nominal (15.0 Volts) threshold level, 2.5 Volts is applied to the comparator input on pin 17. This comparator input is adjacent to the 4 MHz clock signal (pin 16), so it is recommended to educable it with a small capacitor, depending on the PCB layout. The divided d.c. voltage is compared with the voltage from the internal divider chain, and, if enabled as an output, the logic result can be measured on pin 2 (although the software detects the value internally).

The other comparator input (pin 18) receives the DiSEqCTM (22 kHz) carrier tone at almost full-amplitude (nominally 650 mV peak-peak) a.c. coupled from the Bus. The coupling capacitor is chosen to give a suitable "high-pass" characteristic to rapidly remove transient d.c. voltage changes on the Bus (including asymmetric superimposition of the carrier tone on the d.c. level). The output from this comparator is brought out to pin 3, where it is externally connected to the PIC's normal external interrupt input (pin 6) for detection by the DiSEqCTM software.

To prevent this comparator amplifying small-amplitude "noise" on the Bus, its negative input is d.c. offset from the reference input by about 100 mV, using a divider chain of typically 1 M Ω and 39 k Ω resistors. The second (optional) 1 M Ω resistor can restore the nominal division ratio, but more significantly these two bias resistors could be scaled down to typically 2.7 k Ω



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precision values (and 10 Ω replacing the 39 k Ω resistor), to swamp any errors in the internal divider ratio.

The clock-oscillator shown for the PICmicro circuit uses a 3-terminal ceramic resonator, but a 2-terminal resonator or crystal could be used provided that the two oscillator pins (15 and 16) are each connected via a suitable capacitor (typically 22 pF) directly to VSS.

The "reset" input (pin 4) must to be biased high for normal operation, and typically a time constant of 5 - 10 ms is suggested. In some circumstances it may be possible to use one of the "start up" circuits within the PICmicro to eliminate the capacitor.

The logic output drive from the PICmicro is limited to a nominal 5 volt swing, but does have a greater current capability (about ± 5 mA with less than $\frac{1}{2}$ Volt drop), compared with the original DiSEqCTM Slave microcontroller.

Where both the "Standby" and "Option Switch" outputs are not required, these outputs may be used instead to carry inverted output switching signals. They may be used to give a more convenient switching polarity, or both outputs may be used to drive complementary switches (i.e. to select between two alternative sources).

7.

Configuration Selection

To define the exact requirements of each user of the Program Code, a "Faxback" form, Appendix A, has been prepared. The following notes explain the purpose of each section on the form:

E-mail address: The fastest and most "portable" method of transferring the Program Code is an e-mail file attachment. Therefore, if possible, please give the e-mail address of the person / department who ultimately requires the Program Code, and send an e-mail to APG with that address, so that the Code can be sent in a "Reply", thus avoiding any errors.

Hardware Identification: To return the correct "DiSEqCTM Level 2.0" Reply messages, different Program Code may be needed for even quite small differences in the external hardware (for example a different number of switching outputs used, or different Local Oscillator frequencies in LNBs). Therefore, please include a Product Identification if more than one type is to be manufactured (or may be in the future).

Family Type: The Address (and reported "Configuration" data) needs to be in accordance with the $DiSEqC^{TM}$ Bus Specification. For the purposes of the Fax-back form, the following may be helpful:



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A "Normal" LNB (address '11h') is any type of LNB which is always at the "end" of the Bus, i.e. it does not have an electrical (e.g. 'F' connector) input. Thus a "Monoblock" (multiple horn) LNB is defined as "Normal".

A "Loop-through" LNB (address '12h') has an electrical input to extend the $DiSEqC^{TM}$ Bus to another device, usually another LNB. This information can be reported to the "Master" (Tuner-Receiver / IRD), so that it can send commands to the more "distant" device.

A "Bus Blocking" Switcher (address '14h') does not extend the DiSEqCTM Bus (i.e. the 22 kHz carrier) through to its input connectors. This information can be reported so that the "Master" does not need to generate commands for more "distant" devices.

A "Normal" Switcher (address '15h') passes DiSEqCTM messages (and d.c. power) through to its inputs so that more "distant" ("cascaded") Switchers and LNBs can be controlled.

On-chip Resets enabled: See section 3. of this Applications Note.

Type of switching Output: The PICmicro employed has effectively only 6 output pins available for switching control purposes, so it is necessary to allocate them to the particular functions required. The Fax-back form offers the following options:

Single Polarity Outputs are ideal for controlling relays (although a current / voltage driver stage may be required) and similar devices which have a "change-over" action. Since only one pin is required for each selection function (e.g. "Satellite Position A / B"), the 6 pins can easily define any required controllable functions. The Program Code can be adapted to make these logic signals either "Active High" (e.g. Logic '1' = High L.O. frequency) or "Active Low" (e.g. Logic '0' = High L.O. frequency).

Complementary Outputs are used in pairs, so only 3 independent selection functions can be available. This output mode is particularly suitable for "Electronic" (diode) switches which effectively have a single "pole" which is either Open or Closed. Each complementary output can drive one such switch so that when one (e.g. "Satellite A") is open, the other (e.g. "Satellite B") is closed.

Decoded Outputs are suitable for 4-input switchers using "Electronic" (i.e. single-pole) switches, where just one input is to be selected at a time. Again, either "Active High" or "Active Low" modes are possible. Note that a 2-input switcher is catered for by the "complementary outputs" mode, but for an 8-input Switcher a separate decoder needs to be driven from 3 "single polarity" output pins, because there are not sufficient pins available with the present software.

Switching Outputs: Generally, just mark the boxes which correspond to outputs which are ACTUALLY REQUIRED. DO NOT mark control signals which only may be used in future applications, because the incorrect Reply messages may be sent by the Program Code. However, for single-polarity



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outputs, it is acceptable to mark both "Active high" and "Active Low" boxes, even if only one may ultimately be used. If "Uncommitted Switch" control signals are required, mark the relevant box(es) with a 'U'. If different output switching modes are required (see the following paragraphs) then mark the two modes differently, e.g. with '1' and '2' suffices.

Function of Pin 2: Normally, the output from the DiSEqCTM Bus d.c. Voltage comparator (backwards compatible H / V signalling) is output from Pin 2. This is not required functionally, but may be useful for testing purposes. However, some Switchers may give the User / Installer a mechanical "configuration" switch to allow the device to be used in different modes. This switch can be connected to pull Pin 2 either to Logic '0' (earth) or to Logic '1' (VDD) levels. Note that when Pin 2 is configured as an input, it has a very high input impedance and therefore MUST be biased either towards earth or VDD (with a 2-pole switch, or pull-up, or pull-down resistors).

One possible option is the "Swap" function which allows the User / Installer to choose whether a Switcher changes "Position" (from Satellite 'A' to Satellite 'B') when a continuous ("backwards compatible") 22 kHz tone is present on the Bus, or selects a normal "High Band" (Local Oscillator Frequency) source in place of a "Low Band" source. Whichever switching function is not controlled by the continuous tone can instead be selected by the "ToneBurst" ("simple DiSEqCTM") message.

Other possibilities are that the User / Installer may wish to adjust a 2-input Switcher to respond to either "DiSEqCTM Satellite Position" commands (e.g. if he has two single-horn LNBs) or to "DiSEqCTM Option" commands, for example where at least one input may already have "Position" Switching (e.g. from a "Monoblock LNB", or from another Switcher). Similarly, a 4-input Switcher may be chosen to use either the "Position / Option" DiSEqCTM control flags in a DTH environment, or the "Frequency / Polarisation" flags in a SMATV (shared antenna) environment. Yet another possibility is the option to adapt a Switcher to use the "Uncommitted switches" control flags for larger or non-standard switching systems.



8. Contact Details

For further information, please contact:

Guy Wilkinson	Tel: + 33 1 53 98 37 07					
	E-mail: gwilkins@eutelsat.fr					
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Note: All documents are available on the EUTELSAT web site :

http://www.eutelsat.com/docs/diseqc

If you are not already receiving regular DiSEqCTM mailings, please remember to complete the registration form named "Technical Information Service" on the web site.



Appendix A. DiSEqC[™] "Slave" PIC Microcontroller: Programming Functional Requirements

TO: Alan Terry, Fax: +44 1293 815 050 PHILIPS Consumer Electronics, Advanced Projects Group, Cross Oak Lane, Redhill, Surrey, RH1 5HA, UNITED KINGDOM. FROM:

Contact Name:

*E-mail address:

Please tick (]) **ONLY** the functions which are actually used by the hardware, and Fax a copy of this form (for each separate product) to the above address. An Object Code file attachment, and pin connections, for a PIC 16C620 (A) -04, will be returned by E-mail. * For verification, please send an E-mail with the end-user address confirming transmission of the Fax to: TERRY@APG.PHILIPS.COM

Hardware Identification (e.g. Model Number):

Family Type (Address): [Tick one box]			On-chip Resets enabled <u>[Not_</u> recomm Bus-powered]:			<u>ot</u> recommended if	
Normal LNB (11h)		"Bus-blocking" Switcher [Usually SMATV] (14h)			"Brownout" detector		
Loop-through LNB (12h)		Normal Switcher (15h)			Power-up Tin	ner (PWRT)	
Type of Switching Output: [Tick one box this side]			ing Outputs: num 6 pins per mode]		Active High	Active Low	Inverse Signal
Single-Polarity Outputs [Then mark one box in up to 5 rows on the Right-Hand Side]		High L switch 1	O. Frequency [or Uncor]	mmitted			Low L.O. Frequency
Complementary Outputs [Then mark both boxes in up to 3 rows on the Right Hand Side]		Horizo switch 2	ntal Polarisation [or Unco ?]	ommitted			Vertical Polarisation
Decoded (1 of 4) Outputs [Then mark one box in each of 2 rows on		Satelli	te B (or D) [or Uncommit	ted switch	3]		Satellite A (or C)
the Right Hand Side with a 'D'. You may also tick up to 2 other boxes, if appropriate]		"Optio switch 4	n" Switch (Sat. C/D) [or l !]	Jncommitte	ed 🔲		Satellites A / B
		"Stand	by" (Power-Off)				Power On

Function of Pin 2 (Test Out <u>or</u> Mode In): [<i>Tick one box this side</i>]	"Swap" function (Tone Selects Hi/Lo <u>or</u> SB/SA)	
(13/18V) Comparator Output (Test) [Right Hand Side Not Applicable]	Position or "Option" Switch outputs	
Mode Selection Input [Tick one box on the Right Hand Side]	Position/Option or Frequency/Polarisation	
	Committed or Uncommitted outputs	

Please indicate any other relevant details / requests on this form, or on another sheet if necessary: