



SANYO Semiconductors

DATA SHEET

LV23002M — Bi-CMOS IC

For Radio Cassette and Mini Component System

1-chip Tuner IC Incorporating PLL

Overview

The LV23002M is a one-chip tuner IC incorporating PLL for radio cassette and mini component system.

Features

- AM
- FM-FE
- FM-IF
- MPX
- PLL

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	V _{CC}	7.0	V
	V _{DD} max	V _{DD}	5.0	V
Maximum input voltage	V _{IN1} max	CE, DI, CL	5.0	V
	V _{IN2} max	XIN	V _{DD} +0.3	V
Maximum output voltage	V _{O1} max	DO	6.0	V
	V _{O2} max	XOUT, PD	V _{DD} +0.3	V
	V _{O3} max	BO1, BO2, AOUT	12.0	V
Allowable power dissipation	Pd max	Ta≤70°C Mounted on a glass epoxy board. Board size : 114.3 mm×76.1mm = 1.6mm	400	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note : This product should be handled with care because the resistance of one pin against electrostatic discharge damage is low.

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Operating Condition at $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
	V_{DD}		3.0	V
Operating supply voltage range	$V_{CC\text{ op}}$		4.0 to 6.0	V
	$V_{DD\text{ op}}$		2.5 to 3.6	V

Note : Use the product with the supply voltage applied to V_{CC} and V_{DD} .

PLL block Allowable Operating Range at $T_a = -20$ to $+70^{\circ}\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.5		3.6	V
Input high level voltage	V_{IH}	CE, CL, DI	$0.7V_{DD}$		5.0	V
Input low level voltage	V_{IL}	CE, CL, DI	0		$0.3V_{DD}$	V
Output voltage	V_{O1}	DO	0		6.0	V
	V_{O2}	BO1, BO2, AO1, AO2	0		10	V
Operating frequency	f_{IN1}	XIN ; V_{IN1}		75		kHz
	f_{IN2}	FMIN ; V_{IN2}	10		160	MHz
	f_{IN3}	AMIN (SNS = 1) ; V_{IN3}	2		40	MHz
	f_{IN4}	AMIN (SNS = 0) ; V_{IN4}	0.5		10	MHz

Note : Due attention must be paid on leak because the XIN pin has an extremely high input impedance.

Operating Characteristics at $T_a = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$, $V_{DD} = 3.0\text{V}$, See the specified circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FM-FE characteristics] : fc = 98MHz, fm = 1kHz, 22.5kHzdev.						
3dB sensitivity	3dB LS	60dBμV EMF, 30%mod output reference, -3dB input		3		dBμV EMF
Actual sensitivity	QS	S/N = Input at S/N = 30dB		10		dBμV EMF
[FM-IF monaural characteristics] : fc = 10.7MHz, fm = 1kHz, 75kHzdev.						
Demodulation output	V _O	100dBμV, 12pin output	270	330	400	mVrms
Channel balance	CB	100dBμV, 13pin output /12pin output	-1.5	0	+1.5	dB
Signal-to-noise ratio	S/N	100dBμV, 12pin output	68	75		dB
Total harmonic distortion (Monaural)	THD	100dBμV, 12pin output		0.3	1.5	%
3dB sensitivity	3dB LS	V _O reference, Input level at which V _O reference is -3dB.		38	44	dBμV
IF count sensitivity	IF-C3	SDC0 = 1, SDC1 = 0,18pin(DO) output	47	52	58	dBμV
Mute attenuation	Mute-Att	100dBμV, 12pin output		68		dB
[FM-IF stereo characteristics] : fc = 10.7MHz, fm = 1kHz, L+R = 90%, Pilot = 10%, V _{IN} = 100dBμV						
Separation	SEP	L-mod, 12pin output /13pin output	28	40		dB
Total harmonic distortion (Main)	THD	Main-mod, 12pin output		0.5	1.5	%

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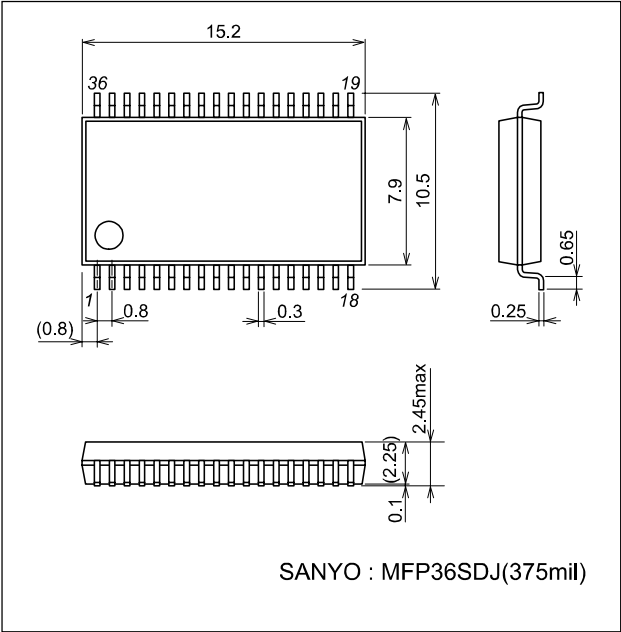
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[AM characteristics] : fc = 1000kHz, fm = 1kHz, 30%mod						
Detection output 1	V _{O1}	23dBμV, 12pin output	25	40	80	mVrms
Detection output 2	V _{O2}	80dBμV, 12pin output	80	110	145	mVrms
Signal-to-noise ratio 1	S/N1	23dBμV, 12pin output	15	20		dB
Signal-to-noise ratio 2	S/N2	80dBμV, 12pin output	47	54		dB
Total harmonic distortion	THD	80dBμV, 12pin output		1.2	3.0	%
IF count sensitivity	IF-C	18pin (DO) output	22	28	33	dBμV
Low-range attenuation	LOW-CUT	V _{O2} reference, Pin 12 output at fm = 100Hz	5	8	11	dB
[Current dissipation]						
Current dissipation	I _{CCFM}	No input in FM mode	20	30	40	mA
	I _{CCAM}	No input in AM mode	10	20	30	
	I _{DD}	fr = 83MHz, X'tal = 75kHz, No input to tuner	1	2	5	
[PLL characteristics]						
Internal return resistance	Rf	XIN		8		MΩ
Built-in output resistance	Rd	XOUT		250		kΩ
Hysteresis width	V _{HIS}	CE, CL, DI		0.1V _{DD}		V
Output high level voltage	V _{OH}	PD ; I _O = -1mA	V _{DD} -1.0			V
Output low level voltage	V _{OL1}	PD ; I _O = 1mA			1.0	V
	V _{OL2}	BO1, BO2 ; I _O = 1mA			0.25	V
		BO1, BO2 ; I _O = 5mA			1.25	V
	V _{OL3}	DO ; I _O = 1mA			0.25	V
	V _{OL4}	AOUT ; I _O = 1mA, AIN = 2.0V			0.5	V
Input high level current	I _{IH1}	CE, CL, DI ; V _I = 6.0V			5.0	μA
	I _{IH2}	XIN ; V _I = V _{DD}	0.16		0.9	μA
	I _{IH3}	AIN ; V _I = 6.0V			200	nA
Input low level current	I _{IL1}	CE, CL, DI ; V _I = 0V			5.0	μA
	I _{IL2}	XIN ; V _I = 0V	0.16		0.9	μA
	I _{IL3}	AIN ; V _I = 0V			200	nA
Output off-leak current	I _{OFF1}	BO1, AOUT, BO2 ; V _O = 10V			5.0	μA
	I _{OFF2}	DO ; V _O = 6.0V			5.0	μA
"H" level 3-state off-leak current	I _{OFFH}	PD ; V _O = 6.0V		0.01	200	nA
"L" level 3-state off-leak current	I _{OFFL}	PD ; V _O = 0V		0.01	200	nA

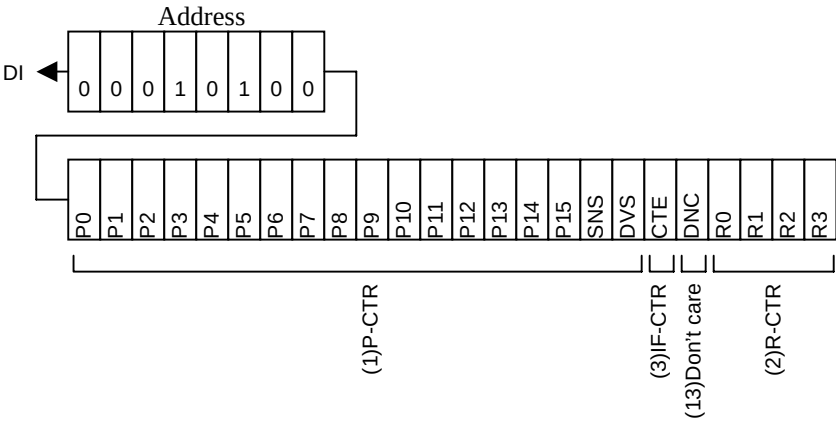
Package Dimensions

unit : mm
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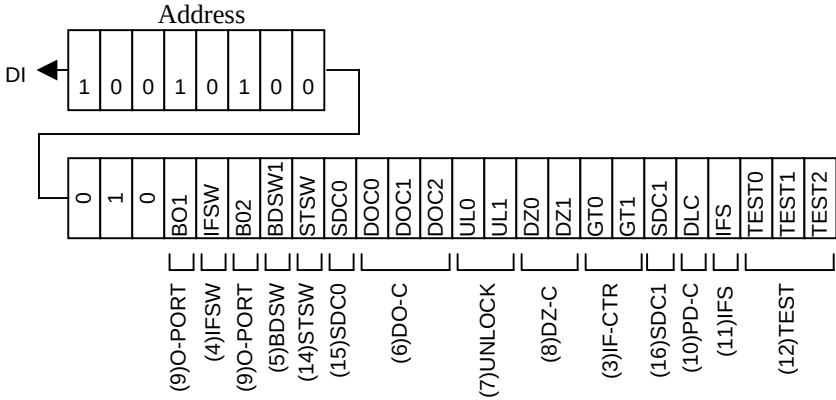


Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode

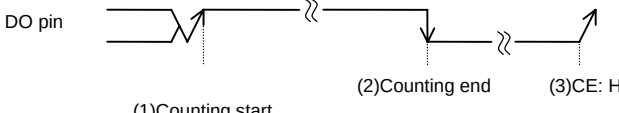


Description of DI control Data

No.	Control block data	Description	Related data																																																																																					
(1)	Programmable divider data P0 to P15 DVS, SNS	- Data to set the dividing number of programmable divider Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (*: don't care) <table><tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Set dividing number(N)</th><th>Actual dividing number</th></tr><tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr><tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr><tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr></table> * P0 to P3 invalid when LSB:P4 - To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (*: don't care) <table><tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr><tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr><tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr><tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr></table>	DVS	SNS	LSB	Set dividing number(N)	Actual dividing number	1	*	P0	272 to 65535	Twice the set value	0	1	P0	272 to 65535	Set value	0	0	P4	4 to 4095	Set value	DVS	SNS	Input	Operation frequency range	1	*	FMIN	10 to 160MHz	0	1	AMIN	2 to 40MHz	0	0	AMIN	0.5 to 10MHz																																																		
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(2)	Reference divider data R0 to R3	- Reference frequency (fref) selection data <table><tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr></table> * PLL INHIBIT - The programmable divider and IF counter stop, with FMIN, AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.	R3	R2	R1	R0	Reference frequency	0	0	0	0	25kHz	0	0	0	1	25kHz	0	0	1	0	25kHz	0	0	1	1	25kHz	0	1	0	0	12.5kHz	0	1	0	1	6.25kHz	0	1	1	0	3.125kHz	0	1	1	1	3.125kHz	1	0	0	0	5kHz	1	0	0	1	5kHz	1	0	1	0	5kHz	1	0	1	1	1kHz	1	1	0	0	3kHz	1	1	0	1	15kHz	1	1	1	0	PLL INHIBIT+X'tal OSC STOP	1	1	1	1	PLL INHIBIT	
R3	R2	R1	R0	Reference frequency																																																																																				
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1	1	1	1	PLL INHIBIT																																																																																				
(3)	IF counter control data CTE GT0, GT1	- IF counter counting start data CTE = 1: Counting start = 0: Counting reset - Determines the counting time of universal counter <table><tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr><tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr><tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr><tr><td>1</td><td>0</td><td>16</td><td>3 to 4</td></tr><tr><td>1</td><td>1</td><td>32</td><td>3 to 4</td></tr></table>	GT1	GT0	Counting time	Wait time	0	0	4ms	3 to 4ms	0	1	8	3 to 4	1	0	16	3 to 4	1	1	32	3 to 4	IFS																																																																	
GT1	GT0	Counting time	Wait time																																																																																					
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1	1	32	3 to 4																																																																																					

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No.	Control block data	Description	Related data																																				
(4)	MUTE control data IFSW	• Data to determine the output of output port IFSW, controlling the MUTE function. "Data" = 0: at receiving 1: MUTE																																					
(5)	FM/AM BAND selection control data BDSW	• Data to determine the output of output port BDSW, controlling selection of BAND. "Data" = 0: AM 1: FM																																					
(6)	DO pin control data DOC0 DOC1 DOC2	• Data to control DO pin output <table border="1"><thead><tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr><tr><td>0</td><td>1</td><td>0</td><td>end-UC (See the item with asterisk below)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Low when SDON</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Low when stereo</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr></tbody></table> • The open condition is selected at power ON/reset. * IF counter counting end check  (1) Counting start (2) Counting end (3) CE: HI (1) With end-UC set and IF counter starting (CTE=0→1), DO pin opens automatically. (2) At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made. (3) DO pin opens when serial data is entered/output (CE pin: Hi) Note: DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE: Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).	DOC2	DOC1	DOC0	DO pin condition	0	0	0	Open	0	0	1	Low when unlock is detected.	0	1	0	end-UC (See the item with asterisk below)	0	1	1	Open	1	0	0	Open	1	0	1	Low when SDON	1	1	0	Low when stereo	1	1	1	Open	UL0, UL1 CTE
DOC2	DOC1	DOC0	DO pin condition																																				
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1	1	0	Low when stereo																																				
1	1	1	Open																																				
(7)	Unlock detection data UL0, UL1	• Phase error (ϕE) detection width selection data to judge if PLL is locked. Phase error exceeding the detection width is judged that PLL is locked (*:don't care) <table border="1"><thead><tr><th>UL1</th><th>UL0</th><th>ϕE Detection width</th><th>Detection output</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Direct output of ϕE</td></tr><tr><td>1</td><td>*</td><td>$\pm 6.67\mu$</td><td>ϕE extended by 1 to 2ms</td></tr></tbody></table> * DO pin is LOW. Serial data output: UL = 0.	UL1	UL0	ϕE Detection width	Detection output	0	0	Stop	Open	0	1	0	Direct output of ϕE	1	*	$\pm 6.67\mu$	ϕE extended by 1 to 2ms	DOC0 DOC1 DOC2																				
UL1	UL0	ϕE Detection width	Detection output																																				
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1	*	$\pm 6.67\mu$	ϕE extended by 1 to 2ms																																				
(8)	Phase comparator control data DZ0, DZ1	• Data to control the dead zone of phase comparator <table border="1"><thead><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></tbody></table> Dead zone width: DZA<DZB<DZC<DZD	DZ1	DZ0	Dead zone mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD																						
DZ1	DZ0	Dead zone mode																																					
0	0	DZA																																					
0	1	DZB																																					
1	0	DZC																																					
1	1	DZD																																					
(9)	Output port data $\overline{BO1}$, $\overline{BO2}$	• Data to determine the output of output ports $\overline{BO1}$ and $\overline{BO2}$ "Data" = 0: OPEN 1: Low																																					

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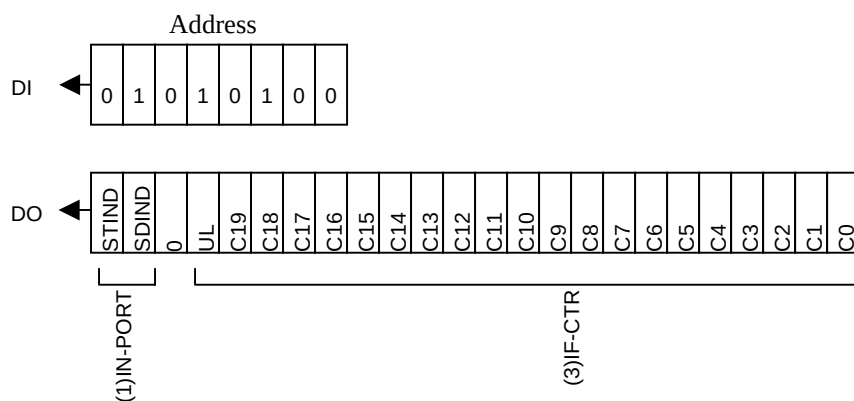
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No.	Control block data	Description	Related data						
(10)	Charge pump control data DLC	Data to enforce control of charge pump output <table><tr><td>DLC</td><td>Charge pump output</td></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Forced to LOW</td></tr></table> In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V_{CC}. (Dead lock clear circuit)	DLC	Charge pump output	0	Normal	1	Forced to LOW	
DLC	Charge pump output								
0	Normal								
1	Forced to LOW								
(11)	IFS	Normally, set Data = 1. Setting Data = 0 causes the input sensitivity worsening mode and the sensitivity decreases by about 10 to 30mVrms.							
(12)	LSI test data TEST0 to 2	LSI test data <table><tr><td>TEST0</td><td rowspan="3">All to be set to "0"</td></tr><tr><td>TEST1</td></tr><tr><td>TEST2</td></tr></table> All set to zero at power ON/reset	TEST0	All to be set to "0"	TEST1	TEST2			
TEST0	All to be set to "0"								
TEST1									
TEST2									
(13)	DNC	Set data = 0.							
(14)	Forced monaural control data STSW	Data to determine the output of output port STSW, controlling the forced stereo functions. "Data" = 0: MONO 1: STEREO							
(15) (16)	SD sensitivity control data SDC0 SDC1	Data to determine the output of output ports SDC0 and SDC1, controlling the SD sensitivity "Data" = SDC0: 0, SDC1: 0 → SD sensitivity = 42dBμV (typ) SDC0: 0, SDC1: 1 → SD sensitivity = 45dBμV (typ) SDC0: 1, SDC1: 0 → SD sensitivity = 51dBμV (typ) SDC0: 1, SDC1: 1 → SD sensitivity = 56dBμV (typ)							

DO control data (serial data output) composition

(1) OUT mode



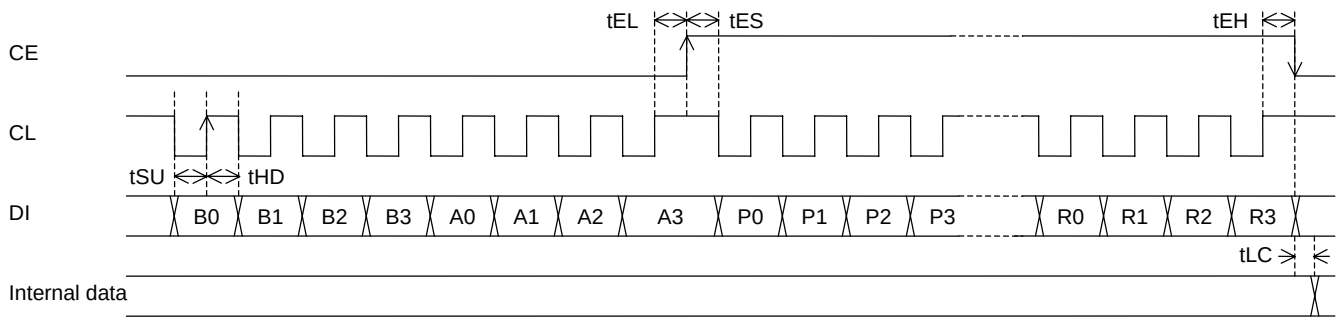
Description of the DO output data

No.	Control block data	Description	Related data
(1)	Stereo and SD indicators control data STIND, SDIND	Data latching stereo and SD indicator conditions. Latching made in the data output (OUT) mode. STIND ← Stereo indicator condition 0: ST ON, 1: ST OFF SDIND ← SD indicator condition 0: SD ON, 1: SD OFF	
(2)	PLL unlock data UL	Data latching the content of unlock detection circuit UL ← 0: At unlock 1: At lock or detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	Data latching the content of IF counter (20-bit binary counter) C19 ← MSB of binary counter C0 ← LSB of binary counter	CTE GT0 GT1

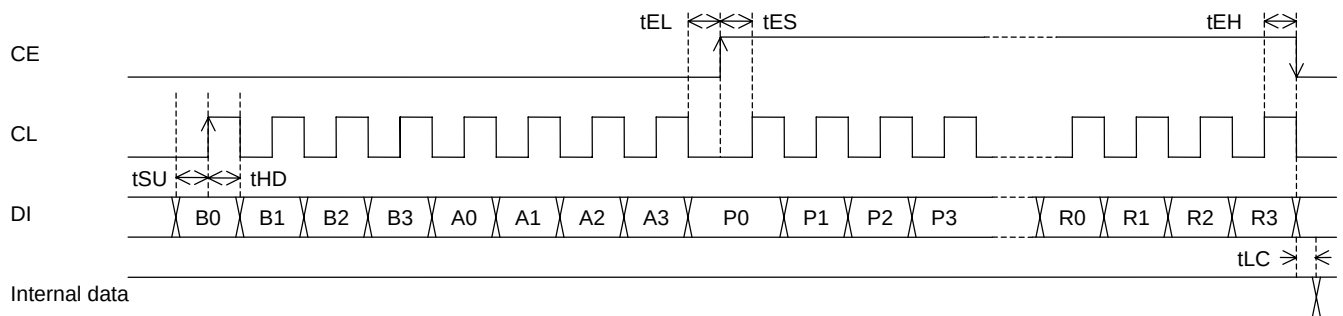
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Serial data input (IN1/IN2) $t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$ $t_{LC} < 0.75\mu s$

(1) CL: Normally HI

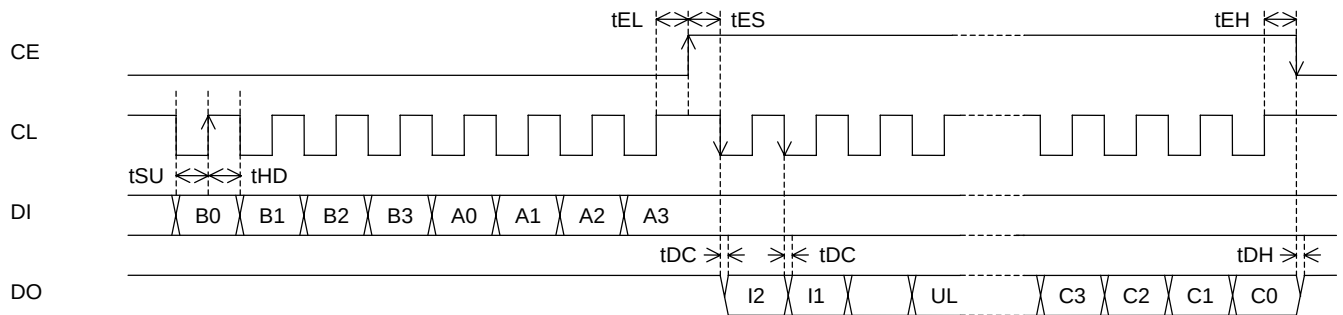


(2) CL: Normally LOW

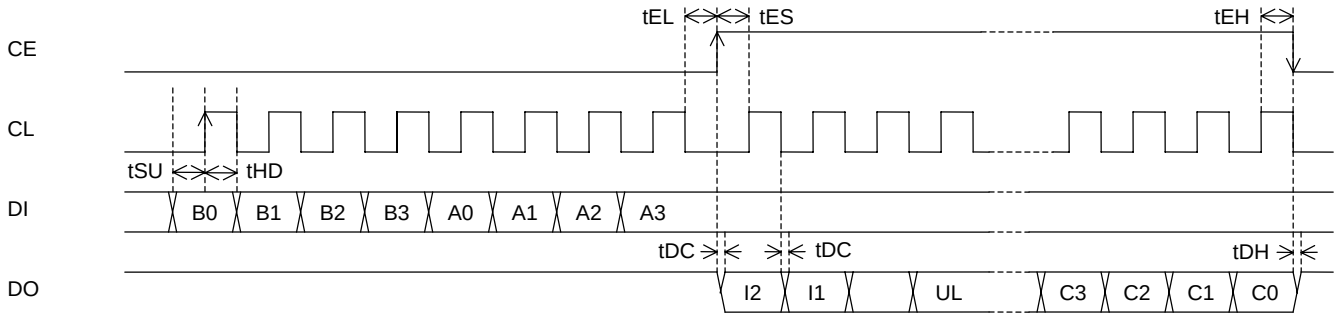


Serial data output (OUT) $t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$ $t_{DC}, t_{DH} < 0.35\mu s$

(1) CL: Normally Hi

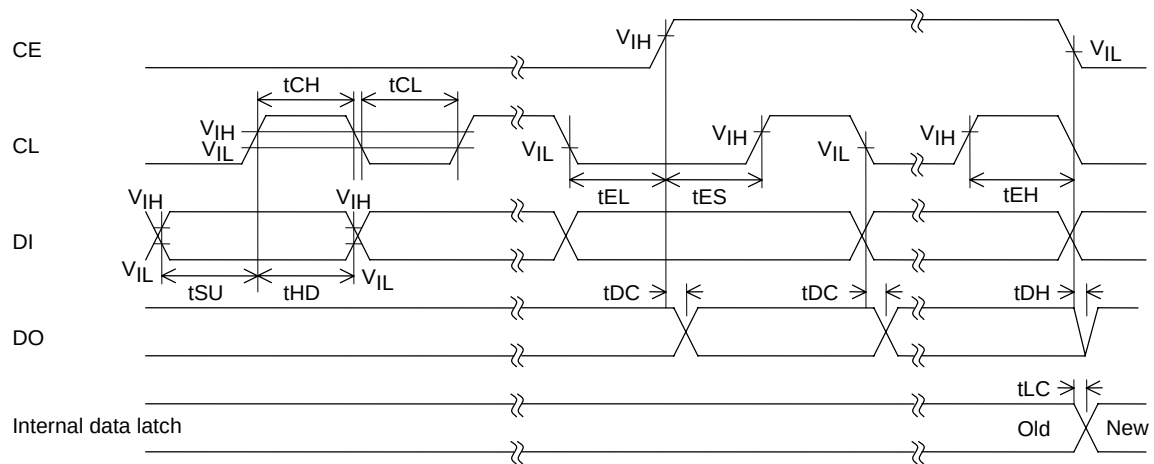


(2) CL: Normally low

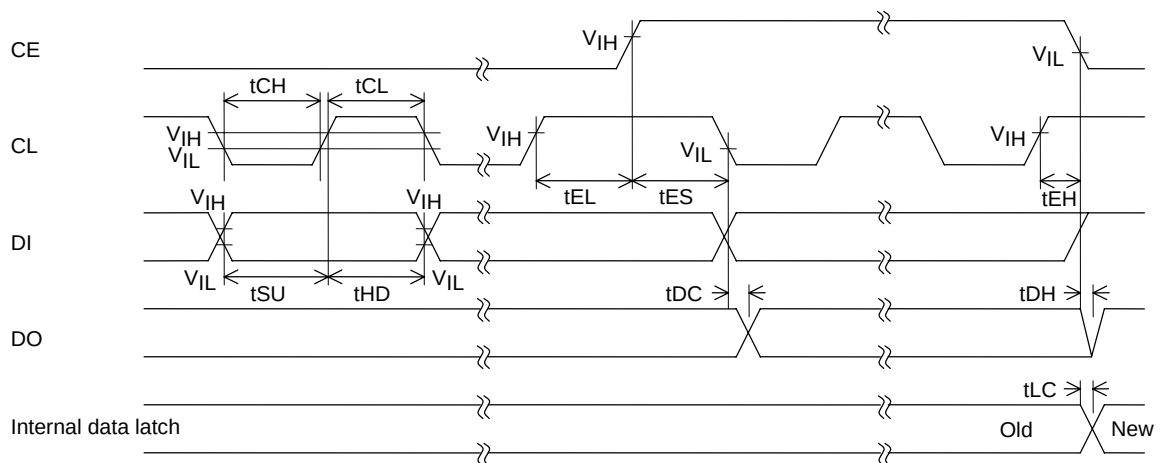


(Note) DO pin is an Nch open drain pin, so that the data varying time (tDC and tDH) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



<< When CL stops at the "L" level >>

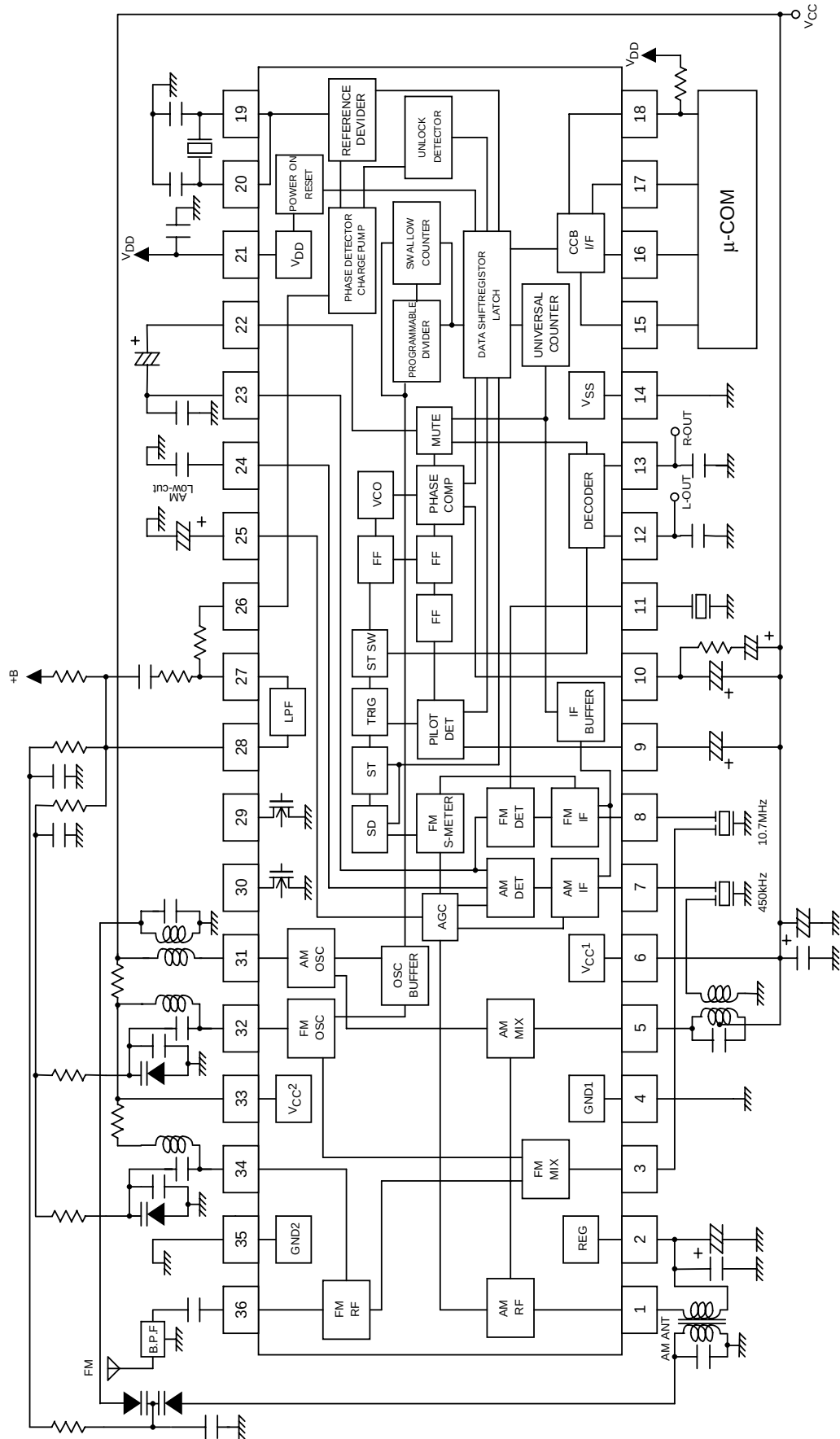


<< When CL stops at the "H" level >>

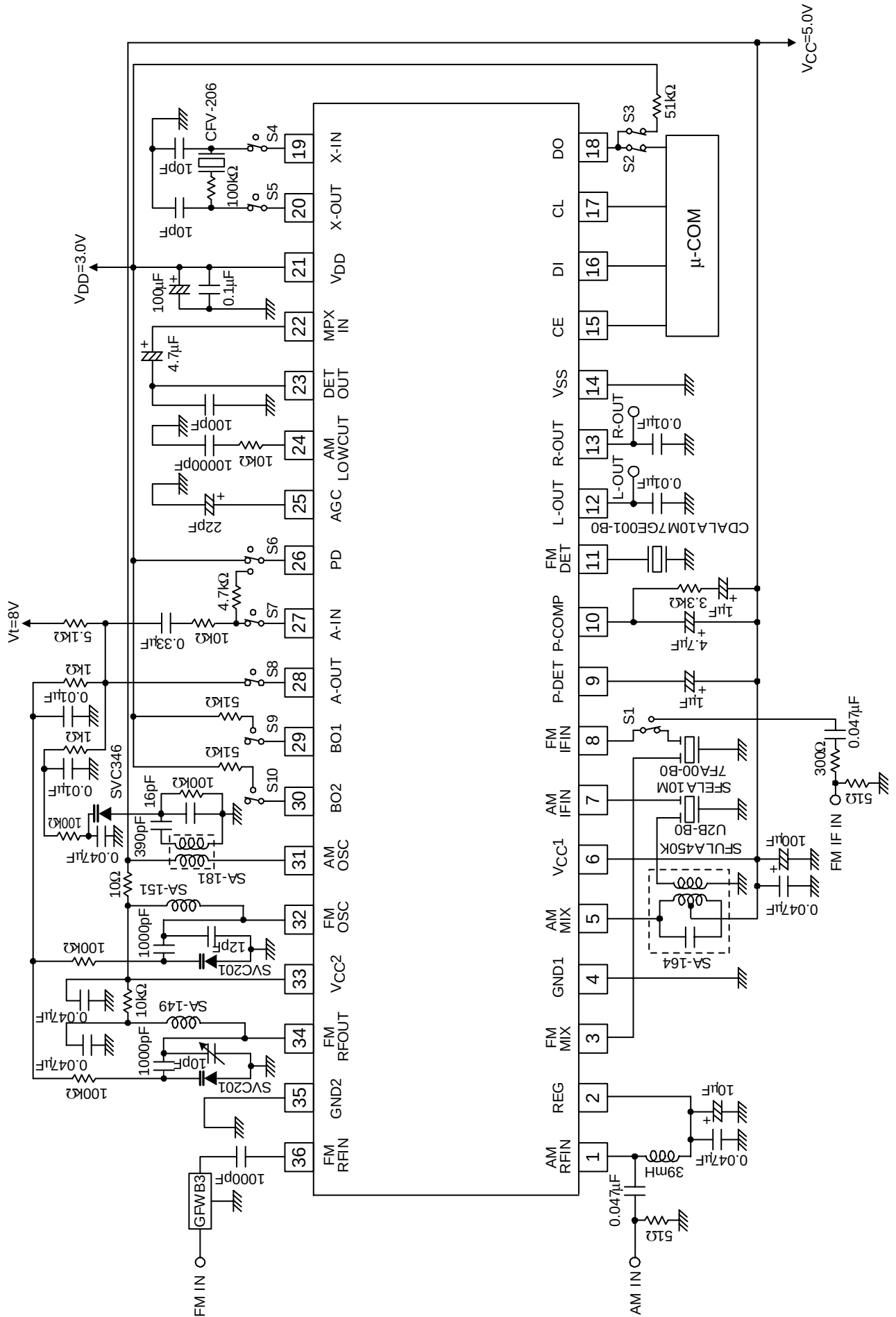
LV23002M

Parameter	Symbol	Pin	Conditions	min	typ	max	unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	tEH	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					

Block Diagram



Test Circuit Diagram



Coil specifications (bottom view)

• FM BPF : GFWB3 (Soshin) 76MHz to 108MHz	
• FM RF : SA-149 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 4.5T: US band	
• FM OSC : SA-151 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 3.5T: US band	
• FM IF filter: SFELA10M7FA00-B0 (Murata)	
• FM Ceramic-discriminator: CDALA10M7GE001-B0 (Murata)	
• AM OSC: SA-181 (Sumida)	• AM MIX: SA-164 (Sumida)
• AM IF filter: SFULA450KU2B-B0 (Murata)	
• MW Bar-antenna: C8E-A0105 (Toko)	

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