# An Improved $LLC$ Resonant Inverter for Induction-Heating Applications With Asymmetrical Control

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***Abstract*—This paper proposes a modified $LLC$ resonant load configuration of a full-bridge inverter for induction-heating applications. The $LLC$ load configuration is a combination of a series inductor, a matching transformer, and an inductor and a capacitor connected in parallel. The output power is controlled using the asymmetrical voltage-cancellation technique. With the use of a phase-locked loop control, the operating frequency is automatically adjusted to maintain a small constant lagging phase angle under load-parameter variation during the heating process. The proposed configuration has the benefit of smaller inductance and inherent short-circuit protection capability in case a short circuit occurs at the induction coil or from transformer saturation. The validity of the proposed method is verified through computer simulation and hardware experiment at an operating frequency range of 108.7–110.6 kHz.**

***Index Terms*—Asymmetrical control, induction heating, zero-voltage switching (ZVS).**

## I. Introduction

INDUCTION heating is a well-known technique to produce very high temperature for applications like steel melting, brazing, and surface hardening. In each application, an appropriate frequency must be used depending on the workpiece geometry and skin-depth requirements [1], [2]. In general, the induction-heating technique requires high-frequency current supply that is capable of inducing high-frequency eddy current in the workpiece that results in the heating effect [1]. A large number of topologies have been developed in this area. Current-fed and voltage-fed inverters are among the most commonly used types [2]. Recent developments in switching schemes and control methods have made the voltage-source resonant inverters to be widely used in applications that require output-power control capability. For example, in pulse-frequency modulation (PFM), the output power can be controlled by varying the switching frequency while the inverter operates under zero-voltage switching (ZVS) scheme [3]. The pulse-density modulation method regulates the output power by varying the period in which the inverter supplies high-frequency current to the induction coil [4], [5]. The phase-shift (PS) control technique in [6] and [8] varies the output power by shifting the phase of the switch conduction sequences. The asymmetrical duty-cycle control technique employs an unequal duty-cycle operation of the switches in the converter [9]–[12]. The asymmetrical voltage-cancellation (AVC) is then proposed in [13] and [14] where the authors describe voltage-cancellation for conventional fixed-frequency control strategies. In [15], the AVC is implemented in a full-bridge series-resonant inverter. The series-resonant inverter needs an output transformer for matching the output power to the load. Most induction-heating applications require accuracy in output-power control capability. For example, cooking appliances require accurate power control over a wide range of power for different cooking purposes where a ZVS condition must be met to ensure high efficiency [16]–[23]. By using the mentioned techniques in fixed frequency and the optimum duty cycle for ZVS operation, it is rather difficult to control the output power due to variation of parameters in the resonant load during the heating process. In high-temperature applications, a high current must flow in the surface of the metal for heating effect. The series-resonant inverter may need a transformer for matching the output power and high current in the induction coil. Previous work has shown that an $LLC$ configuration can offer a better performance than the series resonant while providing short-circuit immunity and lower current on the transformer's secondary [24], [25]. Note that the closed-loop PFM method presented in [25] may sacrifice the efficiency due to switching losses at high-frequency operation. However, the $LLC$ resonant load offers better performance with high-quality factor $(Q > 30)$ and only requires a small series inductance in the circuit configuration. This implies that the output transformer can be omitted. The disadvantage of the $LLC$ resonant load is that the output current may no longer be sinusoid in the case of low $Q$ $(Q < 10)$ [26]. The current in the induction coil is unavoidably small and distorted. Therefore, system efficiency is a price to pay.

In this paper, an improved $LLC$ resonant inverter with asymmetrical control technique is proposed. The aim is to control the output power for high-temperature applications including steel melting, brazing, and hardening, where the load parameters and resonant frequency vary substantially throughout the system operation. The operating frequency is controlled using phase-locked loop to track for the resonant frequency. The output power is controlled by adjusting the switch duty cycle.

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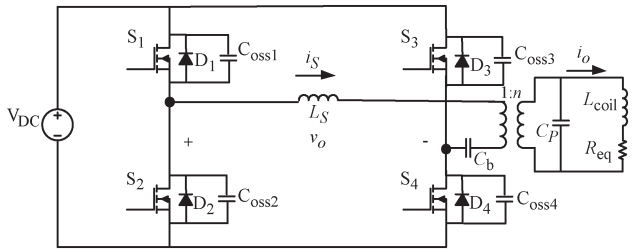


Fig. 1. Full-bridge $LLC$ resonant inverter.

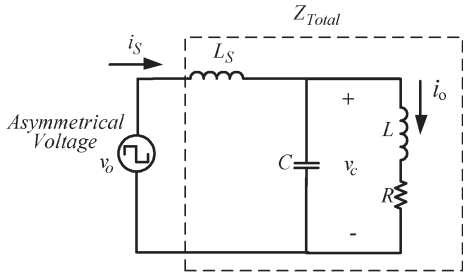


Fig. 2. Equivalent circuit.

The difference between this paper and [15] is that the focus of [15] is on a series-resonant load for cooking applications where the load temperature is low and parameters remain rather constant. In this paper, however, the $LLC$ resonant tank is designed with a matching transformer in between the series inductor and paralleled $LC$ resonant tank. The important advantage of the proposed topology is the short-circuit protection of the transformer and the induction coil. This paper is organized as follows. The circuit configuration and the principle of operation of a full-bridge $LLC$ resonant inverter is described in Section II. Section III presents an analysis of steady-state operation. In Section IV, the asymmetrical control strategy is proposed. Analyses of switching and conduction losses are provided in Section V. A design procedure is given in Section VI. Simulation and experimental results are discussed in Section VII. Section VIII concludes this paper.

## II. Full-Bridge $LLC$ Resonant Inverter

### A. Circuit Description

Fig. 1 shows an $LLC$ resonant inverter configuration for induction-heating applications. The inverter consists of four switches with antiparallel diodes, a resonant capacitor $(C_p)$, a series inductor $(L_s)$, and an induction coil that comprises a series combination of a resistor $(R_{\rm eq})$ and an induction coil inductor $(L_{\rm coil})$ [27], [28]. A dc blocking capacitor $(C_b)$ is inserted in series with the transformer primary. The equivalent circuit of the full-bridge $LLC$ inverter system in Fig. 1 is shown in Fig. 2 where the input voltage can be viewed as an asymmetrical ac voltage supplied to the system. With a negligible value of $C_b$, it is noted that capacitor $C$, inductor $L$, and resistor $R$ represent the equivalent capacitor $C_p$, inductor $L_{\rm coil}$, and resistor $R_{\rm eq}$ referred to the primary side of the transformer, respectively. The stray capacitance of MOSFET switching device $S_1$, $S_2$, $S_3$, and $S_4$ are denoted as $C_{\rm oss1}$, $C_{\rm oss2}$, $C_{\rm oss3}$, and $C_{\rm oss4}$, respectively. The total impedance of the asymmetrical voltage source $(v_o)$ is denoted by $Z_{\rm total}$. The current $i_s$ and $i_o$ are the input and output currents, respectively.

### B. Modes of Operation

As shown in Fig. 3, eight modes of operation exist within one switching cycle when the stray capacitances are taken into account. The corresponding waveforms and circuit topology for each mode of operation are shown in Fig. 3(a) and (b), respectively. The analysis is as follows.

1) Mode 1 $(t_0$–$t_1)$: While switches $S_2$ and $S_3$ are off, at $t = t_0$, switches $S_1$ and $S_4$ receive positive gating signals. The negative input current $(i_s)$ flows through diodes $D_1$ and $D_4$.
2) Mode 2 $(t_1$–$t_2)$: At $t = t_1$, as soon as the antiparallel diodes $D_1$ and $D_4$ are off, switches $S_1$ and $S_4$ conduct, and the ZVS operation is achieved. During this mode, the positive input current $(i_s)$ flows.
3) Mode 2′ $(t_2$–$t_2')$: At $t = t_2$, after switch $S_4$ is off, the current flows in the same direction. The charge in $C_{\rm oss3}$ is gradually decreasing, whereas the charge in $C_{\rm oss4}$ is slowly increasing. At this stage, the output voltage changes from $+V_{\rm dc}$ to zero.
4) Mode 3 $(t_2'$–$t_3)$: At $t = t_2'$, while switch $S_1$ still conducts, switch $S_4$ is turned off, and the antiparallel diode $D_3$ conducts. After the switch dead time, switch $S_3$ receives a positive gating signal.
5) Mode 3′ $(t_3$–$t_3')$: During this period, all switches are off simultaneously. A part of positive current $i_s$ flows through the antiparallel diode $D_3$ and $C_{\rm oss2}$. At the same time, the charge in capacitor $C_{\rm oss2}$ decreases, whereas the charge in capacitor $C_{\rm oss1}$ increases. In this operation, the output voltage $v_o$ changes from zero to $-V_{\rm dc}$.
6) Mode 4 $(t_3'$–$t_4)$: At $t = t_3'$, switch $S_1$ is already turned off. Similar to that in Mode 1, diode $D_2$ starts conducting positive input current $i_s$ together with diode $D_3$. After the switch dead time, switch $S_2$ receives a positive gating signal. The shifted angle $\alpha$ is from $t_2$ to the moment switch $S_2$ is on.
7) Mode 5 $(t_4$–$t_5)$: At $t = t_4$, when the antiparallel diodes $D_2$ and $D_3$ are off, switches $S_2$ and $S_3$, which already received positive gating signals, conduct, and the ZVS operation is achieved. During this mode, the current $i_s$ becomes negative.
8) Mode 5′ $(t_5$–$t_5')$: At $t = t_5$, after switches $S_2$ and $S_3$ are turned off, the negative current $i_s$ flows through the stray capacitors $C_{\rm oss1}$, $C_{\rm oss2}$, $C_{\rm oss3}$, and $C_{\rm oss4}$. The charges in $C_{\rm oss1}$ and $C_{\rm oss4}$ decrease, while the charges in $C_{\rm oss2}$ and $C_{\rm oss3}$ increase. At this point, the full cycle of operation is accomplished. In this operation, $v_o$ changes from $-V_{\rm dc}$ to $+V_{\rm dc}$. The next operating cycle continues, repeating from Modes 1 to 5′.

In many cases, the stray capacitance may be neglected, and the modes of operation for one switching period are reduced to five modes (i.e., modes $1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5$).

Note that in this paper, it is assumed that the charging time of the stray capacitor $(t_{\rm coss})$ is smaller than the switch's dead time.

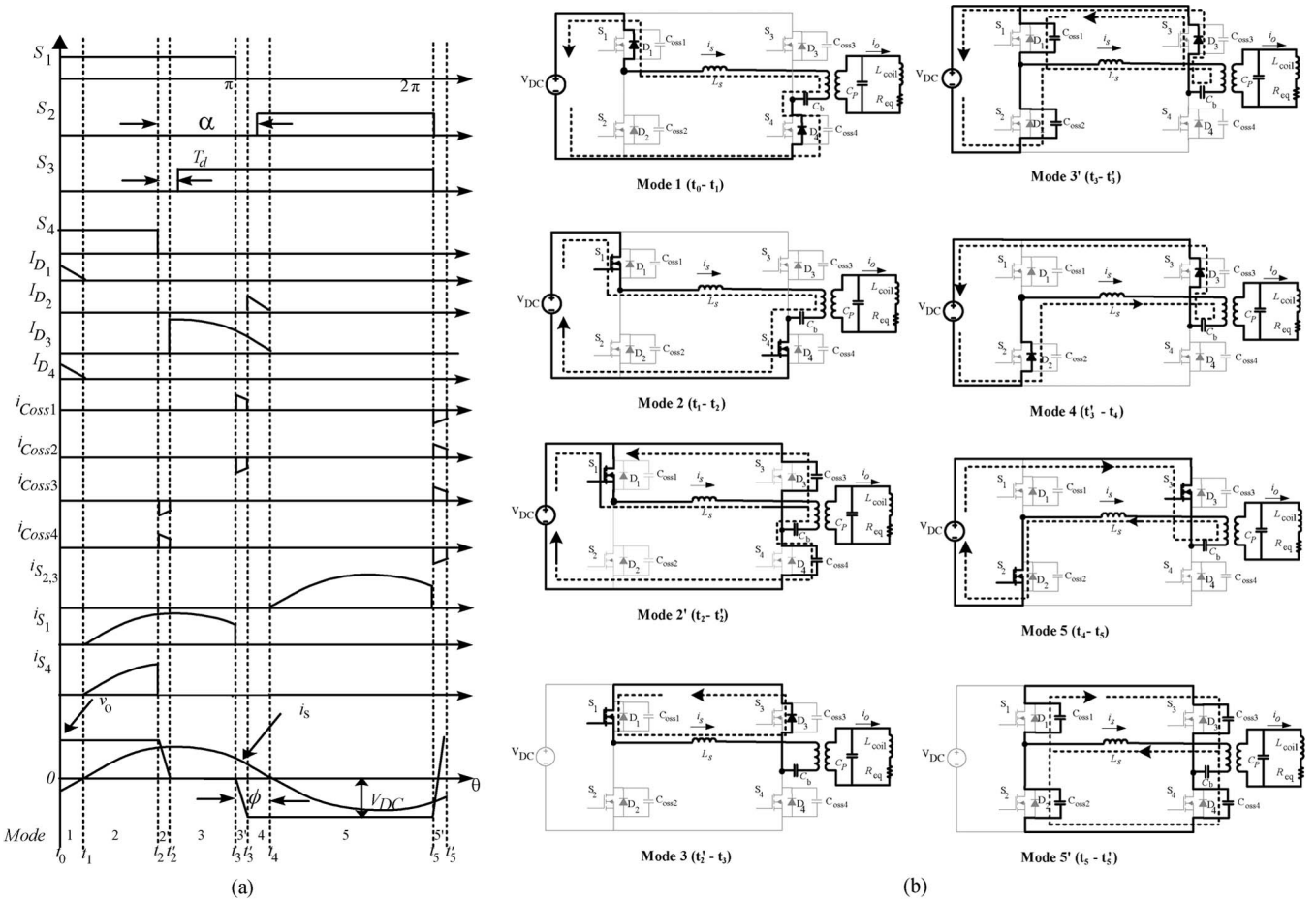


Fig. 3. Inverter operations: (a) Typical waveforms. (b) Modes of operation.

## III. Circuit Analysis

### A. Analysis of the Output Power

The steady-state analysis of the full-bridge $LLC$ inverter is based on the following assumptions.

1) All circuit components are ideal.
2) The dc input voltage $V_{\rm DC}$ is constant.
3) The effects of stray capacitance are neglected.

From Figs. 2 and 3, the relationship between the load voltage (i.e., the capacitor voltage $v_c$) and the inverter output voltage $(v_o)$ is given as

$$\frac{V_c}{V_o} = \frac{R + j\omega L}{(j\omega L_s \times j\omega C)(R + j\omega L) + j\omega L_s + R + j\omega L)} \quad (1)$$

where $L = n^2 L_{\rm coil}$, $R = n^2 R_{\rm eq}$, and $C = C_p/n^2$, given that $n$ is the transformation ratio of the transformer. The inverter is designed to operate such that the switching frequency $(\omega)$ is higher than the resonant frequency $(\omega_0)$ for ZVS operation. The resonant frequency of the system in Fig. 2 is given as

$$\omega_o = \sqrt{\frac{L + L_s}{L \cdot L_s \cdot C}}. \quad (2)$$

Taking only the fundamental component $(V_1)$ of the inverter output voltage $(v_o)$ in Fig. 2 into account, the load voltage is given as

$$V_C = \left( -\frac{L}{L_s} - j\frac{L^2}{RL_s}\sqrt{\frac{L + L_s}{L \cdot L_s \cdot C}} \right) \cdot V_1. \quad (3)$$

The fundamental voltage $V_1$ of the capacitor voltage $v_C$ in (3) can be obtained from the following coefficients of Fourier series of the inverter output voltage $v_o$ [13]:

$$\left.\begin{aligned} \hat{V}_n &= \tfrac{V_m}{\pi}\sqrt{a_n^2 + b_n^2} \\ \phi_{vn} &= \tan^{-1}\tfrac{a_n}{b_n} \\ b_n &= \tfrac{V_m}{n\pi}\left[2 - (-1)^n - \cos n(180 - \alpha)\right] \\ a_n &= \tfrac{V_m}{n\pi}\left[-\sin n(180 - \alpha)\right] \end{aligned}\right\} \quad (4)$$

where $V_m$ is the dc input voltage assuming the same value as $V_{\rm DC}$, $\phi_{vn}$ is the phase of the $n$th harmonic of $v_o$, and $\alpha$ is the shifted angle of the switch $S_4$, as shown in Fig. 3. Using (4), the amplitude of the fundamental voltage $v_1$ can be calculated as

$$\hat{V}_1 = \frac{V_m}{\pi} \times \sqrt{\sin^2(180 - \alpha) + \left(3 - \cos(180 - \alpha)\right)^2} \quad (5)$$

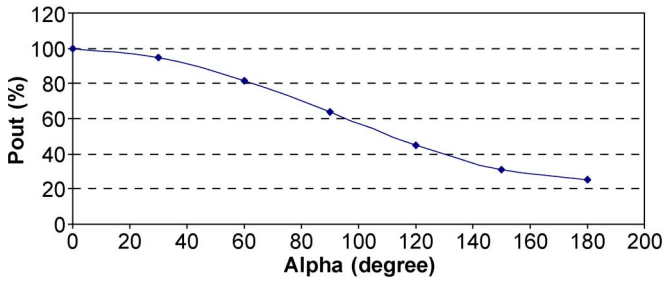


Fig. 4. Output power versus $\alpha$.

and the average output power at the load $(P)$ can be obtained as [24]

$$P = V_1^2 \mathrm{Re}\left\{Z_{\mathrm{total}}(j\omega_0)^{-1}\right\} \tag{6}$$

which is expanded to

$$P = \frac{V_m^2}{2R\pi^2}\left(\sin^2(180-\alpha) + (3-\cos(180-\alpha))^2\right) \times \left(\frac{L}{L_s}\right)^2 \cos(\phi) \tag{7}$$

where $\phi$ is the switching angle. The output power $P$ in (7) depends on the shifted angle $\alpha$. Fig. 4 shows the relationship of the output power and $\alpha$, obtained from (7), with $\cos\phi$ being set to one. It is seen that an increase of $\alpha$ results in reduction of the output power. This means that the output power can be controlled through an adjustment of $\alpha$. The greater the angle $\alpha$, the less power is delivered to the load. The frequency response of the output power $(P_o)$ under different quality factors $(Q)$ is shown in Fig. 5(a) with the angle $\alpha$ set to zero. At higher $Q$ factor, the inverter operates close to the resonant frequency $\omega_0$ (i.e., the normalized frequency $f_s/f_b$ is close to one). Unlike the induction-coil current $(i_o)$ shown in Fig. 5(b), the $Q$ factor has negligible effect on the resonant frequency, i.e., the peak value of $i_o$ occurs at the same frequency regardless of the $Q$ factors. The peak value of $i_o$ is related to the $RLC$ parallel end in Fig. 2, where $L_s$ does not play a roll in the frequency response of $i_o$.

### B. Design of $L_s$

The total impedance $(Z_{\mathrm{total}})$ in Fig. 2 can be expressed as

$$Z_{\mathrm{Total}}(\omega) = \frac{R - \omega^2 C L_s R + j\omega L_s + j\omega L - j\omega^3 L_s L}{-\omega^2 CL + j\omega CR}. \tag{8}$$

At resonant frequency $(\omega_0)$

$$Z_{\mathrm{Total}}(\omega_0) = \frac{\omega_0 L_s^2 R\left(L^2\omega_0 + jR(L_s+L)\right)}{-L\omega_0 - R^2\left(L_s^2 + L_s L + L^2\right)}. \tag{9}$$

The switching angle $\phi$ is given as

$$\phi = \arg\left\{Z_{\mathrm{Total}}(j\omega_0)\right\} = \arctan\left(\frac{R(L_s+L)}{L^2\omega_0}\right) > 0. \tag{10}$$

This results in

$$\frac{L_s}{L} = \frac{L\omega_0}{R}\tan\phi - 1. \tag{11}$$

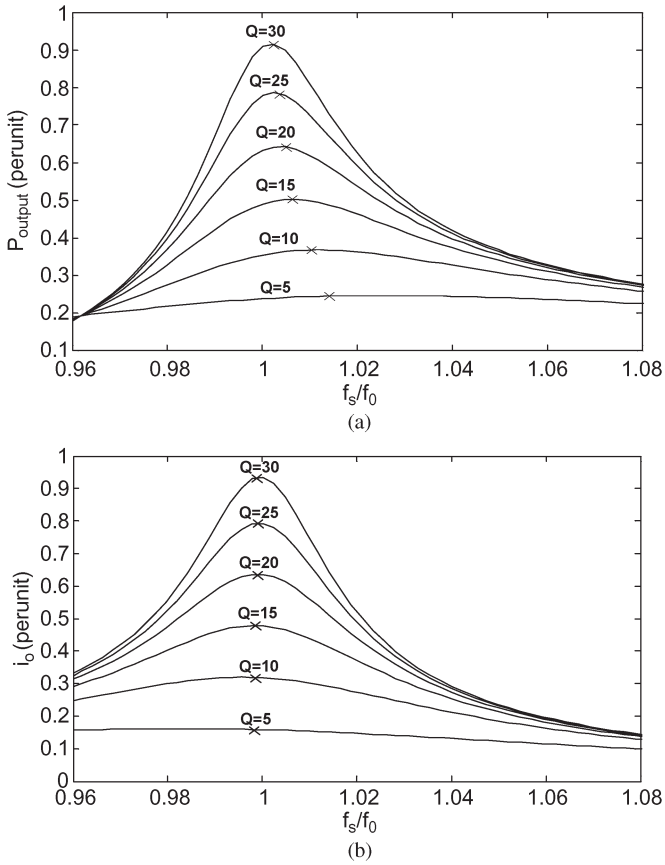


Fig. 5. Frequency response: (a) Output power $(P_o)$ at various $Q$ factors and (b) output current $(i_o)$ at various $Q$ factors.

The current gain is found as

$$\frac{I_o}{I_s} = \frac{1}{j\omega C Z_P(j\omega)} \tag{12}$$

where $Z_P(j\omega) = (1/j\omega C)//(j\omega L + R)$. The current gain at resonant frequency $(\omega_0)$ is given as

$$\left|\frac{I_o}{I_s}(\omega_0)\right| = \frac{L_s}{L}\frac{1}{\sqrt{\frac{CL_S R^2(L+L_s)}{L^3}+1}}. \tag{13}$$

Therefore, the coil current at resonance can be expressed as

$$I_o = \frac{L_s}{L} I_{\mathrm{s}} \cos\phi. \tag{14}$$

At the frequency above resonance, there is always a positive power angle $\phi$ (i.e., lagging current operation). A high-efficiency inverter with $LLC$ topology can be achieved by introducing a small positive switching angle and high current gain in the design. From (11) and (14), it is deduced that a suitable load would be applications with high quality factor $(Q)$ such as brazing, surface hardening, and tube welding. For applications with low $Q$ (less than ten), it is very difficult to obtain both high current gain and resonant operations at the same time. One of the possible solutions would be to increase the power angle $\phi$. This means that the operating frequency must be adjusted further away from the resonant frequency, which results in the operation of the inverter under low efficiency.

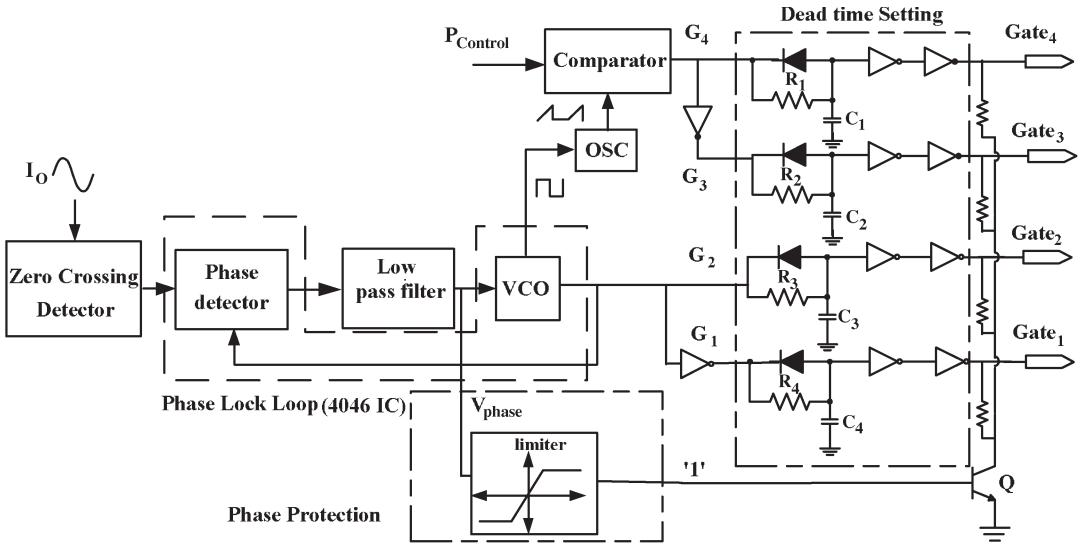


Fig. 6. Proposed control block diagram of the $LLC$ resonant inverter.

This is where the high-frequency transformer is introduced to match the output current and power. In addition to improving the system efficiency, the important advantage of the inclusion of the transformer is the inherent current-limiting capability in case of transformer saturation. The inductor $L_s$ carries low current because it is located on the primary side. Therefore, it is easier and cheaper to construct such an inductor.

## IV. Proposed Control Strategy

The workpiece geometry, conductivity, and permeability of different metals have various effects on the inductance of the heating coil. In addition, the coil inductance is also changed when heated. This is due to the fact that beyond the Curie temperature, the relative permeability $(\mu_r)$ of the workpiece decreases when the temperature increases. This results in the reduction of the equivalent inductance of the workpiece which in turn reduces the coil inductance. On the contrary, when the workpiece temperature is lower than the Curie temperature, the relative permeability of the workpiece decreases with temperature. Therefore, the coil inductance exhibits a change in the opposite direction [29].

Considering the fact that the resonant capacitance is fixed, therefore, the resonant frequency is varied throughout the heating process. The phase-locked loop integrated-circuit (IC) device for load-adaptive resonant-frequency tracking is introduced to the resonant inverter to drive the operating frequency to the new resonant frequency.

The proposed control scheme of the full bridge $LLC$ resonant inverter consists of two parts:

1) power control through the alpha angle $(\alpha)$ of the switch $S_4$;
2) frequency control for ZVS operation.

The controller comprises a current sensor, zero-crossing detector, phase detector, and voltage-controlled oscillator, as shown in Fig. 6. The 4046 phase-locked loop IC is used for frequency control at slightly higher than the resonant frequency. In typical voltage-fed inverter, the gate drive signal is in phase with the asymmetrical inverter output voltage $v_o$. Therefore, we can use the gate drive signal instead of the load-voltage pulse for phase detection. The current signal $i_o$ is compared with the voltage signal in order to detect the phase difference. The output signal of the digital phase detector is filtered by an $RC$ low-pass filter to get an average value that is proportional to the phase difference at the load. The generation of asymmetrical gate drive signals for power control is shown in Fig. 7. The $P_{\rm control}$ signal is compared with the ramp signal from the 4046 IC to generate the gate signal $G_4$.

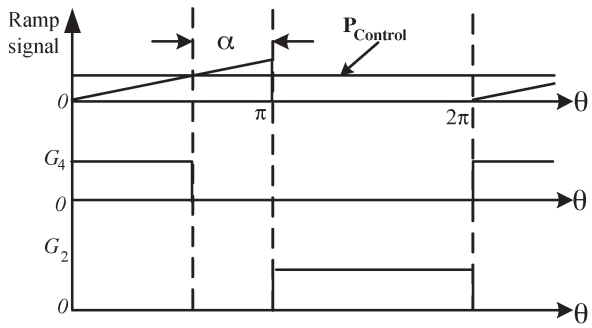


Fig. 7. Waveforms of the asymmetrical gate drive signal.

If the $P_{\rm control}$ signal is greater than the ramp signal, the gate signal $G_4$ is set to high. Otherwise, it is set to low. In this way, $\alpha$ is dependent on the $P_{\rm control}$ signal. The gate signal $G_2$ is always on from $\pi$ to $2\pi$. The $G_1$ and $G_3$ signals are the inverse of $G_2$ and $G_4$ signals, respectively. Note that the ramp signal is generated from the phase detector. Therefore, its frequency is automatically adjusted to track the resonant frequency and turns on as ZVS operation is obtained. The gating signals $G_1$, $G_2$, $G_3$, and $G_4$ are sent into the dead-time circuit where the dead-time setting is adjusted through the pairs $R_1$–$C_1$, $R_2$–$C_2$, $R_3$–$C_3$, and $R_4$–$C_4$. A phase-protection circuit with a limiter is used where the $V_{\rm phase}$ signal, a dc signal proportional to the phase, is put through a limiter [30]. This allows an operation in the desired frequency range for the ZVS mode. If the phase lies in the region that is out of the predetermined limits, an active

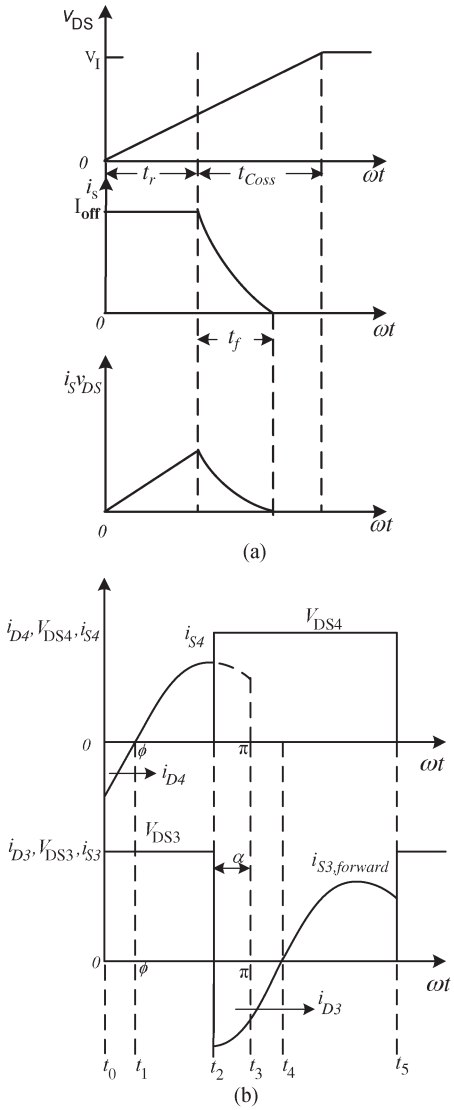


Fig. 8. Theoretical waveforms. (a) Turn-off loss and (b) the conduction loss of switch $S_3$ and switch $S_4$.

signal is sent out to turn the transistor $Q$ on and ground all gate signals $S_1$ to $S_4$. The inverter is turned off.

## V. Switching and Conduction Losses

### A. Switching Loss

To maintain the operation under ZVS conditions, the power angle $\phi$ must be kept greater than both the dead time and charging time of the stray capacitors [31], [32]. This is to allow sufficient time for the diodes to conduct while keeping the voltage across the switch at zero. For the operation at the frequency above resonance, the turn-on switching loss of all switches is zero, but there still is a turn-off switching loss for every switch. It is seen in Fig. 3 during the $t_3$–$t_4$ interval that the switch $S_4$ turns off at a larger current as $\alpha$ becomes larger. This results in a higher switching loss. To consider the switching loss in details, the current and voltage transition at turn off are shown in Fig. 8(a).

The drain-to-source voltage $v_{\rm DS}$ during rise time $(t_r)$ is given as

$$v_{\rm DS} = V_I \left(\frac{\omega t}{\omega t_r}\right) \tag{15}$$

where $V_I$ is the voltage across the switch while the switch is turned off, which is the same as the dc input voltage $(V_{\rm DC})$. The switch current is a small portion of a sinusoid and can be approximated by a constant

$$i_S = I_{\rm OFF} \tag{16}$$

where $I_{\rm OFF}$ is the current through the switch before turning off. The power loss associated with the voltage during rise time $(P_{\rm tr})$ is given as

$$P_{\rm tr} = \frac{1}{2\pi}\int_0^{\omega t_r} i_S v_{\rm DS}\, d(\omega t) = \frac{t_r V_I I_{\rm OFF}}{2T}. \tag{17}$$

During fall time $(t_f)$, the switch current can be approximated by a parabola function as

$$i_S = I_{\rm OFF}\left[1 - \frac{\omega t}{\omega t_f}\right]^2 \tag{18}$$

while the drain-to-source voltage is (15). The power loss associated with $t_f(P_{\rm tf})$ is provided as

$$\begin{aligned} P_{tf} &= \frac{1}{2\pi}\int_{\omega t_r}^{\omega t_f} i_S v_{\rm DS}\, d(\omega t) \\ &= \frac{I_{\rm OFF} V_I (t_f - t_r)(t_f + t_r)\left(t_f^2 + 4t_r t_f + t_r^2\right)}{12T}. \end{aligned} \tag{19}$$

Hence, the turn-off switching loss is combined as

$$\begin{aligned} P_{\rm off} &= P_{tr} + P_{tf} \\ &= f V_I I_{\rm OFF} \\ &\quad \times \left(\frac{t_r}{3} + \frac{(t_f - t_r)(t_f + t_r)\left(t_f^2 + 4t_r t_f + t_r^2\right)}{12}\right). \end{aligned} \tag{20}$$

Therefore, the turn-off loss of the full-bridge $LLC$ resonant inverter with asymmetrical control becomes

$$\begin{aligned} P_{\rm total,off} = f V_I &\left(\frac{t_r}{3} + \frac{(t_f - t_r)(t_f + t_r)\left(t_f^2 + 4t_r t_f + t_r^2\right)}{12}\right) \\ &\times \left(3I_{\rm OFF,S_1,S_2,S_3} + I_{\rm OFF,S_4}\right) \end{aligned} \tag{21}$$

where $I_{\rm OFF,S_1,S_2,S_3}$ and $I_{\rm OFF,S_4}$ assume the forms

$$I_{\rm OFF,S1,S2,S3} = I_{\rm m}\sin(\phi) \tag{22}$$

$$I_{\rm OFF,S_4} = I_{\rm m}\sin(\alpha + \phi). \tag{23}$$

If a snubber capacitor is added to the circuit, the charging time $(t_{\rm Coss})$ will increase, and the peak of the product of

$i_s$ and $v_{\rm ds}$ in Fig. 8(a) will decrease. Thus, the turn-off loss is decreased. The dead time must be increased to maintain approximately zero turn-off loss. Clearly, the snubber capacitor can always be included. However, there is a tradeoff for adding a snubber capacitor because the power angle $\phi$ must cover the switch dead time and the capacitor charging time. Therefore, the increased power angle $\phi$ results in a reduced range of the angle $\alpha$ ($\alpha_{\max} = \phi - 180$), and therefore, the range of power adjustment will be reduced.

### B. Conduction Loss

Since the intervals $t_2$–$t_2'$ and $t_5$–$t_5'$ in Fig. 3(a) representing the charging and discharging periods of the stray capacitors are small compared with the overall conduction times, both intervals are neglected in the following calculation. Taking the switch conduction loss into account, the current and voltage at switches $S_3$ and $S_4$ from $t_0$ to $t_5$ are shown in Fig. 8(b). Switches $S_1$, $S_2$, and $S_3$ carry the same current and conduction loss through the intervals $t_1$–$t_2$ and $t_4$–$t_5$, respectively. Since the inverter current $i_s$ is given as

$$i_s(t) = I_{\rm S,peak}\sin(\omega t - \phi) \tag{24}$$

the current contribution to conduction losses of the switch $S_1$, $S_2$, and $S_3$ can be found as

$$I_{\rm S_{1,2,3},rms} = \frac{I_{\rm s}}{2}\sqrt{1 - \frac{\phi}{\pi} + \frac{\sin\phi\cos\phi}{\pi}}. \tag{25}$$

For the asymmetrical switch $S_4$, the conduction loss results from the current

$$I_{\rm S_4,rms} = \frac{I_{\rm s}}{4\pi}\sqrt{-2(\alpha - \pi + \phi) + \sin\left(2(\alpha + \phi).\right)} \tag{26}$$

The conduction loss of the switch is given as

$$P_{s,\rm loss} = (I_{\rm S,rms})^2 R_{\rm DS,on}. \tag{27}$$

The aforementioned conduction losses can be calculated by substitution of the currents in (25) and (26) into (27). Next, the diode conduction loss is considered. Clearly, diodes $D_1$–$D_4$ and $D_2$–$D_3$ conduct during the $t_0$–$t_1$ and $t_2$–$t_4$ intervals, respectively. In addition, the conduction loss of diode $D_3$ includes the forward conduction during the $t_2$–$t_3$ interval, similar to the current in (25).

Therefore, the current contribution to the conduction loss of diode $D_3$ is given as

$$I_{\rm D_{3,rms}} = \frac{I_s}{4\pi}\left(\sqrt{2\alpha + \sin(2\phi) - \sin\left(2(\alpha + \phi)\right)}\right). \tag{28}$$

For the other diodes, the current contribution to the conduction loss is found as

$$I_{D_{1,2,4,\rm rms}} = \frac{I_s}{2}\sqrt{\frac{\phi}{\pi} - \frac{\sin\phi\cos\phi}{2\pi}}. \tag{29}$$

The diode conduction loss is

$$P_{D,\rm loss} = I_{\rm Diode,rms} \times V_{\rm FWD,diode}. \tag{30}$$

TABLE I
DESIGN SPECIFICATION AND CIRCUIT PARAMETERS

| Parameter | | Value |
|---|---|---|
| $v_{AC}$ | Input Voltage | 150 $V_{\rm rms}$ |
| $f_o$ | Resonant Frequency | 108.2 kHz |
| $f_s$ | Switching Frequency | 108.7 -110.6 kHz |
| $C_{\rm P}$ | Parallel resonant capacitor | 2.35 μF |
| $L_{\rm s,total}$ | Series inductor + Primary Leakage inductance of transformer | 56 μH+79 μH ($L_s$+$L_{\rm lkp}$) |
| $L_{Coil}$ | Induction coil inductor (From room temperature to 625°C) | 1.11-0.95μH |
| $R_{\rm eq}$ | Equivalent resistor (with workpiece) (From room temperature to 625°C) | 100 – 110 $m\Omega$ |
| $n=n_1/n_2$ | Transformation ratio | 5 |
| $S_1$, $S_2$, $S_3$, $S_4$ | Switches | IRFP460 |
| $C_b$ | DC blocking capacitor | 3.3 μF |

Similarly, the conduction loss of each diode is computed by substituting (28) and (29) into (30).

## VI. DESIGN PROCEDURE

In this section, a design example of the major components of the system in Fig. 1 is discussed.

### A. Resonant Load

The targeted application is a 450-W induction-melting system for a 30-g aluminum workpiece. The desired frequency is at 110 kHz. The readily available induction-coil inductance ($L_{\rm coil}$) and equivalent resistance ($R_{\rm eq}$) are 1.11 $\mu$H and 100 m$\Omega$, respectively. The power angle $\phi$ is set to 36°. Using (11), the maximum series inductance ($L_{s,\max}$) is obtained from (11) as

$$L_{s,\max} = \frac{L^2\omega_0}{R}\tan\phi - L = 5.1\ \mu\text{H}. \tag{31}$$

Next, the resonant capacitor is obtained from (2) as

$$C = \frac{L + L_{s,\max}}{L \cdot L_s \cdot \omega_o^2} = 2.29\ \mu\text{F}. \tag{32}$$

Five 30-kvar 400-V 100-$A_{\rm rms}$ 0.47-$\mu$F capacitors with a total capacitance of 2.35 $\mu$F are used as $C_P$. Since the available capacitance is slightly changed, the resonant frequency is recalculated to be

$$f_o = \frac{1}{2\pi}\sqrt{\frac{L + L_{s,\max}}{L \cdot L_s \cdot C}} = 108.2\ \text{kHz}. \tag{33}$$

From (14), the current gain is found as

$$\frac{L_{s,\max}}{L}\cos(\phi) = 4.1. \tag{34}$$

### B. Matching Transformer

The current gain is found to be only 4.1, which is not sufficient to heat the workpiece to the desired temperature; therefore, a matching transformer is introduced. Taking into

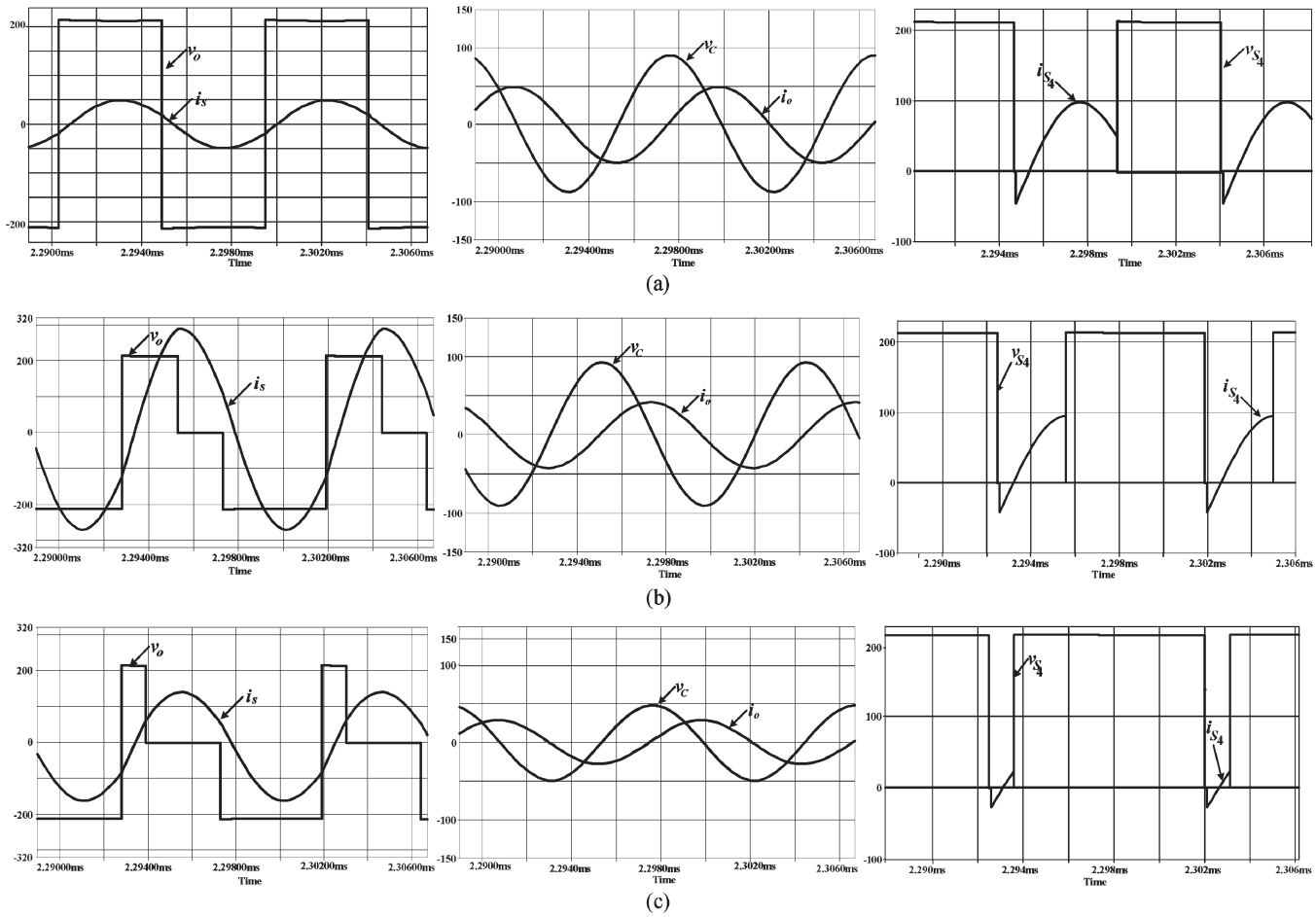


Fig. 9. Simulated results of the $LLC$ full-bridge inverter with asymmetrical control. (a) $v_o$, $i_s$, $v_C$, $i_o$, $v_{s4}$, and $i_{s4}$ waveforms with no PS at the full load. ($i_s$: 4 A/div, $v_o$: 50 V/div, $i_o$: 100 A/div, $v_C$: 50 V/div $i_{s4}$: 4 A/div, $v_{s4}$: 100 V/div, and time: 2 $\mu$s/div). (b) $v_o$, $i_s$, $v_C$, and $i_o$ waveforms at 62.5% load. ($i_s$: 1.33 A/div, $v_o$: 100 V/div, $i_o$: 100 A/div, $v_C$: 50 V/div $i_{s4}$: 4 A/div, $v_{s4}$: 100 V/div, and time: 2 $\mu$s/div). (c) $v_o$, $i_s$, $v_C$, and $i_o$ waveforms at 32% load. ($i_s$: 1.33 A/div, $v_o$: 100 V/div, $i_o$: 100 A/div, $v_C$: 50 V/div $i_{s4}$: 4 A/div, $v_{s4}$: 100 V/div, and time: 2 $\mu$s/div).

account only the fundamental component of the voltage, the primary current of the transformer is calculated using

$$I_{s,\mathrm{rms}} = \frac{\pi P}{2\sqrt{2}V_m \cos\phi} \tag{35}$$

which gives $I_{s,\mathrm{rms}} = 2.72$ A. From the calculated current gain, the maximum output current $(I_{o,\max})$ is 11.15 A. To utilize only 60% of the capacitor-rated current of 60 A, the required current ratio for the transformer is found from

$$I_{C_P,\max} = nI_{o,\max} \tag{36}$$

i.e., $n = 5.38 \approx 5$. The transformer used has a leakage reactance of 3.16 $\mu$H and must be taken into consideration. Therefore, a series inductance $(L_s)$ of 2.24 $\mu$H is needed to combine with the transformer's leakage inductance to meet the required inductance of 5.4 $\mu$H. Note that placing $L_s$ on the primary side can achieve benefits of inherent current-limitation protection of the transformer saturation. This means that the required series inductance on the transformer's primary is given as

$$L_s = 2.24n^2 = 56\ \mu\mathrm{H}. \tag{37}$$

## VII. Simulation and Experimental Results

To confirm the validity of the proposed topology and control scheme, a computer simulation and a hardware experiment are performed using the parameters in Table I. The resonant frequency calculated using (2) is 107.866 kHz. The load is a 30-g aluminum workpiece in a graphite crucible. Due to load-parameter variation when the workpiece temperature increases from 30 °C to 625 °C, the switching frequency is varied from 108.7 to 110.6 kHz. Angle $\alpha$ is varied from 0° to 144° for the purpose of output-power control. With the circuit parameters in Table I, the simulation results under angle $\alpha$ at 0°, 90°, and 144° are shown in Fig. 9(a)–(c), respectively. As $\alpha$ increases, the inverter output current $i_s$, output voltage $v_o$, the induction-coil current $i_o$, and induction-coil voltage $v_C$ decrease. The experimental results shown in Fig. 10 are obtained using the same set of parameters in Table I. The waveforms at full-load condition $(\alpha = 0°)$ are shown in Fig. 10(a) where the inverter operates at 108.7 kHz. Once the workpiece temperature increases, the induction-coil impedance changes in a way that the resonant frequency increases. The phase-locked loop control then increases the switching frequency of the inverter to track for the resonant frequency. This is to ensure the ZVS operation. The shifted angle is then adjusted to 90° to reduce the output

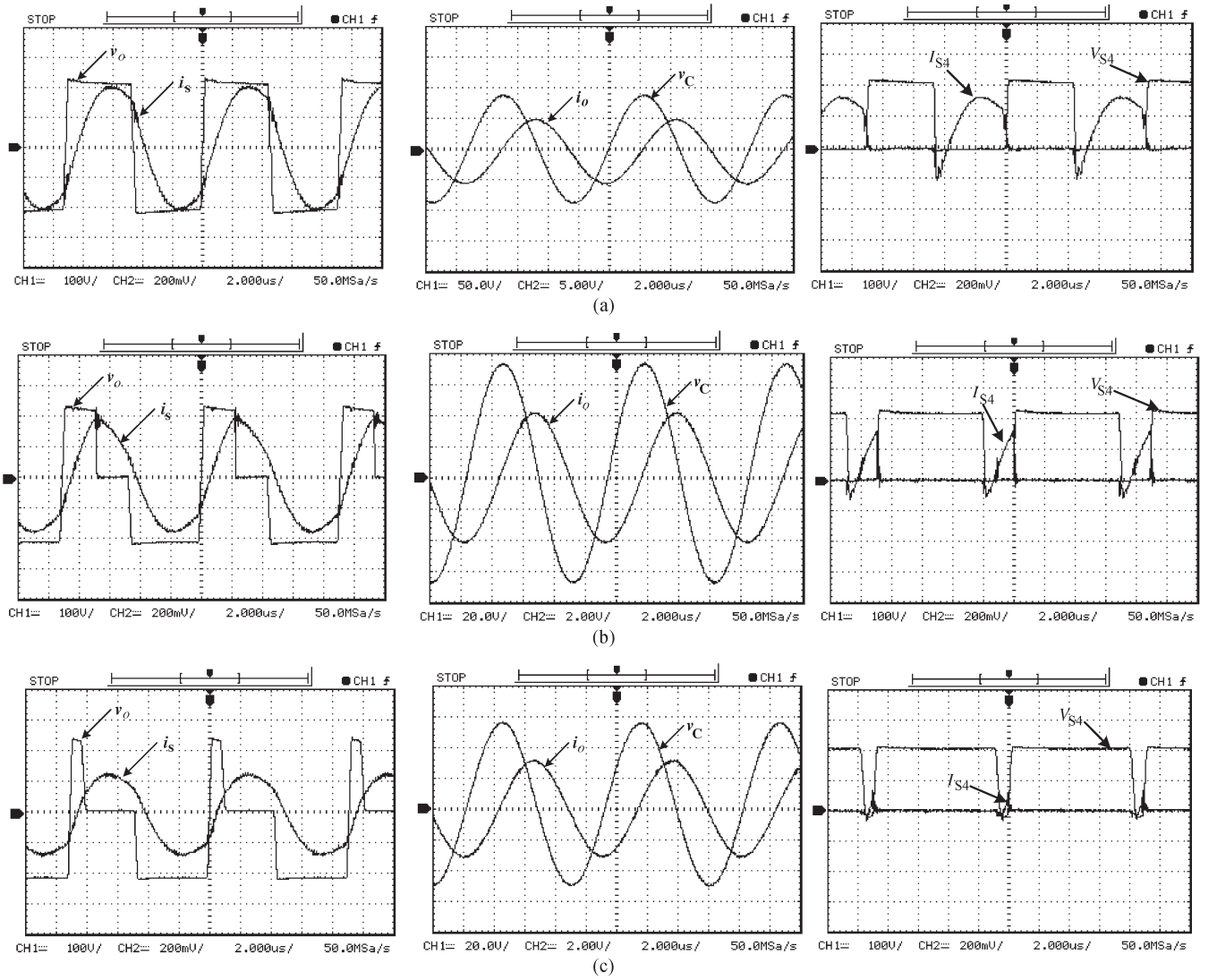


Fig. 10. Experimental results of the $LLC$ full-bridge inverter with asymmetrical control. (a) $v_o$, $i_s$, $v_C$, $i_o$, $v_{s4}$, and $i_{s4}$ waveforms with no PS at full load. ($i_s$: 2 A/div, $v_o$: 100 V/div, $i_o$: 100 A/div, $v_C$: 50 V/div, $i_{s4}$: 2.7 A/div, $v_{s4}$: 100 V/div, and time: 2 $\mu$s/div). (b) $v_o$, $i_s$, $v_C$, and $i_o$ waveforms at 62.5% load. ($i_s$: 2 A/div, $v_o$: 100 V/div, $i_o$: 40 A/div, $v_C$: 20 V/div, $i_{s4}$: 2.7 A/div, $v_{s4}$: 100 V/div, and time: 2 $\mu$s/div). (c) $v_o$, $i_s$, $v_C$, and $i_o$ waveforms at 32% load. ($i_s$: 2 A/div, $v_o$: 100 V/div, $i_o$: 40 A/div, $v_C$: 20 V/div, $i_{s4}$: 2.7 A/div, $v_{s4}$: 100 V/div, and time: 2 $\mu$s/div).

power to 62.5%, and the current and voltage waveforms are shown in Fig. 10(b) along with the switching $S4$ voltage and current waveforms. The switching frequency is increased to 109.17 kHz. In Fig. 10(c), the $i_s$, $v_o$, $i_o$, and $v_C$ waveforms are obtained, while $\alpha$ is adjusted to the limit of 144°. At this point, the output power is reduced to 32.16%. The switching frequency is automatically increased to 110.6 kHz. It is seen that an increase of $\alpha$ results in an increase of the switching frequency. This provides an easy adjustment of the output power with fast response.

Note that, even if the gate signal is forced to turn on $\alpha$ at a value greater than 144°, the switch will still turn on at 144°. This is due to the fact that the average voltage across the total inductor seen by the inverter must be zero. Since the switching frequency is maintained slightly above the resonant frequency, the ZVS operation of the $LLC$ full-bridge inverter with the proposed control scheme is guaranteed for the whole range of variable load parameters and variable output powers. Table II shows the losses of switches and diodes under different load levels from 32%–100%. At 100% of rated condition, switch $S_4$ carries the same loss at 3.45 W as with the other switches. However, when the output power is reduced, the switch $S_4$ conduction interval as well as the loss becomes less. The power angle $\phi$ is set at 36° to accommodate the induction coil and the aluminum-workpiece load, and the power is adjusted through angle $\alpha$. Therefore, the lowest load level that can be achieved is at $\alpha = 144°$, giving the power level at 32% of rated condition. For comparison purposes, the calculated and experimental

TABLE II
LOSS ON COMPONENTS UNDER ASYMMETRICAL CONTROL

| Output power (%) | Loss of switches (w) | | | | LOSS OF DIOSES (W) | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ |
| 100 | 3.45 | 3.45 | 3.45 | 3.45 | 2.13 | 2.13 | 2.13 | 2.13 |
| 50 | 3.05 | 3.05 | 3.05 | 1.98 | 2.13 | 2.13 | 2.97 | 2.13 |
| 32 | 2.65 | 2.65 | 2.65 | 0.29 | 2.13 | 2.13 | 3.00 | 2.13 |

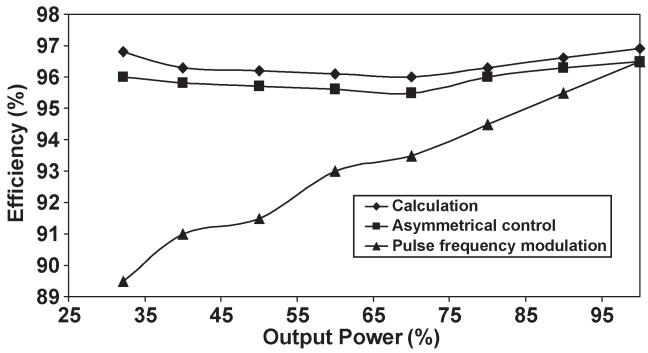


Fig. 11. Efficiency comparison between the calculation, asymmetrical control, and PFM.

efficiencies of the $LLC$ full-bridge inverter with asymmetrical control are shown in Fig. 11 using the parameters given in Table I. The PFM control scheme with the same parameter setting is also shown.

The experimental results for both control schemes are collected while the workpiece is at 625 °C. During the heating process from 30 °C to 625 °C, the equivalent resistance varies from 100 to 110 mΩ, which results in variation of the induction-coil inductance from 0.95 to 1.11 $\mu$H. Thus, the operating frequency is changed in the range of 108.7–110.6 kHz to achieve ZVS operation. At rated power, the efficiency of the $LLC$ full-bridge inverter is the same between the asymmetrical control and the PFM schemes. However, the proposed asymmetrical control has shown up to 6% higher efficiency at low-power operation. It is evident that the output power to the workpiece can be controlled by adjusting $\alpha$.

## VIII. Conclusion

In this paper, an improved full-bridge $LLC$ resonant inverter topology for induction-heating application has been proposed. The validity of the proposed asymmetrical control scheme is verified through simulation and experimental results. It can be concluded that the presented work control technique has the following advantages.

1) The asymmetrical control can be used to control the output power to the induction coil for the $LLC$ resonant tank.
2) The control scheme is in a simple configuration and easy to implement.
3) The resonant-frequency tracking together with the adjustment of the pulse voltage ensures maximum power transfer to the load throughout the heating cycle with minimal loss.
4) The placement of the inductor on the transformer's primary results in a small inductor due to the low current on the transformer's primary.

Therefore, the presented circuit configuration and proposed control scheme can also be used with other applications that require output-power regulation under load-parameter variation.

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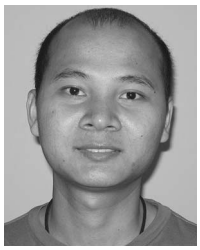

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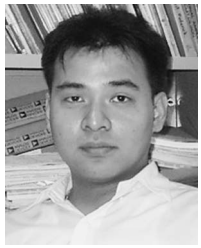

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