

High Efficiency Stereo Audio Power Amplifier

Feature Set

- Stereo audio power amplifier
- 2x25W peak power output (in to 8Ω loads)
- Low power consumption at normal listening levels: 60mW (delivering 2x 13mW in to 8Ω loads; corresponding to a total SPL of 73dB(C) from 89dB(C)/W at 1m speakers)
- Power efficient operation eliminates heat sinks
- Optimised for 1.5V battery supply
 - 0.8 – 1.8V supply range
 - 3.7V & 5V supply options, with external components
- 8Ω - 16Ω load impedance (8Ω optimal)
- 20Hz - 20kHz frequency response
- Digital audio input:
 - I²S, left or right formatted
 - 32 - 48kHz support
 - 16bits per channel
 - Master and slave modes
 - Automatic sample rate adaptation
- Audio processing:
 - 44step volume control 1.5dB per step
 - Mute, with adjustable ramping
 - Stereo-wide
 - Tuneable bass-boost
 - 16 user configurable biquad filters
- Automatic power save mode when the input signal is removed
- Click and pop suppression
- Operation from external clock source
- User interface:
 - Push button inputs
 - Rotary encoder volume control
 - Control pin inputs
 - LED indicator drivers
- 2-wire serial control interface:
 - Slave mode for control by external host
 - Master mode to control external device (for example: external ADC)
- Self configuring on power-up; autonomous operation
- One-Time-Programmable user register defaults
- Single package: 64QFN

General Description

The AS2002 is a stereo (2x 25W peak) highly power efficient switching audio power amplifier devices using Audium's proprietary technology; optimised to operate directly from a low voltage battery supply.

The Audium Advantage

The high peak-to-average-power-ratio characteristics of an audio signal, together with the dynamic range of a volume control, mean that an audio amplifier is very rarely operating at full output power. Existing switching audio power amplifiers only achieve optimum claimed efficiency at or near full output power. In comparison, Audium's power amplifier technology efficiently amplifies an audio signal over its entire operating output power range.

At normal listening levels, Audium's audio power amplifier technology can therefore offer a significant power saving advantage. Furthermore, as the maximum power output rating of a comparative audio amplifier increases, so does the Audium advantage.

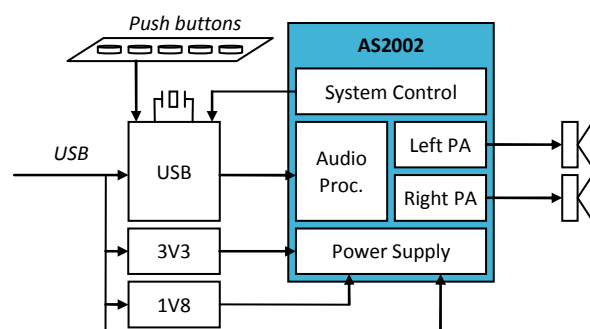
Target Applications

Whilst such characteristics are useful in virtually all audio power amplifier applications, they are most valuable in applications which require a relatively high output power but where the energy source is limited. For example:

- Battery powered MP3 docking station speaker systems
- USB powered speakers
- Battery powered travel speakers
- FM and DAB radios

In a battery powered product, Audium's power saving advantage directly translates into an increased operating lifetime of the product. In the case of a USB powered speaker, power output is greatly increased.

Example: USB Powered Speaker System



DOCUMENT HISTORY

Issue	Date	Notes
1	November 2009	Preliminary release
2	December 2009	Preliminary release • Correct ordering info to 3 digit variant data • Update pinout: changes to pins 57 & 58, see also AS-100234-AN • Add device marking diagram to section 9
3	-	Preliminary release • Separate in to dedicated AS2002 datasheet • Update recommended power supply topology in section 4.3 • Update clocking options in section 4.7

TABLE OF CONTENTS

1	Introduction	6
1.1	Background	6
1.2	Traditional Technologies	6
1.3	The Audium Advantage	6
1.4	Conclusion	7
2	Ordering Information and Device Options	8
3	Pin Assignments	9
3.1	Pin Diagram	9
3.2	Pin Descriptions	10
4	Device Description	12
4.1	Low Power Operation	12
4.2	Block Diagram	12
4.3	Power Supplies	13
4.3.1	Power Amplifier Supplies	13
4.3.2	Amplifier Control Supplies	15
4.3.3	Power Supply Sequencing	16
4.4	Operating Modes	17
4.5	Audio Signal Path	18
4.5.1	Digital Audio Interface	18
4.5.2	Input Clipping Detector	18
4.5.3	Silence Detector	19
4.5.4	DC Remover	19
4.5.5	Audio DSP	19
4.5.6	Audio Power Amplifier(s)	19
4.6	Control Interfaces	21
4.6.1	Reset, Software-reset, User-reset	21
4.6.2	Volume Control Pins	22
4.6.3	State Control pins	23
4.6.4	Two Wire Interface	25
4.7	Clocking Options	26
4.7.1	Internal Oscillator	28
4.7.2	Crystal Oscillator	28
4.7.3	External Clock Input	29
4.7.4	External Full System Clock Input	30
4.7.5	Clock Output	30
4.7.6	Clocking Strategy	30
5	Audio Digital Signal Processing	31
5.1	Matrix 1, 2 & 3 and Audio Modes	31
5.1.1	Stereo Modes	33
5.1.2	Active Crossover Modes	33
5.1.3	Single- and Dual-Mono Modes	34
5.2	Trim1, 2 & 3	35
5.3	Bass-Boost	35
5.4	Stereo-Wide	37
5.5	Biquad Filters	37
5.5.1	Configuration of Individual Biquad Filters	37
5.5.2	Mapping of Biquad Configuration Register Sets to Biquad Filters	38
5.5.3	Biquad Filters Repeat Mode	39
5.5.4	Biquad Filter Configuration Register Set Switching	40
6	Register Map	41
6.1	Register 0x00: CONFIG0	41
6.2	Register 0x01: BUTTON_CONTROL	41
6.3	Register 0x02: MUTE_RAMP	41
6.4	Register 0x03: VOLUME	42
6.5	Register 0x04: ROTARY_ENCODER	42
6.6	Register 0x05: VOLUME_DELAY	42
6.7	Register 0x06: VOLUME_RAMP	42
6.8	Register 0x07-0x0E: RESERVED0-7	42

6.9	Register 0x0F: I2S_CLIPPING	43
6.10	Register 0x10: STANDBY_CLK_DIV.....	43
6.11	Register 0x11: I2S_CLIP_THRESHOLD	43
6.12	Register 0x12: TWI_DEVICE_ADDRESS	43
6.13	Register 0x13-0x32: TWI_MASTER_DATA_0-31	44
6.14	Register 0x33: TWI_MASTER_PREAMBLE	44
6.15	Register 0x34: TWI_MASTER_POSTAMBLE.....	44
6.16	Register 0x35: TWI_MASTER_CONFIG	44
6.17	Register 0x36: SYSTEM_CLK_CONFIG.....	44
6.18	Register 0x37: CLK_OUT_CONFIG	45
6.19	Register 0x38: SILENCE_DETECT_THRESHOLD	45
6.20	Register 0x39: SILENCE_DETECT_HOLDOFF	45
6.21	Register 0x3A: AUDIO_DSP_OTP_VALID	46
6.22	Register 0x3B: AUDIO_DSP_CONFIG0	46
6.23	Register 0x3C: AUDIO_DSP_CONFIG1	46
6.24	Register 0x3D: AUDIO_DSP_CONFIG2	46
6.25	Register 0x3E: AUDIO_DSP_RESERVED	47
6.26	Register 0x3F: BIQUAD_OUTPUT	47
6.27	Register 0x40: BIQUAD_CONTROL	47
6.28	Register 0x41/46/4B/50/55/5A/5F/64/69/6E/73/78/7D/82/87/8C: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_0	48
6.29	Register 0x42/47/4C/51/56/5B/60/65/6A/6F/74/79/7E/83/88/8D: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_1	48
6.30	Register 0x43/48/4D/52/57/5C/61/66/6B/70/74/7A/7F/84/89/8E: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_2	48
6.31	Register 0x44/49/4E/53/58/5D/62/67/6C/71/75/7B/80/85/8A/8F: BIQUAD4/5/6/7/8/9/10/11/12/13/14/15_3 48	
6.32	Register 0x45/4A/4F/54/59/5E/63/68/6D/72/76/7C/81/86/8B/90: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_4	48
6.33	Register 0x91-0x92: RESERVED8-9.....	49
6.34	Register 0x93: BIQUAD_SELECT	49
6.35	Register 0x94: AUDIO_DSP_CLIPPING.....	49
6.36	Register 0x95: SOFT_RESET	50
6.37	Register 0x96: BATTERY	50
6.38	Register 0xFF: OTP_CONFIG	50
7	One-Time-Programmable Memory.....	51
7.1	Post-reset Device Initialisation from OTP Memory.....	51
7.2	OTP Memory Read Procedure	51
7.3	OTP Memory Write Procedure	52
7.4	Special OTP Memory Locations	54
7.4.1	OTP 0x92: DEVICE_ID	54
8	Performance Data	55
9	Package Information.....	56

TABLE OF FIGURES

Figure 1: Ordering information.....	8
Figure 2: Pin diagram (top)	9
Figure 3: Block diagram	12
Figure 4: Audio power amplifier power supplies (1.5V battery supply)	13
Figure 5: Audio power amplifier power supplies (3.7V or 5V system supply)	15
Figure 6: Digital power supplies.....	16
Figure 7: External schottky diode to remove power-up supply sequencing requirements	17
Figure 8: External regulator to remove power-down supply sequencing requirements	17
Figure 9: Digital audio interface input – I ² S	18
Figure 10: Digital audio interface - left-justified	18
Figure 11: Digital audio interface - right-justified	18
Figure 12: Audio power amplifier architecture	20
Figure 13: External Power-On-Reset circuit	22
Figure 14: Volume control pin external circuit, push button control.....	22
Figure 15: Volume control pins external circuit, rotary encoder control	22
Figure 16: Volume control pins external circuit, pins unused	23
Figure 17: State control pin external circuit, level-sensitive control.....	23
Figure 18: State control pin external circuit, edge-sensitive control	24
Figure 19: State control pin external circuit, pin control not required	24
Figure 20: State control pins external circuit, no pin control required	24
Figure 21: TWI write	25
Figure 22: TWI read	26
Figure 23: TWI write-read	26
Figure 24: TWI master 'byte-pairs' write	26
Figure 25: TWI master 'all at once' write	26
Figure 26: Clocking domains	27
Figure 27: Clock generation.....	28
Figure 28: Crystal oscillator schematic.....	29
Figure 29: Audio DSP functional blocks	31
Figure 30: Normal LR Stereo - Audio Mode: 24, (28 & 30)	33
Figure 31: Asymmetric LR Stereo - Audio Mode 26	33
Figure 32: Simple Mono Crossover - Audio Modes 16 & 17	33
Figure 33: Stereo to Mono Crossover - Audio Modes 18 & 19.....	34
Figure 34: Simple Mono Select - audio modes 8 & 9	34
Figure 35: Mono Select - audio modes 10 & 11	34
Figure 36: Mono Select (MS filtering) - audio modes 12 & 13.....	35
Figure 37: Stereo to Mono Combine - audio modes 14 & 15	35
Figure 38: Bass-boost corner frequency	36
Figure 39: Bass-boost gain.....	36
Figure 40: Bass-boost shape.....	37
Figure 41: Biquad filter structure.....	38
Figure 42: Biquad filter transfer function.....	38
Figure 43: OTP post-reset read procedure.....	51
Figure 44: OTP read procedure.....	52
Figure 45: OTP write procedure, single register writes	53
Figure 46: OTP write procedure, multiple register writes	54
Figure 47: QFN-64 package	56
Figure 48: QFN-64 package example marking.....	56

1 INTRODUCTION

To appreciate the advantages of an Audium audio power amplifier, it is first necessary to understand the normal operating conditions of a typical audio power amplifier.

1.1 BACKGROUND

Audium's audio power amplifier technology has been designed to exploit the characteristics of an audio signal; specifically the high PAPR (Peak to Average Power Ratio).

Research¹ shows that typical music content has a PAPR of between 10dB and 20dB (a factor of between x10 and x100). Audium's own research concurs, and for TV and film content shows an even higher PAPR of between 20dB and 25dB (a factor of between x100 and x300).

By definition peaks in the audio signal are therefore infrequent and of relatively short duration.

For an audio amplifier to cleanly reproduce the input signal it must therefore be able to handle these transitory peaks without distortion. For example, an audio power amplifier rated at 100W peak output power operating at 'full output power' would actually only be delivering an average output power of 3.2W. (Assuming a PAPR of 15dB, a factor of x32.)

If one was to actually drive a speaker at this average level of output power it would produce an extremely high, even damaging, volume level in a consumer environment (assuming typical speaker sensitivity in the order of 85-90dB(C) at 1W at 1m).

So, when including the effect of a volume control (typically a 30dB range) the total PAPR actually seen at the output of an audio amplifier is much higher; between 40dB and 50dB (a factor of between x10,000 and x100,000).

In fact, perhaps surprising to some, at normal listening levels the power actually required to drive a speaker is very low; only a few mW. For example, independent¹ and Audium research shows that an average power of around just 2mW is delivered to a satellite speaker in a 5.1 home theatre application at normal listening levels (approximately 70dB(C) at 1m, per speaker).

This analysis therefore reveals three key characteristics of an audio power amplifier under normal operating conditions:

1. At normal listening levels the required average output power is very low
2. An audio signal has a high PAPR
3. Even when operating at 'full output power' the actual average output power is therefore significantly lower than an amplifiers rated maximum peak output power

1.2 TRADITIONAL TECHNOLOGIES

A traditional class-D audio power amplifier is generally considered to be the most power efficient type of audio power amplifier, with power efficiency claims in the region of 90% common.

However a study of such efficiency data will reveal these efficiency levels are only achievable when operating at, or close to, maximum output power. As the output power is reduced, the power efficiency also reduces, often reaching single figure efficiency levels at a normal average output power level as defined above.

Similar to other traditional amplifier technologies, as the output power of a class-D audio power amplifier reduces to zero, the input power consumption approaches a quiescent non-zero value. This quiescent power consumption is inherent to the design of a class-D amplifier and can be quite significant. For a class-D amplifier rated at 100W peak output power, this quiescent power consumption can be in the order of 1W. Consuming around 1W to deliver an average of a few mW is clearly not power efficient!

1.3 THE AUDIUM ADVANTAGE

Audium has developed an innovative switching audio amplifier technology that radically reduces power consumption under quiescent, normal and all other listening conditions, whilst still being capable of producing high peak output power levels. The result is a scalable audio power amplifier which is power efficient across its entire operating range.

¹'High Efficiency Audio Power Amplifiers, design and practical use'

Ronan van der Zee, Academic Publication on line of University of Twente, the Netherlands, 1999 (ISBN: 90-36512875).

Audium is able to achieve this through a series of techniques that address the inefficiencies of a traditional class-D switching amplifier by exploiting the high PAPR of an audio signal.

The output power stage in a traditional class-D amplifier uses a H-bridge arrangement of power FETs driven by a PWM (Pulse Width Modulation) signal at a frequency of several hundred kHz, or greater. The H-bridge is then connected to a fixed voltage supply capable of meeting the maximum output power requirements for a given load.

The quiescent power draw for such a design is mainly due to switching losses in the power devices which make up the H-bridge. These losses are dependent on the physical properties of the devices themselves and are proportional to the switching frequency and (predominantly) the square of the supply voltage.

Instead of PWM, Audium uses a proprietary low-rate modulation scheme with a frequency that averages around x10 lower than typical PWM implementations. Reducing the average switching frequency reduces associated switching losses by a similar factor of x10.

Instead of a single fixed voltage rail, Audium uses a fixed low voltage rail together with a variable higher voltage rail to supply the power output stage. The system controller adjusts the high voltage rail according to the required peak output power, as indicated by the volume control. The system controller also dynamically selects between these rails according to the instantaneous audio content. Using a lower voltage supply rail(s) greatly reduces switching losses. For example, under the normal listening conditions previously defined, this can reduce switching losses by a factor of around x400.

The above techniques retain the integrity and fidelity of a full frequency range, uncompressed, 'CD quality' audio signal. The above savings are multiplicative and create a scalable audio power amplifier with high efficiencies over all operating conditions.

The fixed low voltage rail and high power efficiency makes Audium's audio power amplifier technology ideally suited to battery powered applications. The fixed low voltage rail can be supplied directly from the battery, and the variable higher voltage rail generated from it.

The variable high voltage rail needs to be capable of providing power to the output stage up to the amplifiers peak output power rating. However, since this is an audio amplifier, the PAPR tells us that the high voltage rail does not need to be capable of sustaining this condition. By attaching a high capacity, low resistance reservoir to the high voltage rail, both the battery and the high voltage generation circuitry need only be capable of sustaining the required average output power.

For example, when operating at full volume, a 100W peak output power audio amplifier will only be producing an average output power of 3.2W (assuming a PAPR of 15dB). A single alkaline battery can provide a continuous output power to between approximately 1.5W and 1W. (The power output reduces over the battery lifetime discharge cycle). Four batteries in parallel can therefore produce between 6W and 4W of continuous power, which is sufficient to power this example.

1.4 CONCLUSION

Audium's ground breaking improvements to audio power amplifier efficiency are realised through a new switching architecture using a standard industry silicon process.

The high efficiencies of the Audium audio power amplifier mean greatly reduced losses in the power drive stages, and completely eliminate the need for bulky and costly heat-sinks. As a standalone product, Audium's high efficiency audio power amplifier can significantly increase the lifetime of battery operated audio devices.

In conclusion Audium introduces a new, innovative, and highly efficient and 'green' technology audio power amplifier design, capable of both drastically improving the lifetime of existing products, and enabling new markets.

2 ORDERING INFORMATION AND DEVICE OPTIONS

AS2002-QNC-030

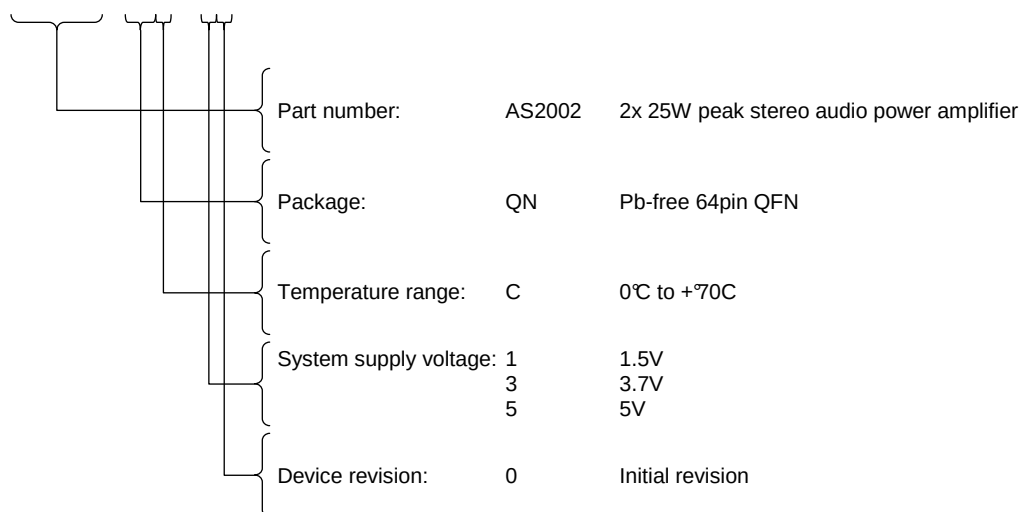


Figure 1: Ordering information

The following device options are available:

Device	Output power	System supply voltage		
		1.5V	3.7V	5V
AS2002	25W peak per channel			AS2002-QNC-050

Table 1: Available device options

3 PIN ASSIGNMENTS

The AS2002 is packaged in a 64pin TQFP with an exposed paddle on the underside of the package.

The exposed paddle provides the main electrical and thermal ground for the device. It is therefore important to ensure that this paddle has a robust connection to an electrical and thermal ground plane.

3.1 PIN DIAGRAM

The AS2002 pinout is shown in Figure 2 below.

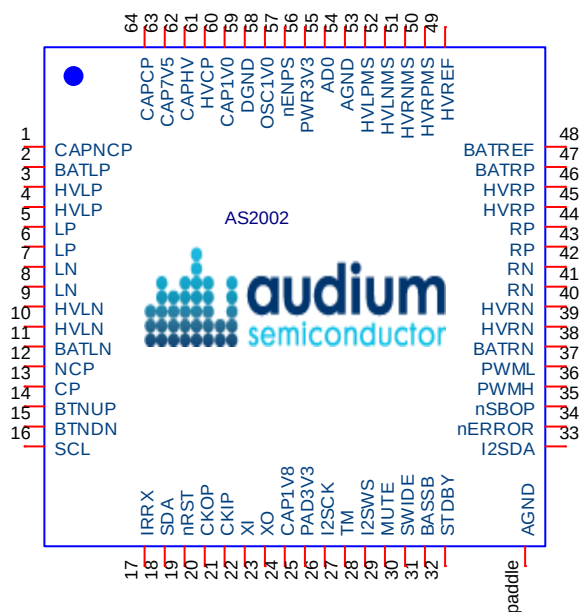


Figure 2: Pin diagram (top)

3.2 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Description
Paddle	AGND	Supply	Exposed paddle on the bottom of the package This is the main device GND connection. Connect to DGND and AGND and to a common GND
1	CAPNCP	Analogue Input	7V5 charge pump inverted clock input, connect to NCP via a capacitor
2	BATLP	Supply	Low-rail supply for the left positive side half bridge
3	HVLN	Analogue Input	High-rail supply for the left positive side half bridge, connect pins together externally
4			
5	LP	Analogue Output	Left positive side half bridge output, connect pins together externally
6			
7	LN	Analogue Output	Left negative side half bridge output, connect pins together externally
8			
9	HVLN	Analogue Input	High-rail supply for the left negative side half bridge, connect pins together externally
10			
11	BATLN	Supply	Low-rail supply for the left negative side half bridge
12	NCP	Digital Output	7V5 charge pump inverted clock output, connect to CAPNCP via a capacitor
13	CP	Digital Output	7V5 charge pump clock output, connect to CAPCP via a capacitor
14	BTNUP	Digital Input	Volume up button or rotary encoder input
15	BTNDN	Digital Input	Volume down button or rotary encoder input
16	SCL	Digital Input/Output Open drain	Two-Wire-Interface control clock
17	IRRX	Digital Input	Infrared interface receiver input. Not used. Tie to AGND
18	SDA	Digital Input/Output Open drain	Two-Wire-Interface control data
19	nRST	Digital Input	Active low external reset input
20	CKOP	Digital Output	Clock output
21	CKIP	Digital Input	Clock input
22	XI	Digital Input	Crystal oscillator input
23	XO	Digital Output	Crystal oscillator output
24	CAP1V8	Decoupling	Decoupling capacitor connection for internal 1V8 supply
25	PAD3V3	Supply	3V3 supply for digital I/O pins
26	I2SCK	Digital Input/Output	Audio interface clock
27	TM	Digital Input	Test-mode enable pin. Tie to PAD3V3
28	I2SWS	Digital Input/Output	Audio interface word select (sample rate clock)
29	MUTE	Digital Input/Output	Mute button input and indicator output
30	SWIDE	Digital Input/Output	Stereo-wide button input and indicator output
31	BASSB	Digital Input/Output	Bass-boost button input and indicator output
32	STDBY	Digital Input/Output	Standby/Active mode button input and indicator output
33	I2SDA	Digital Input	Audio interface data input
34	nERROR	Digital Output Open drain	Active low error output indicator
35	nSBOP	Digital Output	Active low standby mode indicator
36	PWMH	Digital Output	High-rail voltage PWM reference, connect to HVREF via a RC filter
37	PWML	Digital Output	Low-rail voltage PWM reference, connect to BATREF via a RC filter
38	BATRN	Supply	Low-rail supply for the right negative side half bridge
39	HVRN	Analogue Input	High-rail supply for the right negative side half bridge, connect pins together externally
40			
41	RN	Analogue Output	Right negative side half bridge output, connect pins together externally
42			
43	RP	Analogue Output	Right positive side half bridge output, connect pins together externally
44			
45	HVRP	Analogue Input	High-rail supply for the right positive side half bridge, connect pins together externally
46			
47	BATRP	Supply	Low-rail supply for the right positive side half bridge
48	BATREF	Analogue Input	Low-rail voltage reference input, filtered version of PWML
49	HVREF	Analogue Input	High-rail voltage reference input, filtered version of PWMH

Pin #	Pin Name	Type	Description
50	HVRPMS	Analogue Input	Right positive side half bridge high-rail voltage reference, from potential divider
51	HVRNMS	Analogue Input	Right negative side half bridge high-rail voltage reference, from potential divider
52	HVLNMS	Analogue Input	Left negative side half bridge high-rail voltage reference, from potential divider
53	HVLPMS	Analogue Input	Left positive side half bridge high-rail voltage reference, from potential divider
54	AGND	Supply	Analogue supply ground, connect to paddle
55	AD0	Digital Input	Two-Wire-Interface device address LSB
56	PWR3V3	Supply	3V3 supply for internal analogue components and internal 1V8 and 1V0 DC-DC converters
57	nENPS	Digital Input	Active low internal 1V8 & 1V0 supply enable, should be tied to GND for normal operation
58	OSC1V0	Supply	Dedicated 1V0 supply to the internal oscillator, connect to CAP1V0 & DGND via RC filter
59	DGND	Supply	Digital supply ground. Used as 'clean' GND for internal oscillator supply decoupling
60	CAP1V0	Analogue output	Decoupling capacitor connection for internal 1V0 supply
61	HVCP	7V5 Digital Output	High-rail boost circuit switching output
62	CAPHV	Analogue output	High-rail charge pump reservoir capacitor
63	CAP7V5	Analogue output	7V5 charge pump reservoir capacitor
64	CAPCP	Analogue Input	7V5 charge pump clock input, connect to CP via a capacitor

Table 2: Pin descriptions

4 DEVICE DESCRIPTION

The AS2002 is a highly efficient, switching stereo audio power amplifier, capable of delivering 2x 25W peaks in to 8ohms.

The AS2002 integrates audio processing, amplifier control and output drive stages in to a single device.

4.1 LOW POWER OPERATION

The AS2002 is a highly power efficient audio power amplifier incorporating a multitude of power saving features:

- Innovative, patented audio power amplifier
 - o Modified, bridged output drive stages
 - o Proprietary low-rate modulated switching design
 - o Dual supply rails to the output drive stages
 - Low voltage supply rail
 - Volume tracking, variable, higher voltage supply rail
 - o Dynamic switching between supply rails based on instantaneous audio content
- Audio silence detection and auto-muting
- Internal low-power oscillator
- Low voltage digital core

4.2 BLOCK DIAGRAM

A high level block diagram of the AS2002 is shown below.

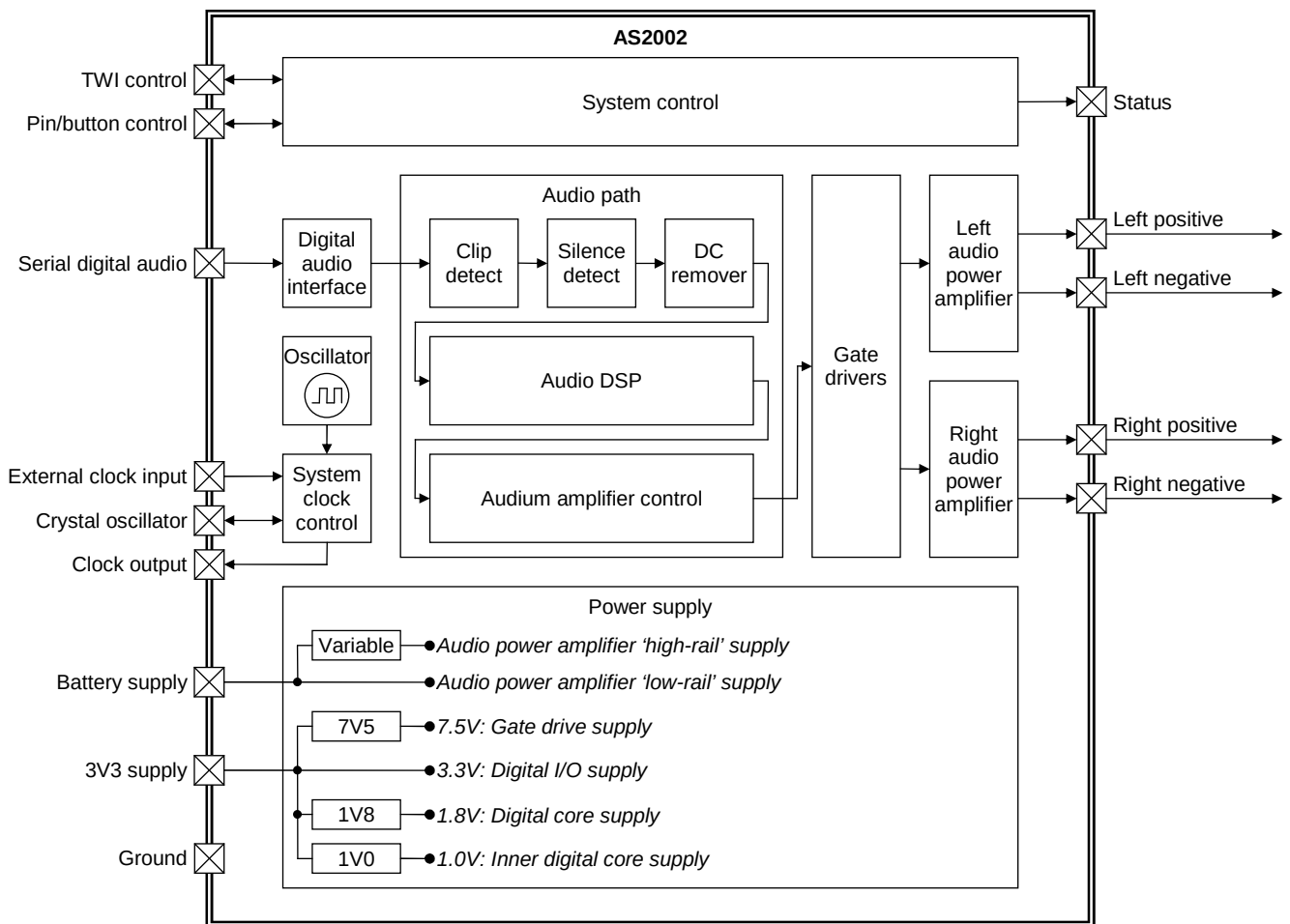


Figure 3: Block diagram

4.3 POWER SUPPLIES

4.3.1 POWER AMPLIFIER SUPPLIES

Figure 4 shows a block diagram of the audio power amplifier power supplies.

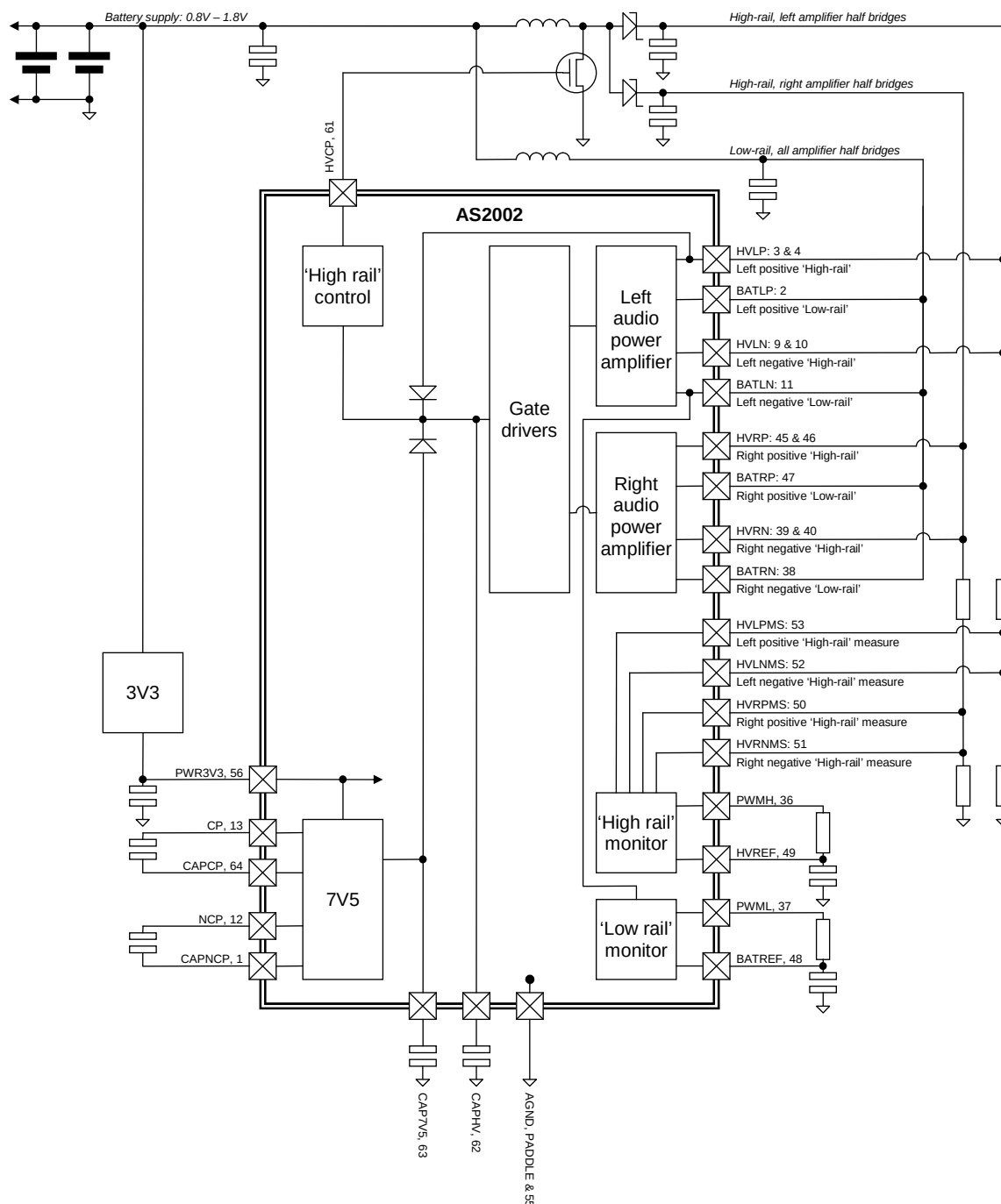


Figure 4: Audio power amplifier power supplies (1.5V battery supply)

The audio power amplifiers in the AS2002 operate directly from a low voltage battery supply over the range 0.8V to 1.8V, typically 1.5V. The audio power amplifiers use this battery supply (referred to as the 'low-rail') directly.

Through external components the AS2002 also boosts the battery supply to generate additional, variable, higher voltage supplies for the audio power amplifiers (referred to as the 'high-rail'). The voltage on the high-rail varies (over the range of approximately 3.3V to 25V) and is defined by the user volume setting.

HVCP (pin 61) controls an external power FET, which together with an external inductor, schottky diodes and capacitors form a boost converter that generates the high-rail supplies used by the audio power amplifiers.

Each audio amplifier output stage is based on a bridged architecture (see section 4.5.6.2). Separate high-rail supplies are required for each half-bridge in the output stages. Since the AS2002 is a stereo amplifier there are four half-bridges. Separate left and right high-rail supplies are required.

The AS2002 monitors the voltage on the high-rail supplies through HVLPMs (pin 53), HVLNMs (pin 52), HVRPMs (pin 50) & HVRNMs (pin 51) and adjusts the signal on HVCP to automatically maintain the required high-rail voltage. Potential dividers are used to reduce the high-rail voltages to the 0V to 3.3V input range of the HVMS pins. Internally the voltages on the HVMS pins are compared against a reference voltage on HVREF (pin 49). This reference voltage is generated by passing a PWM signal on PWMH (pin 36) through an external resistor-capacitor network.

Internally the AS2002 also monitors the voltage on the low-rail (ie the battery voltage when using a 0.8V to 1.8V system supply voltage) and uses this information to ensure consistent volume behaviour, independent of the actual battery supply voltage. The battery voltage is reported in register [0x96\[5:0\]](#). The low-rail monitoring function requires a resistor-capacitor network to be connected between PWML (pin 37) and BATREF (pin 48).

The device includes an internal 7.5V charge pump. This requires external capacitors be connected between CP (pin 13) and CPCAP (pin 64), and between NCP (pin 12) and CAPNCP (pin 1). A decoupling capacitor should also be connected to CAP7V5 (pin 63). The 7.5V rail is used to drive the HVCP (pin 61). Either the 7.5V rail or the high-rail (whichever is greater) is used to power the output power stage FET gate drivers. A decoupling capacitor should be connected to CAPHV (pin 62).

As Figure 4 shows, the AS2002 operates directly from a 0.8V to 1.8V (1.5V nominal) system supply voltage.

The AS2002 can also operate from system supply voltages higher than 1.8V with external support components; as shown in Figure 5 below.

In this application the low-rail is fixed at 1.8V and generated by an external (switching) regulator from the higher system supply voltage. The high-rail boost converter is supplied directly from the higher system supply voltage.

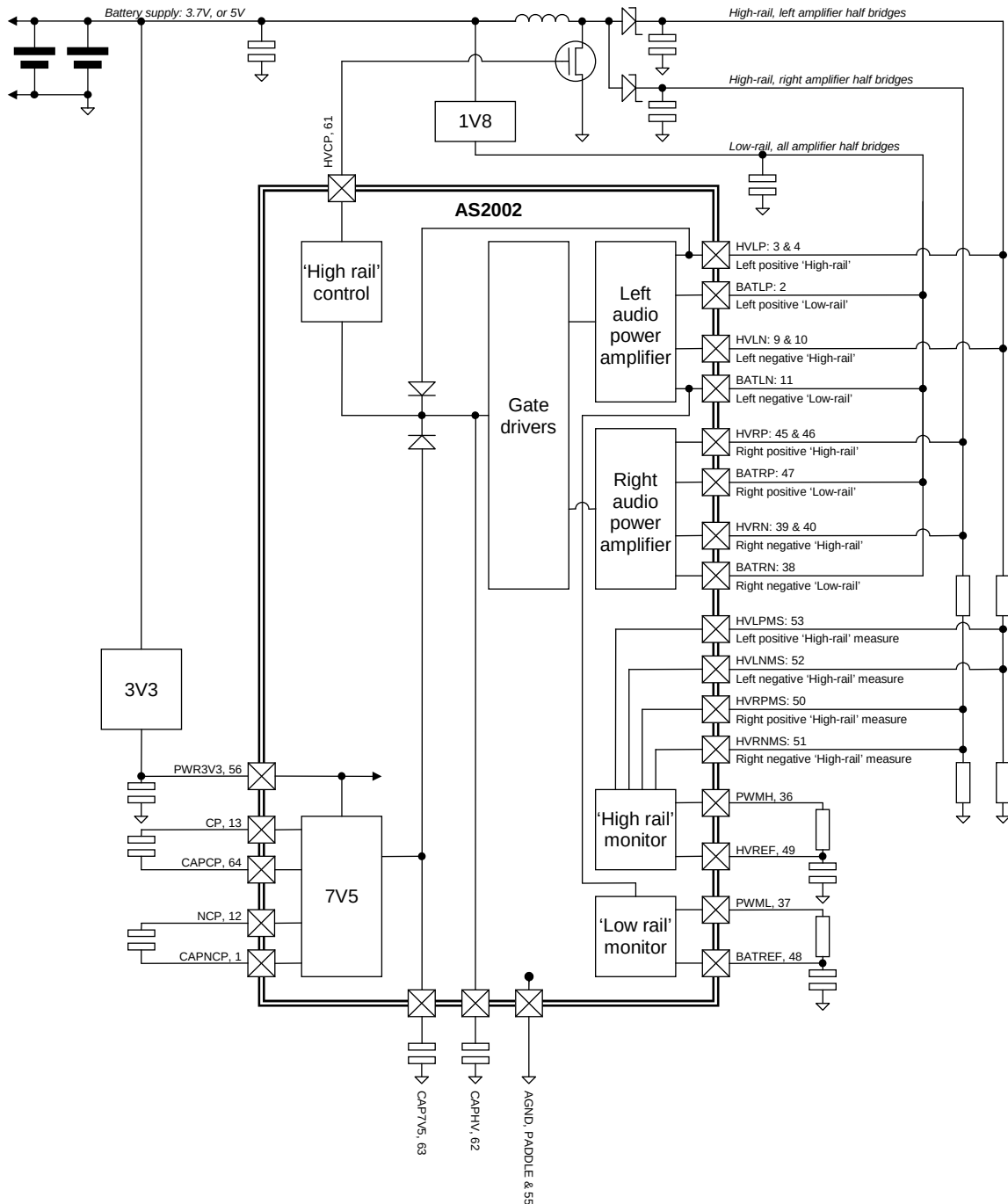


Figure 5: Audio power amplifier power supplies (3.7V or 5V system supply)

4.3.2 AMPLIFIER CONTROL SUPPLIES

In addition, the AS2002 requires a fixed 3.3V supply. Typically this is generated from the battery supply by an external switching regulator.

The 3.3V supply powers the digital I/O pins via PAD3V3 (pin 25) and internal switching voltage regulators via PWR3V3 (pin 56). The digital core operates from 1.8V and 1.0V supplies. Internal switching regulators generate these supplies from the external 3.3V supply. nENPS (pin 57) should be tied low to always enable these switching regulators. Decoupling capacitors should be connected to CAP1V8 (pin 24) and CAP1V0 (pin 60).

OSC1V0 (pin 58) is a dedicated 1.0V supply connection to the internal oscillator. An external resistor-capacitor filter should be connected between CAP1V0 (pin 60), OSC1V0 (pin 58) and DGND (pin 59).

Note that the 1.8V and 1.0V internal switching regulators are not designed to provide power to any external devices.

The 7.5V charge pump is also supplied from the external 3.3V rail via PWR3V3 (pin 56).

Care should be taken in the choice of the 3.3V regulator to ensure that 3.3V output is not affected by any fluctuations in the battery voltage.

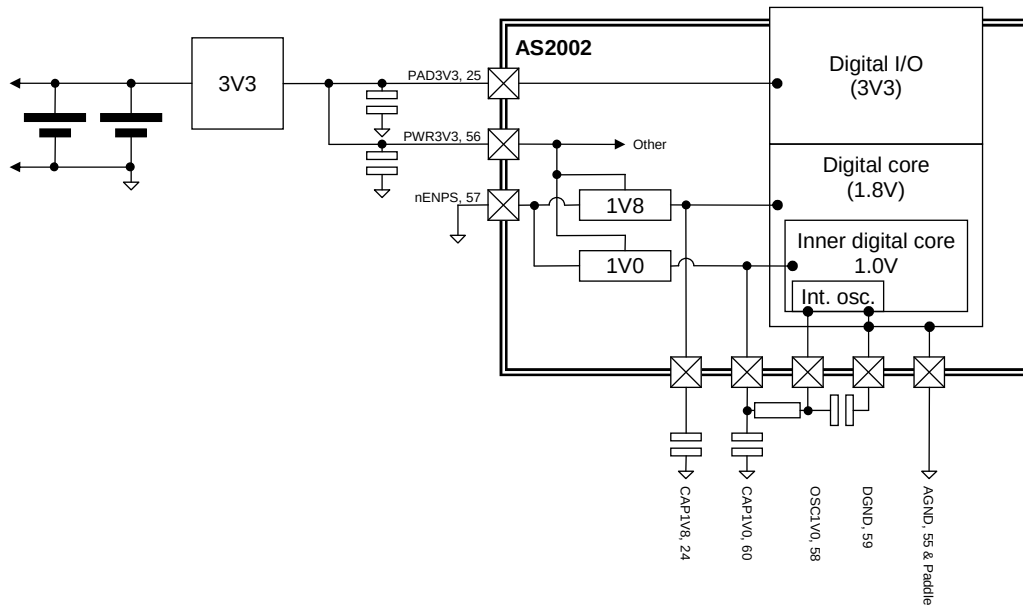


Figure 6: Digital power supplies

Internally the AS2002 has a single GND structure. Externally the AS2002 has three ground connections:

- PADDLE
- AGND, pin 54
- DGND, pin 59

PADDLE is the exposed paddle on the underside of the device package and is the main device ground. This exposed paddle must be connected to a solid ground plane on the PCB.

AGND is should also be connected to the same solid ground plane on the PCB.

DGND is used as a 'clean' ground connection for the internal-oscillator power supply filter, and should be connected to OSC1V0 via a decoupling capacitor. DGND should not be connected to the ground plane on the PCB.

4.3.3 POWER SUPPLY SEQUENCING

4.3.3.1 Power-up Sequencing

As described in sections 4.3.1 and 4.3.2 above, there are two external supplies to the AS2002:

- Low-rail supply (pins: BATLP: 2, BATLN: 11, BATRP: 47 & BATRN: 38)
- 3V3 supply (pins: PWR3V3: 56 & PAD3V3: 25)

The 3V3 supply should always be present when the low rail supply is applied:

- The 3V3 supply should be powered-up at the same time as, or before, the low-rail supply.
- The low-rail supply should be powered-down at the same time as, or before, the 3V3 supply.

In some applications the 3V3 supply may be derived from the low-rail supply. In these applications, on power-up the 3V3 will be applied after the low-rail; which violates the above power-up rule.

In these applications a low power, low forward-voltage (<250mV) schottky diode should be added between the low-rail and the internal 1V8 supply. With this schottky in place there are no power supply sequencing requirements.

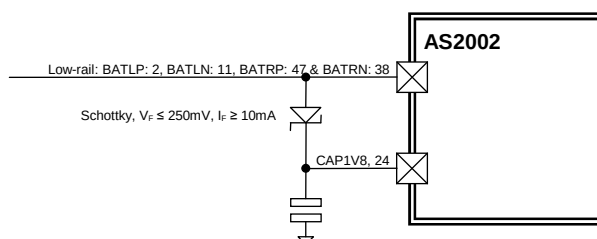


Figure 7: External schottky diode to remove power-up supply sequencing requirements

4.3.3.2 Power-down Sequencing

Always set the device in to standby mode before powering-down.

During active operation the AS2002 will generate a high-rail voltage. On power down this high-rail voltage should always be allowed to decay before the 3V3 supply is removed.

The addition of a simple linear voltage regulator, as shown in Figure 8 below, between the high-rail and the 3V3 supply can ensure this condition is always met. In normal operation the 3V3 supply will be present and the regulator will be inactive. However if a voltage exists on the high-rail, but there is no 3V3 supply, then the regulator will act to hold up the 3V3 supply (at a nominal 3V) until the high-rail has decayed.

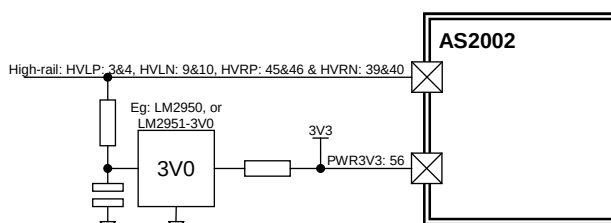


Figure 8: External regulator to remove power-down supply sequencing requirements

4.4 OPERATING MODES

The AS2002 has two basic operating modes:

- Standby
- Active

The operating mode is indicated by register [0x01\[6\]](#) and by nSBOP, pin 35. Register [0x01\[6\]](#) and nSBOP will be 0 / low when in standby mode, 1 / high when in active mode.

The operating mode may be set by writing to register [0x01\[7:6\]](#) or via STBY, pin 32 (see section 4.6.3).

Standby mode is a low power mode that should be used when audio amplification is not required. In standby mode only the internal oscillator and the control interfaces are active; all other sections of the device are switched off.

Active mode has two sub-modes:

- Active-normal
- Active-mute

In active-normal mode all sections of the device are active allowing the device to receive a digital audio signal, amplify it and drive an attached load.

In active-mute mode, the audio power amplifier is gracefully muted and then switched off as a power saving feature. When in active-normal mode, if any of the following conditions occurs then the device will automatically enter active-mute mode:

- Digital audio input signal not present (see section 4.5.3)
- Digital audio input signal below a threshold (see section 4.5.3)
- Volume level set, or reduced, to 0
- Mute activated

When all of the above conditions have cleared the device will automatically return to active-normal mode and resume normal operation.

4.5 AUDIO SIGNAL PATH

4.5.1 DIGITAL AUDIO INTERFACE

The digital audio interface uses three pins:

- I2SCK, pin 26: bit clock
- I2SDA, pin 33: data input
- I2SWS, pin 28: word-select clock

I2SDA receives the serial digital audio data. I2SWS is an alignment word-select clock which indicates if the data on I2SDA represents the left or right channel data. I2SDA and I2SWS are synchronous to the I2SCK clock and are sampled on a low to high transition of I2SCK.

The digital audio interface may be configured to act as a master-receiver or slave-receiver through register [0x00\[6\]](#).

4.5.1.1 Master Mode

When the digital audio interface is configured as a master, I2SDA is an input and I2SCK & I2SWS are outputs.

The bit clock frequency is the same as the system-clock frequency. (See section 4.7 below.) The word-select clock frequency is always 1/32 times the bit clock frequency. In master mode the digital audio interface therefore always captures 16bits of data per channel.

Note that the I2SCK and I2SWS signals are only present when the device is in active mode. In standby mode these outputs are low.

4.5.1.2 Slave Mode

When the digital audio interface is configured as a slave, I2SCK, I2SDA & I2SWS are all inputs. The digital audio interface automatically adapts to the clock and sample rate of the incoming audio data stream.

The optimal data bit width is 16bits per channel. If fewer than 16 bits of data are received then zero padding bits are added to promote the data to 16bit samples. If more than 16 bits of data are received then any excess least significant bits are discarded.

4.5.1.3 Audio Formats

The digital audio interface supports three audio data formats:

- I²S
- Left-justified
- Right-justified

The format may be selected through register [0x00\[5:4\]](#).

In all formats the data is assumed to be in a 2's-complement format and presented MSB first.

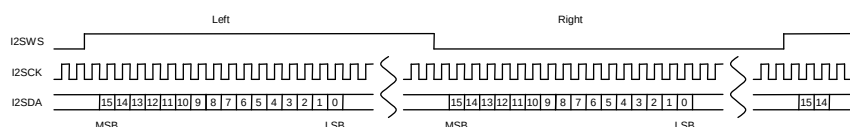


Figure 9: Digital audio interface input – I²S

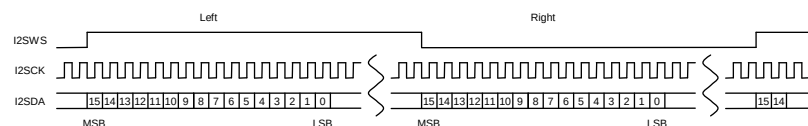


Figure 10: Digital audio interface - left-justified

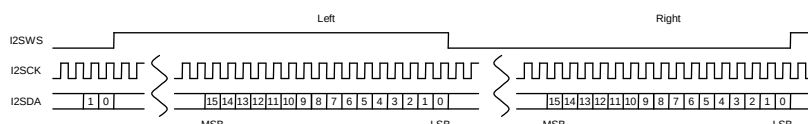


Figure 11: Digital audio interface - right-justified

4.5.2 INPUT CLIPPING DETECTOR

The clipping detector monitors both channels of the signal from the digital audio interface and compares the absolute magnitude of each sample against a threshold. If the threshold is exceeded a clipping event is deemed to

have occurred, which is reported in register [0x0F\[1\]](#). Register [0x11\[6:0\]](#) contains the most significant 7bits of the 15bit threshold value (the least significant bits of the threshold are all preset to 1).

Since input clipping events tend to be transitory, once triggered, the input clip flag remains asserted for a further $0.768/SystemClockMHz$ ms after the clipping event has cleared.

The input clipping flag may be made fully 'sticky', through register [0x0F\[3\]](#). This will latch the clip flag event until cleared by register [0x0F\[7\]](#).

The input clipping flag may also be mapped to the nERROR pin through register [0x0F\[5\]](#).

Note that any DC offset present on the input signal may affect the operation of the clipping detector.

4.5.3 SILENCE DETECTOR

The silence detector monitors both channels of the signal from the digital audio interface and compares the absolute magnitude of each sample against a threshold. If all values are below the threshold for a hold-off period of time then the device considers there to be no audio signal present and enters active-mute mode. For as long as the audio data remains below the threshold the device will remain in active-mute mode. As soon as any audio data exceeds the threshold, the device will automatically return to active-normal mode and resume normal operation.

Register [0x38\[7\]](#) indicates if the device has entered this condition. The least significant 7bits of the magnitude threshold are defined by register [0x38\[6:0\]](#) (the most significant bits are all preset to 0). The hold-off time is defined by register [0x39\[7:0\]](#).

Setting the threshold and/or the wait period to 0 will disable the silence detect feature.

If the digital audio signal is not present (i.e. I2SCK and/or I2SWS are not present) the device will automatically enter active-mute mode after a timeout period of $3.072/SystemClockMHz$ ms.

Setting both the threshold and the wait period to 0 will disable this feature (as well as disabling the silence detect feature).

Note that any DC offset present on the input signal may affect the operation of the silence detector.

4.5.4 DC REMOVER

The DC remover is implemented using a first order high pass filter and may be enabled through register [0x3B\[7\]](#).

The DC remover filter response varies linearly with the sample-rate of the incoming digital audio signal. Table 3 below details the filter response for common sample rates.

SampleRate kHz	-3dB cut-off Hz	Gain at 20Hz dB
32	5.0	-0.26
44.1	6.9	-0.49
48	7.5	-0.57

Table 3: DC remover filter characteristics

4.5.5 AUDIO DSP

For information on the Audio DSP block see section 5.

4.5.6 AUDIO POWER AMPLIFIER(S)

4.5.6.1 Mute & Volume Control

The AS2002 incorporates volume and mute controls.

The AS2002 should always be fed a line-level signal input and **the volume control should always be used as the system master volume control. Operating the device as a fixed (maximum) gain amplifier is not recommended.** The device uses the volume information to provide only the required amount of gain headroom, thus maintaining the Audium power efficiency advantage.

The volume range varies by system supply voltage, as shown in Table 4 below.

System supply voltage (V)	Volume range
1.5	0 – 44
3.7	0 – 39
5.0	0 – 37

Table 4: AS2002 volume ranges

A maximum volume value corresponds to full output power. A volume value of 0 is equivalent to the mute condition ($-\infty$ dB). Each volume step equates to a 1.5dB change in output power.

The current volume level is indicated in register [0x03\[5:0\]](#).

The volume level may be controlled through external pins (see section 4.6.2) or through register [0x03\[7:0\]](#). Register control allows the current volume to be incremented, decremented or a new absolute volume level to be set.

The mute control is a soft mute. When entering the mute condition the volume is ramped down to zero. When exiting the mute condition the volume is ramped back up from zero to the previous volume level (as defined by register [0x03\[5:0\]](#)). The volume ramp rate is defined by register [0x02\[6:0\]](#).

4.5.6.2 Power Drive Stage

The switching output amplifiers use a modified 'H-bridge' arrangement of FETs (similar to a traditional class-D switching amplifier) to drive the load in a bridge-tied fashion; as shown in Figure 12 below.

Each output amplifier stage has 2 half-bridges; a positive and negative. Each half-bridge has its own low-rail and high-rail supply connection pins, as shown in Figure 4, Figure 5 and Figure 12.

The amplifier controller switches the FETs to reproduce each individual audio sample from either the high-rail or the low-rail supply, depending on the actual required output voltage (a combination of the audio content and the user volume setting).

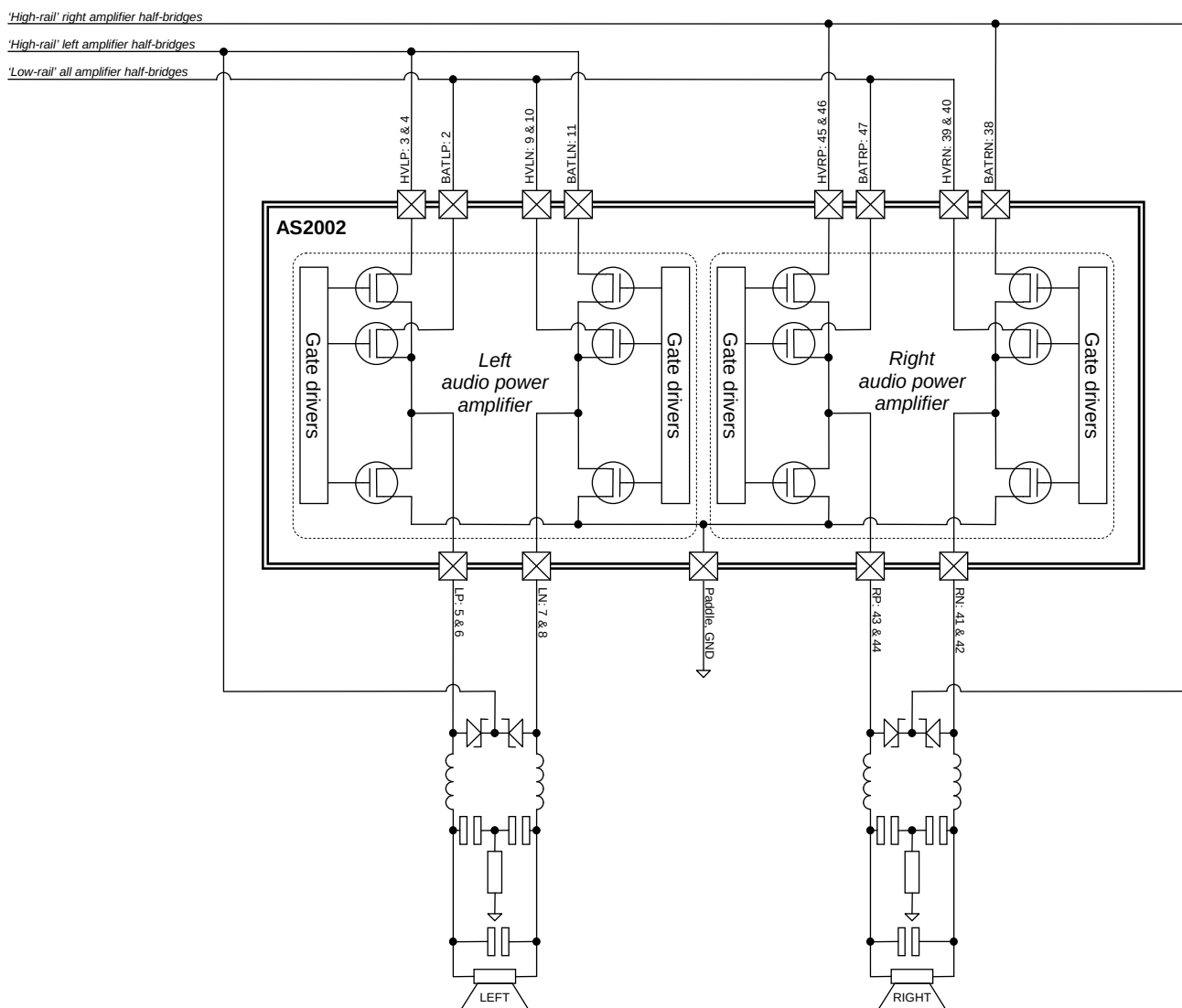


Figure 12: Audio power amplifier architecture

LP (pins 5 & 6) and LN (pins 7 & 8) are the output from the left audio power amplifier. RP (pins 43 & 44) and RN (pins 40 & 41) are the output from the right audio power amplifier. Note that these are differential outputs and should never be connected to ground.

To clamp any excessive switching voltage spikes and thereby prevent device damage, Schottky diodes should be connected between each output terminal and its high-rail supply.

In common with other switching amplifier designs, the AS2002 requires filters on its outputs to prevent energy at the switching frequency from being dissipated in the load.

The voltage on the high-rail supplies is variable and is controlled by the user volume setting. The relationship between user volume and high-rail voltage also depends on the system supply voltage. See Table 5 below.

In standby mode and active-mute mode the high-rail boost converter will always be off.

For a 5V system supply voltage, at volumes 23 and below the high-rail boost converter will also always be off. In active mode and at volumes 24 and above the high rail boost converter will always be on and will generate a high-rail voltage as listed in column seven of Table 5 below.

For a 3.7V system supply voltage, at volumes 25 and below the high-rail boost converter will also always be off. In active mode and at volumes 26 and above the high rail boost converter will always be on and will generate a high-rail voltage as listed in column five of Table 5 below.

For a 0.8V to 1.8V system supply voltage, the volume threshold where the boost converter is active varies depending on the actual system supply voltage. In active mode and at volumes 31 and above the high rail boost converter will always be on and will generate a high-rail voltage as listed in column three of Table 5 below. In active mode and at volumes 26 to 30, the high-rail boost converter may be active depending on the low-rail battery voltage (as reported in register [0x96\[5:0\]](#)). For volumes 26 to 30, if the low-rail battery voltage is below the threshold listed in column two of Table 5 then the high-rail boost converter will be on. If the low-rail battery voltage is above the threshold then the high-rail boost converter will be off.

System supply: 1.5V (0.8V to 1.8V)			System supply: 3.7V		System Supply: 5V	
Volume #	Low rail voltage High-rail active threshold (V)	High-rail voltage (V)	Volume #	High-rail voltage (V)	Volume #	High-rail voltage (V)
44		20.7	39 *	20.7	37	20.7
43		17.4	38	17.4	36	17.4
42		14.7	37	14.7	35	14.7
41		12.4	36	12.4	34	12.4
40		10.4	35	10.4	33	10.4
39		8.73	34	8.73	32	8.73
38		7.35	33	7.35	31	7.35
37		6.18	32	6.18	30	7.35
36		5.20	31	5.20	29	7.35
35		4.38	30	5.20	28	7.35
34		3.68	29	5.20	27	7.35
33		3.68	28	5.20	26	7.35
32		3.68	27	5.20	25	7.35
31	1.99	3.68	26	5.20	24	7.35
30	1.67	3.68	25 – 0	Off	23 – 0	Off
29	1.41	3.68				
28	1.18	3.68				
27	1.00	3.68				
26	0.84	3.68				
25	0.71	3.68				
24 – 0	n/a	Off				

Table 5: High-rail voltage, verses user volume setting

4.6 CONTROL INTERFACES

The AS2002 may be controlled via a two wire serial interface, a set of input pins, or a combination of both.

4.6.1 RESET, SOFTWARE-RESET, USER-RESET

The AS2002 has a dedicated active low, external reset input pin:

- nRST, pin 19

It is always recommended to perform a reset after power-on to ensure the device is in a known state after power up. This can be easily achieved with a simple external resistor-capacitor network on the nRST pin, see Figure 13.

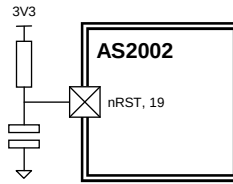


Figure 13: External Power-On-Reset circuit

The device can also be subsequently reset through register [0x95\[0\]](#), or via the STDBY pin (see section 4.6.3).

After a reset the device will copy any programmed OTP values in to their corresponding registers (see section 7) before entering either standby or active mode (depending on the value in register [0x01\[6\]](#)). Registers should not be written to (via the TWI bus) until this OTP copy procedure has been completed. Any TWI reads or writes performed during this time will not be acknowledged.

Holding the nRST pin low may also be used to hold the AS2002 in a low power 'sleep' mode.

4.6.2 VOLUME CONTROL PINS

The BTNUP and BTNDN input pins can be used to implement a user volume control:

- BTNUP, pin 14: increment volume
- BTNDN, pin 15: decrement volume

Two user interface types are supported and may be configured through register [0x04\[7\]](#):

- Push buttons
- Rotary encoder

When configured for push button control then BTNUP and BTNDN are active low; so should be normally held high and then pulled low when the user presses a button. A momentary press of a button will increment/decrement the volume level by 1 step. If the button is held down, then after a delay the volume will automatically ramp up/down until the maximum/zero volume level is reached. Both the hold-off delay time and the ramp rate are configurable through registers [0x05\[7:0\]](#) and [0x06\[6:0\]](#) respectively. Switch de-bounce circuits are built in to the device.

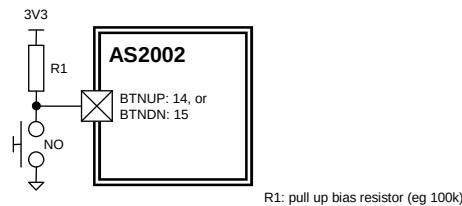


Figure 14: Volume control pin external circuit, push button control

When configured for rotary encoder control then an incremental rotary encoder with a 2-bit, quadrature gray code output may be connected to the BTNUP and BTNDN pins. BTNUP should lead BTNDN to increment the volume. The number of rotary encoder steps required to effect 1 volume step may be set through register [0x04\[6:0\]](#).

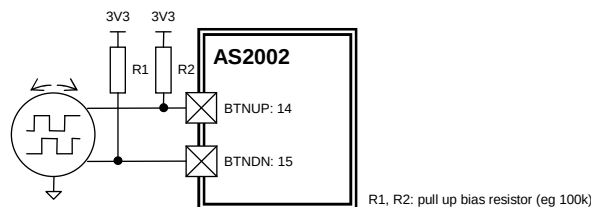


Figure 15: Volume control pins external circuit, rotary encoder control

De-bounce logic is also used on the rotary encoder inputs. The BTNUP and BTNDN pins are sampled every $6/\text{SystemClockMHz}$ ms. If the pin values are the same for 5 contiguous samples then the device considers the rotary encoder to be in a valid state. If the new valid state is one state away from the previous valid state then the volume is incremented, or decremented, accordingly. (Although note that the number of rotary encoder steps required to effect 1 volume step may be greater than 1, as set through register [0x04\[6:0\]](#).)

To ensure correct operation, the rate of state change should be less than $\text{SystemClockMHz} / (0.006 \times 6)$ Hz.

If the BTNUP and BTNDN pins are not required they should both be tied to 3.3V.

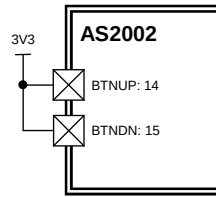


Figure 16: Volume control pins external circuit, pins unused

Note that the volume may also be controlled directly through register [0x03\[7:0\]](#).

4.6.3 STATE CONTROL PINS

The STBY, BASSB, SWIDE and MUTE pins can be used to implement control over the standby/active mode and bass-boost, stereo-wide & mute functions of the device.

- STDBY, pin 32: control active/standby state. The STBY pin can also be used to perform a device reset.
- BASSB, pin 31: control bass-boost on/off state.
- SWIDE, pin 30: control stereo-wide on/off state.
- MUTE, pin 29: control mute/un-muted state

Note that the mute control is a soft mute. See section 4.5.6.1 for details.

The state control pins are nominally input pins.

However, during reset and for up to $217.6 / \text{InternalOscillatorClockMHz} + 48 / \text{SystemClockMHz}$ ms afterwards, the state control pins are configured as output pins, driving a high level.

Two modes of pin control are supported and may be individually configured through register [0x00\[3:0\]](#):

- Edge-sensitive: a low-to-high edge transition on the pin will toggle the state
- Level-sensitive: the low or high state of the pin will set the state

When configured as level-sensitive the pin(s) may be driven directly; for example by a microprocessor GPIO. A high level on the pin will activate the respective feature and a low level on the pin will deactivate the feature.

Figure 17 shows a recommended application circuit for level-sensitive control. The series resistor ensures there is no conflict during a reset event. The pull down resistor provides bias to a default (feature disabled) state.

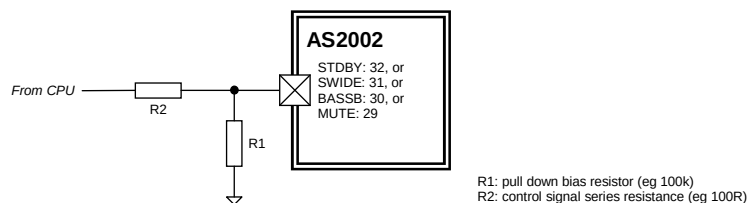


Figure 17: State control pin external circuit, level-sensitive control

When configured as edge-sensitive the pin(s) may be connected to user push buttons. The pin(s) should be normally pulled low and be pulled high when the user presses a button.

When configured as edge-sensitive the pin(s) may also be used to drive an indicator LED. If the state of the corresponding function is active (i.e. active-mode, stereo-wide-on, bass-boost-on or muted), the pin periodically changes from an input to an output driving a high level. A LED connected between the pin and GND will therefore be illuminated when the pin is an output. Since the pin is also periodically an input, and the user is still able to press the button to interact with the device.

Figure 18 shows a recommended application circuit for edge-sensitive control; with and without an indicator LED. The pull down resistor provides bias to a default pin value. When pressed, the switch pulls the pin high.

Note that during a reset the pin is a high level output, so the LED will be illuminated.

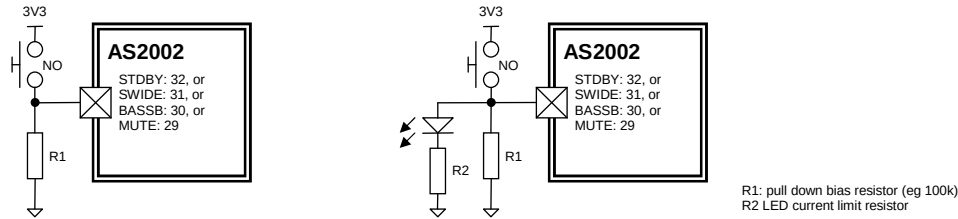


Figure 18: State control pin external circuit, edge-sensitive control

When configured as edge-sensitive, and a function is activated, the pin toggles between an:

- Input: for $0.032/\text{SystemClockMHz}$ ms
- Output: for $47.968/\text{SystemClockMHz}$ ms

After the state has been active for $10752/\text{SystemClockMHz}$ ms, then the pin toggles between an:

- Input: for $1536.032/\text{SystemClockMHz}$ ms
- Output: for $47.968/\text{SystemClockMHz}$ ms

Visually this behaviour appears to the user that the LED is illuminated constantly for a few seconds when the function is activated, followed by brief flashes to remind the user that the function is still active.

In both level- and edge-sensitive modes the pins are simultaneously sampled every $48/\text{SystemClockMHz}$ ms. If two consecutive pin samples are identical the value is accepted. This provides a switch de-bounce mechanism.

When the STDBY pin is configured as edge-sensitive and held high for $12288/\text{SystemClockMHz}$ ms (256 consecutive pin samples), then a device reset is performed (see section 4.6.1 for more details).

If a state control pin is not used then the pin should be pulled to GND via a resistor. (Since the pins are a high level output during reset, the unused pin should not be directly connected to GND.)

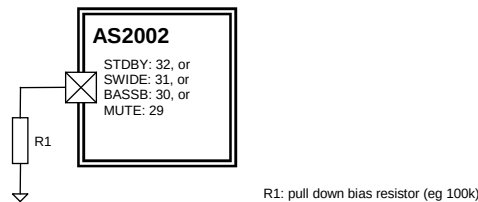


Figure 19: State control pin external circuit, pin control not required

If multiple state control pins are not required, then they may be connected together and communally pulled to GND. (Again, since the pins are high level outputs during reset, unused pins should not be connected directly to GND.)

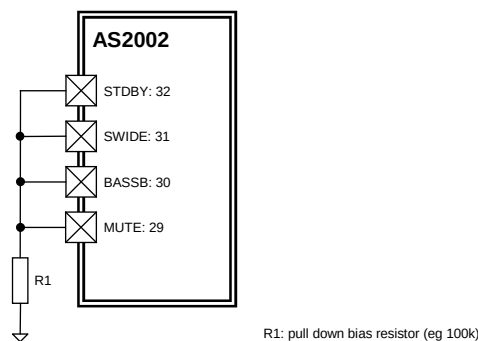


Figure 20: State control pins external circuit, no pin control required

When using the circuit in Figure 20, it is recommended that all the pins be configured for the same type of control; either level- or edge-sensitive control.

Note that in all cases the pin(s) may be overridden and the state of the feature controlled directly through register [0x01\[7:0\]](#).

4.6.4 TWO WIRE INTERFACE

The AS2002 supports software control via a TWI (two wire interface)² on pins:

- SCL, pin 16: TWI clock
- SDA, pin 18: TWI data

The SCL and SDA pins are open drain and connect to a TWI bus which allows one or more system hosts (or masters) to control one or more slaves attached to the same TWI bus.

If the TWI is not required, both SCL and SDA should be tied (or pulled) to 3.3V.

Each device on the TWI bus requires a unique device address. This 8bit address consists of a 7bit device identifier and a 1bit read/write action.

The AS2002 device address is defined by register [0x12\[5:0\]](#) and an external pin.

- AD0, pin 55: LSB of device address

The AS2002 will also respond to an address consisting of the AD0 pin value repeated 7 times.

	DeviceAdd. Bit7	DeviceAdd. Bit6	DeviceAdd. Bit5	DeviceAdd. Bit4	DeviceAdd. Bit3	DeviceAdd. Bit2	DeviceAdd. Bit1	DeviceAdd. Bit0
AS2002 TWI address:	0x12[5]	0x12[4]	0x12[3]	0x12[2]	0x12[1]	0x12[0]	AD0	Read/Write
	AD0	AD0	AD0	AD0	AD0	AD0	AD0	Read/Write

Table 6: TWI device address

The AD0 pin can also be used to control signal routing in the audio DSP block (see sections 5.1 and 5.5.4). Note that if this additional AD0 functionality is used, then the TWI address will also change as the AD0 pin is toggled.

The AS2002 can act as both a slave and a master.

4.6.4.1 Slave mode

The AS2002 TWI slave mode allows an external master to write-to and read-from internal registers.

A master indicates the start of a data transfer with a high to low transition on SCK whilst SDA remains high. The master then transfers the 7bit device address, followed by an eighth Rd/Wr bit (1 for a read operation, 0 for a write operation).

If the transferred device address matches the AS2002 device address, the AS2002 responds by pulling SDA low until the next low to high SCK clock edge as an acknowledgment.

If Rd/Wr is set to 0 (indicating a write operation) the master shall then transfer one, or more, bytes of information to the AS2002. The first byte transferred indicates the address of an internal register. The second byte indicates data to be loaded in to that register. The AS2002 supports auto-register-address-incrementing, thus any subsequent bytes transferred will be loaded in to successive register addresses. The auto-register-address-incrementing will wrap back to register address 0x00 after register address 0xFF.

After each byte received the AS2002 will pull SDA low to acknowledge successful receipt of the byte. After all the required bytes have been transferred, the master shall stop the data transfer with a low to high transition on SCK whilst SDA remains high.

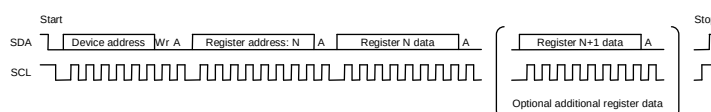
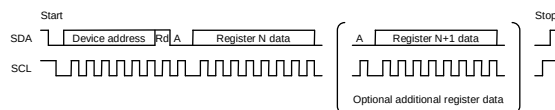


Figure 21: TWI write

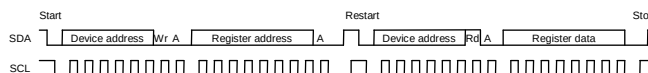
If Rd/Wr is set to 1 (indicating a read operation) then after acknowledging the device address and read bit, the AS2002 will respond with the current value of the last register to be addressed. If this is the first read operation after a reset the contents of register 0x00 will be returned.

If the master acknowledges this data byte, then the AS2002 will respond with the current value of the next register address. (The auto-register-address-incrementing will wrap back to register address 0x00 after register address 0xFF). This will continue until the master does not acknowledge, but instead issues a stop condition, which will terminate the read operation.

² The Audium TWI is compatible with the 100kHz I²C protocol

**Figure 22: TWI read**

A complete register read operation will typically consist of both a write (to set the register address) followed by a read (to actually read the register value).

**Figure 23: TWI write-read**

4.6.4.2 Master mode

The AS2002 TWI can also act as a master, allowing the device to control an attached slave device.

On the transition from standby mode to active mode the device can send a series of commands to an attached slave device; referred to as the 'TWI master preamble'. (For example: this might be used to power-up an analogue to digital converter.)

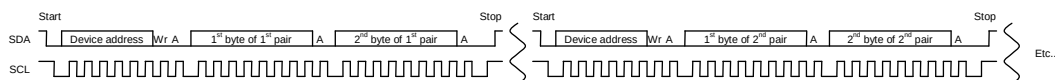
Similarly, on the transition from active mode back to standby mode the device can send a separate series of commands to the same attached slave device; referred to as the 'TWI master postamble'. (For example: this might be used to power-down an analogue to digital converter.)

The 7bit TWI device address of the target slave device is held in register [0x35\[6:0\]](#). (The AS2002 automatically appends the extra write bit.)

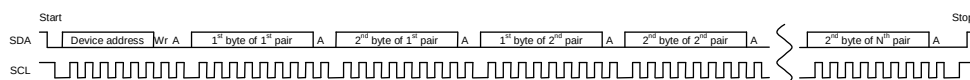
The data to be transferred is stored as a series of byte pairs in registers [0x13](#) to [0x32](#). Preamble data (sent on a standby to active transition) is stored first (starting in register [0x13](#)), followed by postamble data (sent on an active to standby transition).

The number of preamble byte pairs is stored in register [0x33\[4:0\]](#), and the number of postamble byte pairs is stored in register [0x34\[4:0\]](#). (The sum of these two values should therefore not exceed the total byte pair storage size of 16pairs.) If the number of byte pairs to transfer is 0, then no action is performed on that respective mode transition.

Register [0x35\[7\]](#) defines how the data is transferred. When [0x35\[7\]](#) is set to 0 each byte pair associated with a mode transition is transferred as a separate transaction on the TWI bus:

**Figure 24: TWI master 'byte-pairs' write**

When [0x35\[7\]](#) is set to 1 all the byte pairs associated with a mode transition are transferred as a single transaction on the TWI bus.

**Figure 25: TWI master 'all at once' write**

Note that when operating in TWI master mode, the AS2002 assumes that it is the only master on the TWI bus. The AS2002 does not check if the bus is available, performs no multi-master arbitration and does not check for an acknowledge from the slave device.

Enabling the TWI master mode and then using an external master to control the AS2002 will result in conflicts on the TWI bus if the external master writes to the AS2002 to toggle between active and standby-modes.

If an external master is used then master mode should be disabled. (Set registers [0x33\[4:0\]](#) and [0x34\[4:0\]](#) to 0x00.)

4.7 CLOCKING OPTIONS

The AS2002 requires a clock to operate and has several clocking options:

1. Internal oscillator
2. Crystal oscillator; driving an external crystal

3. External clock input
4. External full system clock input

The first three options all use the internal oscillator (together with the crystal oscillator and/or external clock input). The fourth method does not use the internal oscillator; instead the AS2002 is entirely clocked by an external clock.

For optimal performance, operation from an external full system clock is the only recommended clocking method. However, for completeness, all modes are described in this chapter.

A simplified clocking diagram is shown below.

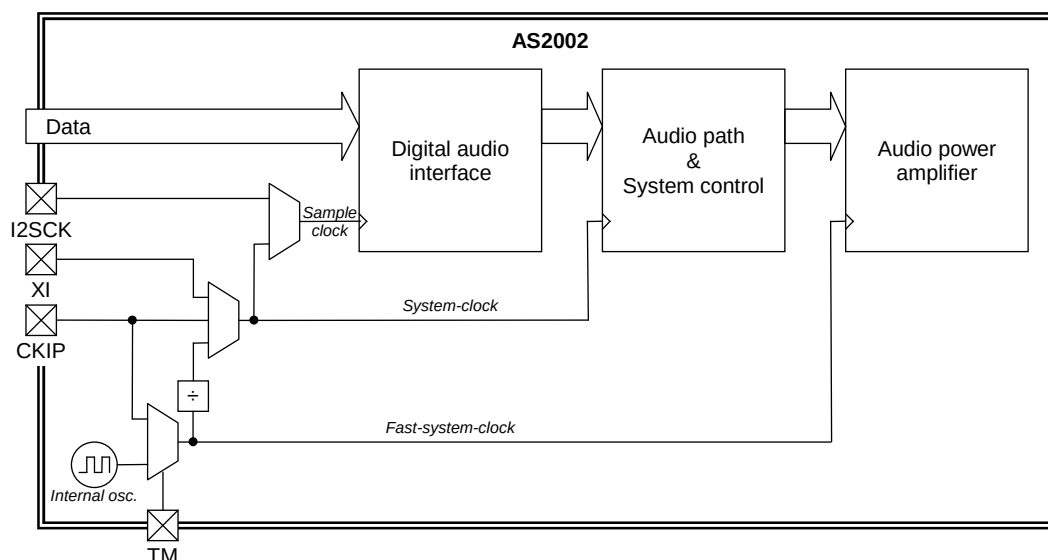


Figure 26: Clocking domains

Internally the device contains three clock domains:

- Digital audio interface
- System control and audio path
- Power amplifier control

When configured as a slave-receiver the digital audio interface is clocked by the I2SCK pin. When configured as a master-receiver the digital audio interface is clocked by the system-clock. The audio path and system control sections are clocked by the system-clock. The power amplifier sections are clocked by the fast-system-clock.

The system-clock may be derived from the internal oscillator, the crystal oscillator or the external clock input. The fast-system-clock may be derived from the internal oscillator, or the external clock input (recommended).

A clock output is also available from the AS2002, which may be sourced from any of the above options.

A more detailed block diagram of the device clocking options is shown below.

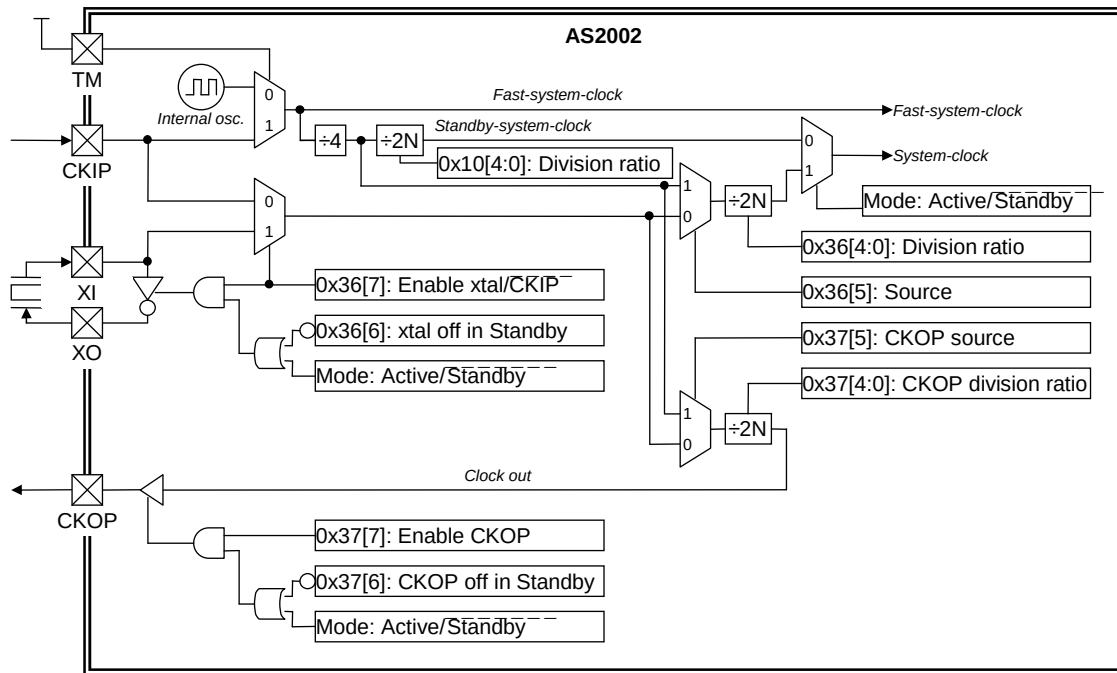


Figure 27: Clock generation

4.7.1 INTERNAL OSCILLATOR

This clocking method is not recommended. Use external full system clock method instead (see section 4.7.4).

The AS2002 incorporates a low power, high frequency oscillator which generates the fast-system-clock. This oscillator is completely internal to the device, requires no external components or pins to operate and is always operational.

In active mode a divided down version of the output from this oscillator may be used as the system-clock to clock the rest of the device.

To reduce power consumption in standby mode the device always automatically switches to the standby-system-clock, a further divided down version of the output from this oscillator.

Since the internal oscillator uses no external pins, using the internal oscillator is the most power efficient method of clocking the device.

The frequency of the internal oscillator will vary between device to device, and also over operating conditions. The device has been designed to accommodate this variation and will operate normally with no degradation in performance or fidelity.

However if an associated external device (for example an analogue to digital converter) requires a more accurate clock for optimal operation, then the AS2002 provides several alternative clocking options.

4.7.2 CRYSTAL OSCILLATOR

This clocking method is not recommended. Use external full system clock method instead (see section 4.7.4).

The AS2002 includes a crystal oscillator block with two external pins:

- XI, pin 22: crystal oscillator input
- XO, pin 23: crystal oscillator output

The inclusion of a crystal oscillator provides the flexibility for the device to clock external devices which require a clock with the stability and accuracy of a crystal, but perhaps do not have a built-in crystal oscillator.

Register [0x36\[7\]](#) enables the crystal oscillator. Note that the crystal oscillator and the external clock input are mutually exclusive. Enabling the crystal oscillator will therefore prevent the external clock input from being used.

When enabled, the crystal oscillator will always operate when the device is in active mode. Register [0x36\[6\]](#) defines if the crystal oscillator will also operate when the device is in standby mode.

A schematic of the crystal oscillator is shown below.

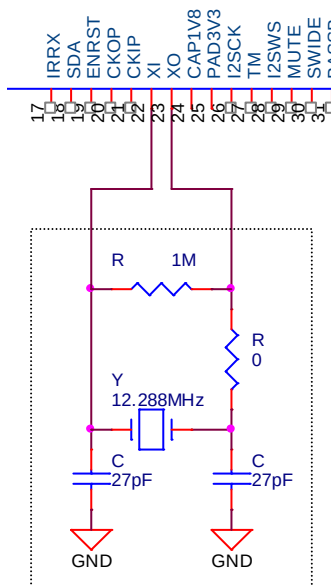


Figure 28: Crystal oscillator schematic

A 1Mohm feedback resistor is required across the crystal terminals to ensure successful start up. The series damping resistor may be omitted, or included to reduce power. If inserted it should not be too large or the oscillator could fail to operate.

A crystal with the following specification may be attached to the XI and XO pins:

Parameter	Specification			
	Min	Recommended	Max	Unit
Type	-	Parallel resonant	-	-
Cut	-	Fundamental	-	-
Frequency	2^3	$\geq \text{SampleRate} \times 32$	30	MHz
Load	-	20 (for 2 – 6MHz) 16 (for 6 – 10MHz) 12 (for 10 – 20MHz) 8 (for 20 – 30MHz)	-	pf
ESR	-	-	1000 (for 2 – 6MHz) 160 (for 6 – 10MHz) 90 (for 10 – 20MHz) 40 (for 20 – 30MHz)	Ohms

Table 7: Crystal specification

Provided the rules on the minimum, maximum and recommended frequency (as per Table 7 above) are met, then the actual clock frequency is not important. The only reason to use the crystal oscillator would be to provide a crystal derived clock to an external device. The tolerance requirements would therefore be defined by that external device. For this reason no specifications for frequency tolerance are given.

If the internal crystal oscillator is not required, connect XI to GND and leave XO unconnected.

4.7.3 EXTERNAL CLOCK INPUT

This clocking method is not recommended. Use external full system clock method instead (see section 4.7.4).

It is also possible to provide an external clock signal in to the device:

- CKIP, pin 21: external clock input

Register [0x36\[7\]](#) selects this input. Note that this input and the crystal oscillator are mutually exclusive. Enabling the external clock input will therefore disable the crystal oscillator.

If the external clock input is not required, connect CKIP to GND.

³ This is the minimum frequency the crystal oscillator will operate at.

If the crystal oscillator is used to derive the system-clock, then the crystal frequency and system clock division ratio should be selected such that the system-clock is always greater than, or equal to, 32x the I²S sample-rate.

4.7.4 EXTERNAL FULL SYSTEM CLOCK INPUT

This clocking method is the only recommended clocking method.

It is further possible to provide an external clock signal in place of the internal oscillator:

- CKIP, pin 21: external full system clock input
- TM, pin 27: test mode pin, tie to PAD3V3 (pin 25) to enable the external full system clock input

The external full system clock should be synchronised to the incoming I²S stream at exactly 512 times the sample rate clock, or an integer multiple thereof. For example: a 24.576MHz external clock may be used with a 48kHz I²S audio signal.

4.7.5 CLOCK OUTPUT

The AS2002 has a clock output pin:

- CKOP, pin 20: clock output

Register [0x37\[7\]](#) enables the clock output. When enabled, the clock output will always operate when the device is in active mode. Register [0x37\[6\]](#) defines if the clock output will also operate when the device is in standby mode.

The source of the clock output may be selected through register [0x37\[5\]](#) and register [0x36\[7\]](#).

The division-ratio between the selected clock source and the clock output can be specified through register [0x37\[4:0\]](#).

4.7.6 CLOCKING STRATEGY

The only recommended clocking method is external full system clock input (see section 4.7.4).

In standby mode the device always uses standby-system-clock, which is derived from the external full system clock input. This ensures a clock source is always present and reduces power consumption. (When in standby mode only the system control section is active, so a slower clock frequency may be used thereby reducing power consumption.

The division ratio between the external full system clock input and the standby-system-clock may be specified in register [0x10\[4:0\]](#). To ensure the TWI can operate correctly (at 100kHz) the standby-system-clock must be at least 1MHz. If this division ratio is too large, or the external full system clock input too slow, then it will be necessary to use a proportionally slower TWI clock speed (at least until a smaller division ratio can be written).

In active mode the source of the system-clock may be selected from: the full system clock input, the internal oscillator, the crystal oscillator or the external clock through register [0x36\[5\]](#) and register [0x36\[7\]](#).

For optimal performance it is always recommended to use the internal oscillator as the source of the system-clock.

The division-ratio between the selected clock source and the system-clock can be specified through register [0x36\[4:0\]](#).

A division-ratio should be chosen to always ensure that the system-clock frequency is greater than or equal to 32 times the frequency of the word-select clock present at the digital audio interface.

5 AUDIO DIGITAL SIGNAL PROCESSING

The audio DSP (digital signal processing) block provides a highly configurable set of audio DSP functions, as shown in Figure 29 below.

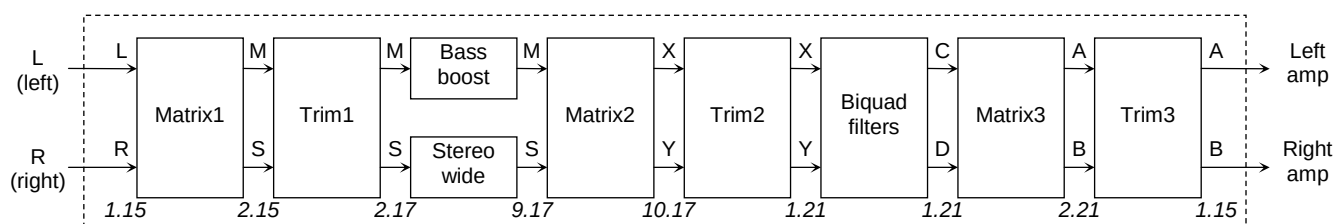


Figure 29: Audio DSP functional blocks

The input to the audio DSP is always left and right channel audio data, and the single output from the audio DSP is always fed to the left and right audio power amplifiers.

Between the input and output of the audio DSP the signal can be routed and processed in many ways, depending on the configuration of the individual blocks that make up the audio DSP. Each of the letters in Figure 29 represent a potentially different audio signal. (If the letters are the same at the input and output of a block, then that block cannot change the signal routing.)

Fixed point signal precisions are shown below each signal path of Figure 29; annotated as $\alpha.\beta$. α represents the number of bits above the decimal point (including the sign bit), and β represents the number of bits below the decimal point.

5.1 MATRIX 1, 2 & 3 AND AUDIO MODES

Each matrix takes two input audio signals and allows them to be passed through untouched, re-routed or combined together as sum and difference signals. Creating sum and difference signals allows one to move from the conventional stereo left and right (LR) domain to the mid and side (MS) domain. No information is lost during this transformation.

- $M = L + R$
- $S = L - R$

One can then process the audio information in the MS domain. Performing certain functions (for example stereo-wide and bass-boost) in the MS domain provides higher levels of computational efficiency than the equivalent operation in the LR domain. (This computational efficiency translates to lower device power consumption.)

Repeating this process by taking the sum and difference of the MS domain signal returns the data to the LR domain. (Again, no information is lost during this transformation.)

- $L = (M + S) / 2$
- $R = (M - S) / 2$

Together, Matrix1, 2 & 3 therefore allow for several different audio routing configurations and processing options, or 'audio modes'. For example: stereo, mono-left-only, mono-right-only or mono-left-plus-right.

The audio mode is set through register [0x3B\[4:0\]](#) and a list of all possible modes is shown in Table 8 below. Table 8 is intended primarily as a reference, with the key audio modes discussed below in more detail.

For standard stereo operation, it is suggested to use audio mode 24.

Mode 0x3B[4:0]	AD0 Pin ⁴	Matrix1		Matrix2		Matrix3		Equivalent output ⁵
		M	S	X	Y	A	B	
Single-mono modes								
In these modes only the left amplifier is active. The right amplifier is muted and its output pins are internally connected to GND.								
0 (0x00)	0 1	L R	-	M	-	C	-	A = L A = R
1 (0x01)	0 1	R L	-	M	-	C	-	A = R A = L
2 (0x02)	0 1	L + R	L - R	M + S M - S	-	C	-	A = 2L A = 2R
3 (0x03)	0 1	L + R	L - R	M - S M + S	-	C	-	A = 2R A = 2L
4 (0x04)	0 1	L + R	L - R	M	S	C + D C - D	-	A = 2L A = 2R
5 (0x05)	0 1	L + R	L - R	M	S	C - D C + D	-	A = 2R A = 2L
6 (0x06)	0 1	L + R	L - R	M S	-	C	-	A = L + R A = L - R
7 (0x07)	0 1	L + R	L - R	S M	-	C	-	A = L - R A = L + R
Dual-mono modes								
In these modes both the left and right audio amplifiers are active, and produce identical outputs.								
8 (0x08)	0 1	L R	-	M	-	C	C	A = B = L A = B = R
9 (0x09)	0 1	R L	-	M	-	C	C	A = B = R A = B = L
10 (0x0A)	0 1	L + R	L - R	M + S M - S	-	C	C	A = B = 2L A = B = 2R
11 (0x0B)	0 1	L + R	L - R	M - S M + S	-	C	C	A = B = 2R A = B = 2L
12 (0x0C)	0 1	L + R	L - R	M	S	C + D C - D	C + D C - D	A = B = 2L A = B = 2R
13 (0x0D)	0 1	L + R	L - R	M	S	C - D C + D	C - D C + D	A = B = 2R A = B = 2L
14 (0x0E)	0 1	L + R	L - R	M S	-	C	C	A = B = L + R A = B = L - R
15 (0x0F)	0 1	L + R	L - R	S M	-	C	C	A = B = L - R A = B = L + R
Active crossover modes								
In these modes both the left and right audio amplifiers are active, and produce independent outputs.								
16 (0x10)	0 1	L R	-	M	-	C	D	A = B = L A = B = R
17 (0x11)	0 1	R L	-	M	-	C	D	A = B = R A = B = L
18 (0x12)	0 1	L + R	L - R	M + S M - S	-	C	D	A = B = 2L A = B = 2R
19 (0x13)	0 1	L + R	L - R	M - S M + S	-	C	D	A = B = 2R A = B = 2L
20 (0x14)	0 1	L R	-	M	-	C + D	C - D	A = B = L A = B = R
21 (0x15)	0 1	R L	-	M	-	C + D	C - D	A = B = R A = B = L
22 (0x16)	0 1	L + R	L - R	M S	-	C	D	A = B = L + R A = B = L - R
23 (0x17)	0 1	L + R	L - R	S M	-	C	D	A = B = L - R A = B = L + R
Stereo modes								
In these modes both the left and right audio amplifiers are active, and produce independent outputs.								
24 (0x18)	-	L + R	L - R	M	S	C + D	C - D	A = 2L, B = 2R
25 (0x19)	-	L + R	L - R	M	S	C	D	A = L + R, B = L - R
26 (0x1A)	-	L + R	L - R	M + S	M - S	C	D	A = 2L, B = 2R
27 (0x1B)	-	L + R	L - R	M + S	M - S	C + D	C - D	A = 2(L + R), B = 2(L - R)
28 (0x1C)	-	L + R	L - R	M	S	C + D	C - D	A = 2L, B = 2R
29 (0x1D)	-	L + R	L - R	M	S	C	D	A = L + R, B = L - R
30 (0x1E)	-	L + R	L - R	M	S	C + D	C - D	A = 2L, B = 2R
31 (0x1F)	-	L + R	L - R	M + S	M - S	C + D	C - D	A = 2(L + R), B = 2(L - R)

Table 8: Audio DSP modes reference

⁴ The AD0 pin defines the TWI device address (section 4.6.4), and can also be used to control the audio mode.⁵ The Equivalent Output is the output that would be seen if stereo-wide, bass-boost and biquad filters are all disabled, and all trim stages were set to unity gain.

The audio modes are discussed in more detail below.

5.1.1 STEREO MODES

The stereo modes provide a stereo output in a conventional LR (left and right) format.

5.1.1.1 Normal Left-Right Stereo

Audio mode 24 is the default audio mode and provides a 'normal LR stereo' output. Matrix1 converts the LR input signal in to the MS (mid and side) domain. Matrix2 has no effect on the signal data and matrix3 converts from the MS domain back in to the LR domain.

The bass-boost processes the mid channel data only and stereo-wide the side channel data only. Biquad processing is also done in the MS domain. For identical left and right output speakers, this gives flexibility to perform frequency selective filtering which affects the stereo image.

Audio mode 28 is a variant on audio mode 24 in which the stereo-wide block is disabled and the stereo-wide control (see section 4.6.3) is instead used to switch biquad register sets. (See section 5.5.4 for more details.)

Mode 30 is a similar variant on mode 24 but with the AD0 pin used to switch biquad register sets.

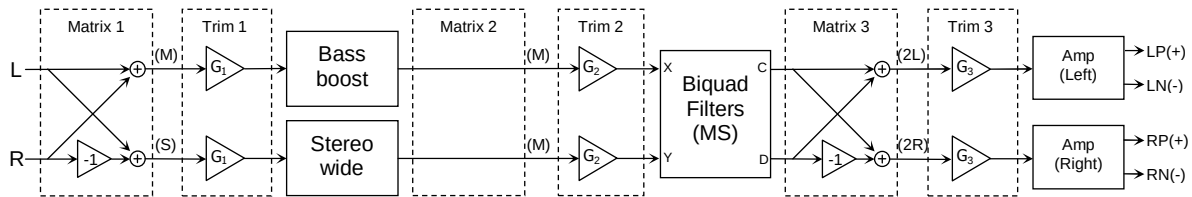


Figure 30: Normal LR Stereo - Audio Mode: 24, (28 & 30)

5.1.1.2 Asymmetric Stereo

In audio mode 26 (asymmetric LR stereo), matrix3 has no effect and matrix2 converts from the MS domain back to the LR domain. Biquad processing is therefore done in the LR domain. In a system where left and right speaker driver units have different frequency responses (for example only one unit having any bass drive capability), this mode can be used to perform different equalisation for the two outputs.

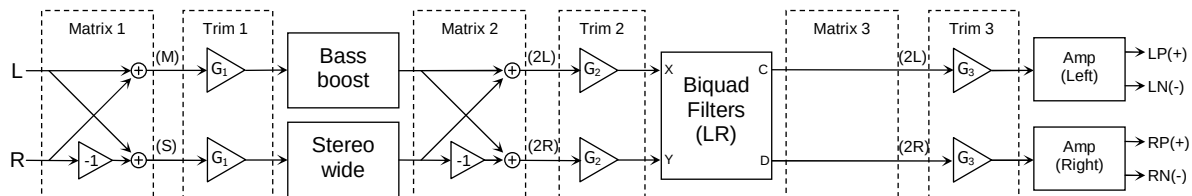


Figure 31: Asymmetric LR Stereo - Audio Mode 26

5.1.2 ACTIVE CROSSOVER MODES

Audio modes 16 and 17 can be used to implement an active crossover circuit. In these modes the biquad filters implement the required low pass and high pass filtering to separate a mono signal in to high and low frequency signals suitable for tweeter and woofer speaker units. Input channel selection is determined in exactly the same manner as for mono modes 8 and 9.

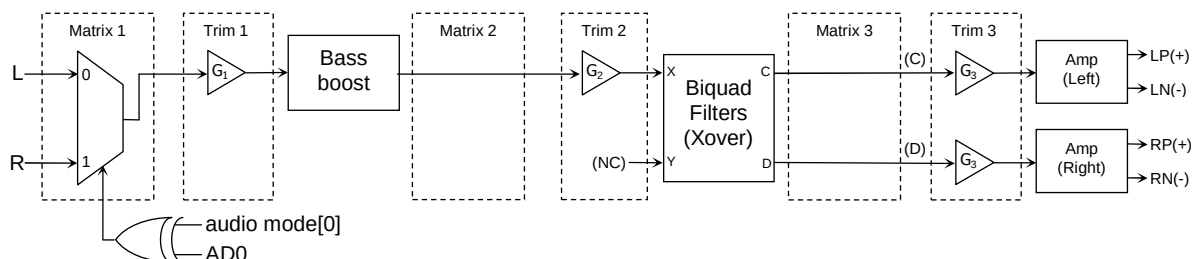


Figure 32: Simple Mono Crossover - Audio Modes 16 & 17

Similarly, audio modes 18 and 19, 'stereo to mono crossover', allow a stereo system with active crossover to be created from two Audium devices.

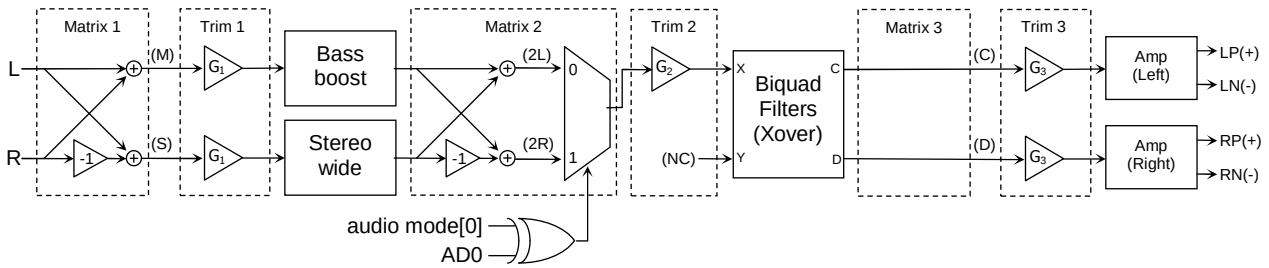


Figure 33: Stereo to Mono Crossover - Audio Modes 18 & 19

5.1.3 SINGLE- AND DUAL-MONO MODES

The single-mono and dual-mono modes provide different methods of creating a mono signal from the stereo input.

- In single-mono modes only the left amplifier is active. The right amplifier is muted and its output pins are internally connected to GND.
- In dual-mono modes both the left and right audio amplifiers are active, and produce identical outputs.

5.1.3.1 Simple Mono Select

In 'simple mono select' modes (audio modes 0, 1, 8 & 9) matrix1 selects the mono signal from either the left or right input signal. The selection is controlled by the exclusive-OR-ed combination of the LSB of the audio mode (register [0x3B\[0\]](#)) and the AD0 pin (see Figure 34).

Note that in 'simple mono select' modes, the system gain will be half that of the other modes as there is no channel summing (see Table 8), so trim2 gain should be adjusted accordingly.

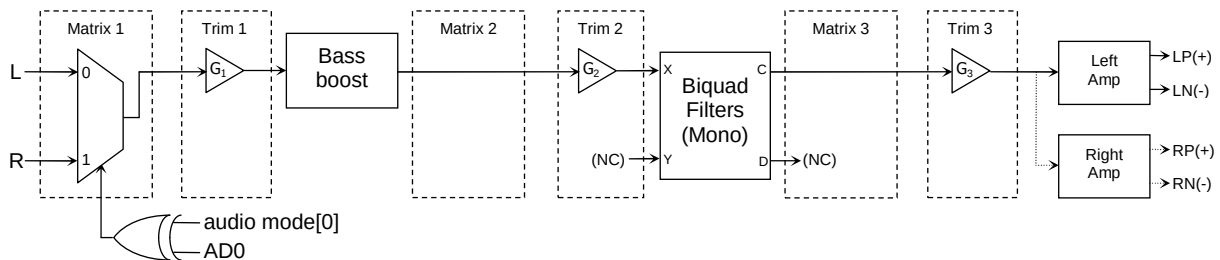


Figure 34: Simple Mono Select - audio modes 8 & 9

5.1.3.2 Mono Select

In audio modes 2, 3, 10 and 11, 'mono select', matrix2 selects between the left or right channel.

For example, two devices, both configured in audio mode 10, could be used to implement a stereo amplifier. Pin AD0 could then be used to select the left (set AD0 low) or the right (set AD0 high) input signal. Alternatively, with pin AD0 held low on both devices, one device could be configured for audio mode 10 (left channel) and the other for audio mode 11 (right channel). If using two devices to build a stereo amplifier, these modes are preferable to modes 8 and 9 as they enable the full stereo processing involved in the bass-boost and stereo-wide functions.

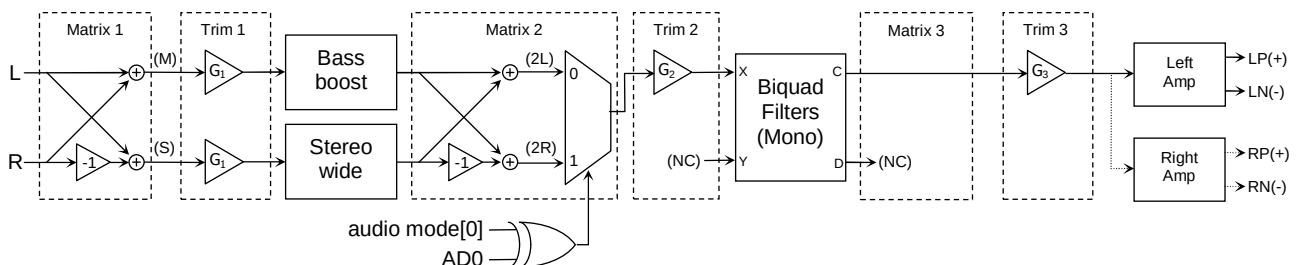


Figure 35: Mono Select - audio modes 10 & 11

5.1.3.3 Mono Select (MS filtering)

In audio modes 4, 5, 12 and 13, 'mono select (MS filtering)', matrix3 selects between the left and right channel.

These modes differ from modes 2, 3, 10 and 11 in that the biquad filters process the signal whilst it is still in the MS (mid and side) domain.

Note that in these modes the stereo-wide block is disabled and the stereo-wide control signal is instead routed to the biquad filters, where it is exclusively-OR-ed with the most significant bit of the biquad filters set switching control register. See section 5.5.4.

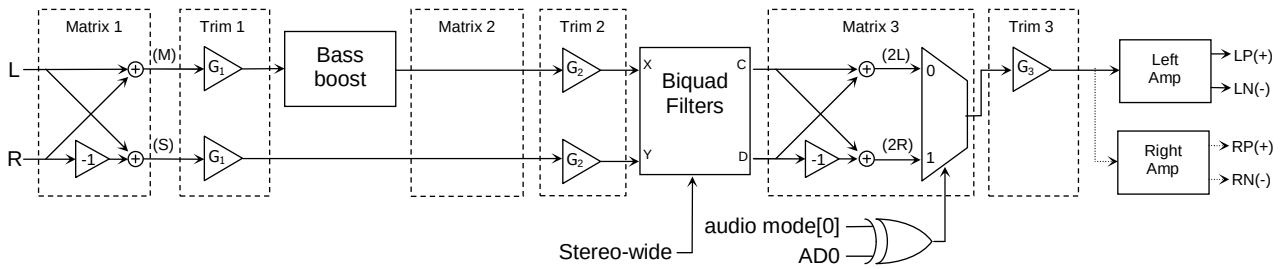


Figure 36: Mono Select (MS filtering) - audio modes 12 & 13

5.1.3.4 Stereo to Mono Combine

Audio modes 6, 7, 14 and 15 combine the left and right audio data together to generate a mono channel.

Matrix1 generates mid, or sum ($M = L + R$) and side, or difference ($S = L - R$) signals. Matrix2 selects either the 'mono sum' (audio modes 6 and 14) or the 'mono difference' (audio modes 7 and 15) signal.

For example, audio mode 14, 'mono sum' could be used to generate a common channel; such as a centre channel, or where there is only one speaker in a system.

Note that in these modes the AD0 signal is also routed to the biquad filters, where it is exclusively-OR-ed with the most significant bit of the biquad filters set switching control register. See section 5.5.4.

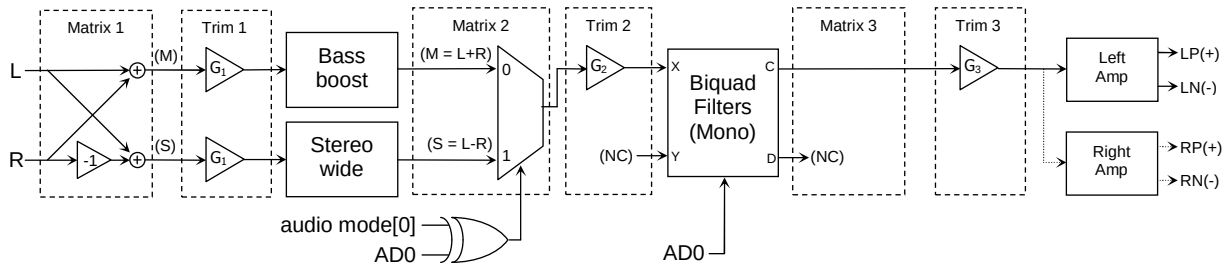


Figure 37: Stereo to Mono Combine - audio modes 14 & 15

5.2 TRIM1, 2 & 3

Trim1, Trim2 and Trim3 each apply a common gain to both channels. This allows dynamic headroom to be maximized without unduly raising the noise floor for the chosen settings of matrix1, 2, & 3, the bass-boost, stereo-wide and biquad filter blocks.

Where output quantization is required, dither is added to effectively lower the audible noise level.

When setting the gain at each trim stage, several factors should be considered:

- Fixed point precisions through the pipeline (see annotations in Figure 29)
- Any audio mode dependent gains (see Table 8)
- Gain across the full bandwidth for the chosen settings of the bass extender or image widener
- The overall transfer function of the biquad filter coefficient sets used

The gain of Trim1 may be set through register [0x3B\[6:5\]](#), Trim2 through register [0x3D\[2:0\]](#) and Trim3 through register [0x40\[5:0\]](#).

Trim2 and Trim3 will apply saturation on a positive or negative overflow. Overflow (or clipping) events will be indicated by register [0x94\[2\]](#) and [0x94\[0\]](#) respectively.

5.3 BASS-BOOST

The bass-boost is implemented using a biquad IIR filter, is applied to the mid ($M = L + R$) channel only, and applies a gain to all frequencies below a programmable corner frequency. Typically the bass-boost is used to extend the low frequency response beyond the natural roll-off of a speaker.

Bass-boost may be enabled through the BASSB pin (see section 4.6.3) or through register [0x01\[1:0\]](#).

The corner frequency, gain and shape of the bass-boost response are all adjustable:

- Register [0x3C\[5:0\]](#) defines the bass-boost corner frequency
- Register [0x3D\[7:6\]](#) defines the bass-boost gain
- Register [0x3D\[5:4\]](#) defines the 'Q', or shape of the bass-boost response

The bass-boost corner frequency may be configured through register [0x3C\[5:0\]](#), as detailed below.

$$\text{CornerFrequencyHz} = f \cdot \text{SampleRateHz} / \sqrt{2} \cdot \pi$$

Where f is defined by Table 9 below.

0x3C[5:4]	f	Corner Frequency Range		
		32kHz sample rate	44.1kHz sample rate	48kHz sample rate
0x0	$0x3C[3:0] / 2^{12}$	0 to 26.4Hz, in 1.76Hz steps	0 to 36.4Hz, in 2.42Hz steps	0 to 39.6Hz, in 2.64Hz steps
0x1	$(0x3C[3:0] + 16) / 2^{12}$	28.1 to 54.5Hz, in 1.76Hz steps	38.8 to 75.1Hz, in 2.42Hz steps	42.2 to 81.8Hz, in 2.64Hz steps
0x2	$(0x3C[3:0] + 16) / 2^{11}$	56.3 to 109Hz, in 3.52Hz steps	77.5 to 150Hz, in 4.85Hz steps	84.8 to 164Hz, in 5.28Hz steps
0x3	$(0x3C[3:0] + 16) / 2^{10}$	113 to 218Hz, in 7.03Hz steps	155 to 300Hz, in 9.69Hz steps	169 to 327Hz, in 10.6Hz steps

Table 9: Bass-boost corner frequency

Note that the above calculation will return the theoretical corner frequency (or -3dB point). The actual corner frequency will be affected by the bass-boost gain and bass-boost shape.

This range of corner frequencies is shown in Figure 38 below (for maximum gain and a critically damped shape). The default value of 0x2D for register [0x3C\[5:0\]](#) is emphasised in bold and corresponds to 141Hz (with a 44.1kHz sample rate).

Note that the values on the X (frequency) axis in the following 3 plots are for a 44.1kHz sample rate. Different sample rates will linearly scale this axis.

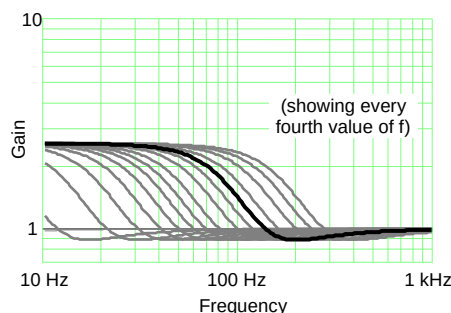


Figure 38: Bass-boost corner frequency

The bass-boost gain is configurable through register [0x3D\[7:6\]](#).

Register 0x3D[7:6]	DC Gain	
	Linear	dB
0x0	7.11	17.04
0x1	4.00	12.04
0x2	2.56	8.16
0x3	1.78	5.00

Table 10: Bass-boost gain

This range of bass-boost gains is show in Figure 39 below. The default value is emphasised in bold.

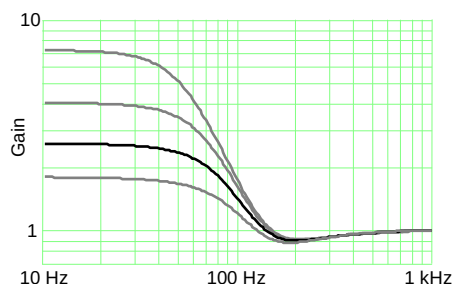


Figure 39: Bass-boost gain

The bass-boost shape, or 'Q', is configurable through register [0x3D\[5:4\]](#).

Register 0x3D[5:4]	'Q' of response corner
0x0	1.13
0x1	0.94
0x2	0.81
0x3	0.71 (Critically damped)

Table 11: Bass-boost shape

This range of response shapes is shown in Figure 40 below. The default value is emphasised in bold.

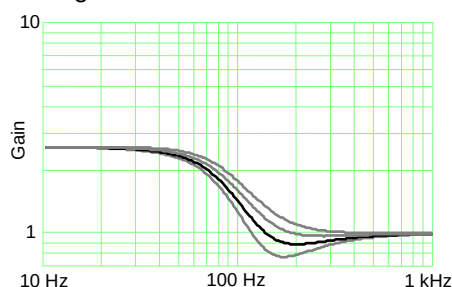


Figure 40: Bass-boost shape

5.4 STEREO-WIDE

The stereo-wide feature provides variable stereo image widening by applying gain to the side ($S = L - R$) channel only. Typically this is used to enhance the perception of spacing with stereo speakers.

Stereo-wide may be enabled through the SWIDE pin (see section 4.6.3) or through register [0x01\[3:2\]](#). The stereo-wide gain may be controlled through register [0x3C\[7:6\]](#).

Note that the stereo-wide function is disabled in audio modes 12 and 13. In these audio modes the SWIDE control is instead used for biquad register set switching, see section 5.5.4.

5.5 BIQUAD FILTERS

Sixteen fully programmable biquadratic Infinite Impulse Response (IIR) filters (also known as Second-Order Section (SOS) filters) are available to perform frequency-selective signal processing; such as compensating for the frequency response of the output filter and/or speaker enclosure used.

Signal routing from the X & Y inputs to the biquad filters block to the C & D outputs from the biquad filters block is very flexible allowing the biquad filter resources to be shared equally, or unequally, between signal paths as required.

Each biquad filter has a single input which can be individually sourced from either of the X or Y inputs to the biquad filters block, or from the output of a previous biquad filter.

The configuration of matrix1 and matrix2 (as controlled by the audio mode, see section 5.1) determines if the biquad filters will process audio data in the LR (left & right) domain or in the MS (mid & side) domain.

The biquad filters block may be globally enabled through register [0x40\[7\]](#).

The outputs from the biquad filters block appear on terminals C and D. Register [0x3F\[7:4\]](#) and [0x3F\[3:0\]](#) select the biquad filters whose output is connected to the C and D terminals respectively.

Note that the biquad filter connected to the D terminal (register [0x3F\[3:0\]](#)) is assumed to be the last active biquad filter in the processing chain. All biquad filters after this biquad filter are therefore automatically disabled. Thus, always ensure register [0x3F\[3:0\]](#) $\geq$ register [0x3F\[7:4\]](#).

The latency from input to output of the whole biquad filters block is one sample period regardless of how many biquad filters are used for each output.

5.5.1 CONFIGURATION OF INDIVIDUAL BIQUAD FILTERS

The sixteen biquad filters are identical. The structure of an individual biquad filter is shown in Figure 41, below.

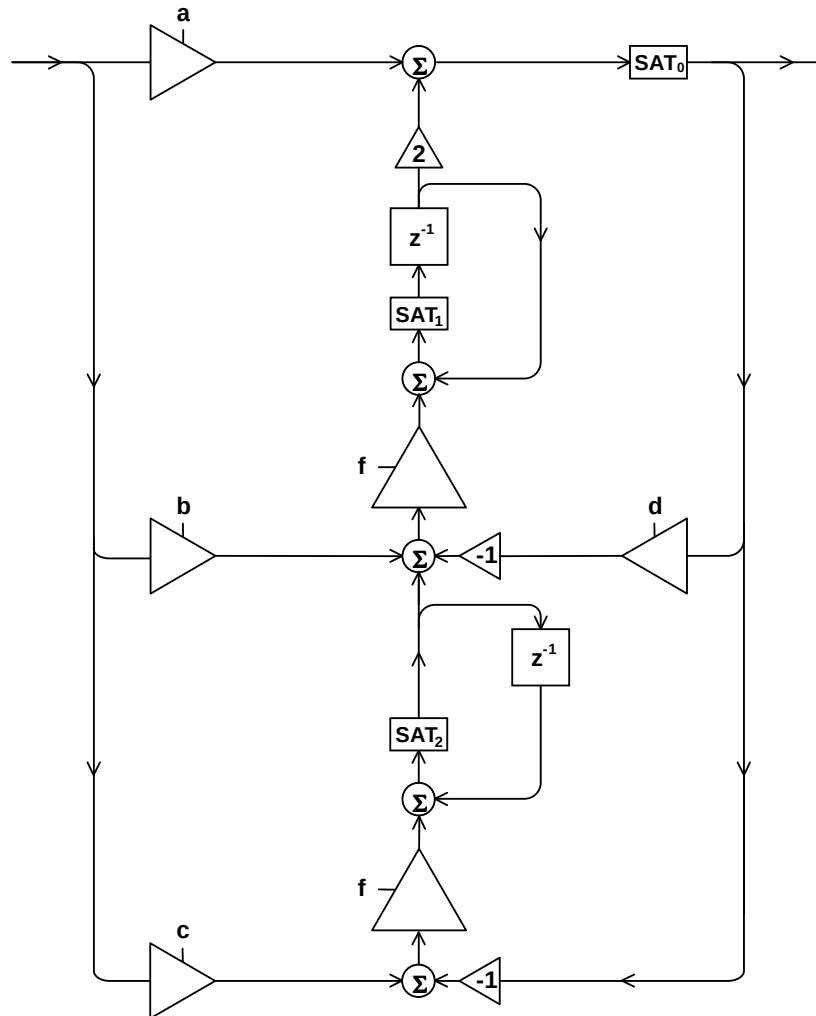


Figure 41: Biquad filter structure

A biquad filter's structure is similar to a 'Direct Form II Transposed' arrangement, but with changes made to improve computational efficiency and effective precision. Each biquad filter will give performance generally comparable to that of a direct form filter having at least 24-bit coefficients, 40-bit internal datapaths and 70-bit accumulation.

The transfer function of each biquad filter is:

$$\frac{a - (2 \cdot a - 2 \cdot b \cdot f - 2 \cdot c \cdot f^2) \cdot z^{-1} + (a - 2 \cdot b \cdot f) \cdot z^{-2}}{1 - (2 - 2 \cdot d \cdot f - 2 \cdot f^2) \cdot z^{-1} + (1 - 2 \cdot d \cdot f) \cdot z^{-2}}$$

Figure 42: Biquad filter transfer function

Saturation in the event of positive or negative overflow is implemented at several stages (marked SAT₀, SAT₁ and SAT₂ in Figure 41).

Saturation at the final output (SAT₀) in any of the biquad filters is indicated in register [0x94\[1\]](#).

5.5.2 MAPPING OF BIQUAD CONFIGURATION REGISTER SETS TO BIQUAD FILTERS

Each biquad filter may be configured through a biquad configuration register set. A biquad configuration register set is a group of five registers ($p = 0 - 4$);. There are sixteen groups of biquad configuration register sets ($n = 0 - 15$). This give a total of 80 biquad configuration registers, which are denoted as BIQUADn_p in registers [0x41](#) – [0x90](#).

Each biquad configuration register set defines the following parameters:

- Input Data Source: [BIQUADn_4\[5:3\]](#)
Defines the source of the input signal for biquad filter n. May be selected from either the X or Y input to the biquad filter block (see Figure 29), or from the output of a previous, or previous but one, biquad filter.
- Functional Configuration: [BIQUADn_4\[7:6\]](#)
Allows one to selectively disable parts of biquad filter n, or negate the b coefficient.

- Coefficient a:
A 6 bit number over the range: 0 / 32 to 63 / 32
 $A[5:0] = \text{BIQUADn_4}[2:0], \text{BIQUADn_3}[7:5]$
Where: $a = A / 32$
- Coefficient b:
A 7 bit number over the range: 0 / 64 to 127 / 64
 $B[6:0] = \text{BIQUADn_3}[4:0], \text{BIQUADn_2}[7:6]$
Where: $b = B / 64$
Note that b may also be negated through [BIQUADn_4\[7:6\]](#)
- Coefficient c:
A 6 bit number over the range: 0 / 32 to 63 / 32
 $C[5:0] = \text{BIQUADn_2}[5:0]$
Where: $c = C / 32$
- Coefficient d:
A 7 bit number over the range: 0 / 64 to 127 / 64
 $D[6:0] = \text{BIQUADn_1}[7:1]$
Where: $d = D / 64$
- Coefficient f:
A 15 bit floating point number over the range: 0 to $(2^{15} - 1)/2^{14}$.
 $F[8:0] = \text{BIQUADn_1}[0], \text{BIQUADn_0}[7:0]$
Where: if: $F[8:5] < 5$, Reserved, should not be used
if: $F[8:5] = 5$, $f = F[4:0] * 2^{-14}$
if: $F[8:5] > 5$, $f = (32 + F[4:0]) * 2^{(F[8:5] - 20)}$

5.5.3 BIQUAD FILTERS REPEAT MODE

By default, there is a one-to-one mapping between the biquad configuration register sets and to the actual biquad filters. However, if exactly the same filter functions are required for both channels being processed by the biquad filters block, then only the register sets for one channel need be configured and a repeat function can be used as follows.

Register [0x40\[6\]](#) enables biquad repeat mode. When enabled, the least significant bit of the biquad filter number is ignored, and each biquad configuration register set is used for two successive biquad filters.

The first biquad filter should be configured to select the X input as its data source. In repeat mode this will then automatically select the Y input as the data source for the second biquad filter. To do this set register [BIQUAD0_4\[5:3\]](#) ($0x45[5:3]$) to 0x1.

All subsequent biquad filters should be configured to select the output from the biquad filter before the previous biquad filter as the input source. To do this set register [BIQUADn_4\[5:3\]](#) to 0x4 or 0x5.

Repeat mode effectively interleaves the biquad filters used for each channel. Table 12 shows an example routing for 3 biquad filters per channel (so a total of 6 biquad filters):

Biquad filter	Biquad configuration register set	Biquad input data source	BIQUADn_4[5:3]
0	0	X input	$\text{BIQUAD1_4}[5:3] = 0x1$
1		Y input	
2	1	Output from biquad 0	$\text{BIQUAD2_4}[5:3] = 0x4$
3		Output from biquad 1	
4	2	Output from biquad 2	$\text{BIQUAD3_4}[5:3] = 0x4$
5		Output from biquad 3	

Table 12: Example routing for biquad repeat mode

In the above example one would also set register [0x3F\[7:4\]](#) to 0x4 (to connect the output of biquad filter 4 to the C output of the biquad filter block) and [0x3F\[3:0\]](#) to 0x5 (to connect the output of biquad filter 5 to the D output of the biquad filter block).

The advantage of using repeat mode is that only half the normal amount of configuration data need be written.

This feature is clearly only useful in modes where identical biquad filtering of two channels of audio data is required, i.e. in stereo audio modes 24, 25, 28, 29, 30 and in mono audio modes 4, 5, 12 and 13 (Mono Select (MS filtering)) where the biquad filters block processes two channels of audio data.

5.5.4 BIQUAD FILTER CONFIGURATION REGISTER SET SWITCHING

By default, there is a one-to-one mapping between the biquad configuration register sets and to the actual biquad filters. However it is possible to change this relationship by using the biquad filter register set switch, register [0x93\[3:0\]](#).

The value of register [0x93\[3:0\]](#) is exclusive-OR-ed with the biquad filter number. The result identifies the configuration register set that will be used to configure that individual biquad filter.

This feature is useful when only a subset of the biquad filters is being used, and the ability to quickly change the configuration of the biquad filters being used is required.

For example, suppose only 4 biquad filters are required for a mono channel being processing by the biquad filters block.

So biquad filters 0 – 3 are used, which by default are configured by registers BIQUAD0_0-4 to BIQUAD3_0-4. The remaining biquad configuration register sets could then be configured with variations of these parameters. By changing the value of register [0x93\[3:0\]](#) these different configuration register sets can be used to configure biquad filters 0 – 3 on the fly; thus implementing a fast switch of the filter characteristics.

Register 0x93[3:0]	Configuration register set used to control...			
	Biquad filter 0	Biquad filter 1	Biquad filter 2	Biquad filter 3
0x0	0	1	2	3
0x4	4	5	6	7
0x8	8	9	10	11
0xC	12	13	14	15

Table 13: Example routing for biquad register set switching

Note that in the above example one would also need to set register [0x3F\[7:4\]](#) = 0x3 (to connect the output of biquad filter 3 to the C output of the biquad filter block). In this example even though the D output of the biquad filter block is not used, register [0x3F\[3:0\]](#) should also be set to 0x3 to switch off the remaining unused 12 biquad filters.

In certain audio modes it is also possible to additionally swap the upper and lower 8 biquad filter register sets under pin control. (This is the equivalent to toggling the most significant bit of the register [0x93\[3:0\]](#).)

Depending on the audio mode, there are 2 pins which may be used to effect this register set switch; either AD0 or SWIDE.

In audio modes 12 and 13 SWIDE controls this biquad filter switch, and in audio modes 14 & 15 AD0 controls this biquad filter switch.

Audio mode 30 is a variant on the Normal Left Right Stereo mode 24 (see section 5.1.1.1) but with the AD0 pin performing this biquad filter configuration register set switching. Similarly, mode 28 is a variant on mode 24, where the stereo-wide function is disabled and SWIDE performs the biquad filter configuration register set switch.

Biquad filter configuration register set switching can also be used in conjunction with biquad repeat mode. If both are used then:

- the top 8 biquad configuration register sets are ignored
- the odd/even pairs of biquad filters each use same configuration register set
- the biquad configuration register set = $\text{subset_ip}[3:1] \wedge \text{biquad_filter}[3:1]$
- the MSB of subset (or AD0 or stereo-wide) can still toggle between 2 lots of 4 biquad filters.

6 REGISTER MAP

This section details the internal registers which are accessible via the TWI.

All register locations may be read from or written to. Bit fields marked 'RW' may be read from or written to. Data written to bit fields marked 'R' will be ignored. Reading from or writing to register locations other than those listed below will have no effect, but is not recommended.

6.1 REGISTER 0x00: CONFIG0

Register 0x00 configures Serial Digital Audio interface, and the functionality of the STDBY, MUTE, SWIDE & BASSB pins.

Field name	Bits	Access	Default	Value	Description
Configuration OTP Valid	7	R	0x1	0x0 0x1	Configuration OTP registers have not been programmed Configuration OTP registers have been programmed See also section 7
Serial Digital Audio Interface Mode	6	RW	0x0	0x0 0x1	Serial Digital Audio interface is a slave Serial Digital Audio Interface is a master
Serial Digital Audio Interface Data Format	5:4	RW	0x0	0x0 0x1 0x2 0x3	I ² S Left-justified Right-justified Reserved, do not use
STDBY Control	3	RW	0x0	0x0 0x1	Edge sensitive: a pulse on STDBY pin toggles Standby/Active state Level sensitive: the state of STDBY pin defines Standby/Active state
MUTE Control	2	RW	0x0	0x0 0x1	Edge sensitive: a pulse on MUTE pin toggles Mute state Level sensitive: the state of MUTE pin defines Mute state
SWIDE Control	1	RW	0x0	0x0 0x1	Edge sensitive: a pulse on SWIDE pin toggles Stereo-Wide state Level sensitive: the state of SWIDE pin defines Stereo-Wide state
BASSB Control	0	RW	0x0	0x0 0x1	Edge sensitive: a pulse on BASSB pin toggles Bass-Boost state Level sensitive: the state of BASSB pin defines Bass-Boost state

Table 14: Register 0x00: CONFIG0

6.2 REGISTER 0x01: BUTTON_CONTROL

Register 0x01 allows the user to control and/or monitor the state of the operating mode (Standby or Active) and the state of Mute, Stereo-wide and Bass-Boost features.

Reading the state bits will return the current state of each feature.

To control a feature, set its override bit to 0x1 and the corresponding state bit set to the desired value. (To leave a feature under pin control, set its override bit to 0x0.)

If the feature is set to edge sensitive, then the respective override bit is automatically reset to 0x0 after a write.

Field name	Bits	Access	Default	Value	Description
Override Standby/Active state	7	RW	0x0	0x0 0x1	Value in bit 6 ignored on a write Value in bit 6 used as new Standby/Active state on a write
Standby/Active state	6	RW	0x0	0x0 0x1	Standby mode Active mode
Override Mute state	5	RW	0x0	0x0 0x1	Value in bit 4 ignored on a write Value in bit 4 used as new Mute state on a write
Mute state	4	RW	0x0	0x0 0x1	Un-muted Muted
Override Stereo-wide state	3	RW	0x0	0x0 0x1	Value in bit 2 ignored on a write Value in bit 2 used as new Stereo-Wide state on a write
Stereo-wide state	2	RW	0x0	0x0 0x1	Normal Stereo-wide active
Override Bass-boost state	1	RW	0x0	0x0 0x1	Value in bit 0 ignored on a write Value in bit 0 used as new Bass-Boost state on a write
Bass-boost state	0	RW	0x0	0x0 0x1	Normal Bass-boost active

Table 15: Register 0x01: BUTTON_CONTROL

6.3 REGISTER 0x02: MUTE_RAMP

Register 0x02 controls the rate of volume change when entering and exiting a mute condition.

(Note that the actual time to mute/un-mute will also depend on the volume level before/after the mute/un-mute event.)

Field name	Bits	Access	Default	Value	Description
Reserved	7	RW	0x0		Reserved for Audium use Always set to 0x0
Mute ramp rate	6:0	RW	0x03	N	The mute/un-mute ramp rate is defined by the interval between volume steps: $\text{VolStepInterval} = (N + 1) \times 6 / \text{SystemClockMHz ms}$

Table 16: Register 0x02: MUTE_RAMP

6.4 REGISTER 0x03: VOLUME

Register 0x03 allows the volume to be set, incremented or decremented; and read back.

Attempting to set a volume level above the maximum will set the volume at maximum. See Table 4 for device maximum volume values.

A volume of 0 is equivalent to a mute condition.

Field name	Bits	Access	Default	Value	Description
Volume Control Action	7:6	RW	0x0	0x0	Set the volume to the value in bits 5:0
				0x1	Decrement volume by 1 step (bits 5:0 ignored)
				0x2	Increment volume by 1 step (bits 5:0 ignored)
				0x3	Reserved
Volume Level	5:0	RW	0x18	N	Volume level

Table 17: Register 0x03: VOLUME

6.5 REGISTER 0x04: ROTARY_ENCODER

Register 0x04 defines the user interface connected to the BTNUP and BTNDN pins and used for volume control.

Field name	Bits	Access	Default	Value	Description
Enable Rotary Encoder	7	RW	0x0	0x0	Push buttons
				0x1	Rotary encoder
Rotary Steps	6:0	RW	0x00	N	Number of rotary encoder steps per volume step: $\text{RotaryStepsPerVolumeStep} = N + 1$

Table 18: Register 0x04: ROTARY_ENCODER

6.6 REGISTER 0x05: VOLUME_DELAY

Register 0x05 defines the time period a volume button must be activated before the volume automatically ramps. This setting affects both incrementing and decrementing the volume.

Note that the sum on Volume Ramp Delay and Volume Ramp Delay should not exceed 255.

Field name	Bits	Access	Default	Value	Description
Volume Ramp Delay	7:0	RW	0x20	N	The volume ramp delay is defined as: $\text{DelayTime} = N \times 48 / \text{SystemClockMHz ms}$ For normal operation, ensure $N > 4$.

Table 19: Register 0x05: VOLUME_DELAY

6.7 REGISTER 0x06: VOLUME_RAMP

Register 0x06 defines the rate of automatic volume ramping, which occurs after the Volume Ramp Delay.

Note that the sum on Volume Ramp Delay and Volume Ramp Delay should not exceed 255.

Field name	Bits	Access	Default	Value	Description
Reserved	7	RW	0x0		Reserved for Audium use Always set to 0x0
Volume Ramp Rate	6:0	RW	0x02	N	The volume ramp rate is defined by the interval between volume steps: $\text{VolumeStepInterval} = (N + 1) \times 48 / \text{SystemClockMHz ms}$

Table 20: Register 0x06, VOLUME_RAMP

6.8 REGISTER 0x07-0x0E: RESERVED0-7

Registers 0x07-0x0E are reserved for Audium use. Only their default values should be written.

Register	Bits	Access	Default	Value	Description
Register 0x07	7:0	RW	0xC1	-	Reserved for Audium use
Register 0x08	7:0	RW	0x44	-	Reserved for Audium use
Register 0x09	7:0	RW	0x45	-	Reserved for Audium use
Register 0x0A	7:0	RW	0xC5	-	Reserved for Audium use
Register 0x0B	7:0	RW	0x85	-	Reserved for Audium use
Register 0x0C	7:0	RW	0x75	-	Reserved for Audium use
Register 0x0D	7:0	RW	0x25	-	Reserved for Audium use
Register 0x0E	7:0	RW	0xB5	-	Reserved for Audium use

Table 21: Register 0x07-0x0E: RESERVED0-7

6.9 REGISTER 0x0F: I2S_CLIPING

Register 0x0f can be used to determine if the digital audio input is exceeding a predefined threshold (see Register 0x11: I2S_CLIP_THRESHOLD).

Field name	Bits	Access	Default	Value	Description
Clear Sticky Flag	7	RW	0x0	0x0 0x1	Do not clear clipping flag Clear input clipping flag (bit 1) This bit will auto reset to 0 after a write
Reserved	6	RW	0x0		Reserved for Audium use Always set to 0x0
Input Clipping Pin Mask	5	RW	0x0	0x0 0x1	Input clipping flag is not mapped to the nERROR pin Input clipping flag is mapped to the nERROR pin
Reserved	4	RW	0x1		Reserved for Audium use Always set to 0x0
Sticky Enable	3	RW	0x1	0x0 0x1	Clipping flag only asserted during input clipping events Clipping flag remains asserted until Clear Sticky Flag (bit 7) is set to 0x1
Reserved	2	RW	0x0		Reserved for Audium use Always set to 0x0
Input Clipping Flag	1	R	0x0	0x0 0x1	Normal operation Clipping event detected at digital audio input
Reserved	0	R	0x0		Reserved for Audium use

Table 22: Register 0x0F: I2S_CLIPING

6.10 REGISTER 0x10: STANDBY_CLK_DIV

Register 0x10 defines the standby system clock frequency.

Field name	Bits	Access	Default	Value	Description
Reserved	7:5	RW	0x0		Reserved for Audium use Always set to 0x0
Standby Clock Division	4:0	RW	0x02	N	Standby clock frequency. If N = 0x00: StandbyClockFreq = InternalOscillatorFreq / 4 Else, if N > 0x00: StandbyClockFreq = InternalOscillatorFreq / (8 x N)

Table 23: Register 0x10: STANDBY_CLK_DIV

6.11 REGISTER 0x11: I2S_CLIP_THRESHOLD

Register 0x11 defines the digital audio input clipping threshold.

Data on the serial digital audio interface with a magnitude above this threshold will cause a clipping event, and assert the clipping flag. (See also Register 0x0F: I2S_CLIPING.)

Field name	Bits	Access	Default	Value	Description
Reserved	7	RW	0x0		Reserved for Audium use Always set to 0x0
Clip Threshold	6:0	RW	0x7f	N	The upper seven bits of absolute audio data are compared against N. If any data value matches or exceeds N the clipping flag is asserted.

Table 24: Register 0x11: I2S_CLIP_THRESHOLD

6.12 REGISTER 0x12: TWI_DEVICE_ADDRESS

Register 0x12 defines the device's TWI address.

Field name	Bits	Access	Default	Value	Description
Reserved	7:6	R	0x0		Reserved for Audium use Always set to 0x0
TWI Address	5:0	RW	0x2a	N	N defines bits 7:2 of the device address. Pin AD0 defines bit 1 of the device address. Bit 0 of the address is the read/write bit.

Table 25: Register 0x12: TWI_DEVICE_ADDRESS

6.13 REGISTER 0x13-0x32: TWI_MASTER_DATA_0-31

Registers 0x13 to 0x32 define data that can be sent to a slave device over the TWI bus when entering Standby or Active modes.

Data should be arranged in byte pairs starting at register 0x13. Preamble data first, followed by postamble data.

Field name	Bits	Access	Default	Value	Description
Vector Data 0 -31	7:0	RW	0x00	-	Pre- and post-amble data

Table 26: Register 0x13-0x32: TWI_MASTER_DATA_0-31

6.14 REGISTER 0x33: TWI_MASTER_PREAMBLE

Register 0x33 defines the number of preamble byte pairs of data that are sent to a slave device over the TWI bus as the device transitions from Standby to Active mode.

The total number of preamble and postamble bytes pairs should not exceed 16.

Field name	Bits	Access	Default	Value	Description
Reserved	7:5	RW	0x0		Reserved for Audium use Always set to 0x0
Preamble Byte Pairs	4:0	RW	0x00	N	Defines the number of byte pairs in the preamble. If no preamble is to be sent, then N should be set to 0x00.

Table 27: Register 0x33: TWI_MASTER_PREAMBLE

6.15 REGISTER 0x34: TWI_MASTER_POSTAMBLE

Register 0x34 defines the number of postamble byte pairs of data that are sent to a slave device over the TWI bus as the device transitions from Active to Standby mode.

The total number of preamble and postamble bytes pairs should not exceed 16.

Field name	Bits	Access	Default	Value	Description
Reserved	7:5	RW	0x0		Reserved for Audium use Always set to 0x0
Postamble Byte Pairs	4:0	RW	0x00	N	Defines the number of byte pairs in the postamble. If no postamble is to be sent, then N should be set to 0x00.

Table 28: Register 0x34: TWI_MASTER_POSTAMBLE

6.16 REGISTER 0x35: TWI_MASTER_CONFIG

Register 0x34 defines how the device interacts with the target slave device over the TWI.

Field name	Bits	Access	Default	Value	Description
All At Once	7	RW	0x0	0x0	Byte pairs are sent individually, with a start and stop condition between them.
				0x1	Byte pairs are sent as one concatenated block with a single start and stop condition.
Target Device Address	6:0	RW	0x00	N	Bits 7:1 of the target's TWI address. Bit 0 of the target's TWI address is always 0, indicating a write operation.

Table 29: Register 0x35: TWI_MASTER_CONFIG

6.17 REGISTER 0x36: SYSTEM_CLK_CONFIG

Register 0x36 configures the source, frequency and standby behaviour of the system-clock.

Care should be taken when setting the System Clock Division Ratio to ensure the system clock is fast enough to cope with the incoming digital audio data stream (ensure $\text{SystemClock} \geq 32 \times \text{SampleRate}$).

When using the internal oscillator as the system-clock source, to ensure the device can receive a signal up to the maximum supported sample rate, always ensure the System Clock Division Ratio $\leq 0x10$.

Field name	Bits	Access	Default	Value	Description
Crystal Oscillator Enable	7	RW	0x0	0x0 0x1	0x0 Disable crystal oscillator (pins XI & XO). External clock input pin (CLKIP) is available for use. 0x1 Enable crystal oscillator pins (XI & XO). External clock input pin (CLKIP) may not be used.
Crystal Oscillator Active in Standby Mode	6	RW	0x0	0x0 0x1	0x0 Crystal oscillator active in standby mode. 0x1 Crystal oscillator disabled in standby mode.
System Clock Source	5	RW	0x1	0x0 0x1	0x0 System-clock is derived from the crystal oscillator or external clock (as defined by bit 7). 0x1 System-clock is derived from the internal oscillator
System Clock Division Ratio	4:0	RW	0x02	N	If N = 0x00: SystemClock = ClockSource Else if N > 0x00: SystemClock = ClockSource / (2 x N) Where, if using the internal oscillator: ClockSource = InternalOscillator / 4 Else, if using the crystal oscillator: ClockSource = CrystalOscillator Else, if using the external clock: ClockSource = ExternalClock

Table 30: Register 0x36: SYSTEM_CLK_CONFIG

6.18 REGISTER 0x37: CLK_OUT_CONFIG

Register 0x37 configures the source, frequency and standby behaviour of the external clock output (pin CLKOP).

Field name	Bits	Access	Default	Value	Description
External Clock Output Enable	7	RW	0x0	0x0 0x1	0x0 Disable external clock output. 0x1 Enable external clock output.
External Clock Output Active in Standby Mode	6	RW	0x0	0x0 0x1	0x0 External clock output active in standby mode. 0x1 External clock output held low in standby mode.
External Clock Output Source	5	RW	0x0	0x0 0x1	0x0 External clock output is derived from the crystal oscillator or external clock (as defined by 0x36[7]). 0x1 External clock output is derived from the internal oscillator.
External Clock Output Division Ratio	4:0	RW	0x00	N	If N = 0x00: ExternalOutputClock = ClockSource If N > 0x00: ExternalOutputClock = ClockSource / (2 x N) Where, if using the internal oscillator: ClockSource = InternalOscillator / 4 Else, if using the crystal oscillator: ClockSource = CrystalOscillator Else, if using the external clock: ClockSource = ExternalClock

Table 31: Register 0x37: CLK_OUT_CONFIG

6.19 REGISTER 0x38: SILENCE_DETECT_THRESHOLD

Register 0x38 reports the state of the silence detector, and configures the detection threshold.

Field name	Bits	Access	Default	Value	Description
Silence Detect Active	7	R	0x0	0x0 0x1	0x0 Silence detector not active (audio data is above threshold) 0x1 Silence detector activated (audio data is below threshold)
Silence Detect Threshold	6:0	RW	0x01	N	Least significant 7bits of magnitude threshold. Setting this threshold and/or the hold-off period (0x39[7:0]) to 0x00 will disable the silence detect feature.

Table 32: Register 0x38: SILENCE_DETECT_THRESHOLD

6.20 REGISTER 0x39: SILENCE_DETECT_HOLDOFF

Register 0x39 configures the silence detector hold-off period.

Field name	Bits	Access	Default	Value	Description
Silence Detect Hold-off	7:0	RW	0x10	N	Holdoff = N x 48 / SystemClockMHz ms Setting this hold-off period and/or the threshold (0x38[6:0]) to 0x00 will disable the silence detect feature.

Table 33: Register 0x39: SILENCE_DETECT_HOLDOFF

6.21 REGISTER 0x3A: AUDIO_DSP_OTP_VALID

Register 0x3A indicates if the Audio DSP OTP register section has been programmed. See also section 7.

Field name	Bits	Access	Default	Value	Description
Audio DSP OTP Valid	7	R	0x0	0x0	Audio DSP OTP registers have not been programmed
				0x1	Audio DSP OTP registers have been programmed See also section 7
Reserved	6:0	RW	0x00	-	Reserved for Audium use Always set to 0x00

Table 34: Register 0x3A: AUDIO_DSP_OTP_VALID

6.22 REGISTER 0x3B: AUDIO_DSP_CONFIG0

Register 0x3B enables the DC remover, sets the trim1 gain and selects the DSP audio mode.

Field name	Bits	Access	Default	Value	Description
DC Remover	7	RW	0x1	0x0	Disable DC remover
				0x1	Enable DC remover
Trim 1 Gain	6:5	RW	0x3	0x0	Trim 1 gain = 1/8
				0x1	Trim 1 gain = 1/4
				0x2	Trim 1 gain = 1/2
				0x3	Trim 1 gain = 1
Audio DSP Mode	4:0	RW	0x18	N	See section Table 8, in section 5.1 for details.

Table 35: Register 0x3B: AUDIO_DSP_CONFIG0

6.23 REGISTER 0x3C: AUDIO_DSP_CONFIG1

Register 0x3C configures the stereo-wide gain and the bass-boost corner frequency.

The values for the bass-boost corner frequency in the table below are for a sample rate of 44.1kHz. For a full description, and other sample rates refer to section 5.3.

Field name	Bits	Access	Default	Value	Description
Stereo-Wide Gain	7:6	RW	0x1	0x0	Side channel gain = 1.5
				0x1	Side channel gain = 2.0
				0x2	Side channel gain = 2.5
				0x3	Side channel gain = 3.0
Bass-Boost Corner Frequency Range	5:4	RW	0x2	0x0	0 to 36.4Hz, in 2.42Hz steps
				0x1	38.8 to 75.1Hz, in 2.42Hz steps
				0x2	77.5 to 150Hz in 4.85Hz steps
				0x3	155 to 300Hz in 9.69Hz steps
Bass-Boost Corner Frequency Value	3:0	RW	0xD	N	Corner frequency of bass-boost filter, within the frequency range as defined by bits 5:4. CornerFrequency $\approx$ RangeMin + N x StepSize The default range (0x2) and value (0xD) correspond to a corner frequency of 141Hz

Table 36: Register 0x3C: AUDIO_DSP_CONFIG1

6.24 REGISTER 0x3D: AUDIO_DSP_CONFIG2

Register 0x3D configures bass-boost gain and shape, and the trim2 gain.

Field name	Bits	Access	Default	Value	Description
Bass-Boost DC Gain	7:6	RW	0x1	0x0 0x1 0x2 0x3	DC gain = 1.78 (5.00dB) DC gain = 2.56 (8.16dB) DC gain = 4.00 (12.04dB) DC gain = 7.11 (17.04dB)
Bass-Boost Shape	5:4	RW	0x1	0x0 0x1 0x2 0x3	'Q' corner response = 1.13 'Q' corner response = 0.94 'Q' corner response = 0.81 'Q' corner response = 0.71 (critically damped)
Reserved	3	RW	0x0		Reserved for Audium use Always set to 0x0
Trim 2 Gain	2:0	RW	0x5	0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7	Trim2Gain = 1/256 Trim2Gain = 1/128 Trim2Gain = 1/64 Trim2Gain = 1/32 Trim2Gain = 1/16 Trim2Gain = 1/8 Trim2Gain = 1/4 Trim2Gain = 1/2

Table 37: Register 0x3D: AUDIO_DSP_CONFIG2

6.25 REGISTER 0x3E: AUDIO_DSP_RESERVED

Register 0x3E is reserved for Audium use. Only the default values should be written.

Register	Bits	Access	Default	Value	Description
Reserved	7:0	RW	0x00	-	Reserved for Audium use Always set to 0x0

Table 38: Register 0x3E: AUDIO_DSP_RESERVED

6.26 REGISTER 0x3F: BIQUAD_OUTPUT

Register 0x3F controls which biquad filters drive the C and D outputs of the biquad filters block.

Field name	Bits	Access	Default	Value	Description
Biquads C Terminal Source	7:4	RW	0x2	N	Biquad N output used to drive C output of biquad filters block
Biquads D Terminal Source	3:0	RW	0x3	M	Biquad M output used to drive D output of biquad filters block Always ensure $M \geq N$ All biquads $> M$ will be disabled

Table 39: Register 0x3F: BIQUAD_OUTPUT

6.27 REGISTER 0x40: BIQUAD_CONTROL

Register 0x40 enables the biquad filter block and defines the gain of trim 3 block.

Field name	Bits	Access	Default	Value	Description
Biquads Enable	7	RW	0x0	0x0 0x1	Biquad filters block disabled. C & D outputs connected to X & Y trim 2 outputs. Biquad filter block enabled. C & D outputs controlled by 0x3F[7:0].
Biquads Repeat	6	RW	0x1	0x0 0x1	Each biquad filter uses its own configuration register data. (For example biquad filter 4 uses BIQUAD4_ register data, and biquad filter 5 uses BIQUAD5_ data.) Consecutive pairs of biquad filters share configuration data from a common configuration register. (For example biquad filter 4 and biquad filter 5 are both configured from BIQUAD4_ data.)
Trim 3 Gain	5:3 2:0	RW RW	0x5 0x0	N M	Trim 3 coarse gain control Trim 3 fine gain control If $N = 0$ Trim3Gain = $M / 32$ If $N \neq 0$ Trim3Gain = $(M + 8) \times 2^{(N-6)}$

Table 40: Register 0x40: BIQUAD_CONTROL

6.28 REGISTER 0x41/46/4B/50/55/5A/5F/64/69/6E/73/78/7D/82/87/8C: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_0

First register in the 5 register set of biquad filter configuration registers. There are 16 occurrences of this register.

Field name	Bits	Access	Default	Value	Description
Biquad Coefficient F[7:0]	7:0	RW	0x00	F[7:0]	Least significant 7 bits of biquad filter coefficient F.

**Table 41: Register 0x41/46/4B/50/55/5A/5F/64/69/6E/73/78/7D/82/87/8C:
BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_0**

6.29 REGISTER 0x42/47/4C/51/56/5B/60/65/6A/6F/74/79/7E/83/88/8D: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_1

Second register in the 5 register set of biquad filter configuration registers. There are 16 occurrences of this register.

Field name	Bits	Access	Default	Value	Description
Biquad Coefficient D[6:0]	7:1	RW	0x00	D[6:0]	Biquad filter coefficient D.
Biquad Coefficient F[8]	0	RW	0x0	F[7]	Most significant bit of biquad filter coefficient F.

**Table 42: Register 0x42/47/4C/51/56/5B/60/65/6A/6F/74/79/7E/83/88/8D:
BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_1**

6.30 REGISTER 0x43/48/4D/52/57/5C/61/66/6B/70/74/7A/7F/84/89/8E: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_2

Third register in the 5 register set of biquad filter configuration registers. There are 16 occurrences of this register.

Field name	Bits	Access	Default	Value	Description
Biquad Coefficient B[1:0]	7:6	RW	0x0	B[1:0]	Least significant 2 bits of biquad filter coefficient B.
Biquad Coefficient C[5:0]	5:0	RW	0x00	C[5:0]	Biquad filter coefficient C.

**Table 43: Register 0x43/48/4D/52/57/5C/61/66/6B/70/74/7A/7F/84/89/8E:
BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_2**

6.31 REGISTER 0x44/49/4E/53/58/5D/62/67/6C/71/75/7B/80/85/8A/8F: BIQUAD4/5/6/7/8/9/10/11/12/13/14/15_3

Forth register in the 5 register set of biquad filter configuration registers. There are 16 occurrences of this register.

Field name	Bits	Access	Default	Value	Description
Biquad Coefficient A[2:0]	7:5	RW	0x0	A[2:0]	Least significant 3 bits of biquad filter coefficient A.
Biquad Coefficient B[6:2]	4:0	RW	0x00	B[6:2]	Most significant 5 bits of biquad filter coefficient B.

**Table 44: Register 0x44/49/4E/53/58/5D/62/67/6C/71/75/7B/80/85/8A/8F:
BIQUAD4/5/6/7/8/9/10/11/12/13/14/15_3**

6.32 REGISTER 0x45/4A/4F/54/59/5E/63/68/6D/72/76/7C/81/86/8B/90: BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_4

Fifth register in the 5 register set of biquad filter configuration registers. There are 16 occurrences of this register.

Field name	Bits	Access	Default	Value	Description
Biquad Functional Configuration	7:6	RW	0x3	0x0	SAT ₁ and SAT ₂ outputs forced to 0 (Reduces biquad filter to a simple gain stage)
				0x1	Negate B coefficient
				0x2	Sat ₂ output forced to 0 (Reduces biquad filter to a first order filter)
				0x3	Normal operation
Biquad Input Data Source	5:3	RW	0x4	0x0	No source signal. Input forced to 0.
				0x1	X input to biquad filters block (or Y input for odd numbered biquad filters when in repeat mode)
				0x2	Y input to biquad filters block
				0x3	Reserved for Audium use.
				0x4	Output of previous biquad filter (or output of biquad filter before previous biquad filter when in repeat mode).
				0x5	Output of biquad filter before previous biquad filter.
				0x6	Reserved for Audium use.
Biquad Coefficient A[5:3]	2:0	RW	0x0	A[5:3]	Reserved for Audium use. Most significant 3 bits of biquad filter coefficient A.

**Table 45: Register 0x45/4A/4F/54/59/5E/63/68/6D/72/76/7C/81/86/8B/90:
BIQUAD0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15_4**

6.33 REGISTER 0x91-0x92: RESERVED8-9

Registers 0x91-0x92 are reserved for Audium use. Only their default values should be written.

Register	Bits	Access	Default	Value	Description
RESERVED8	7:0	RW	0x00	-	Reserved for Audium use Always set to 0x0
RESERVED9	7:0	RW	0x00	-	Reserved for Audium use Always set to 0x0

Table 46: Register 0x91-0x92: RESERVED8-9

6.34 REGISTER 0x93: BIQUAD_SELECT

Field name	Bits	Access	Default	Value	Description
Reserved	7:4	RW	0x0		Reserved for Audium use Always set to 0x0
Biquad Register Set Switch	3:0	RW	0x0	N	Alters the default one-to-one relationship between the biquad filter register sets and the actual biquad filters.

Table 47: Register 0x93: BIQUAD_SELECT

6.35 REGISTER 0x94: AUDIO_DSP_CLIPPING

Register 0x94 reports any clipping events in the audio DSP sections, defines if such events should be 'sticky' and if they should be mapped to the nERROR pin.

Field name	Bits	Access	Default	Value	Description
Clear Sticky Flags	7	RW	0x0	0x0	Do not clear clipping flags.
				0x1	Clear audio DSP clipping flags (bits 2:0). This bit will auto reset to 0 after a write.
Sticky Enable	6	RW	0x0	0x0	Audio DSP clipping flags are not sticky.
				0x1	Audio DSP clipping flags are sticky.
Trim 2 Clipping Pin Mask	5	RW	0x0	0x0	Trim 2 clipping flag is not mapped to nERROR pin.
				0x1	Trim 2 clipping flag is mapped to nERROR pin.
Biquad Clipping Pin Mask	4	RW	0x0	0x0	Biquad filter clipping flag is not mapped to nERROR pin.
				0x1	Biquad filter clipping flag is mapped to nERROR pin.
Trim 3 Clipping Pin Mask	3	RW	0x0	0x0	Trim 3 clipping flag is not mapped to nERROR pin.
				0x1	Trim 3 clipping flag is mapped to nERROR pin.
Trim 2 Clipping Flag	2	R	0x0	0x0	Normal operation
				0x1	Clipping event detected in Trim 2 stage
Biquad Clipping Flag	1	R	0x0	0x0	Normal operation
				0x1	Clipping event detected in Biquad filters
Trim 3 Clipping Flag	0	R	0x0	0x0	Normal operation
				0x1	Clipping event detected in Trim 3 stage

Table 48: Register 0x94: AUDIO_DSP_CLIPPING

6.36 REGISTER 0x95: SOFT_RESET

Register 0x95 allows the device to be completely reset. A reset will clear all register contents and re-initialise them.

Field name	Bits	Access	Default	Value	Description
Reserved	7:1	RW	0x00		Reserved for Audium use Always set to 0x0
Soft Reset	0	RW	0x0	0x0 0x1	No action Reset the device Note that this bit self clears after the reset sequence has completed.

Table 49: Register 0x95: SOFT_RESET

6.37 REGISTER 0x96: BATTERY

Register 0x96 reports the voltage applied to the BAT pins.

Field name	Bits	Access	Default	Value	Description
Reserved	7:6	RW	0x0		Reserved for Audium use Always set to 0x0
Battery Voltage	5:0	R	-	N	The battery voltage applied to the BAT pins may be calculated from: Voltage = $(11 \times N + 624) \times 31.5 / 32768$ Note this value is only valid when using a 0.8V – 1.8V system supply voltage, and when the device is in active mode.

Table 50: Register 0x96: BATTERY

6.38 REGISTER 0xFF: OTP_CONFIG

Register 0xFF allows interaction with the OTP memory. See section 7.

Field name	Bits	Access	Default	Value	Description
OTP Read Enable	7	RW	0x0	0x0 0x1	Disable TWI read access from OTP Enable TWI read access from OTP
OTP Program Enable	6	RW	0x0	0x0 0x1	Disable OTP programming (and complete any necessary programming actions) Enable and initialise OTP for programming
Reserved	5	RW	0x0	-	Reserved for Audium use Always set to 0x0
Reserved	4:3	R	0x0	-	Reserved for Audium use
OTP Status: Programming Failed	2	R	0x0	0x0 0x1	Programming successful Programming failed This bit is automatically cleared on entry to programming mode
OTP Status: Operation failed	1	R	0x0	0x0 0x1	Operation successful Operation failed This bit is automatically cleared at the start of an OTP write
OTP Status: Busy	0	R	0x0	0x0 0x1	OTP ready OTP busy

Table 51: Register 0xFF: OTP_CONFIG

7 ONE-TIME-PROGRAMMABLE MEMORY

The AS2002 includes OTP (One Time Programmable) memory that may be used to predefine register defaults after a reset.

The OTP memory shadows the internal device registers, and is split in to two blocks:

- Configuration OTP: shadows registers 0x00 to 0x39 (inclusive)
- Audio DSP OTP: shadows registers 0x3A to 0x90 (inclusive)

Note that registers 0x91 to 0x96 (inclusive) and 0xFF are not shadowed by the OTP.

7.1 POST-RESET DEVICE INITIALISATION FROM OTP MEMORY

Following a device reset, values in the OTP memory are copied from the OTP memory in to corresponding TWI registers according to the procedure shown in Figure 43 below.

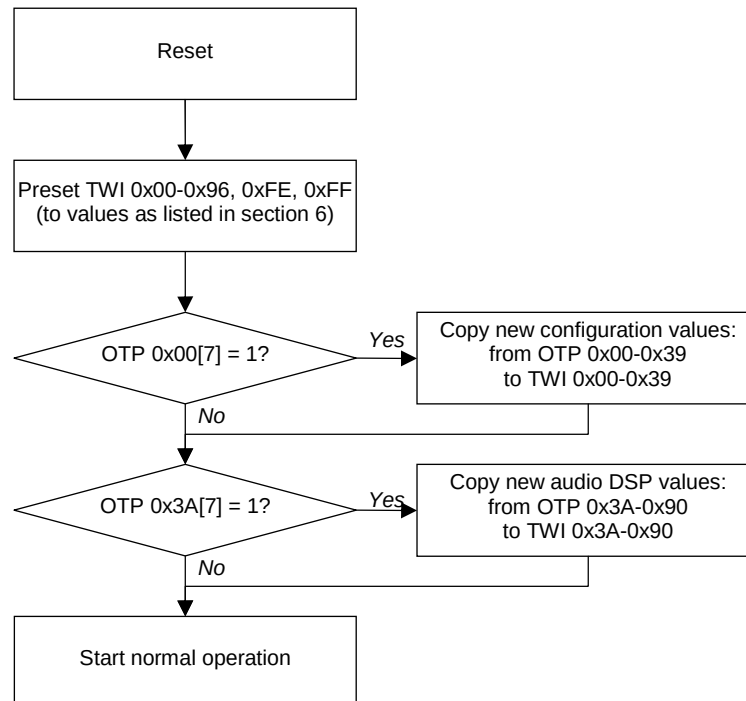


Figure 43: OTP post-reset read procedure

This post-reset copy procedure can take up to up to $217.6 / \text{InternalOscillatorClockMHz}$ ms to complete. Registers should not be written to (via the TWI bus) until this copy procedure has been completed. Any TWI reads or writes performed during this time will not be acknowledged.

7.2 OTP MEMORY READ PROCEDURE

One can read the contents of the OTP memory over the TWI bus.

Similar to normal TWI operations, auto-register-address-incrementing allows successive OTP memory locations to be read in a single TWI transaction.

During an OTP read procedure all TWI writes (except to register 0xFF) will be ignored.

The OTP read procedure is shown in Figure 44 below.

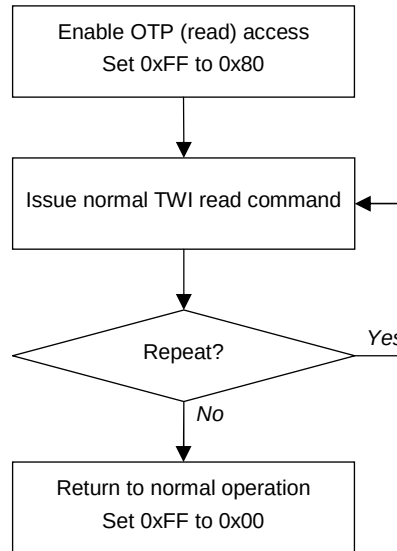


Figure 44: OTP read procedure

7.3 OTP MEMORY WRITE PROCEDURE

As the name suggests, OTP memory may only be written to once. OTP bits are initially zero and may be set to a one; once an OTP bit location has been set to a one it cannot be changed.

Each block has a dedicated access control bit:

- Configuration OTP: OTP [0x00\[7\]](#)
- Audio DSP OTP: OTP [0x3A\[7\]](#)

Like all OTP bits, the access control bits are initially zero. Once the relevant access control bit has been set then all subsequent writes to that OTP block will be acknowledged (but ignored), and following all subsequent reset events that block's OTP values will be copied in to the TWI registers.

Setting an access control bit to a one should therefore always be the last OTP write within that block.

An OTP write is a bit like burning a fuse and there is a small probability that the first attempt to write the data may fail. The OTP controller therefore automatically checks the data actually written to the OTP memory and reports a success or fail condition.

- On enabling OTP write access [0xFF\[2\]](#) is automatically cleared. If any subsequent OTP writes fail [0xFF\[2\]](#) is automatically set to indicate that a write failed.
- On starting an individual OTP register write [0xFF\[1\]](#) is automatically cleared. If the write fails [0xFF\[1\]](#) is automatically set to indicate that this write failed.

The time taken to perform an OTP write varies and depends upon the number of bits to be set to a 1. The (absolute worst case) maximum time for an OTP write is $280/\text{StandbySystemClockMHz}$ ms.

If an OTP write fails then it should be repeated.

During an OTP write procedure all TWI reads (except to register 0xFF) will return 0.

OTP writes should only be performed in active mode; never in standby mode.

The OTP write procedure is shown in Figure 45 below.

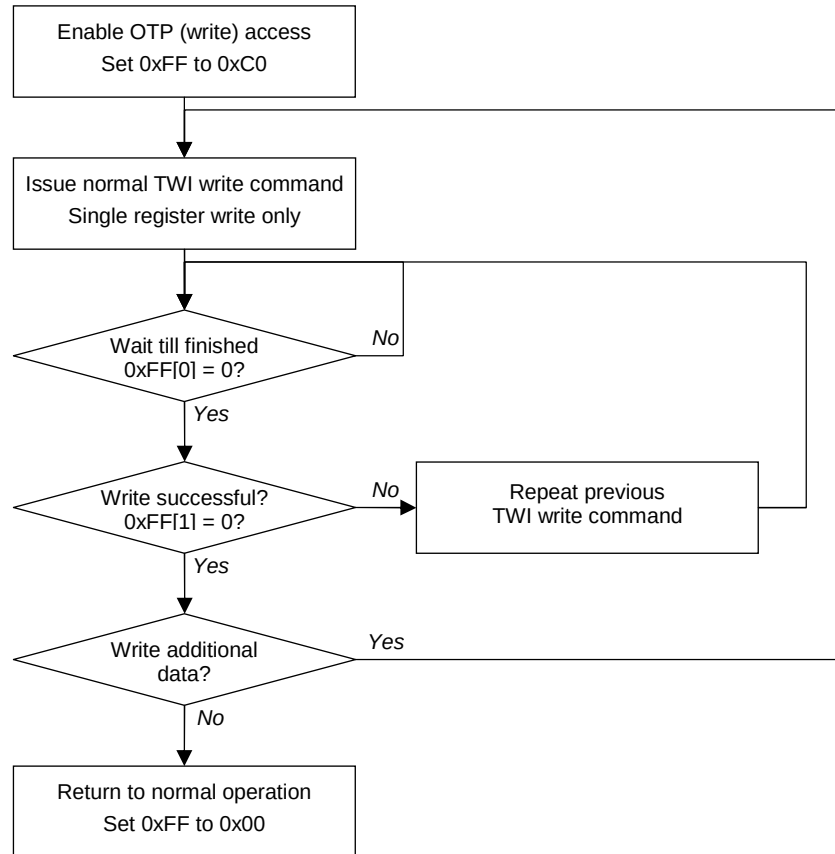


Figure 45: OTP write procedure, single register writes

Similar to normal TWI operations, auto-register-address-incrementing allows successive OTP memory locations to be written to in a single TWI transaction.

The OTP controller will always acknowledge the first data byte written, and start the OTP write procedure. However the OTP write procedure may not have finished before the host sends the next data byte to be written. In this case the OTP controller will not acknowledge the data byte. The host should continue to resend the same data byte until the OTP controller is ready, at which point it will acknowledge the byte and start writing it to the next OTP memory location.

At the end of the multiple register write the host should check [0xFF\[2\]](#) to see if any errors occurred during the write process. If there were any errors the whole process should be repeated.

The OTP multi-byte write procedure is shown in Figure 46 below.

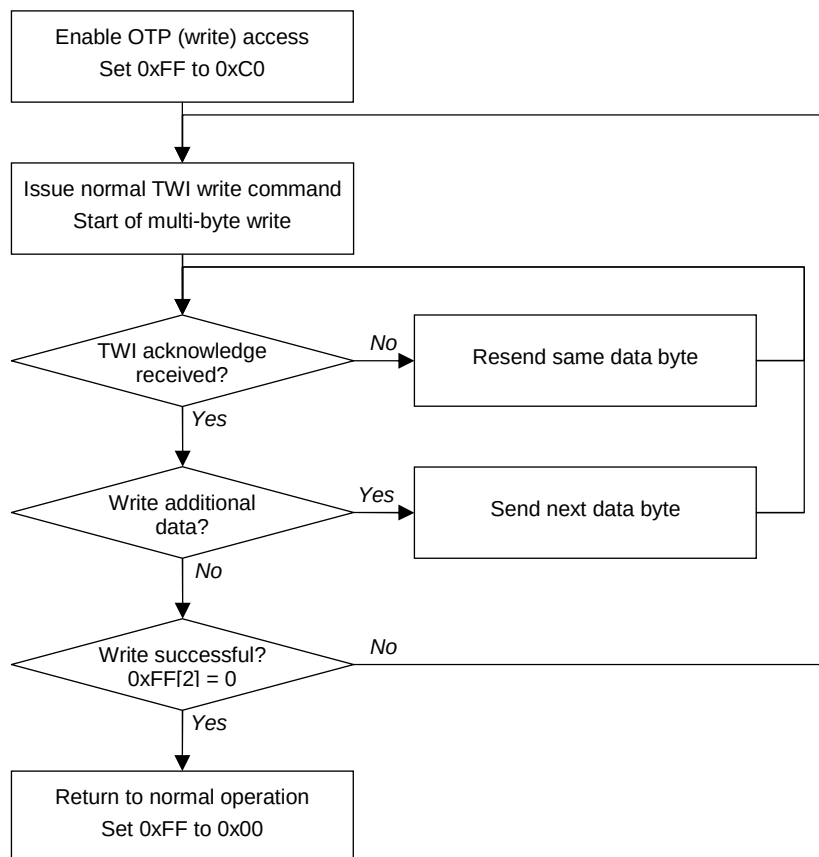


Figure 46: OTP write procedure, multiple register writes

7.4 SPECIAL OTP MEMORY LOCATIONS

Not all OTP memory locations shadow a TWI register. Some locations exist only in OTP.

7.4.1 OTP 0x92: DEVICE_ID

OTP 0x92 reports the device ID.

Field name	Bits	Access	Default	Value	Description
Device ID	7:0	R	-	0x02 AS2002-QNC-050	

Table 52: OTP 0x92: DEVICE_ID

8 PERFORMANCE DATA

To be completed.

The maximum bit clock input frequency is 4.608MHz.

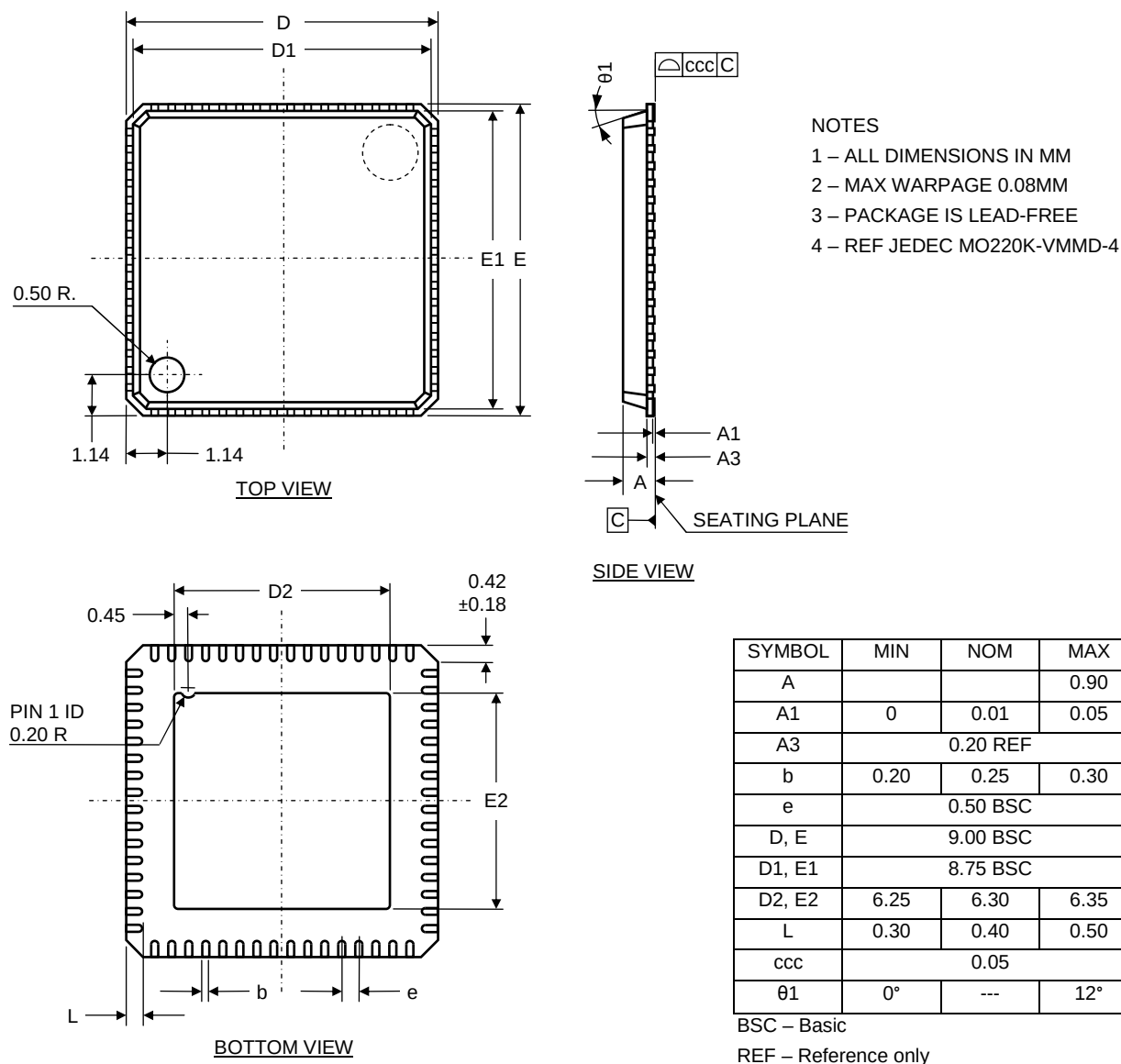
The maximum word-select clock input frequency is 48kHz.

The maximum external clock input frequency is 50MHz.

There is 5ms of audio latency through the AS2002.

The minimum load is 8ohms/channel

9 PACKAGE INFORMATION



QFN64 PUNCH TYPE

Figure 47: QFN-64 package

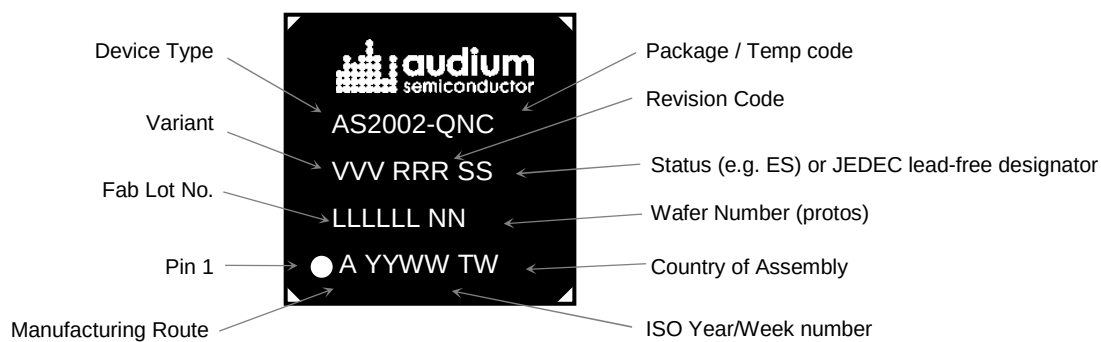


Figure 48: QFN-64 package example marking