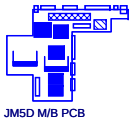
AZEDA-INTEGRATED
Pb-Free

PWA: MF788, SCHEM: CD623
VER : 3A



RUN POWER SW PG 48

AC/BATT CONNECTOR PG 50

BATT SELECTOR PG 43

BATT CHARGER PG 44

Dothan/Yonah
(478 Micro-FCPGA)
PG 4,5

DC/DC +3V_SRC +5VSUS PG 47

CPU VR PG 45

CLOCKS PG 16

RESET CKT PG 42

Panel Connector PG 20

4X133MHZ

LVDS

Alviso
1257 PCBGA
PG 6,7,8,9,10

sDVO

SI1362 PG 17

DVI

TVOUT

I/O(S-Video) PG 33

VGA

VGA PG 21

DDR-SODIMM1 PG 14,15

400/533 MHZ DDR II

DDR-SODIMM2 PG 14,15

400/533 MHZ DDR II

DMI interface

USB2.0 (P5,P7)

USB2.0 (P4,P6)

2 Rear Ports PG 29

2 Right Side(I/O) PG 33

USB2.0 (P1)

PATA - HDD PG 22

88SA8040 PG 22

SATA

ICH6-M
609 BGA
PG 11,12,13

33MHz PCI

Q-SWITCH PG 40

DOCKING CONNECTOR PG 41

CARDBUS PCI6515 PG 24

PCMCIA CON. PG 24

MINI-PCI Wireless LAN PG 25

Internal Media Bay CD-ROM PG 22

IDE

USB2.0 1 port(P0)

AC97

USB2.0 (P3)

USB2.0 (P2)

Bluetooth PG 32

LPC

PCIEx1

BroadCom Lan(5751) PG 37

E-Switch PI3L500 PG 38

I/O(RJ45/Magnetics) PG 33

AUDIO PG 35,36

MDC PG 26

SIO(Macallan 3)
256 Pins LBGA
PG 27,28

DOCK LPC

S/PDIF to DOCK PG 41

Audio Jacks PG 36

RJ11 to DOCK PG 41

Tip Ring PG 26

X-Bus

PS/2

IrDA PG 39

Keyboard PG 39

Serial PG 28

Parallel PG 29

Touchpad/ Stick point PG 32

Flash PG 31

QUANTA COMPUTER

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INDEX

Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Blank Page	
3	Front Page	
4-5	Dothan	
6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3.3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#/5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
GND	ALL PAGES	DIGITAL GROUND	
GNDP		CPU POWER GND	
CGNDP		CHARGER GND	
DGNDP		DC/DC POWER GND	
LANGND		COMBO CONN GND	

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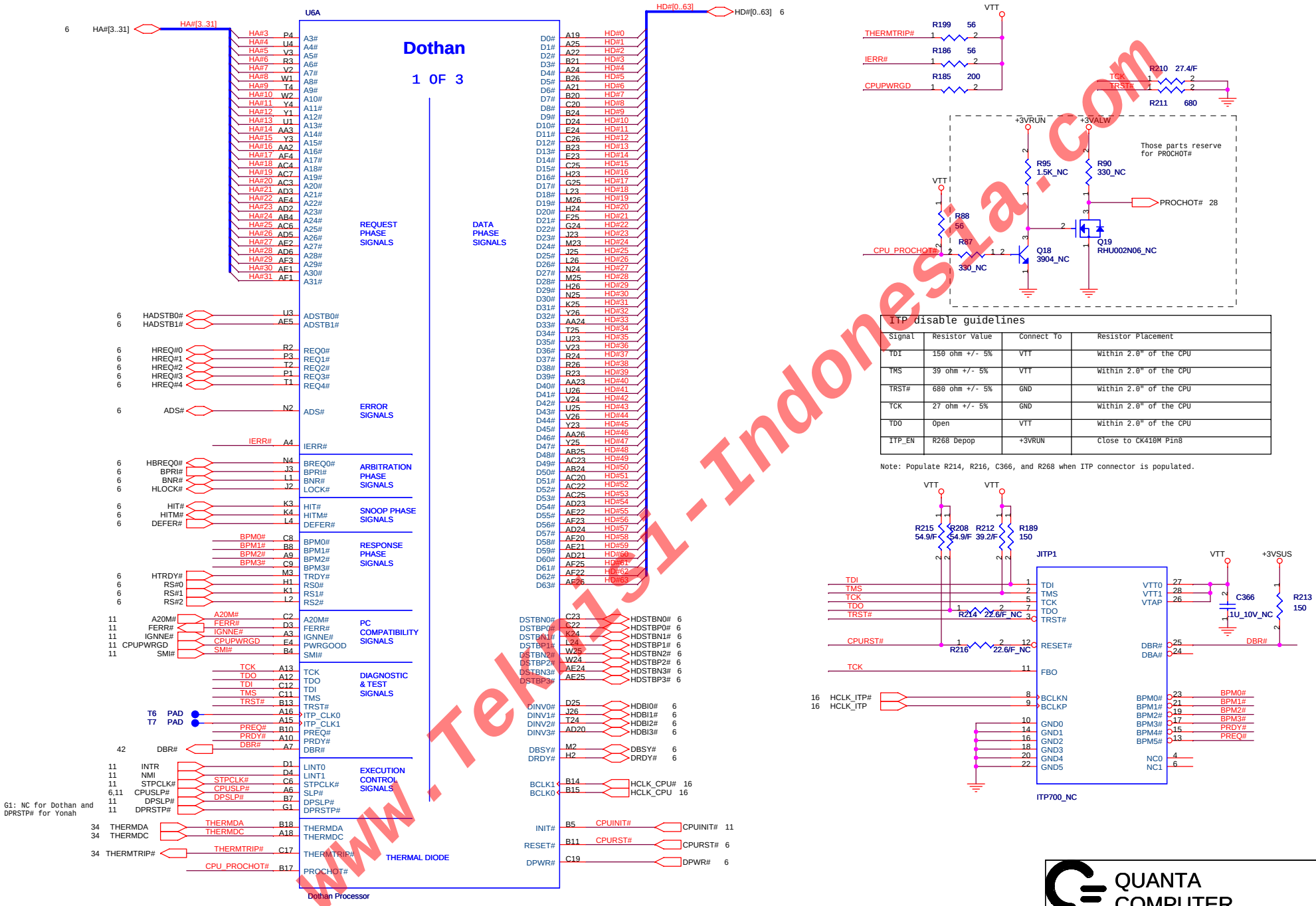

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

Note: Populate R214, R216, C366, and R268 when ITP connector is populated.

QUANTA COMPUTER

Title	Dothan Processor (HOST)	
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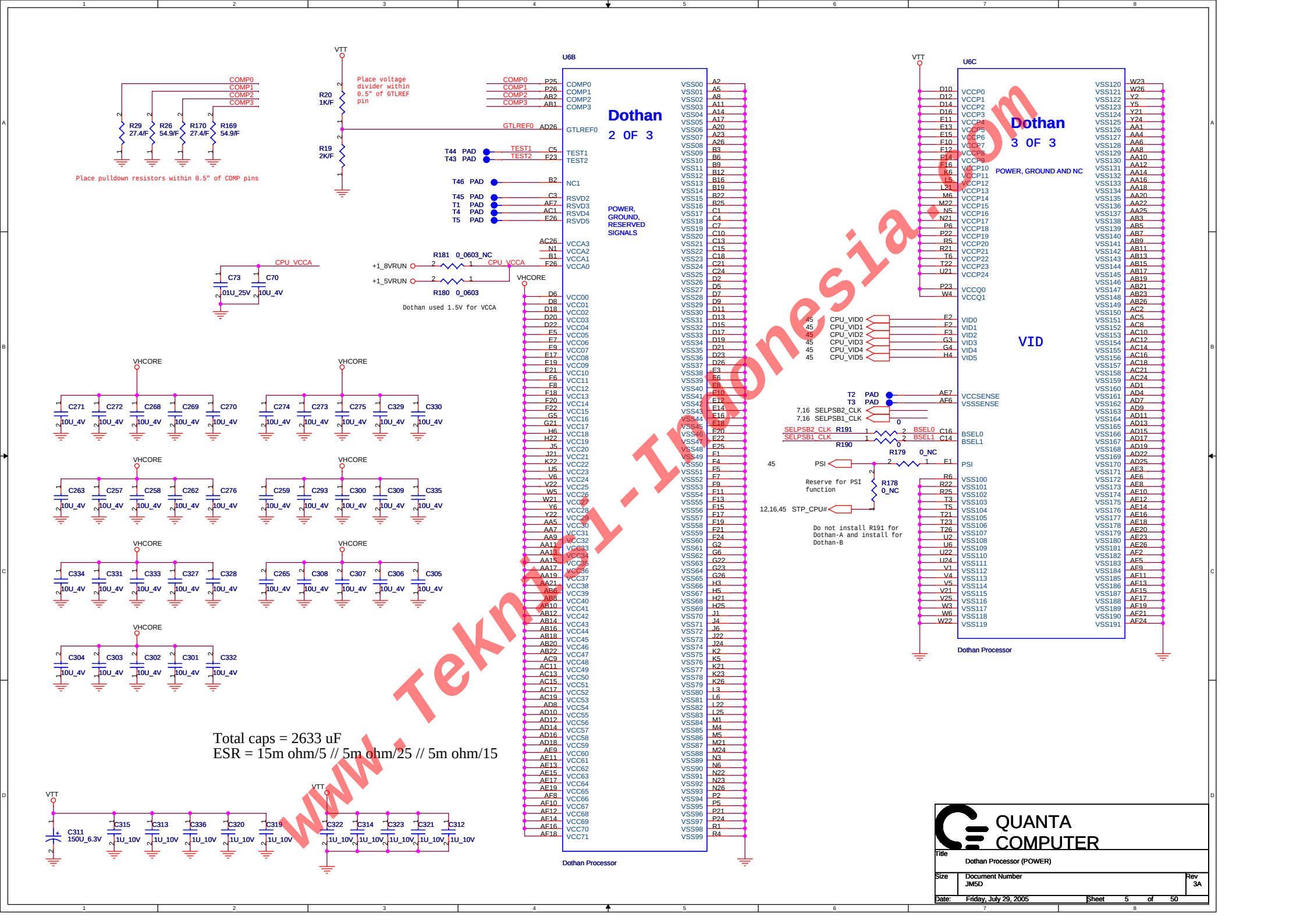

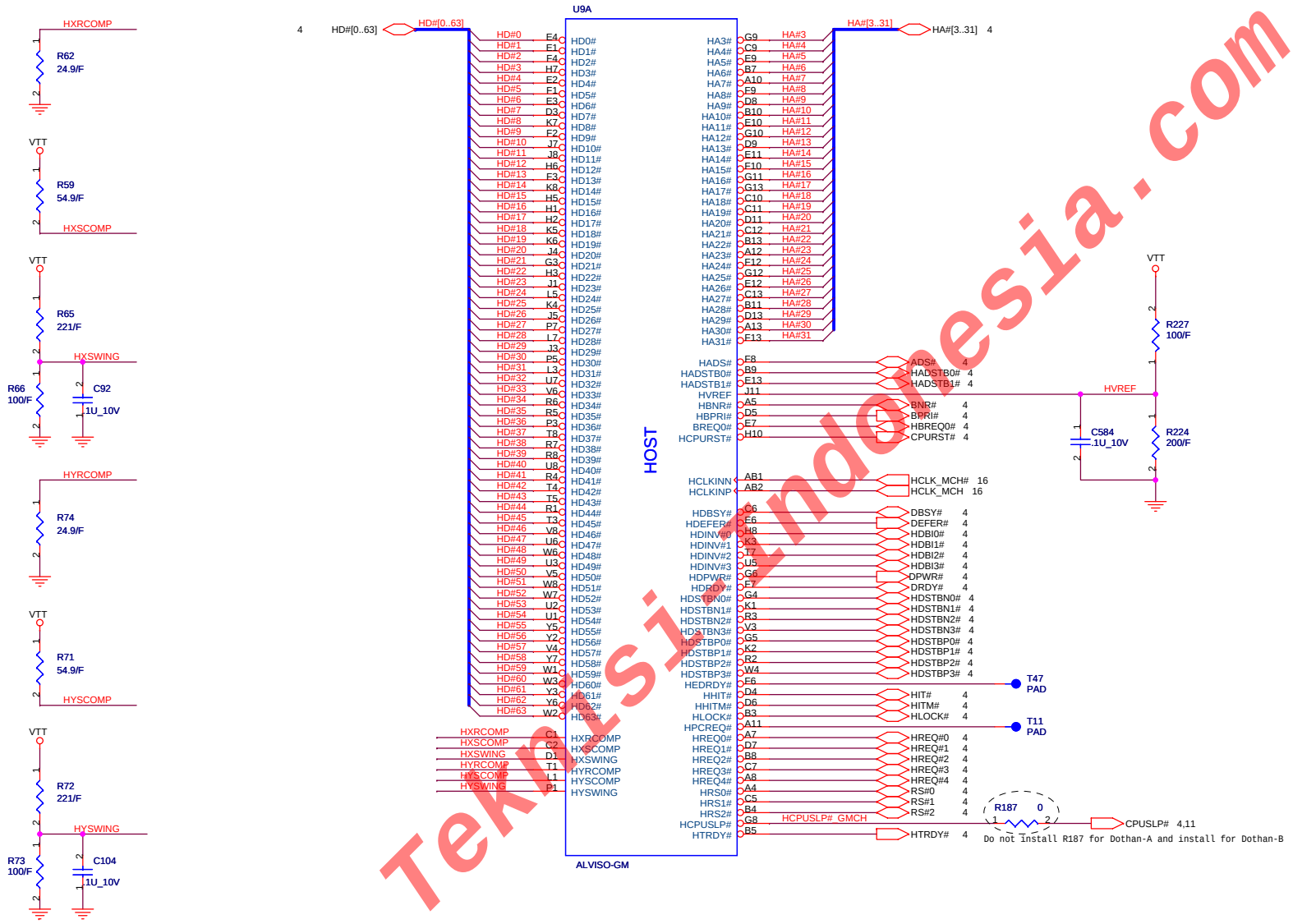

QUANTA COMPUTER

Title	Alviso (Host)	
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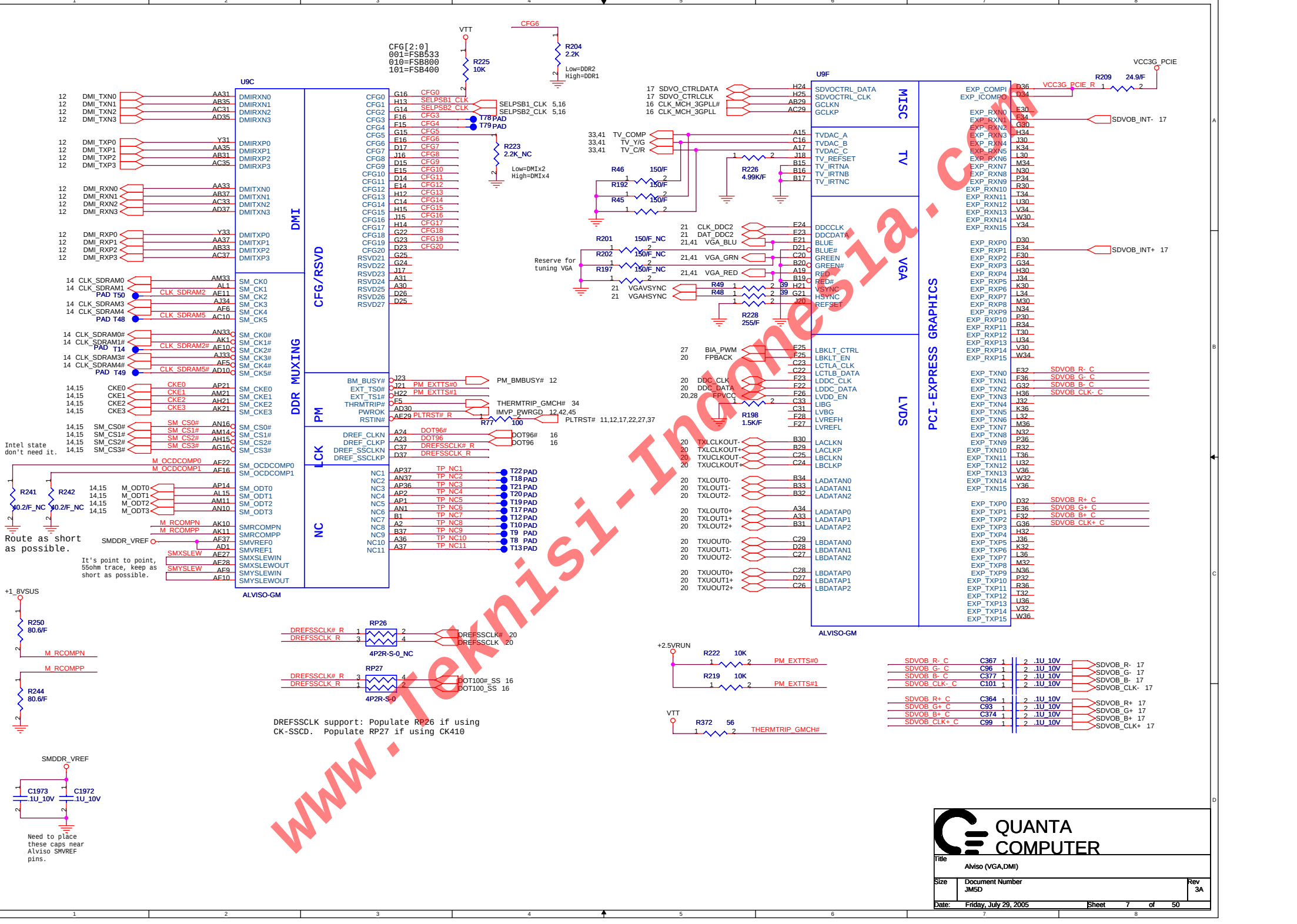

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Title	Alviso (DDR)	
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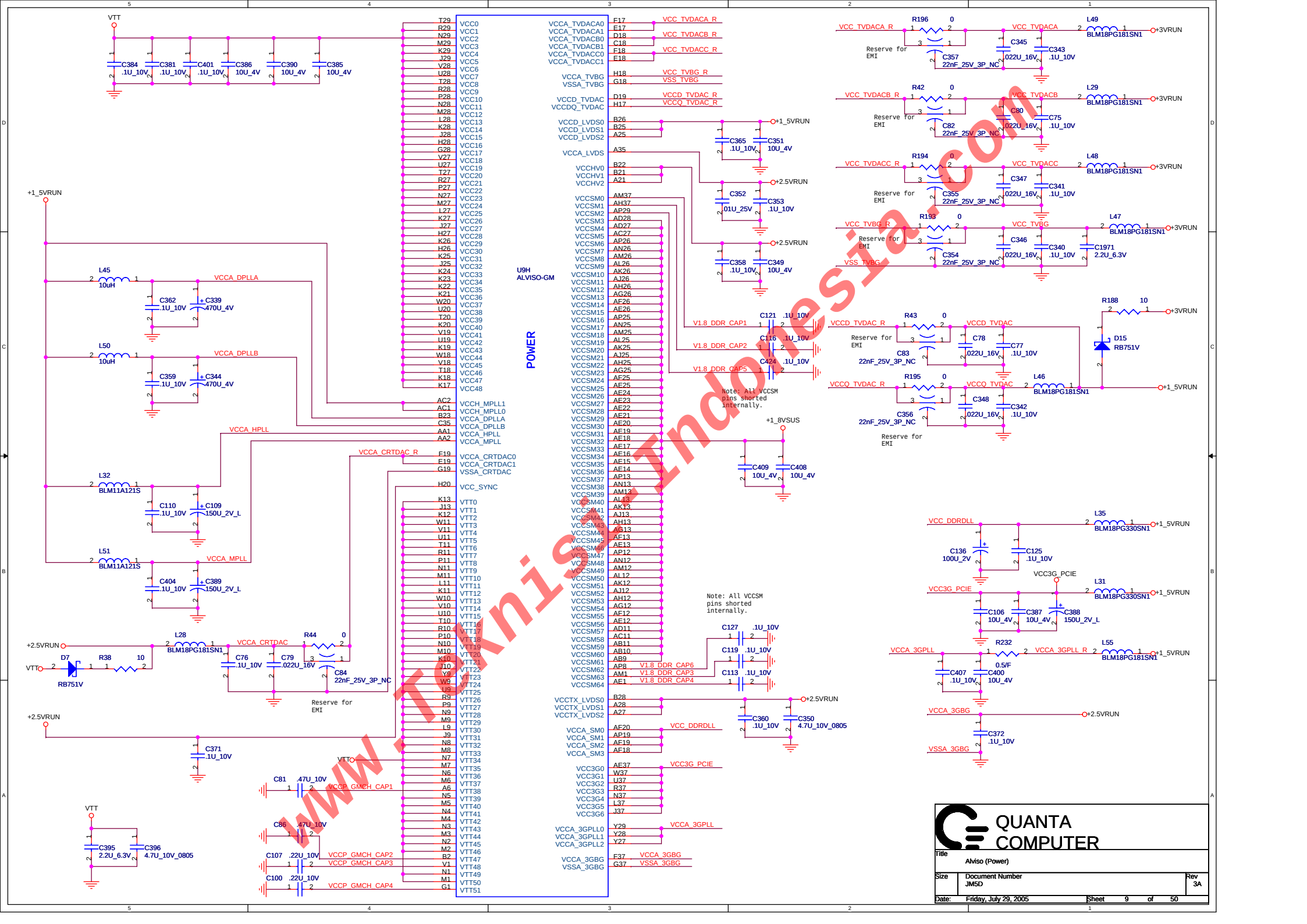

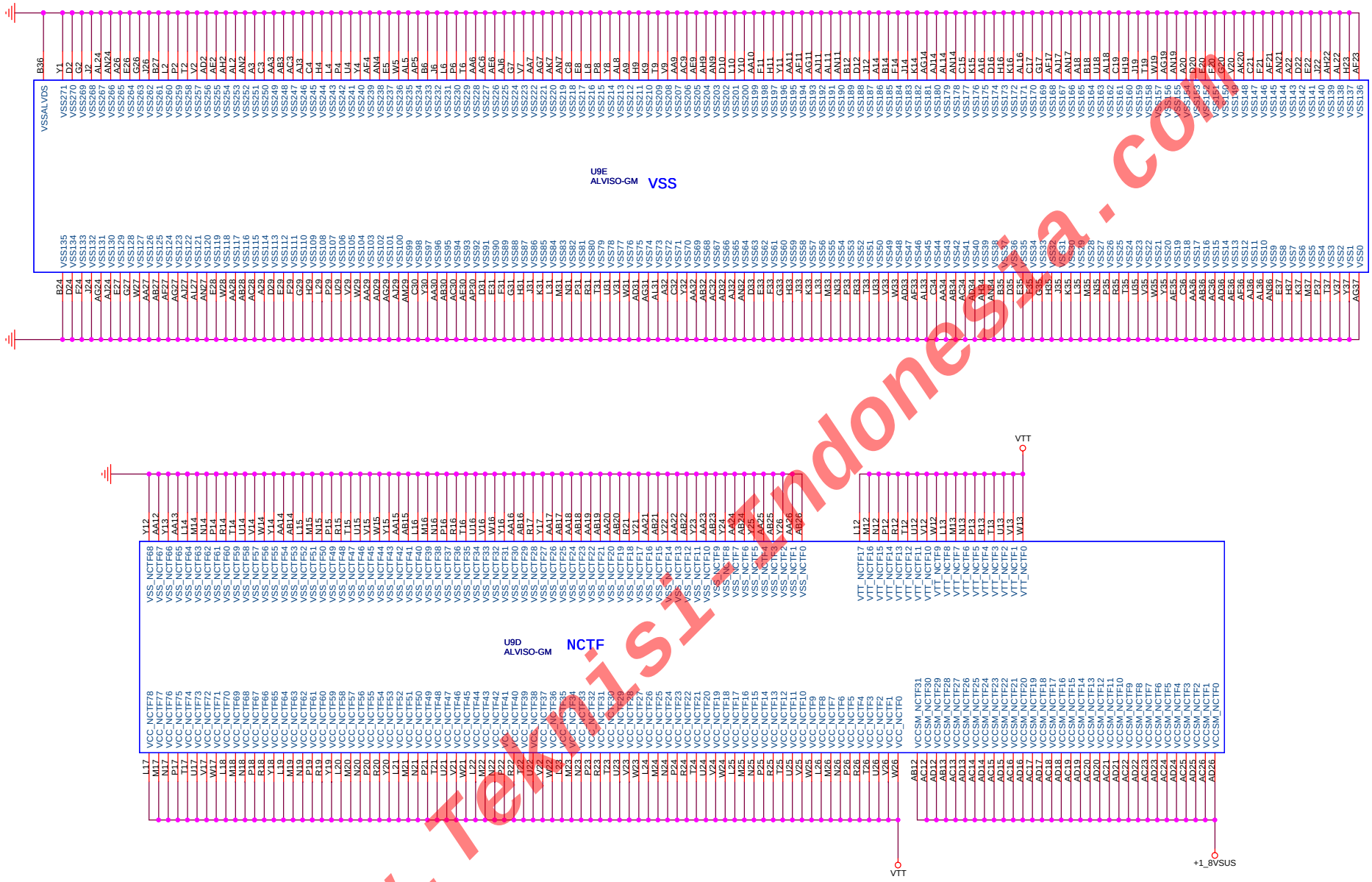

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Title	Alviso (VSS,NCTF)	
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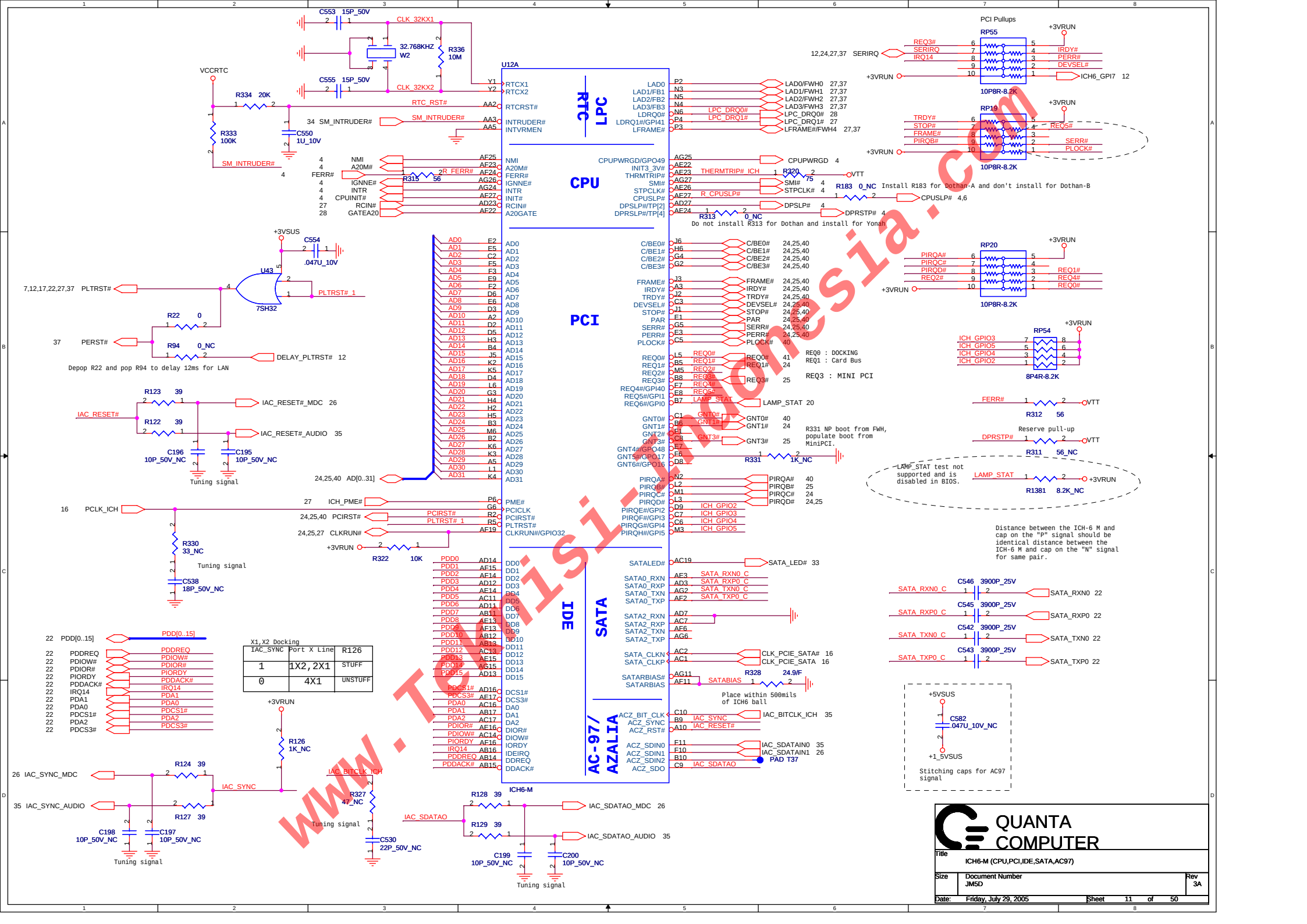

Title	ICH6-M (CPU,PCI,IDE,SATA,AC97)	
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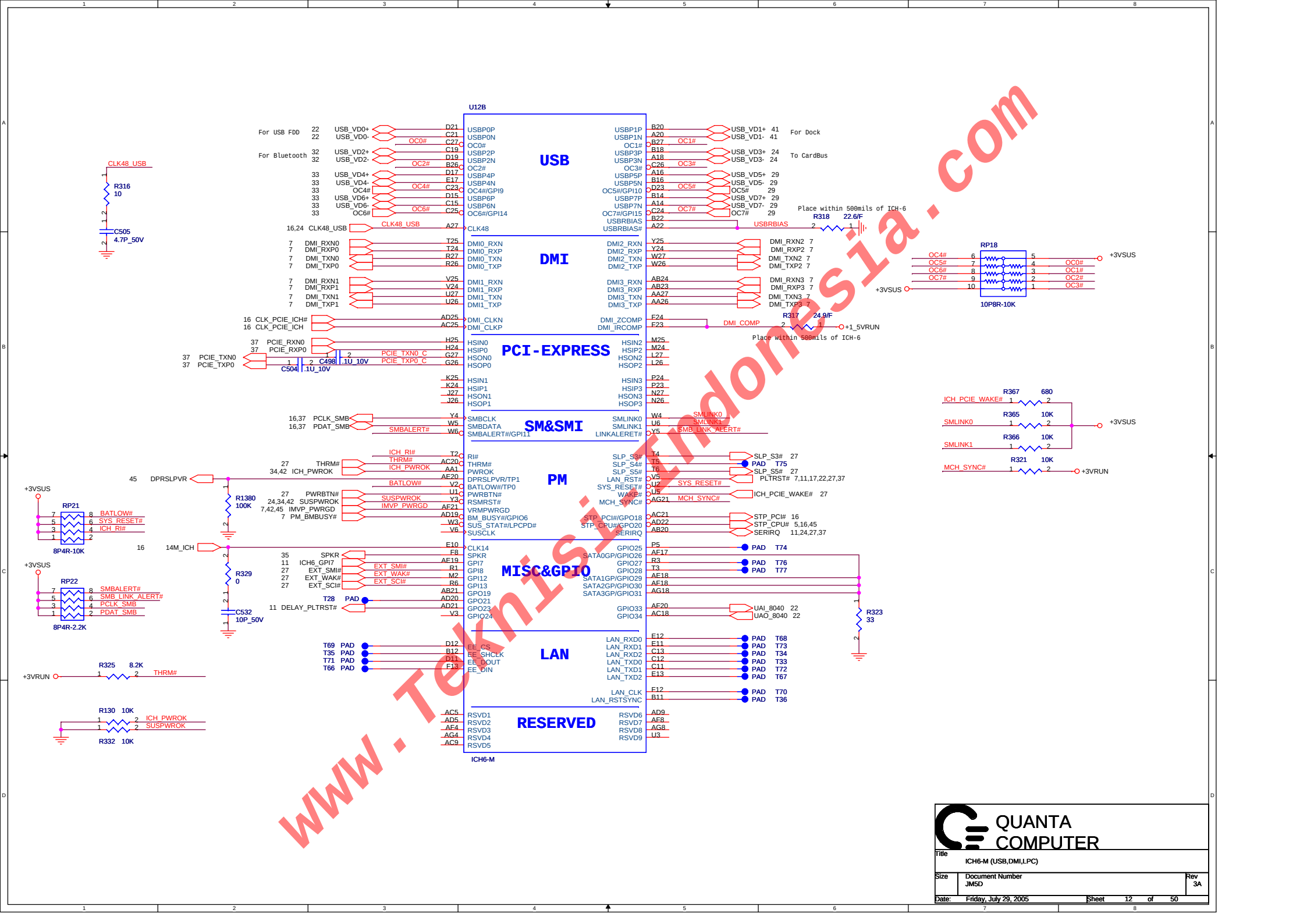

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Title	ICH6-M (USB,DMI,LPC)	
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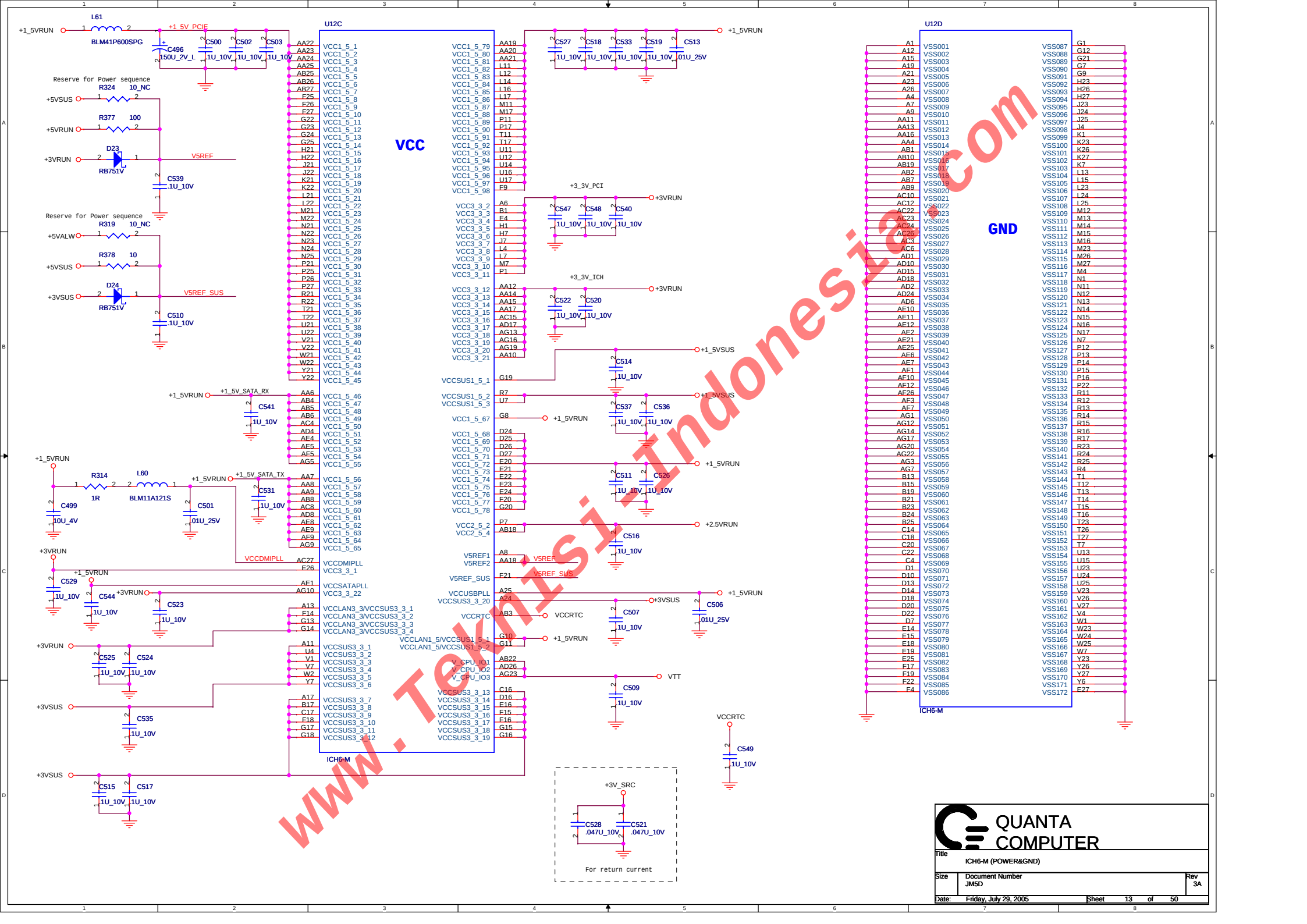

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Title	ICH6-M (POWER&GND)	
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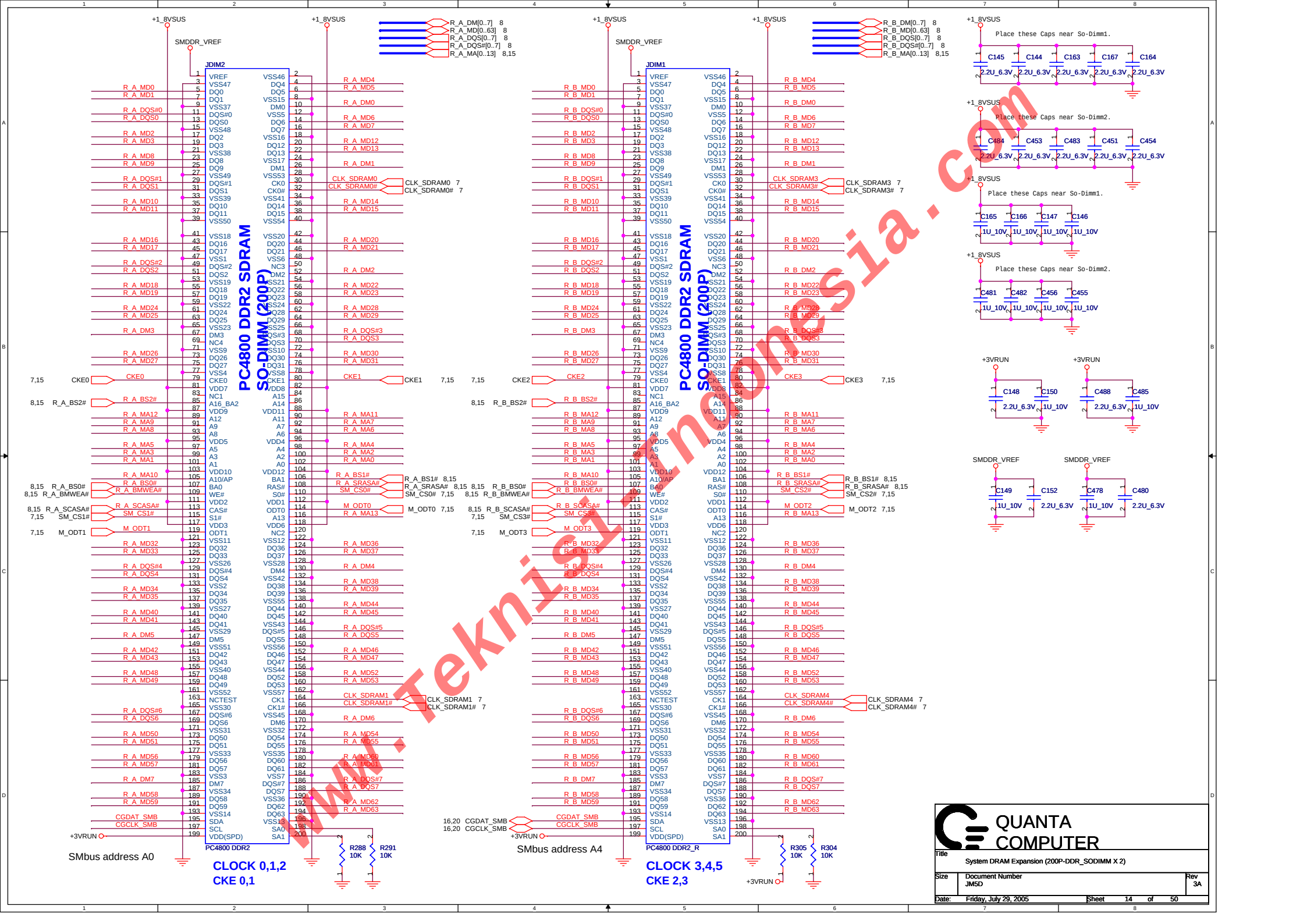
JDIM2
PC4800 DDR2 SDRAM SO-DIMM (200P)
PC4800 DDR2
SMDDR_VREF
+1_8VSUS
+3VRUN
R_A_DM[0..7] 8
R_A_MD[0..63] 8
R_A_DQS[0..7] 8
R_A_DQS#[0..7] 8
R_A_MA[0..13] 8,15
CLK_SDRAM0 7
CLK_SDRAM0# 7
CKE0 7,15
CKE1 7,15
R_A_BS2# 8,15
R_A_BS0# 8,15
R_A_BMWEA# 8,15
R_A_SCASA# 8,15
SM_CS1# 7,15
M_ODT1 7,15
R_A_BS1# 8,15
R_A_SRASA# 8,15
SM_CS0# 7,15
M_ODT0 7,15
CLK_SDRAM1 7
CLK_SDRAM1# 7
R_A_DQS#6
R_A_DQS6
CGDAT_SMB
CGCLK_SMB
R288 10K
R291 10K
SMbus address A0
CLOCK 0,1,2
CKE 0,1
JDIM1
PC4800 DDR2 SDRAM SO-DIMM (200P)
PC4800 DDR2_R
R_B_DM[0..7] 8
R_B_MD[0..63] 8
R_B_DQS[0..7] 8
R_B_DQS#[0..7] 8
R_B_MA[0..13] 8,15
CLK_SDRAM3 7
CLK_SDRAM3# 7
CKE2 7,15
CKE3 7,15
R_B_BS2# 8,15
R_B_BS0# 8,15
R_B_BMWEA# 8,15
R_B_SCASA# 8,15
SM_CS3# 7,15
M_ODT3 7,15
R_B_BS1# 8,15
R_B_SRASA# 8,15
SM_CS2# 7,15
M_ODT2 7,15
CLK_SDRAM4 7
CLK_SDRAM4# 7
R_B_DQS#6
R_B_DQS6
16,20 CGDAT_SMB
16,20 CGCLK_SMB
R305 10K
R304 10K
SMbus address A4
CLOCK 3,4,5
CKE 2,3
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
C145 C144 C163 C167 C164
C484 C453 C483 C451 C454
C165 C166 C147 C146
C481 C482 C456 C455
C148 C150
C488 C485
C149 C152
C478 C480
2.2U_6.3V
1U_10V
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System DRAM Expansion (200P-DDR_SODIMM X 2)
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R_A_MA[0..13] 8,14

R_B_MA[0..13] 8,14

SMDDR_VTERM

C494 C495 C493 C492 C491 C490 C489 C442 C441 C445 C444 C443 C440
1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

SMDDR_VTERM

C187 C191 C135 C186 C188 C189 C190 C129 C134 C130 C131 C132 C133
1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V 1U_10V

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

8,14 R_A_SRASA#
8,14 R_A_BS1#
R_A_MA7 R_A_MA11 R_A_MA4 R_A_MA6 R_A_SRASA# R_A_BS1# RP42 RP43 RP45 4P2R-S-56
SMDDR_VTERM

7,14 M_ODT0
8,14 R_A_BS2#
R_A_MA13 M_ODT0 R_A_BS2# R_A_MA12 R_A_MA9 R_A_MA8 R_A_MA5 R_A_MA3 RP46 RP49 RP50 RP51 4P2R-S-56
SMDDR_VTERM

8,14 R_A_BS0#
8,14 R_A_BMWEA#
8,14 R_A_SCASA#
R_A_MA10 R_A_BS0# R_A_BMWEA# R_A_SCASA# R_A_MA0 R_A_MA2 RP52 RP53 RP44 4P2R-S-56
SMDDR_VTERM

8,14 R_B_SRASA#
8,14 R_B_BS1#
R_B_SRASA# R_B_BS1# R_B_MA12 R_B_MA9 R_B_MA8 R_B_MA5 RP14 RP11 RP10 4P2R-S-56
SMDDR_VTERM

R_B_MA3 R_B_MA1 R_B_MA10 R_B_BS0# R_B_BMWEA# R_B_SCASA# R_B_MA7 R_B_MA11 RP9 RP8 RP7 RP17 4P2R-S-56
8,14 R_B_BS0#
8,14 R_B_BMWEA#
8,14 R_B_SCASA#
SMDDR_VTERM

R_B_MA4 R_B_MA6 R_B_MA0 R_B_MA2 R_B_MA13 M_ODT2 RP16 RP15 RP13 4P2R-S-56
7,14 M_ODT2
SMDDR_VTERM

7,14 CKE0
7,14 CKE1
7,14 CKE2
7,14 CKE3
CKE0 CKE1 CKE2 CKE3 R306 R287 R110 R119 56
SMDDR_VTERM

7,14 SM_CS0#
7,14 SM_CS1#
7,14 SM_CS2#
7,14 SM_CS3#
SM_CS0# SM_CS1# SM_CS2# SM_CS3# R286 R307 R120 R108 56
SMDDR_VTERM

7,14 M_ODT1
7,14 M_ODT3
8,14 R_B_BS2#
M_ODT1 M_ODT3 R_A_MA1 R_B_BS2# R308 R107 R309 R109 56
SMDDR_VTERM

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Title	DDR RES.ARRAY	
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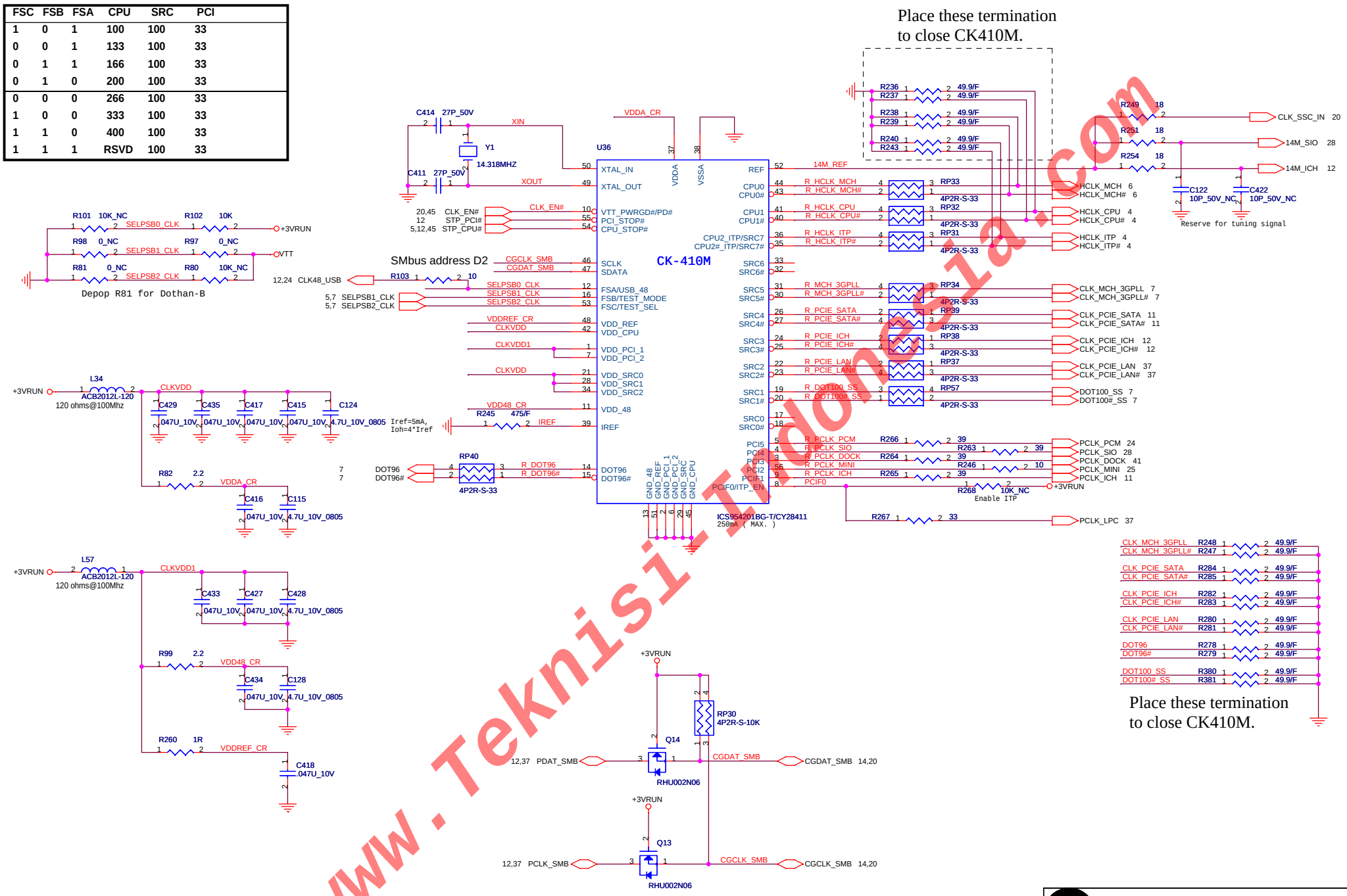
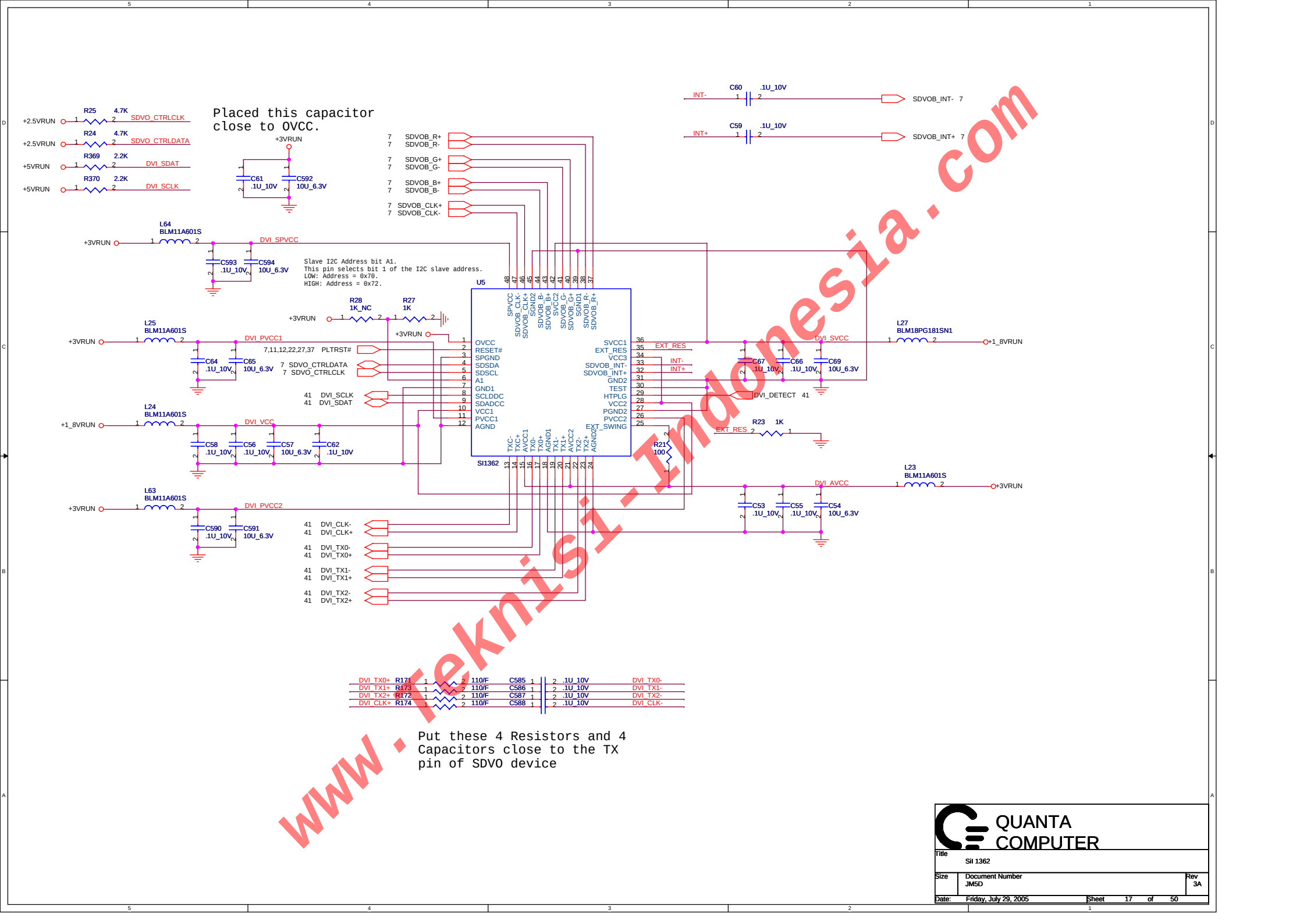
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33




Placed this capacitor close to OVCC.
Slave I2C Address bit A1.
This pin selects bit 1 of the I2C slave address.
LOW: Address = 0x70.
HIGH: Address = 0x72.
SI1362
Put these 4 Resistors and 4 Capacitors close to the TX pin of SDVO device
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Sil 1362
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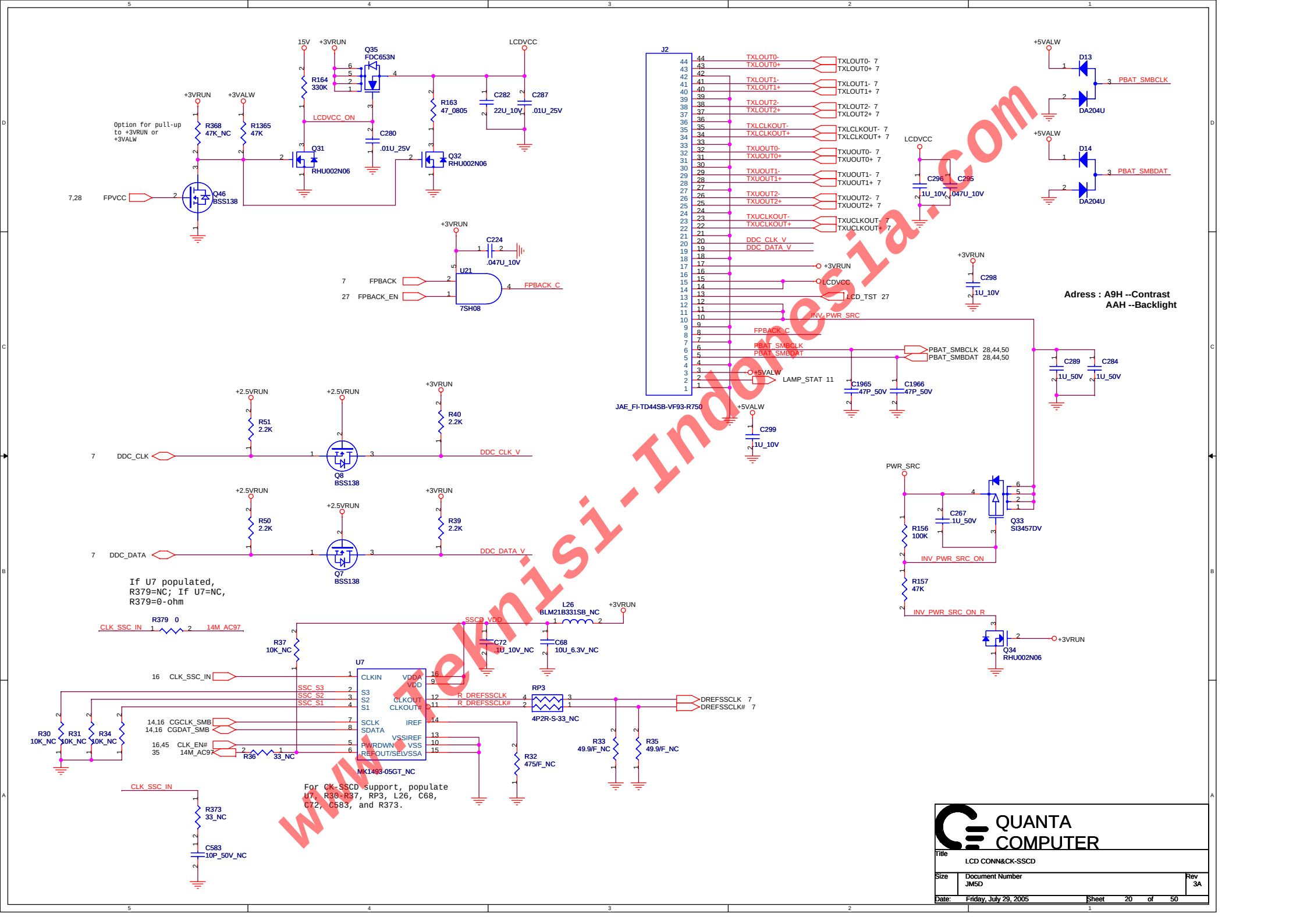

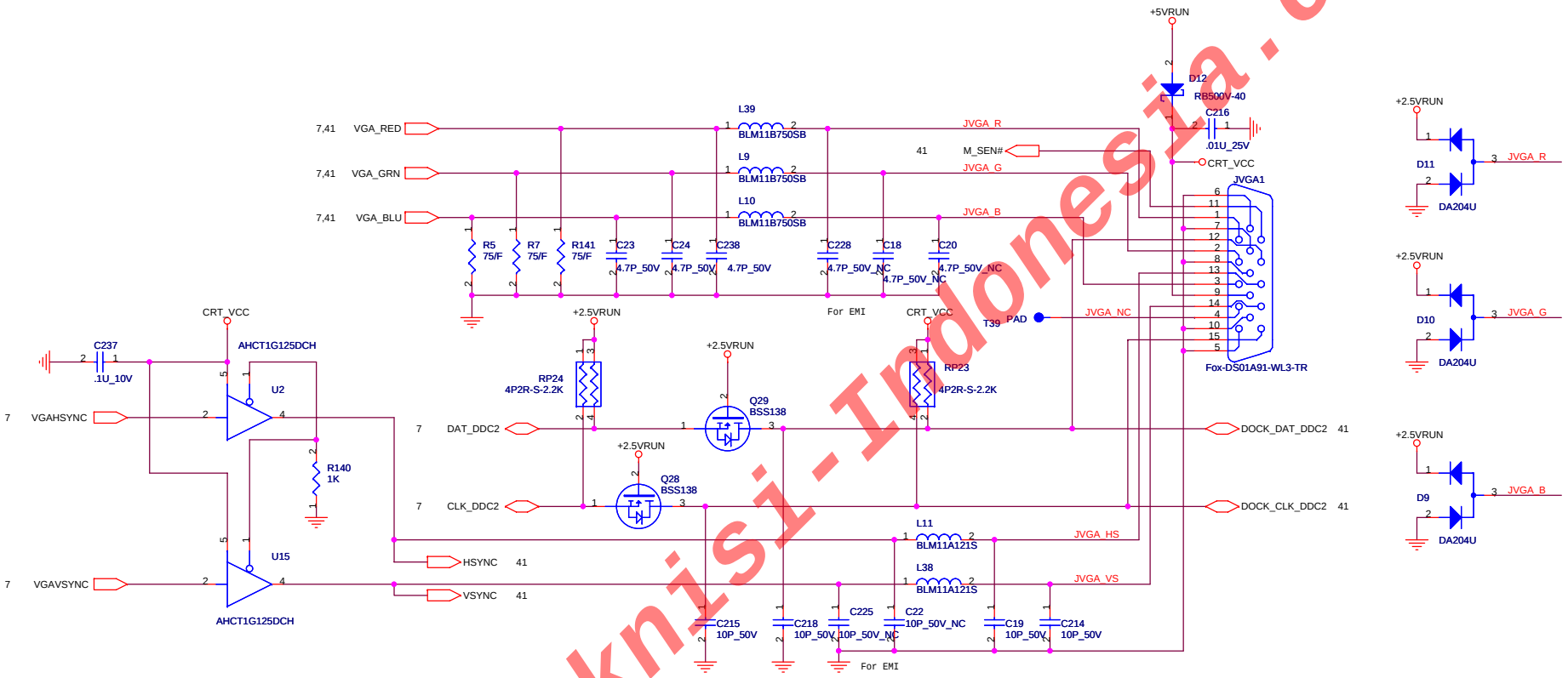

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Title	CRT&TV CONN	
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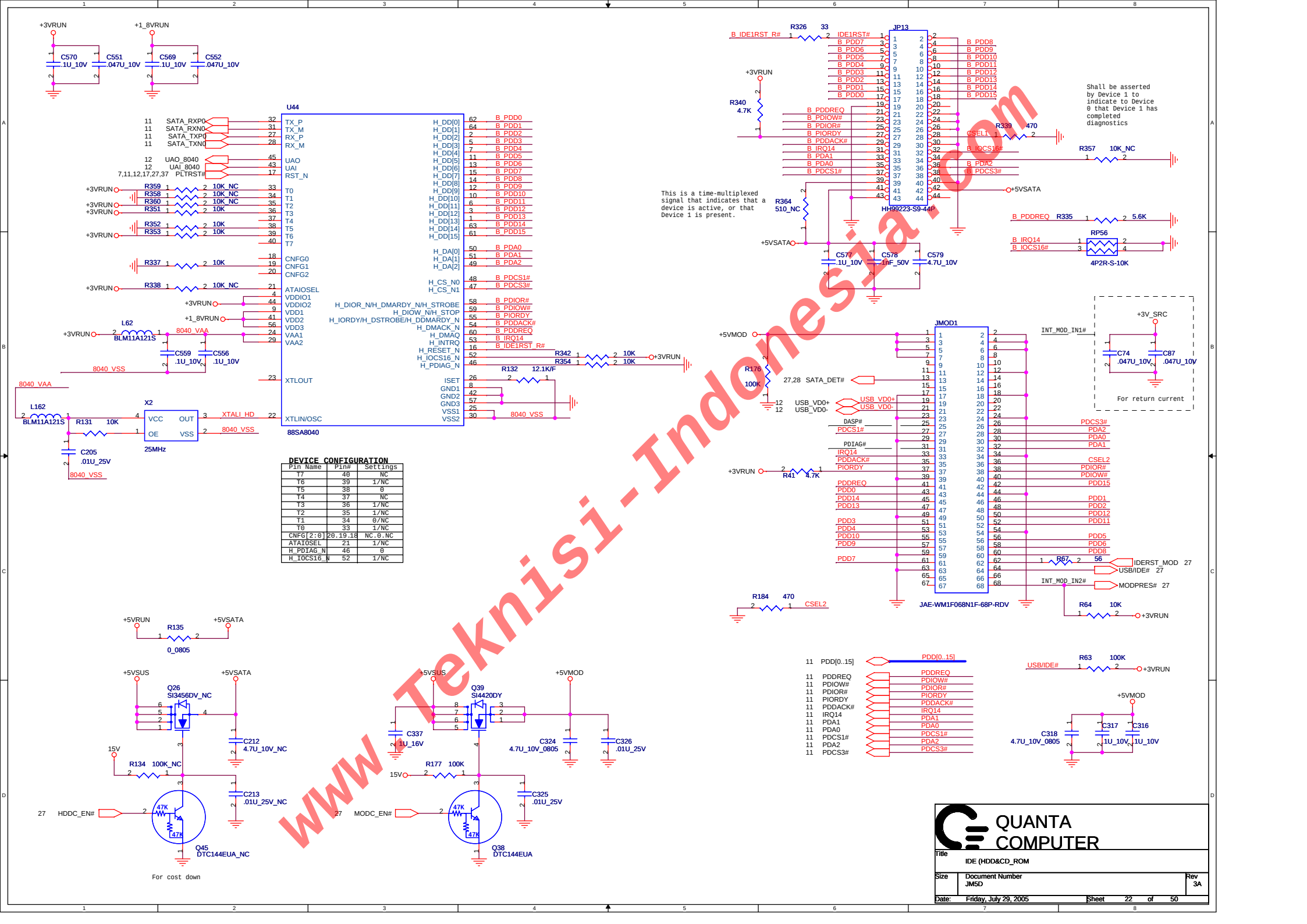

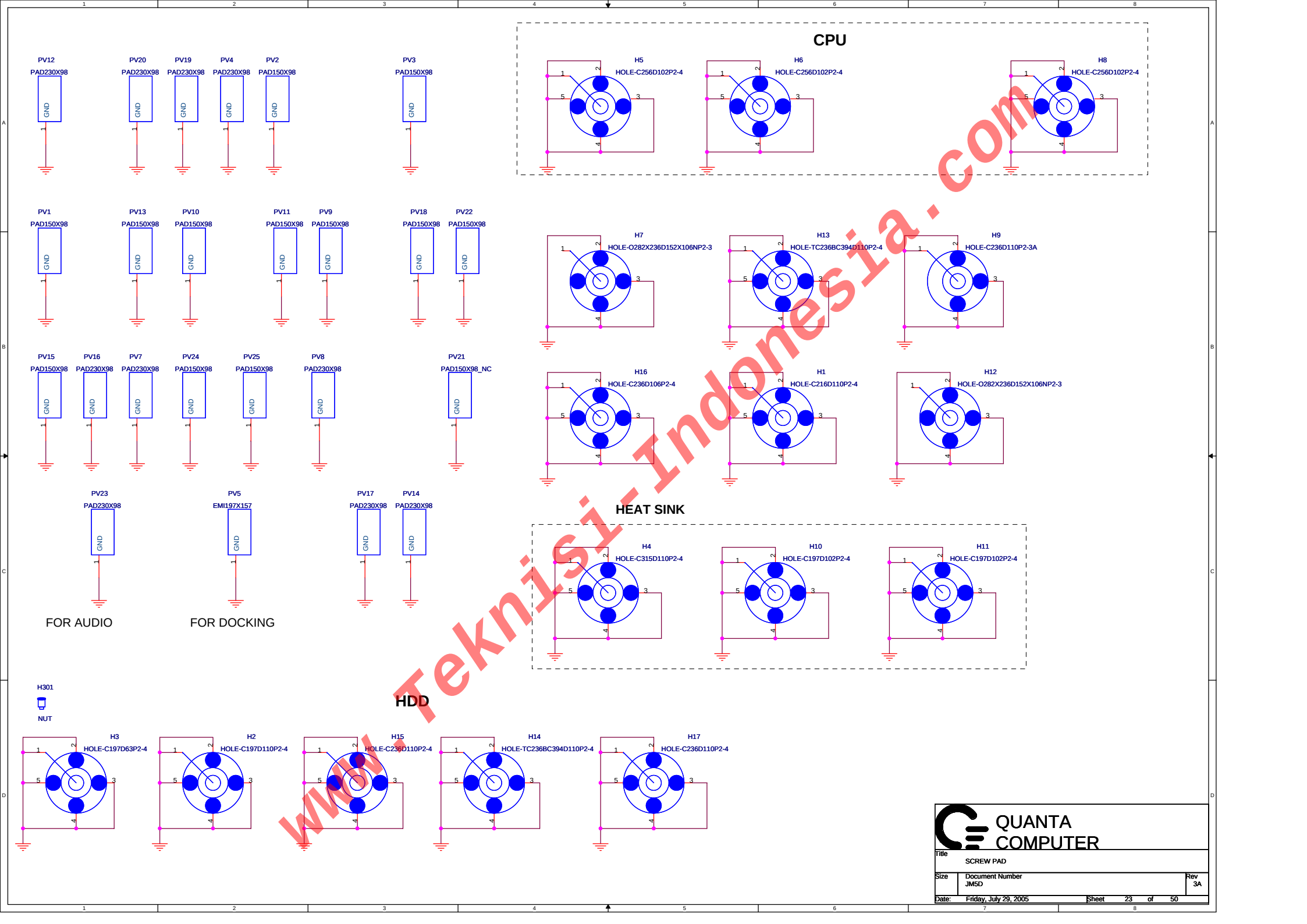

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Title	SCREW PAD	
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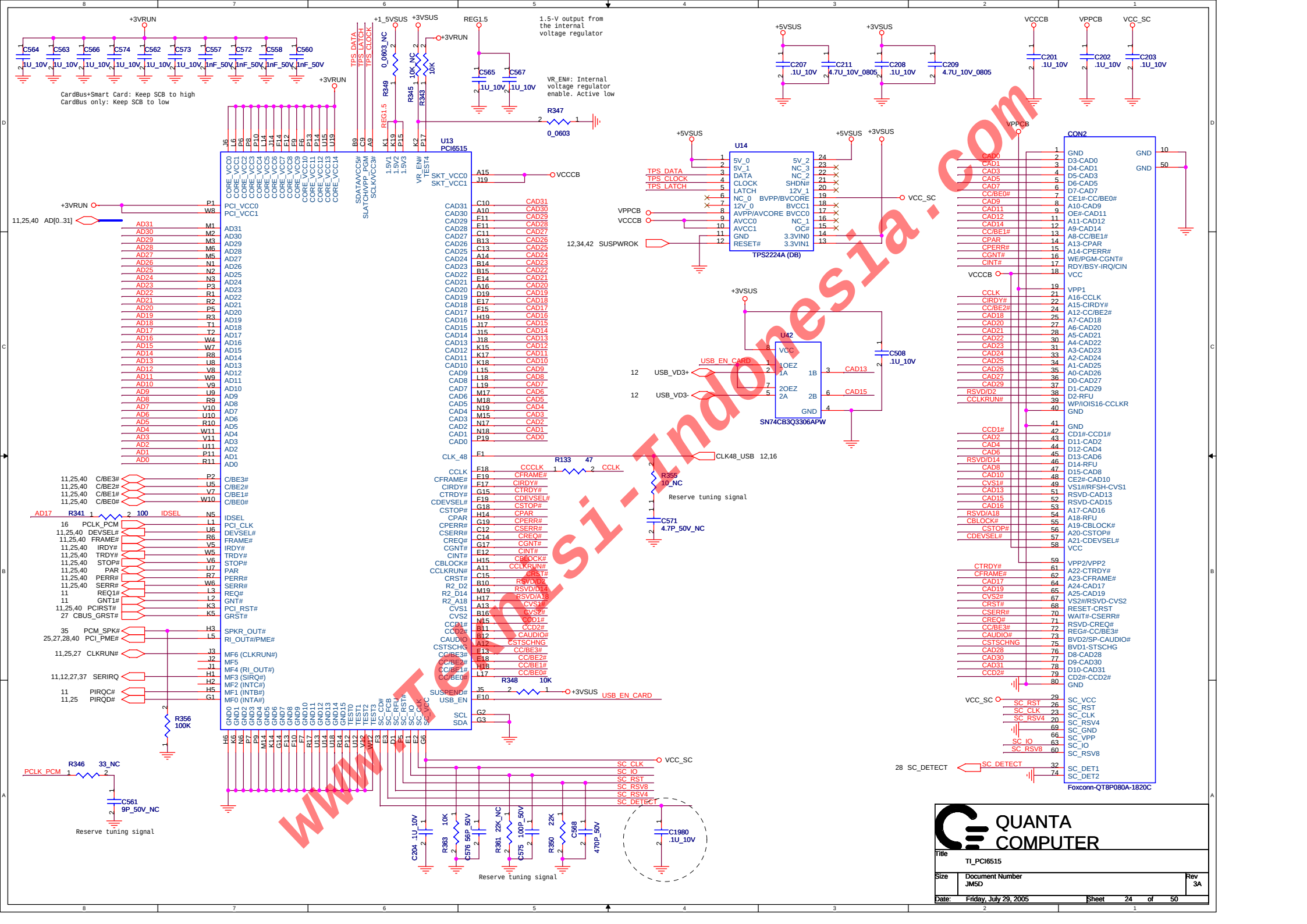
U13
PCI6515
U14
TPS2224A (DB)
U42
SN74CB3Q3306APW
CON2
Foxconn-QT8P080A-1820C
1.5-V output from the internal voltage regulator
VR_EN#: Internal voltage regulator enable. Active low
CardBus+Smart Card: Keep SCB to high
CardBus only: Keep SCB to low
Reserve tuning signal
Reserve tuning signal
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TI_PCI6515
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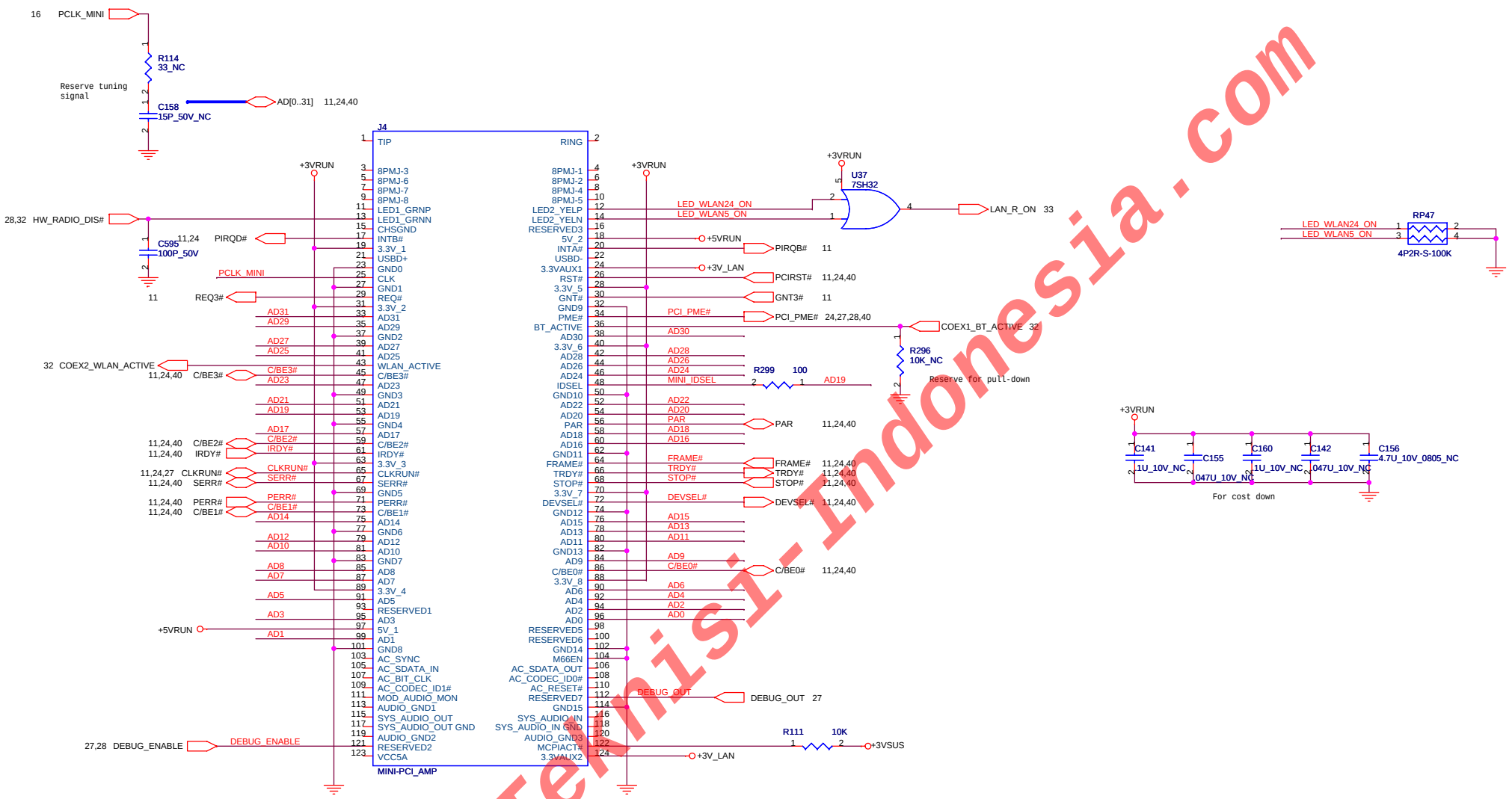

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Title	MINI-PCI &MDC	
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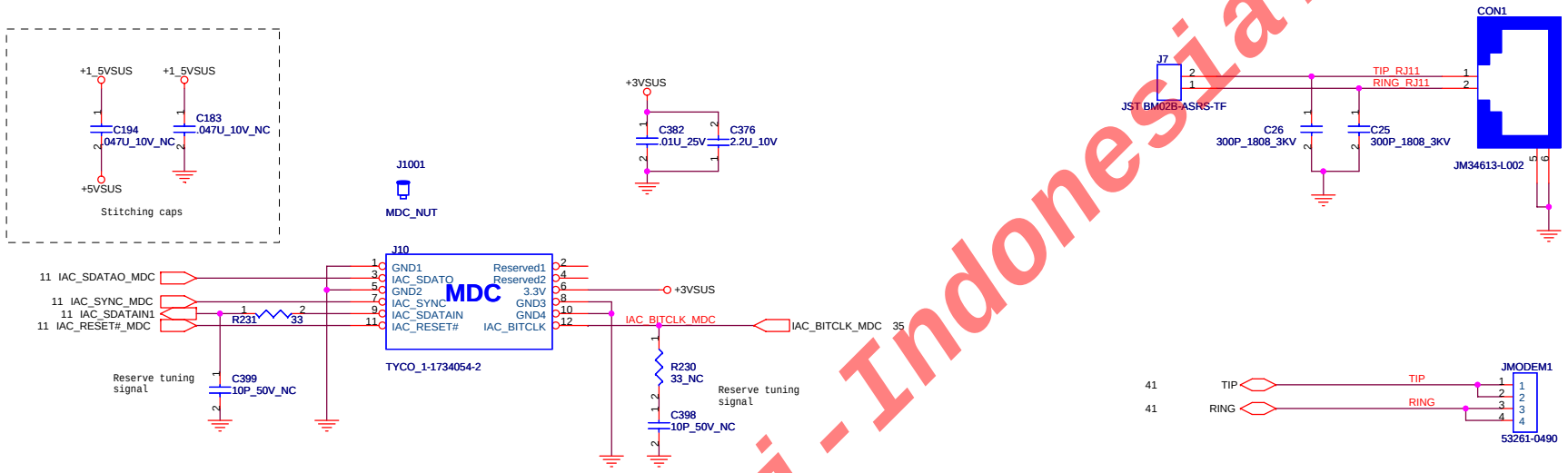

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Title	MDC CONN.	
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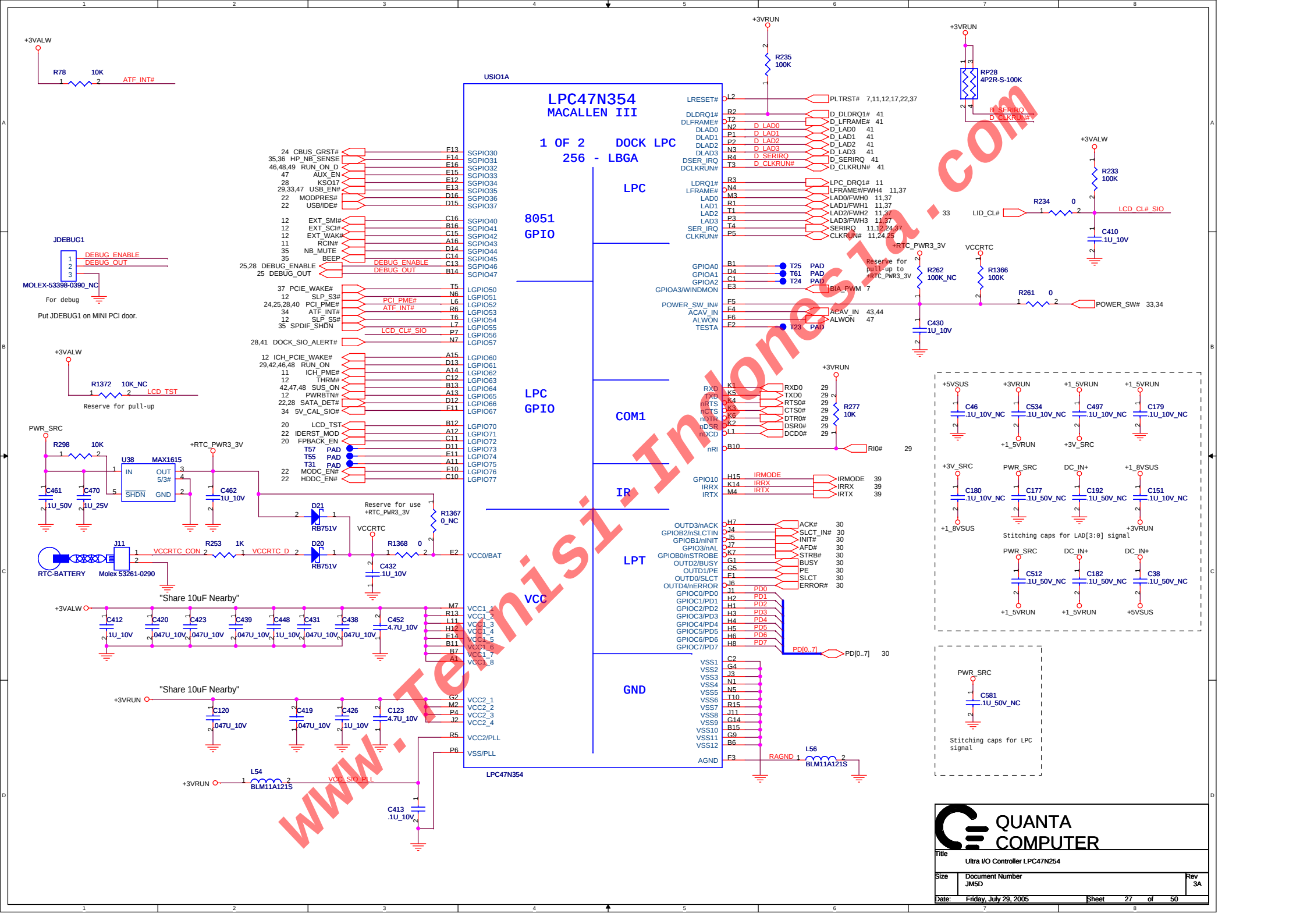
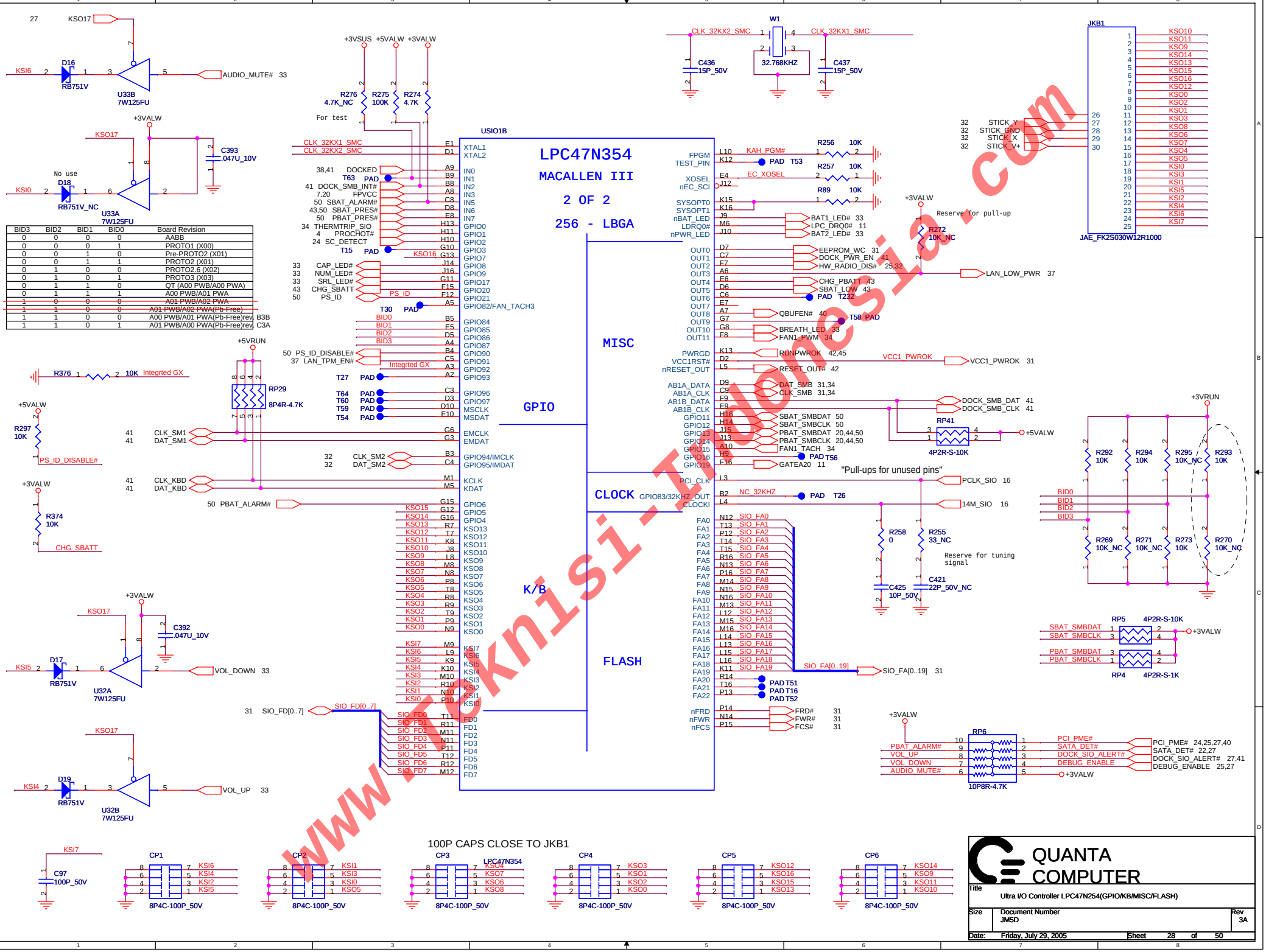
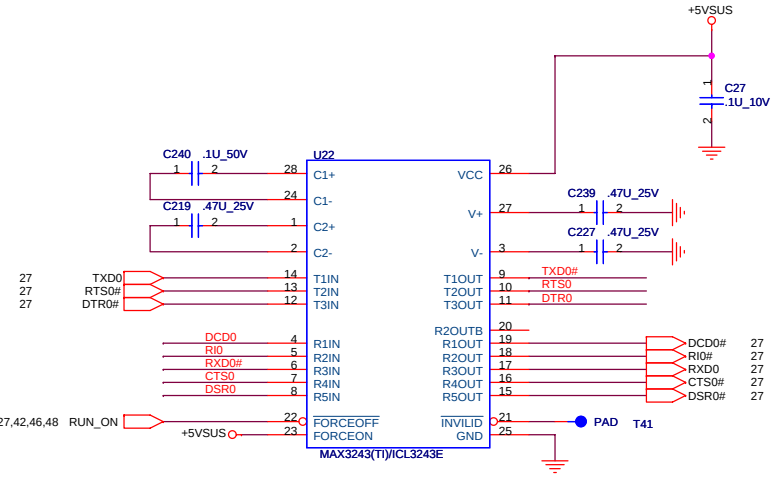
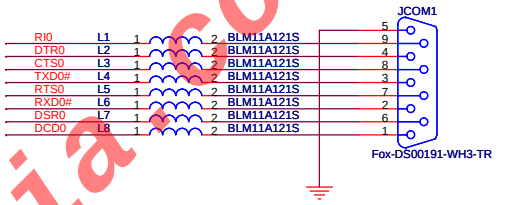




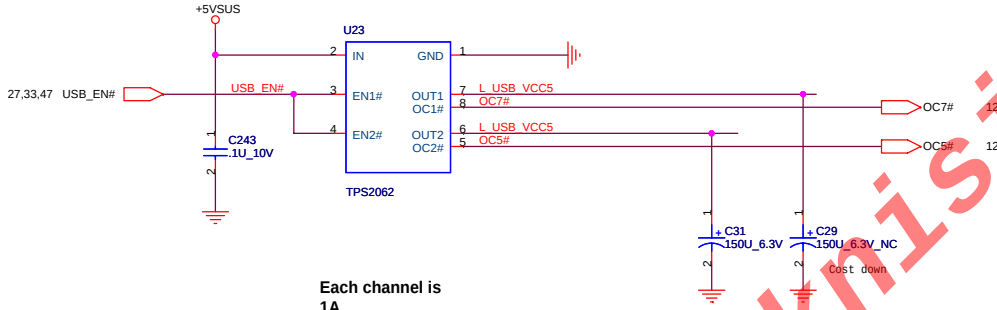
BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	AABB
0	0	0	1	PROTO1 (X00)
0	0	1	0	Pre-PROTO2 (X01)
0	0	1	1	PROTO2 (X01)
0	1	0	0	PROTO2.6 (X02)
0	1	0	1	PROTO3 (X03)
0	1	1	0	QT (A00 PWB/A00 PWA)
0	1	1	1	A00 PWB/A01 PWA
1	0	0	0	A01 PWB/A02 PWA
1	1	0	0	A01 PWB/A02 PWA(Pb-Free)
1	1	0	0	A00 PWB/A01 PWA(Pb-Free)rev B3B
1	1	0	1	A01 PWB/A00 PWA(Pb-Free)rev C3A



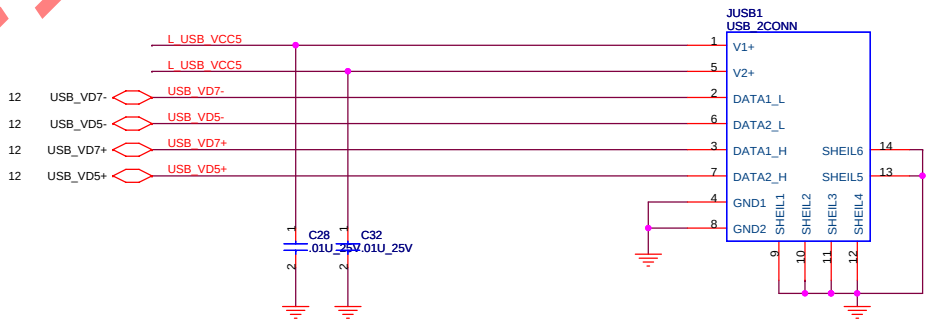
If MAX3243 pin 22 tied to RUN_ON,then it can not support Ring Out



Place these beads close to JCOM1 as soon as possible

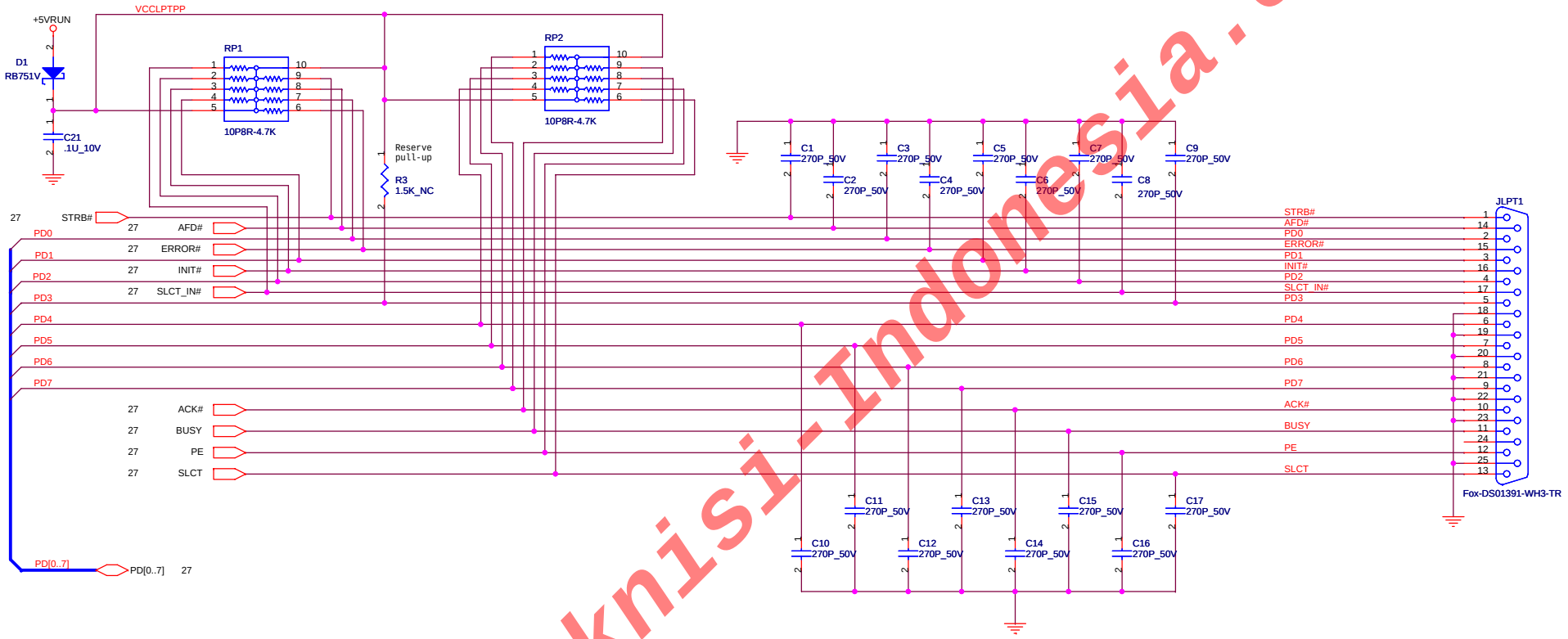


Each channel is 1A



QUANTA COMPUTER

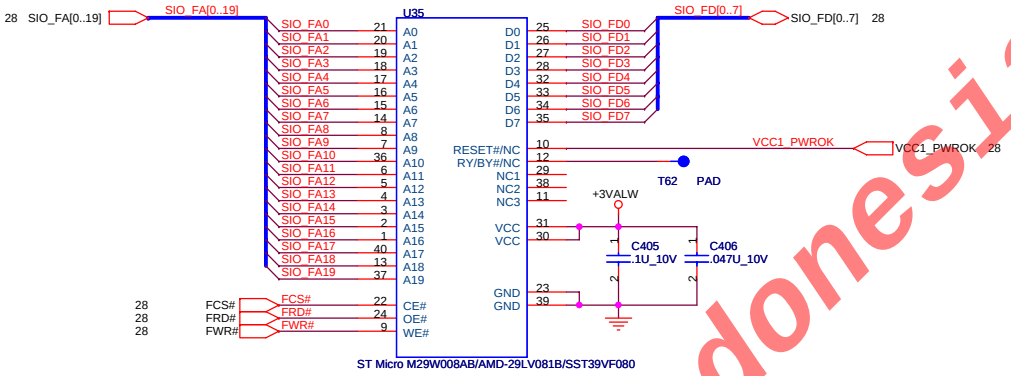
Title	SERIAL PORT & USB	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 29 of 50	



QUANTA COMPUTER

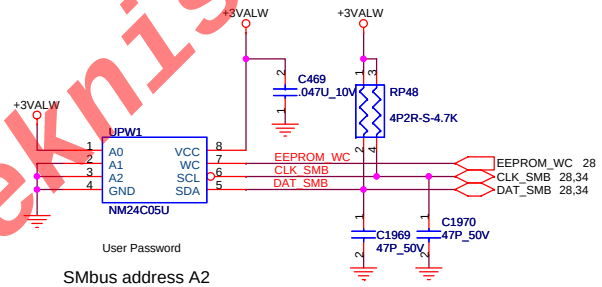
Title	PARALLEL CONN.	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 30 of 50	

8Mbit (1M Byte),NO PLCC TYPE



AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

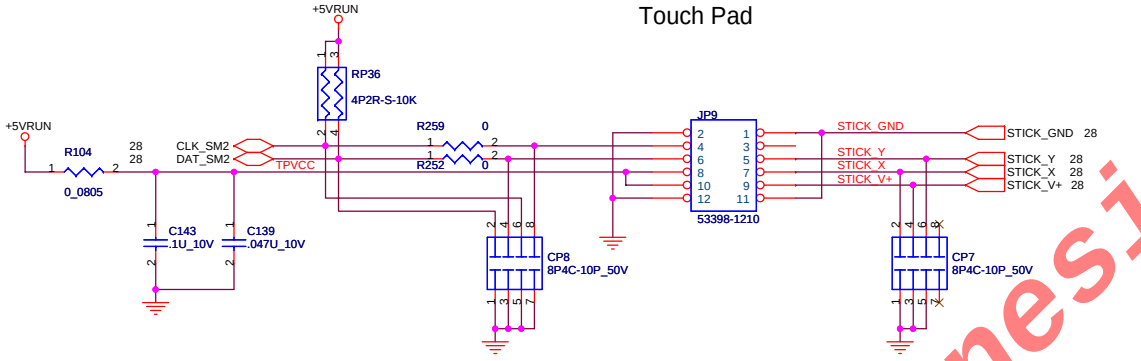


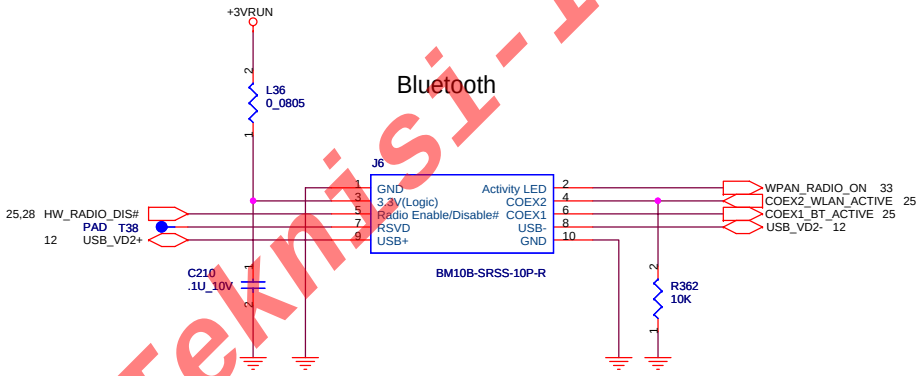
User Password

SMbus address A2

QUANTA COMPUTER

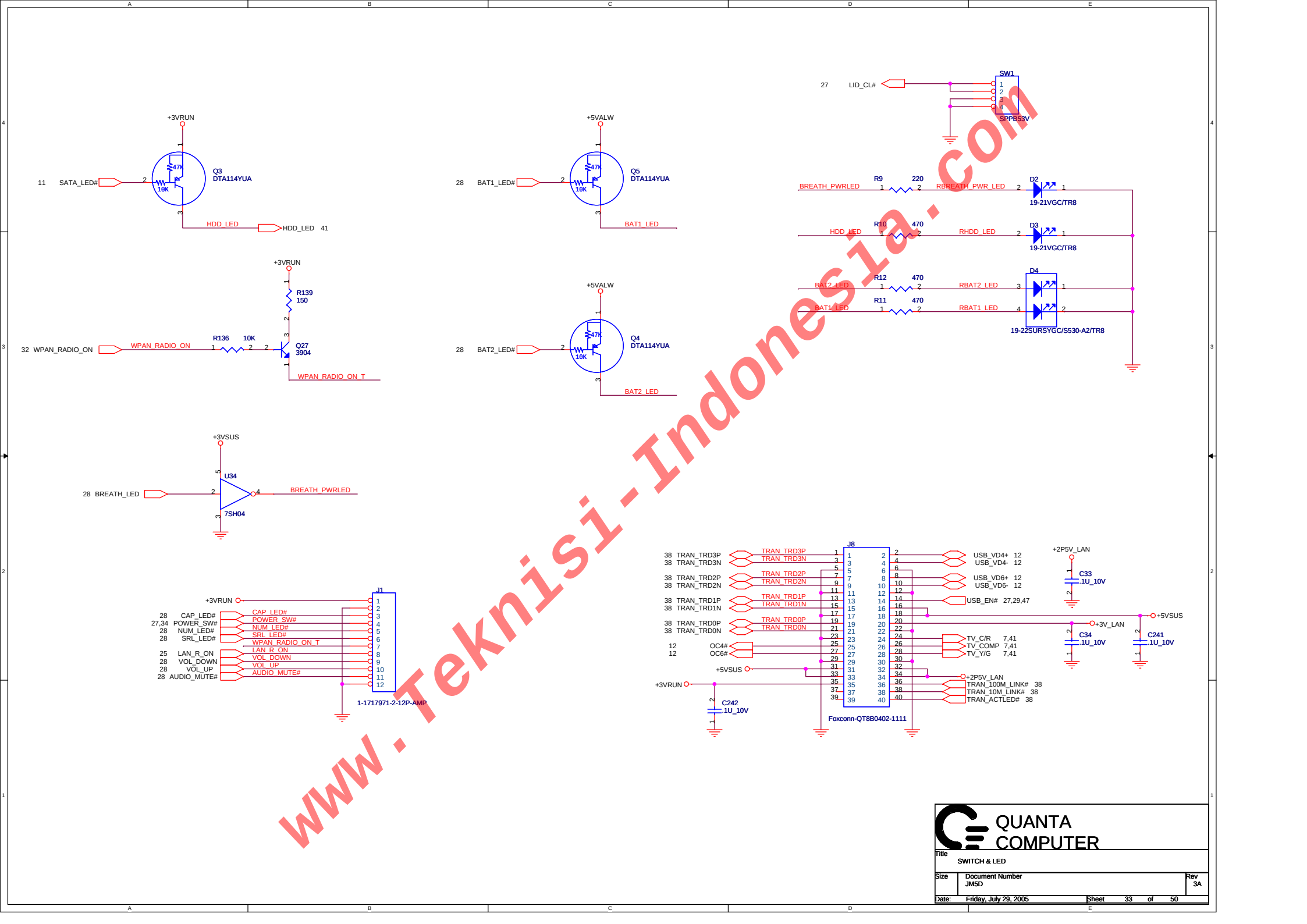
Title	FLASH	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 31 of 50	





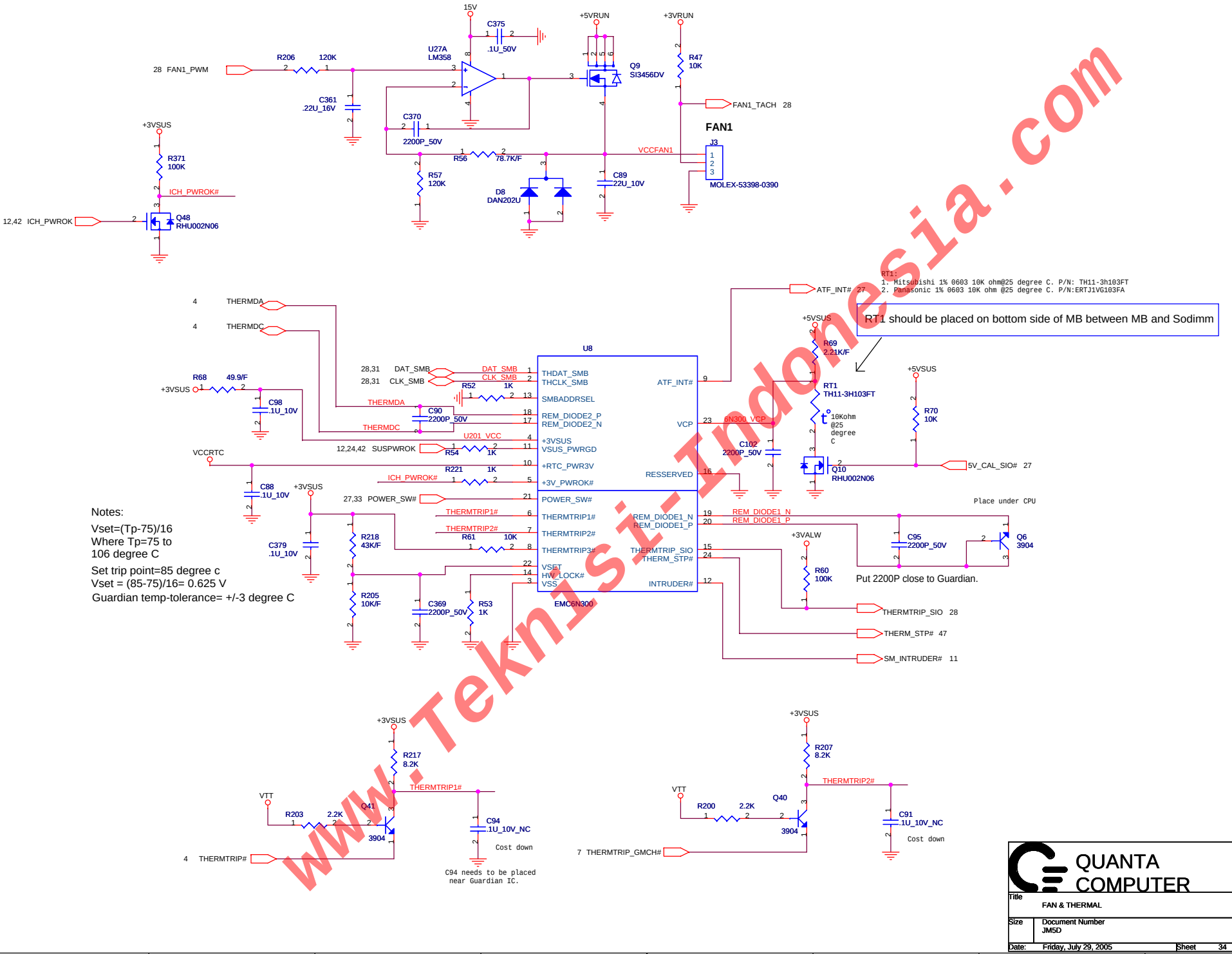
QUANTA COMPUTER

Title	TOUCH PAD & BULE TOOTH	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 32 of 50	



QUANTA COMPUTER

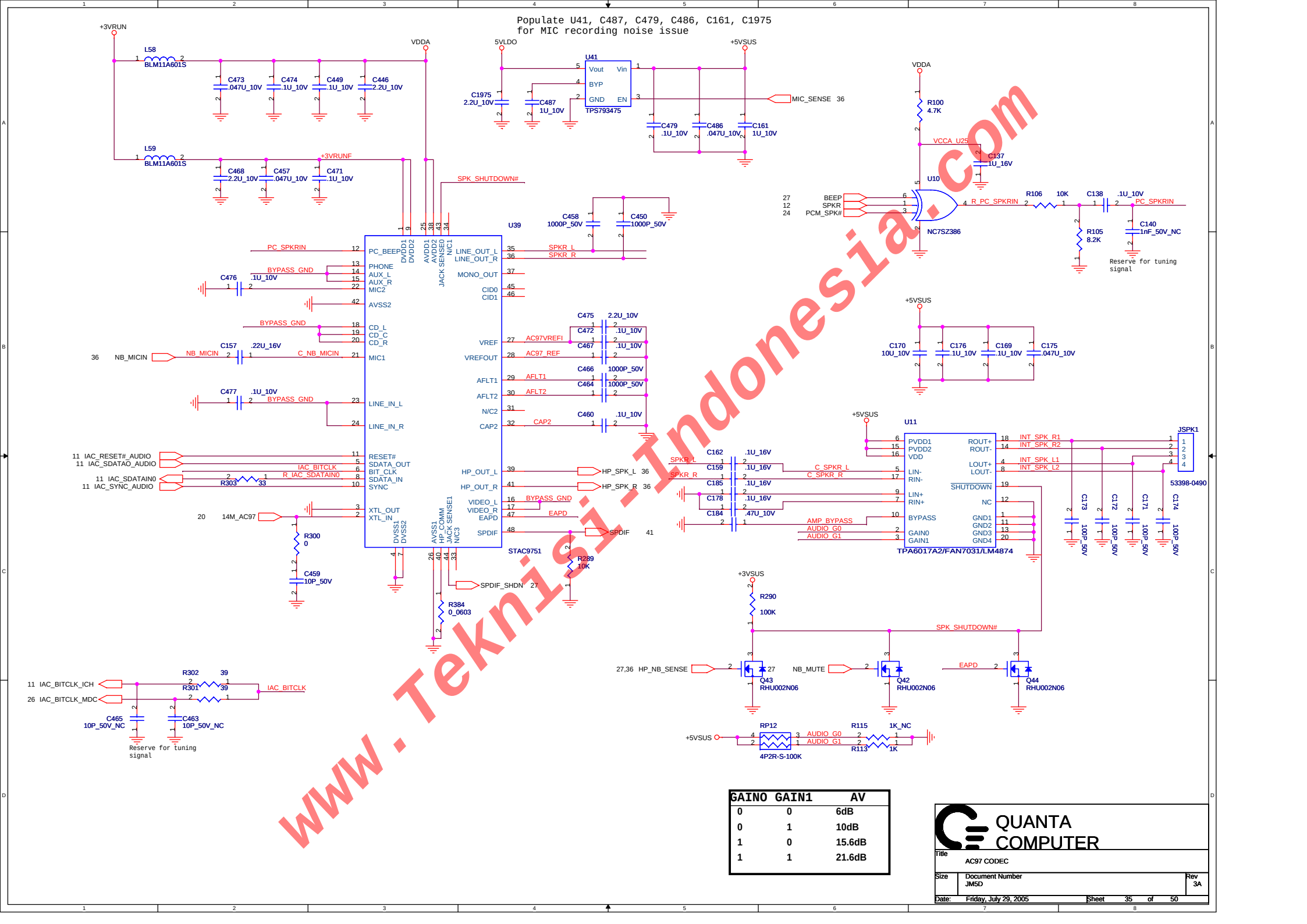
Title	SWITCH & LED	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 33 of 50	



QUANTA COMPUTER

Title	FAN & THERMAL	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 34 of 50	

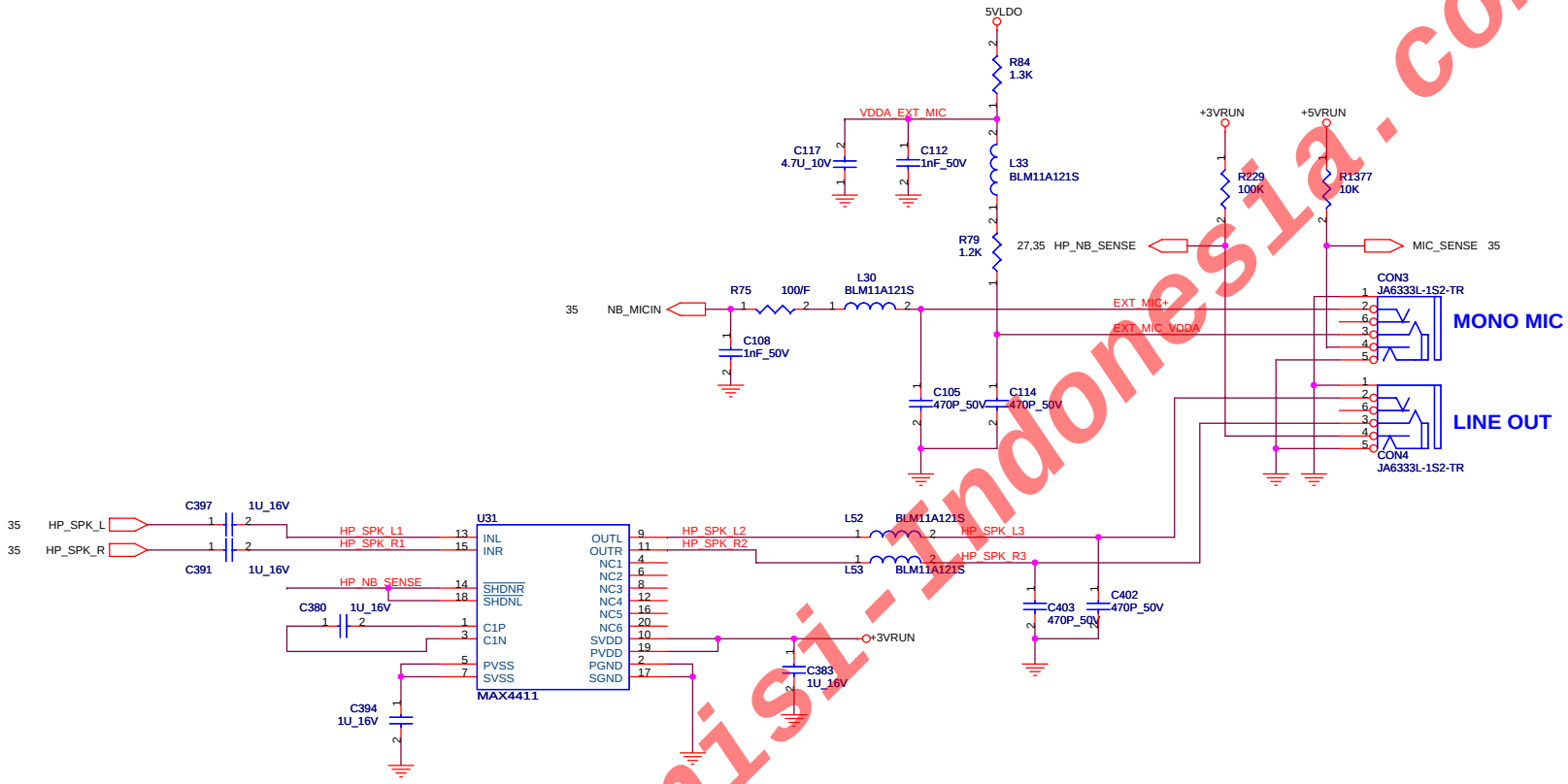
Populate U41, C487, C479, C486, C161, C1975
for MIC recording noise issue



GAINO	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

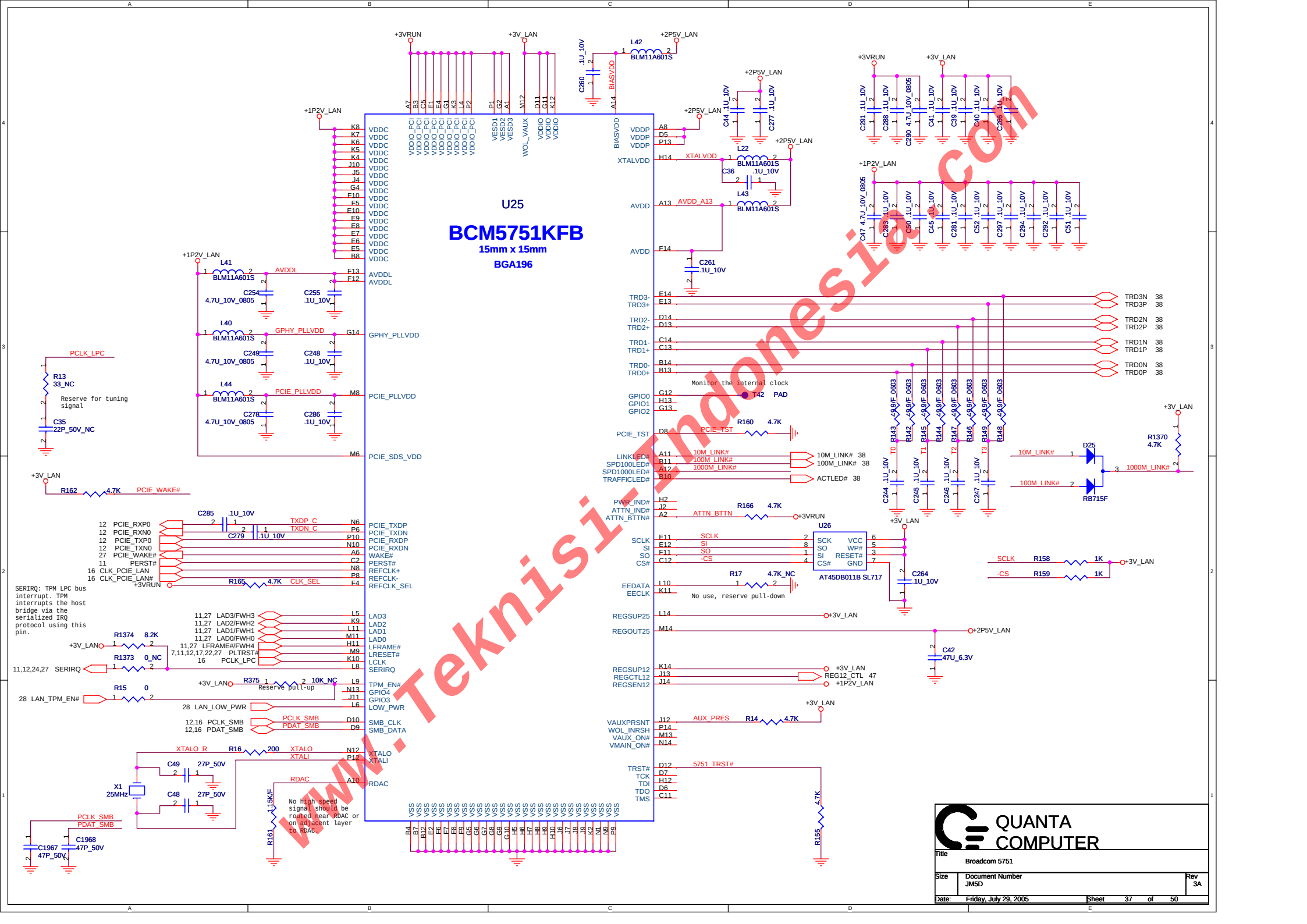
QUANTA COMPUTER

Title	AC97 CODEC	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 35 of 50	



QUANTA COMPUTER

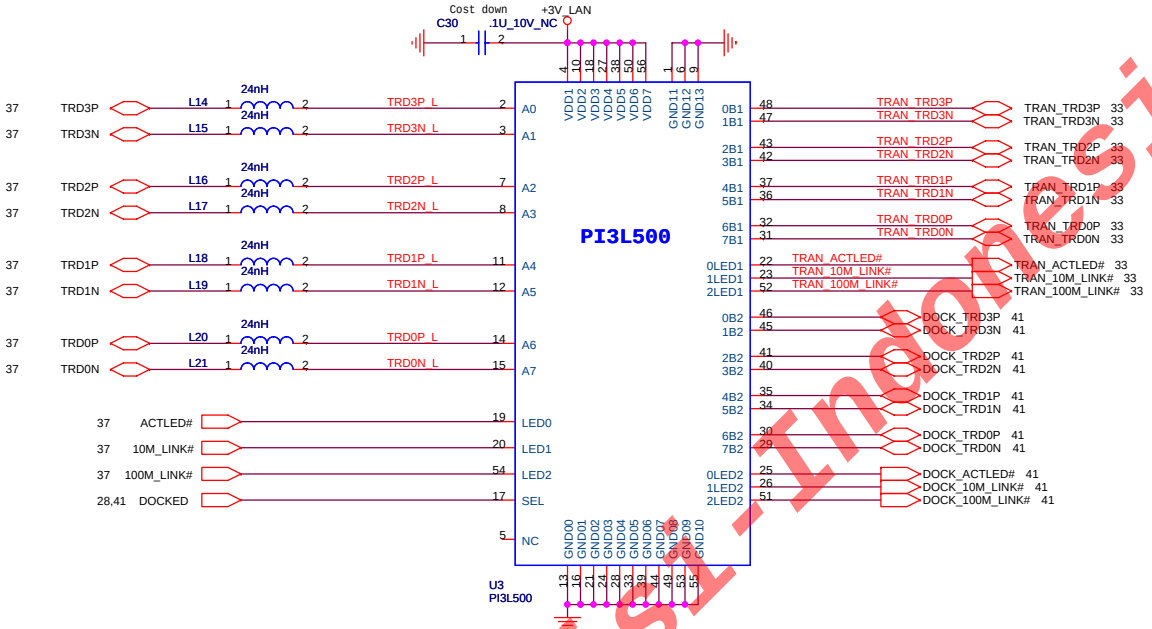
Title	AUDIO CONN	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 36 of 50	



Title	Broadcom 5751		
Size	Document Number JM5D		Rev 3A
Date:	Friday, July 29, 2005	Sheet 37 of 50	

QUANTA COMPUTER

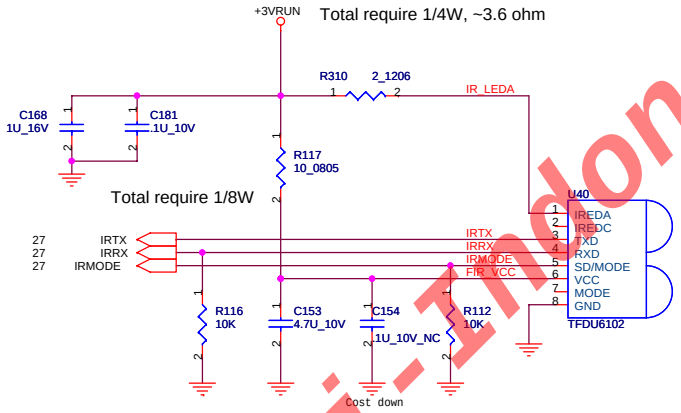
L14/L15/L16/L17/L18/L19/L20/L21 must be 0603



SWITCH

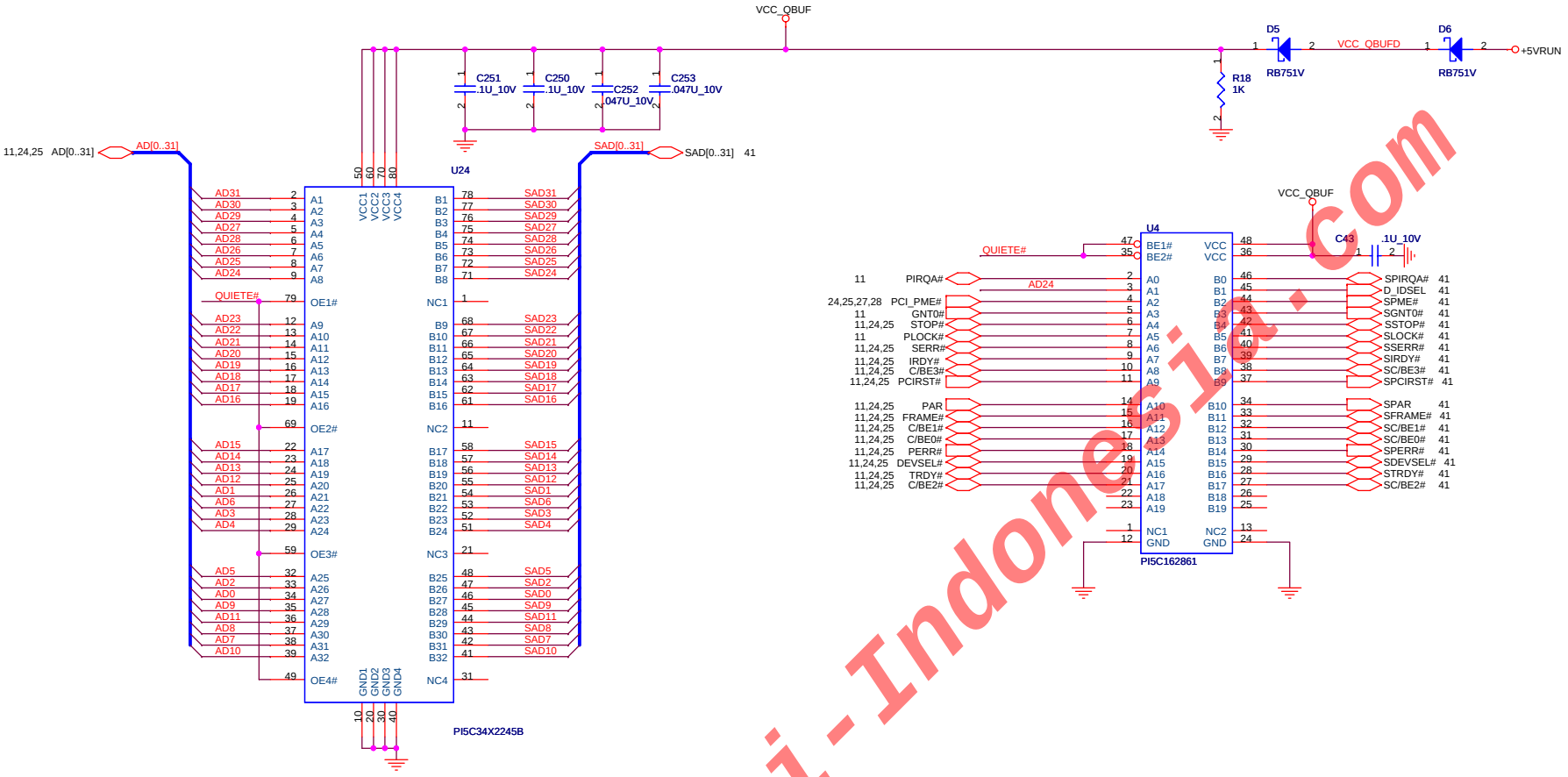
QUANTA COMPUTER

Title	LAN SWITCH	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 38 of 50	



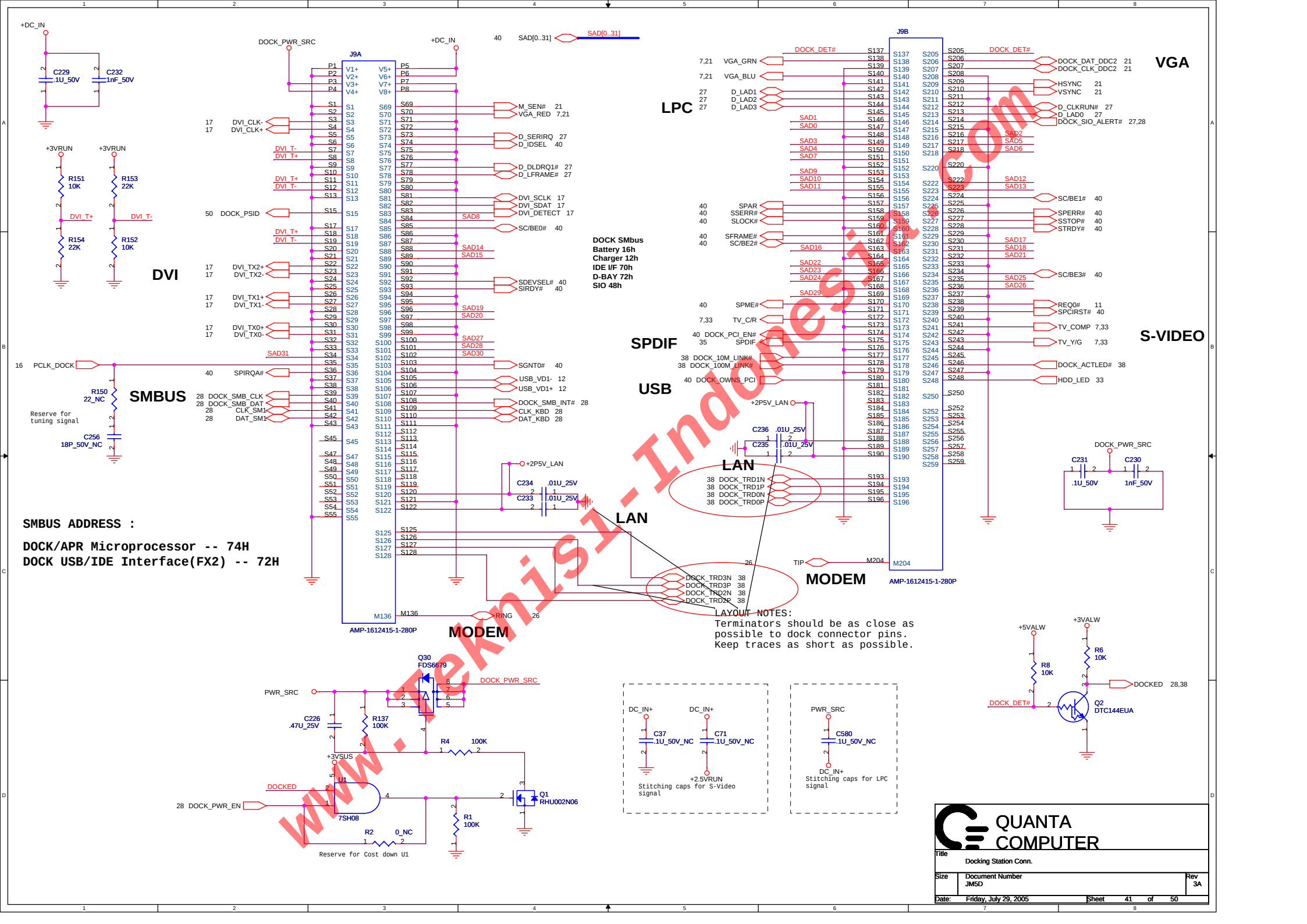
QUANTA COMPUTER

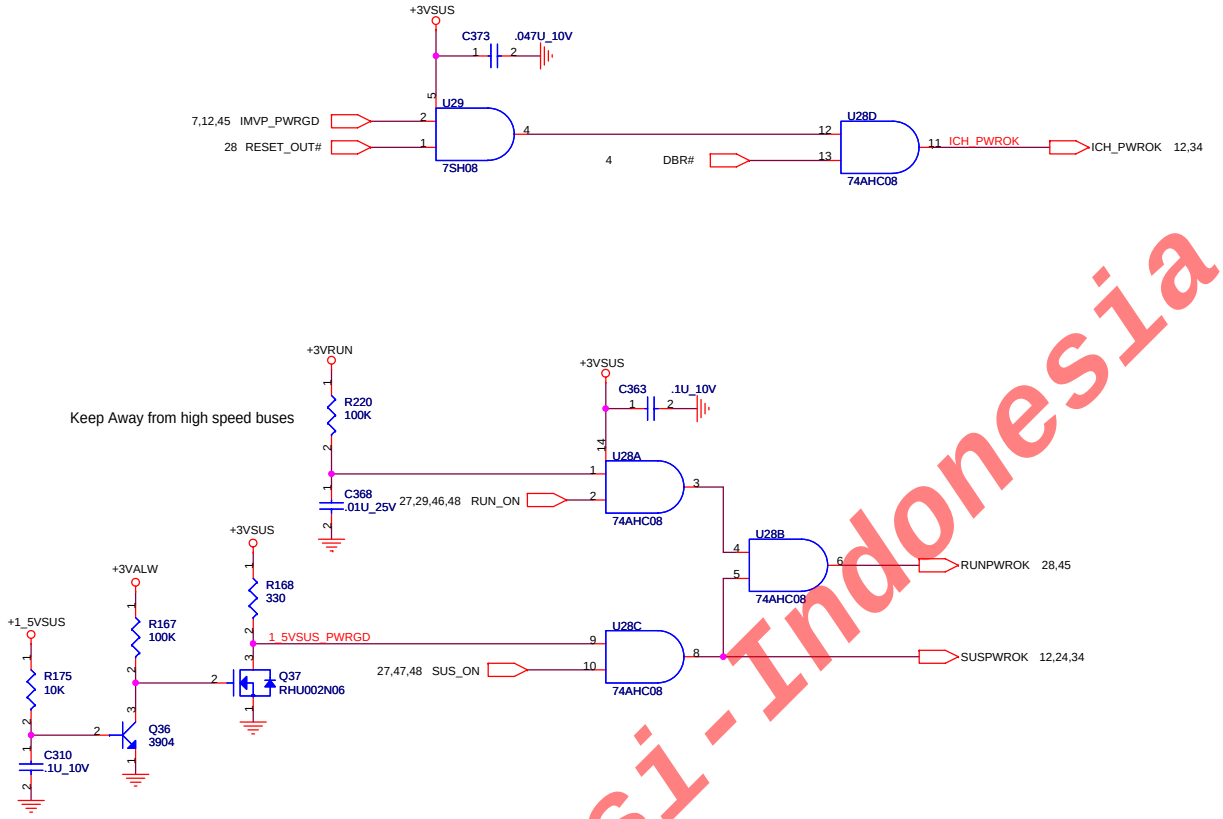
Title	FIR	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 39 of 50	



QUANTA COMPUTER

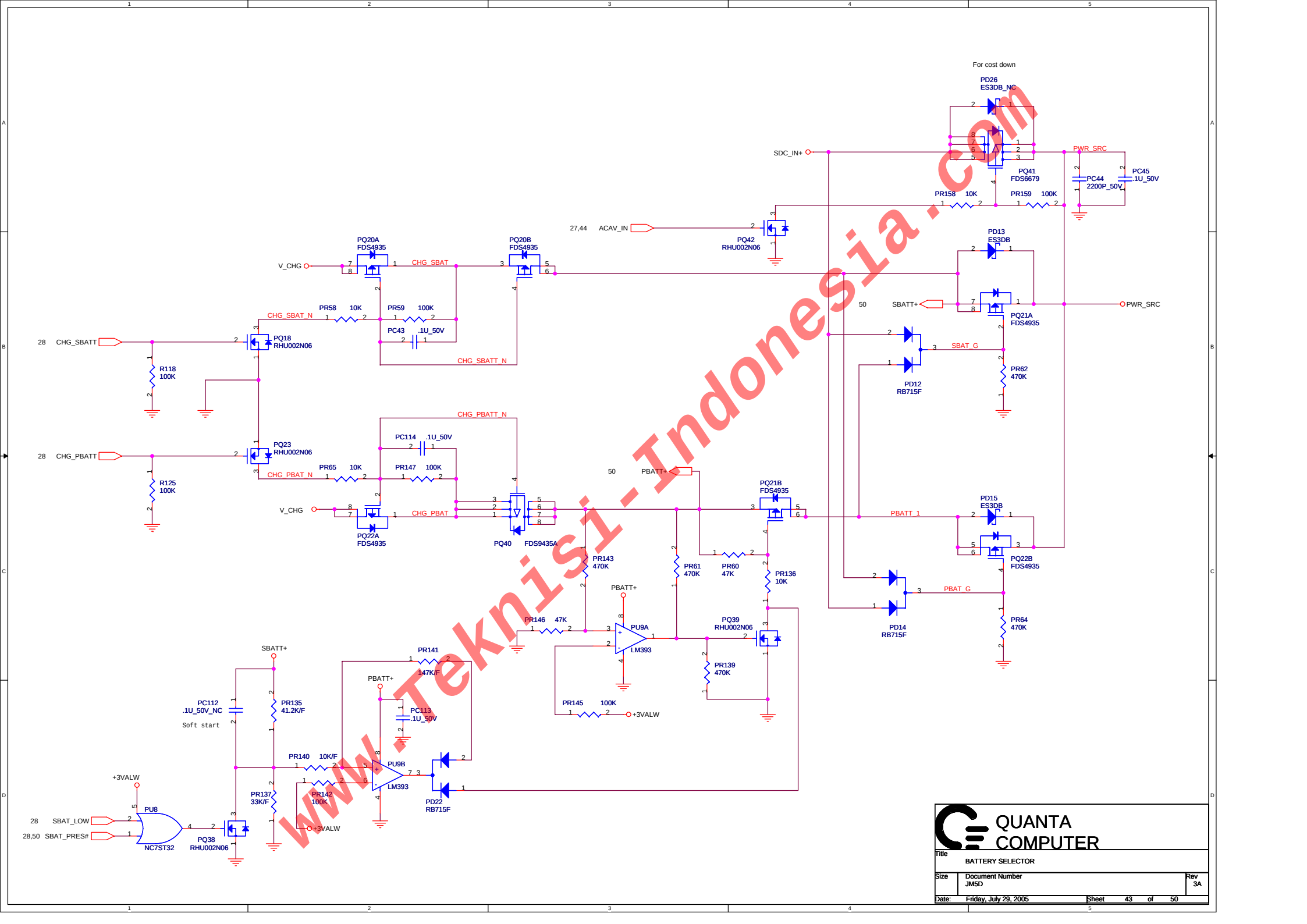
Title	Docking Q-SWITCH	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 40 of 50	





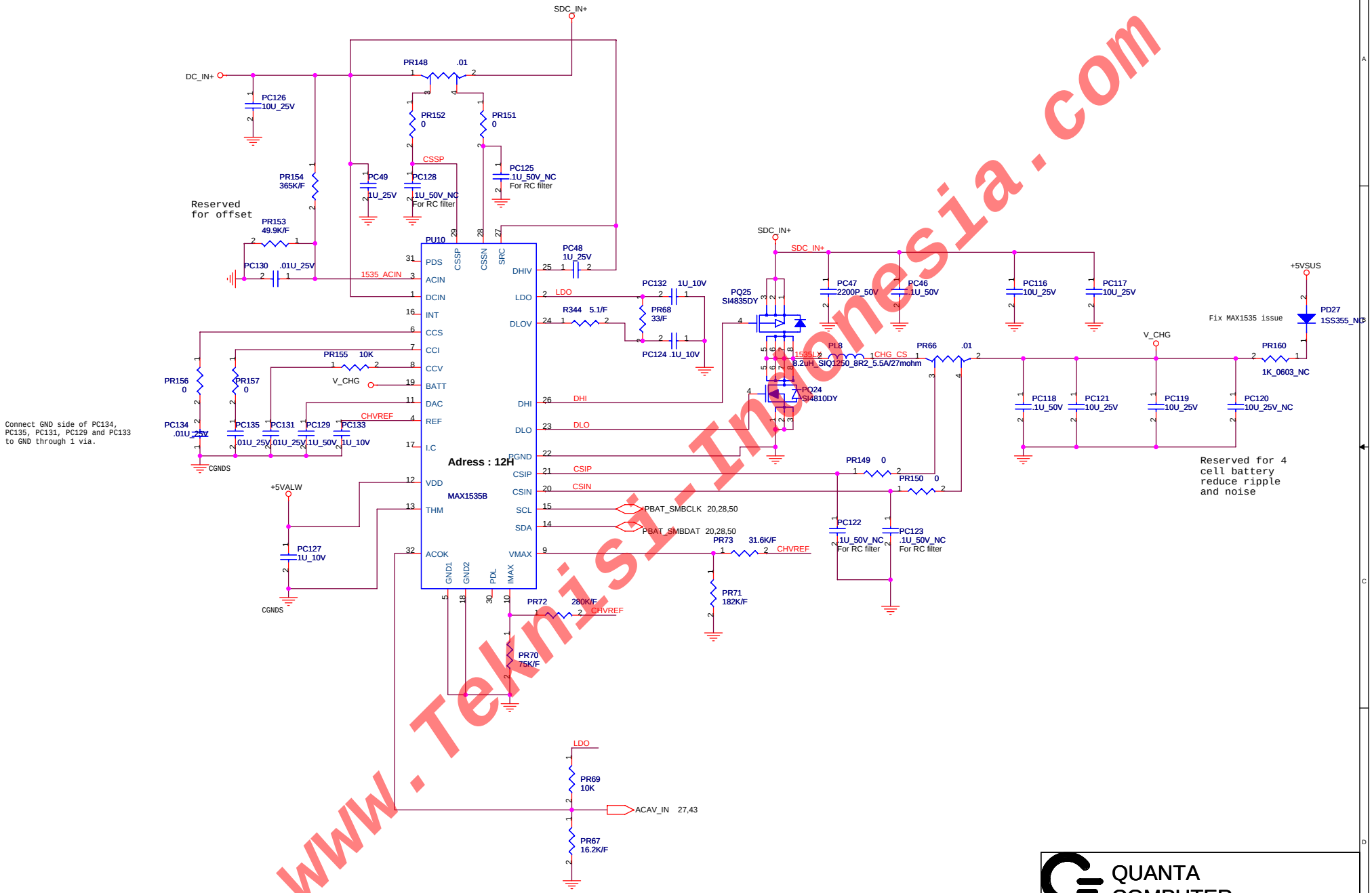
QUANTA COMPUTER

Title	POWER GOOD	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 42 of 50	



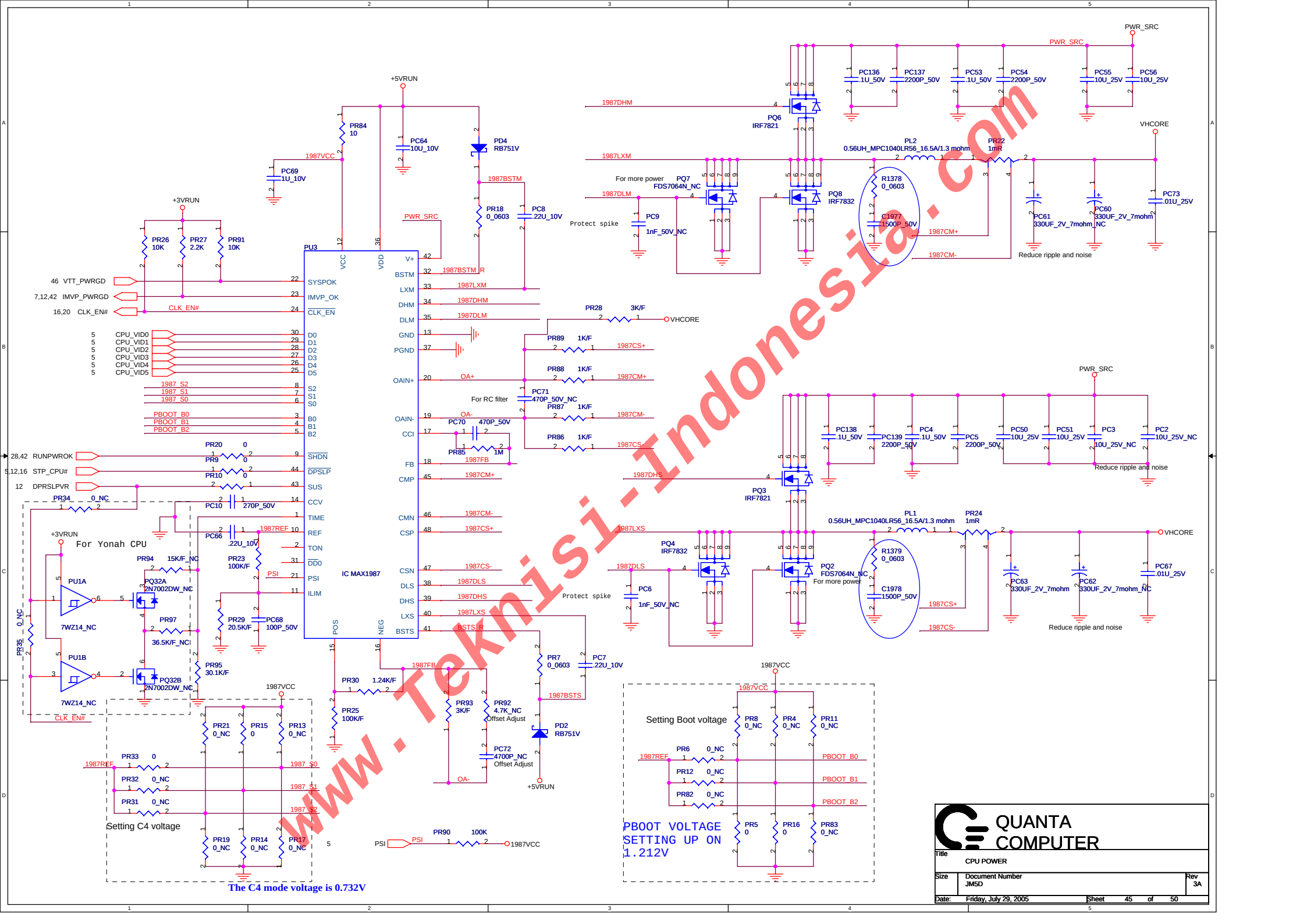
QUANTA COMPUTER

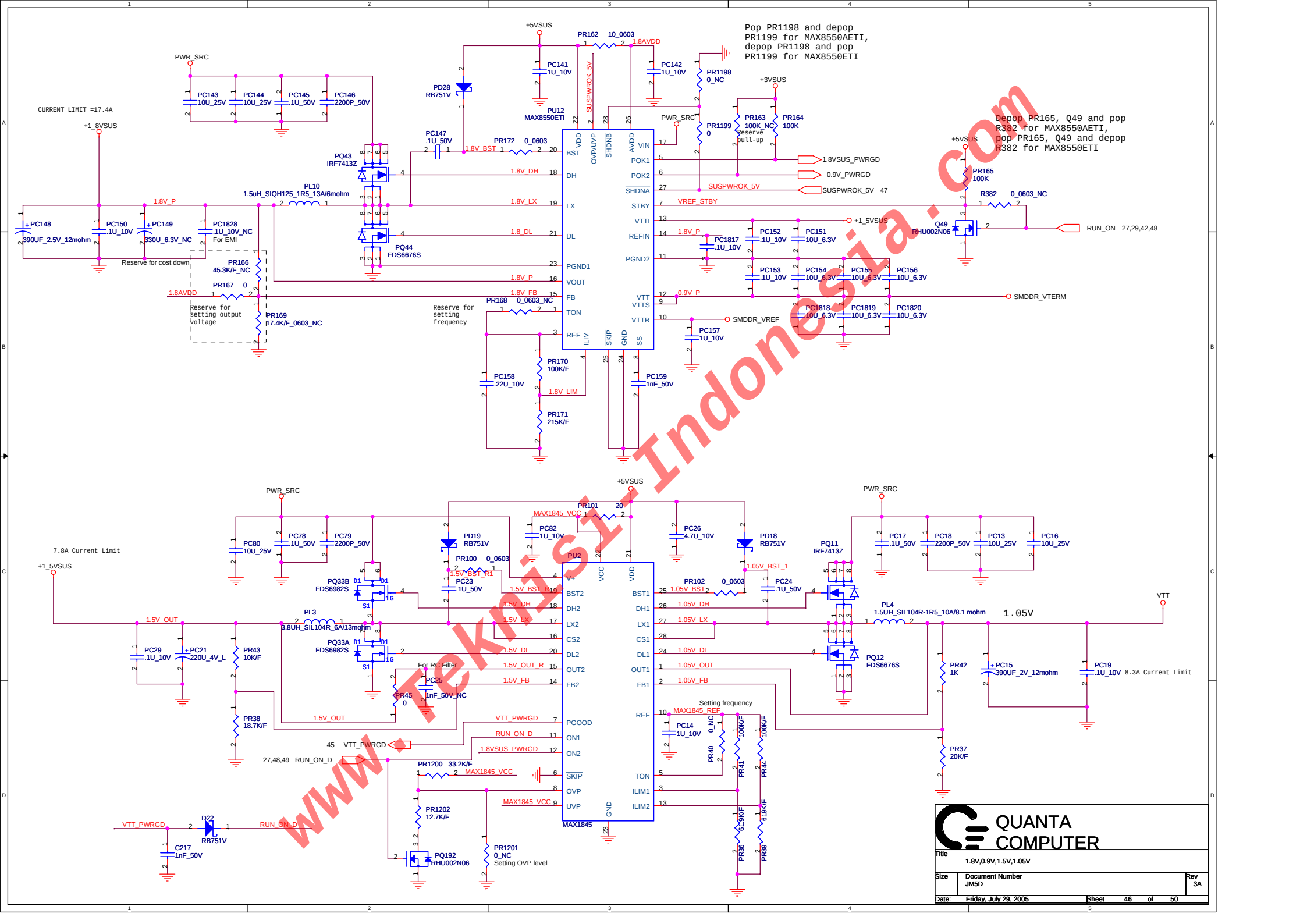
Title	BATTERY SELECTOR	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 43 of 50	

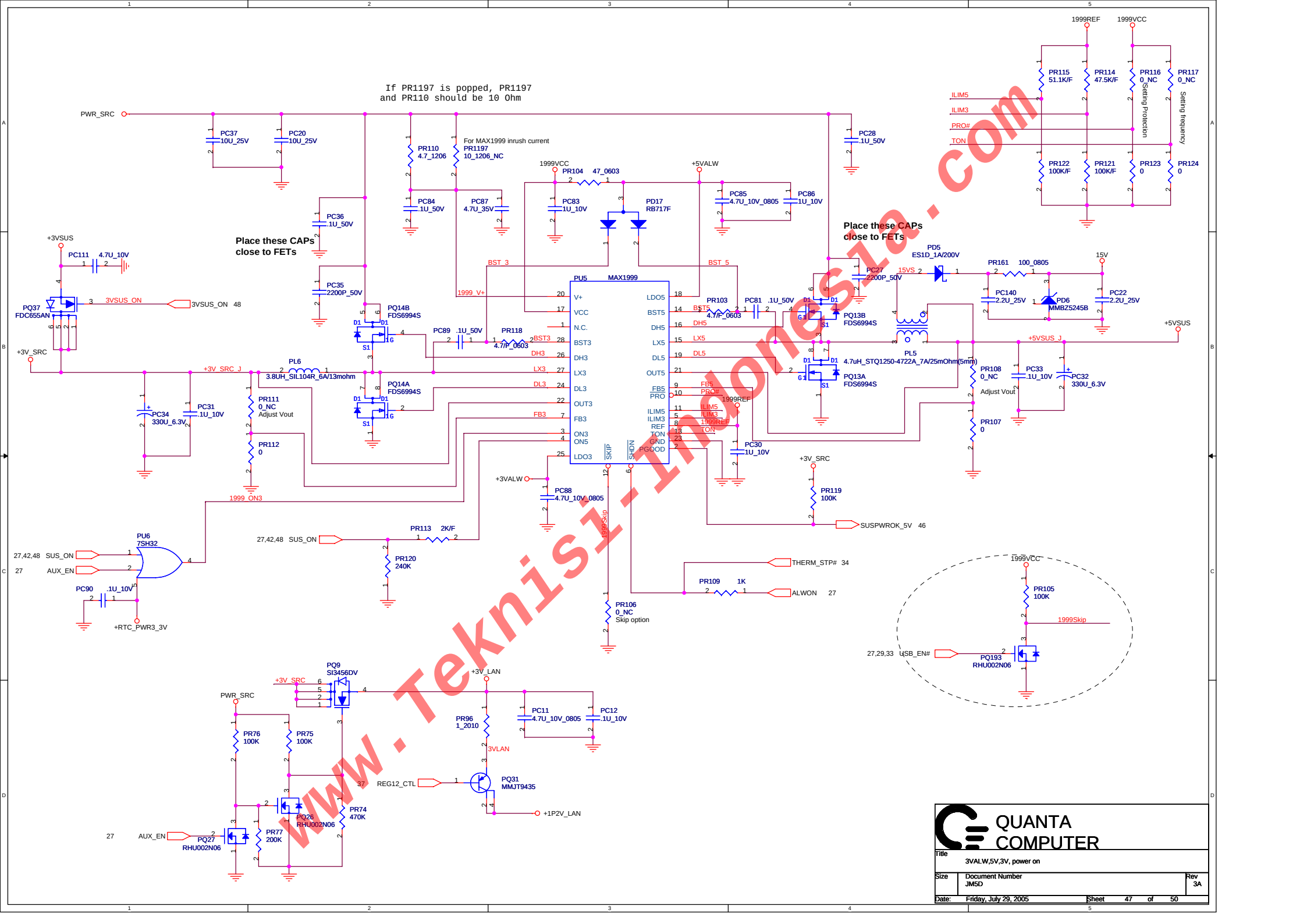


QUANTA COMPUTER

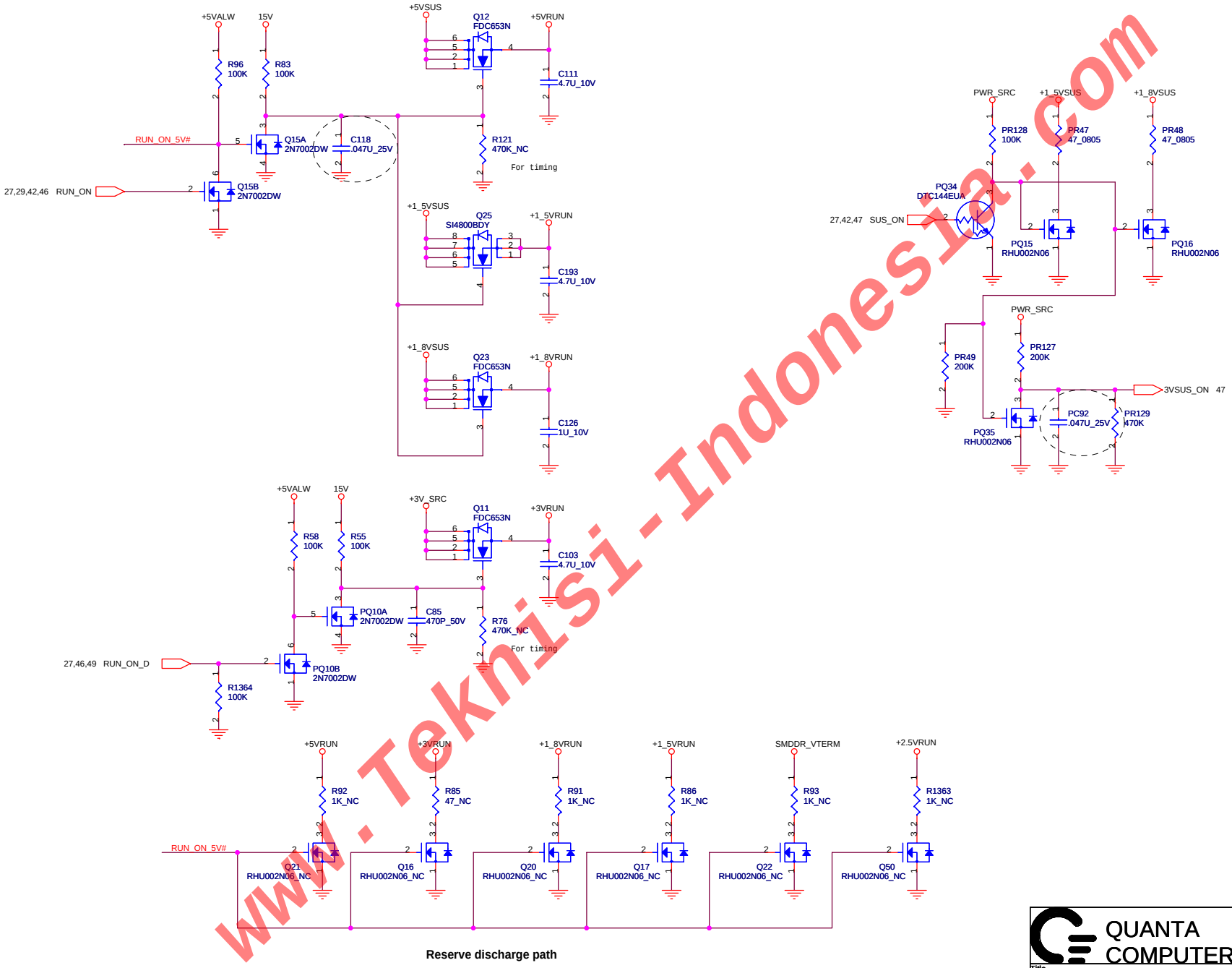
Title	Battery Charger	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 44 of 50	


PWR_SRC
+5VRUN
+3VRUN
VHCORE
1987VCC
PU3
IC MAX1987
PQ6 IRF7821
PQ7 FDS7064N_NC
PQ8 IRF7832
PQ3 IRF7821
PQ4 IRF7832
PQ2 FDS7064N_NC
PL2 0.56UH_MPC1040LR56_16.5A/1.3 mohm
PL1 0.56UH_MPC1040LR56_16.5A/1.3 mohm
PD4 RB751V
PD2 RB751V
PU1A
PU1B
7WZ14_NC
PQ32A 2N7002DW_NC
PQ32B 2N7002DW_NC
For Yonah CPU
For more power
Protect spike
For RC filter
Reduce ripple and noise
Setting C4 voltage
Setting Boot voltage
PBOOT VOLTAGE SETTING UP ON 1.212V
The C4 mode voltage is 0.732V
QUANTA COMPUTER
CPU POWER
JM5D
Friday, July 29, 2005
Sheet 45 of 50
www.Teknisi-Indonesia.com





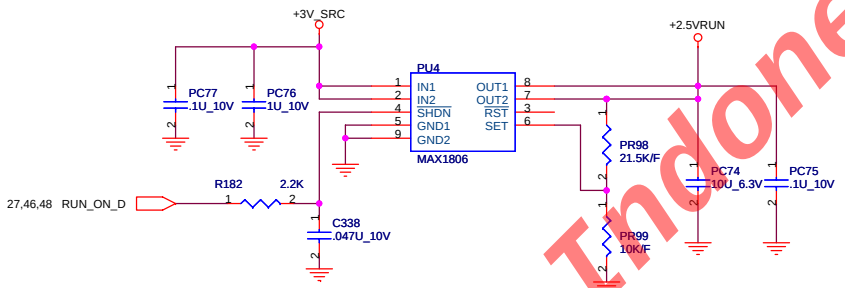
QUANTA COMPUTER		
Title	3VALW,5V,3V, power on	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 47 of 50	



Reserve discharge path

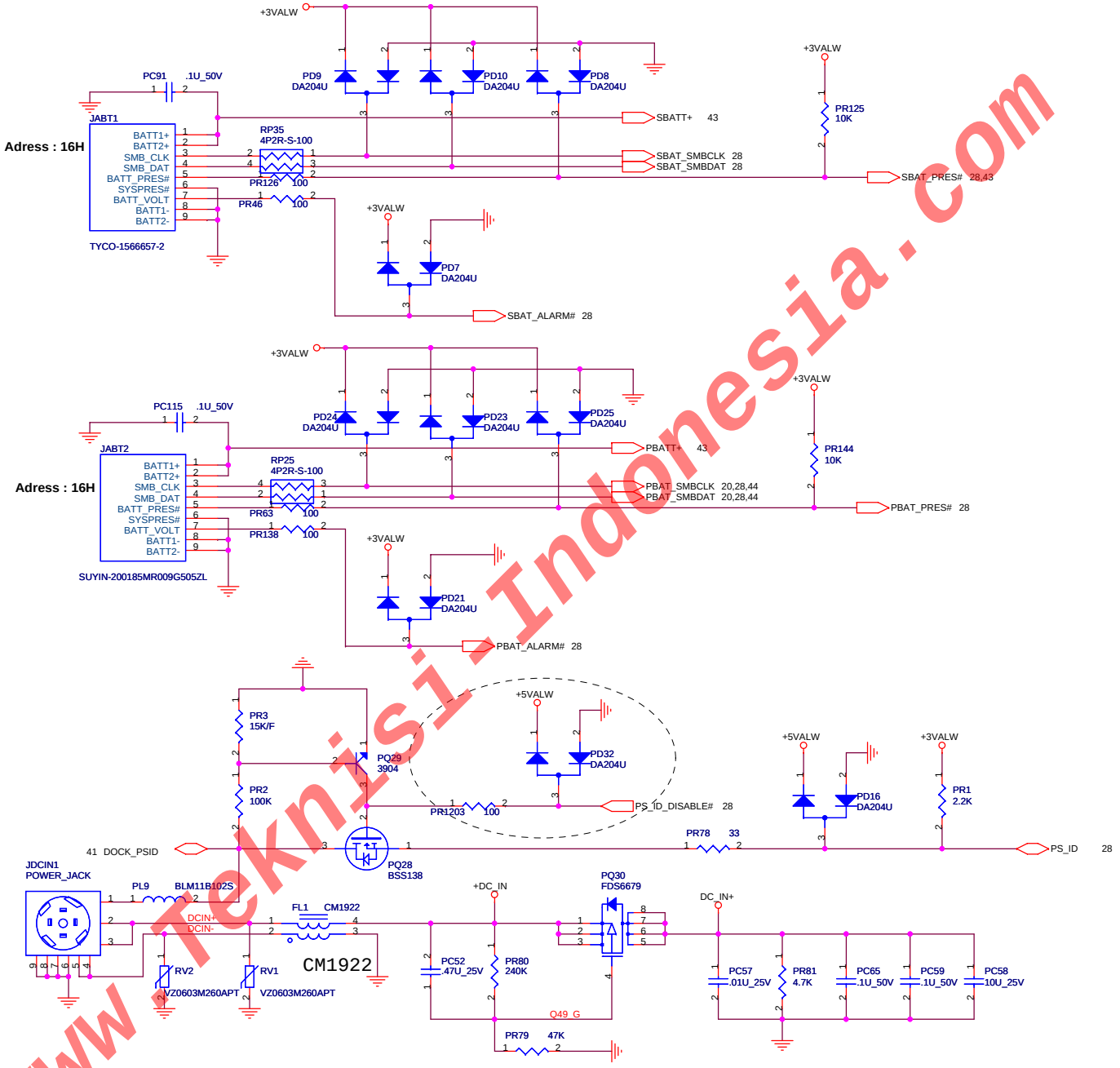
QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 48 of 50	



QUANTA COMPUTER

Title	VGA DC/DC	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 49 of 50	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number JM5D	Rev 3A
Date: Friday, July 29, 2005	Sheet 50 of 50	

MODEL	REV	CHANGE LIST
JM5D MB	3A	Base on 31JM5MB0045 rev. B3B , include below 5 changes. Separate LAMP_STAT from resistor array Smart Card, card detect add de-bounce circuit USB 2.0 HDD Non Compliance PSID protect improvement EMI Snubber circuit change Headphone noise move related components as far away +3VRun as possible by layout modification. Correct BID table & update BID from "1100" to "1101" for A00(rev. B3B) to A01(rev. C3A) Page 28 : depopulate R270 ; populate R293

Model / Page	JM5D MB	
	FM JM5D rev. B3B	TO
1	3A	
2	3A	
3	3A	
4	3A	
5	3A	
6	3A	
7	3A	
8	3A	
9	3A	
10	3A	
11	3A	
12	3A	
13	3A	
14	3A	
15	3A	
16	3A	
17	3A	
18	3A	
19	3A	
20	3A	
21	3A	
22	3A	
23	3A	
24	3A	
25	3A	
26	3A	
27	3A	
28	3A	
29	3A	
30	3A	
31	3A	
32	3A	
33	3A	
34	3A	
35	3A	
36	3A	
37	3A	
38	3A	
39	3A	
40	3A	
41	3A	
42	3A	
43	3A	
44	3A	
45	3A	
46	3A	
47	3A	
48	3A	
49	3A	
50	3A	

QUANTA COMPUTER

PROJECT : JM5D	DOC. NO. 204	REV: 3A	ASSY: 31JM5MB00**(new, wait to apply)	
APPROVED BY : Mike Hwang	CHECKED BY : Mike Hwang	DRAWN BY : Guresu Lo	DATE : Jul., 29, 2005	SHEET 1 OF 1