TEF668X

Low IF Tuner HIgh performance One-chip

Rev. 4 — 15 January 2014 Product data sheet

1. General description

The Low IF Tuner HIgh performance One-chip family TEF668X, are single-chip radio ICs including an AM/FM radio tuner and software-defined radio signal processing. They extend NXP Semiconductors broad, industry-proven car radio single tuner portfolio, offering outstanding radio performance with the widest range of features and state of the art software algorithms at most optimized system costs.

The high-end single tuner family is available in HVQFN packages occupying the smallest PCB space and are suitable for dual- and multi-layer PCBs. The radio receiver includes highest feature sets:

- FM/AM front-ends
- Tuning synthesizer
- Channel filtering
- FM Channel Equalization
- FM multipath improvement
- Demodulation
- FM stereo decoding
- Weak signal processing
- Noise blanking
- RDS
- Provides an interface to a DARC demodulator/decoder

The TEF6687 and TEF6689 include an additional high-end feature, FMSI, which noticeably enhances the stereo performance of the receiver.

The tuner family can provide stereo audio in digital format on the I²S outputs and on the audio DAC outputs. The TEF6688 and TEF6689 support the digital radio standards HD Radio and Digital Radio Mondiale (DRM) when used with NXP Semiconductors digital radio coprocessors such as SAF356X and SAF360X.

2. Features and benefits

- Alignment free digital receiver including tuner and software-defined radio processing
- Command based high-level user interface combining high control flexibility with ease of control

- Read information with device and tuning status, reception quality and RDS data
- FM receiver with a tuning range of 65 MHz to 108 MHz covering Eastern European (OIRT), Japanese, European and US bands
- AM receiver covering LW, MW and full SW
- Fully integrated tuning system with low phase noise and fast tuning
- FM LNA with AGC
- FM Stereo Improvement algorithm - FMSI (TEF6687 and TEF6689)
- State-of-the art FM Improved Multipath Suppression
- FM Channel Equalization
- Soft Mute on Modulation
- Stereo High Blend
- FM mixer for frequency conversion to a low IF complex signal (AM SW)
- AM LNA with AGC, matching active and passive antenna applications
- AM mixer for frequency conversion to a low IF complex signal
- High dynamic range Sigma Delta IF ADC
- Digital IF signal processing including decimation, shift to baseband, AGC control, I/Q correction, variable IF bandwidth filtering (PACS) and demodulation
- FM stereo decoding
- TEF6688 and TEF6689 baseband I^2S output supporting HD Radio and DRM[1] with external digital radio coprocessor (SAF356X or SAF360X)
- Blending function for HD Radio reception (TEF6688 and TEF6689)
- AM and FM noise blanking, Signal quality detection and weak signal processing
- Advanced RDS and RBDS demodulation and decoding
- MPX output supporting DARC demodulator
- One I^2S input and one I^2S output
- Two mono audio DACs
- Single 3.3 V supply voltage
- Fast mode I^2C-bus (400 kHz)
- Configurable GPIO pins for RDS, Quality Status Interrupt and generic I^2C-bus controlled I/O
- Qualified in accordance with AEC-Q100

3. Applications

The TEF668X is a single tuner AM/FM receiver for automotive applications and supports analog AM/FM and HD/DRM reception (HD/DRM is supported in TEF6688 and TEF6689 only).

Additionally, due to a common technology platform, the TEF668X can be combined with TEF701X, SAF775X and SAF360X.

1. DRM includes DRM30 and DRM+ (band I and II)

4. Functionality

Table 1. Feature set

Features	TEF6686	TEF6687	TEF6688	TEF6689
Standard				
Digital to Analog converters (stereo audio DAC)	1	1	1	1
Audio I^2S (can be disabled or enabled)	Yes			
HD Radio	-	-	Yes	Yes
DRM	-	-	Yes	Yes
FM	Yes			
LW - MW	Yes			
SW	Yes			
Standard Radio features				
RDS demodulator and decoder	Yes			
FM PACS	Yes			
Softmute	Yes			
HighCut	Yes			
Stereo Blend	Yes			
Advanced Radio features				
Dynamic LowCut	Yes			
AM IF noise blanking	Yes			
High-end Radio features				
Improved Multipath Suppression (IMS)	Yes			
Channel equalizer	Yes			
FMSI	-	Yes	-	Yes
Softmute on modulation	Yes			
High blend	Yes			

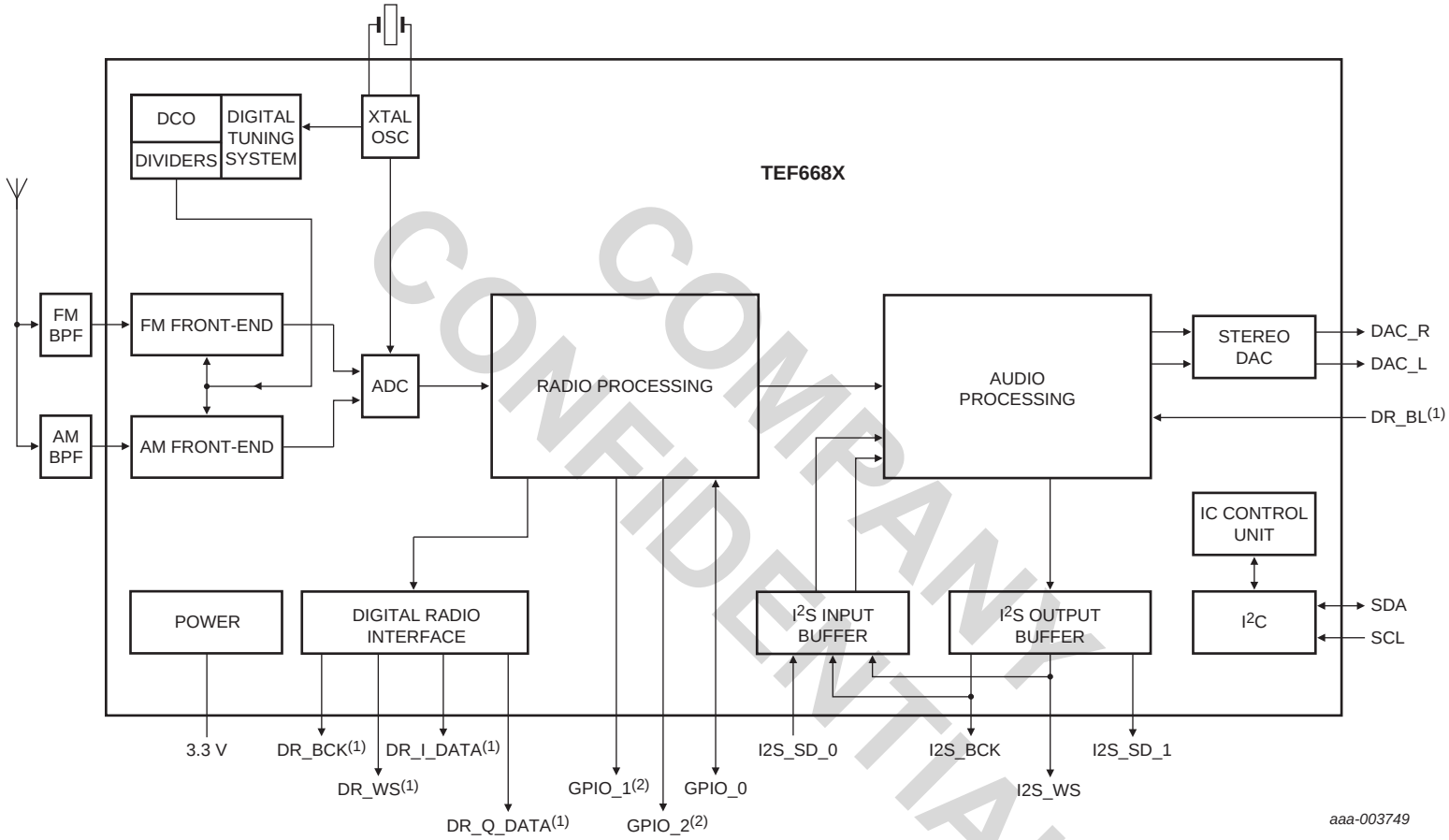
5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEF6686HN/V102	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm[1]	SOT617-3
TEF6687HN/V102			
TEF6688HN/V102			
TEF6689HN/V102			

[1] Wettable sides to allow for optical inspection.

6. Block diagram



(1) TEF6688 and TEF6689.

(2) GPIO_1 and GPIO_2 are output only.

Fig 1. Block diagram

7. Pinning information

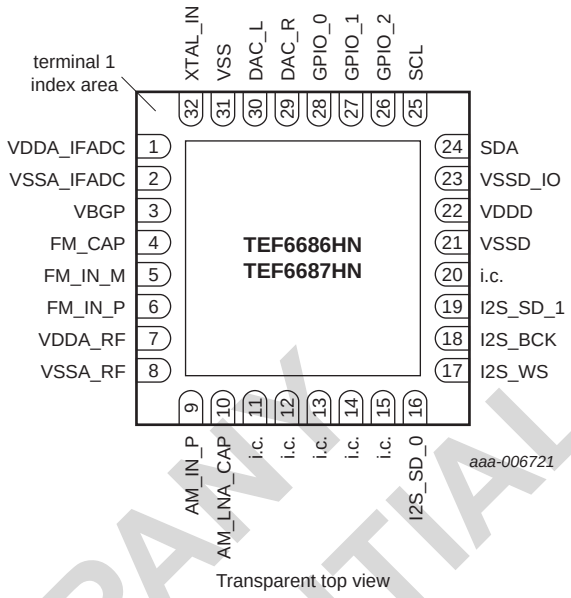


Fig 2. Pin configuration TEF6686HN and TEF6687HN

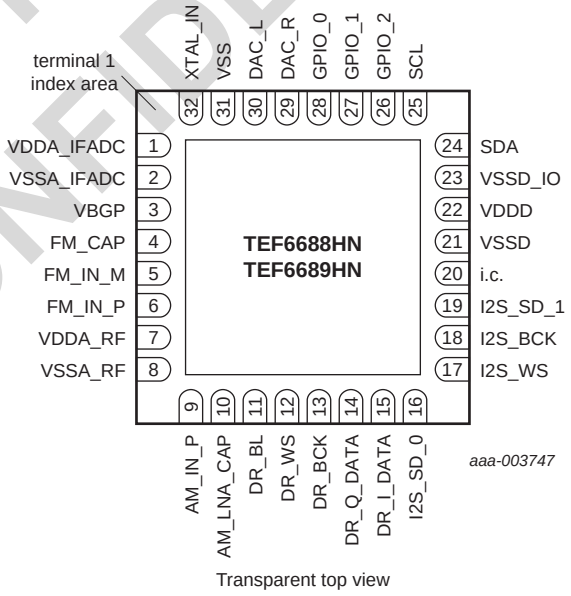


Fig 3. Pin configuration TEF6688HN and TEF6689HN

7.1 Pin description

Table 3. Pin description

Symbol	TEF6686/ TEF6687	TEF6688/ TEF6689	Pull-up or pull-down[1]	Type[2]	Description
	Pin	Pin			
VDDA_IFADC	1	1	n.a.	AP	IF ADC analog supply voltage
VSSA_IFADC	2	2	n.a.	AG	IF ADC analog ground supply voltage
VBGP	3	3	n.a.	AR	bandgap reference voltage decoupling
FM_CAP	4	4	n.a.	AI	FM AGC capacitor
FM_IN_M	5	5	n.a.	AI	negative FM RF input
FM_IN_P	6	6	n.a.	AI	positive FM RF input
VDDA_RF	7	7	n.a.	AP	RF analog supply voltage
VSSA_RF	8	8	n.a.	AG	RF analog ground supply voltage
AM_IN_P	9	9	n.a.	AI	positive AM LNA input
AM_LNA_CAP	10	10	n.a.	AI	AM LNA AGC capacitor
i.c.	11	-	-	-	internally connected, leave open
DR_BL	-	11	n.a.	I	HD Radio signal FM blend
i.c.	12	-	-	-	internally connected, leave open
DR_WS	-	12	n.a.	O	digital radio word select output
i.c.	13	-	-	-	internally connected, leave open
DR_BCK	-	13	n.a.	O	digital radio bit clock output
i.c.	14	-	-	-	internally connected, leave open
DR_Q_DATA	-	14	n.a.	O	serial data output for digital radio quadrature-phase data
i.c.	15	-	-	-	internally connected, leave open
DR_I_DATA	-	15	n.a.	O	serial data output for digital radio in-phase data
I2S_SD_0	16	16	D	I/O	I^2S data
I2S_WS	17	17	D	I/O	I^2S word select input/output[3]
I2S_BCK	18	18	D	I/O	I^2S bit clock input/output[3]
I2S_SD_1	19	19	D	I/O	I^2S data
i.c.	20	20	-	-	internally connected, leave open
VSSD	21	21	n.a.	G	3.3 V ground digital supply voltage
VDDD	22	22	n.a.	P	3.3 V digital supply voltage
VSSD_IO	23	23	n.a.	G	digital input/output ground connection
SDA	24	24	n.a.	I^2C	I^2C-bus serial data input and output
SCL	25	25	n.a.	I^2C	I^2C-bus serial clock input
GPIO_2	26	26	n.a.	O	general purpose output 2
GPIO_1	27	27	n.a.	O	general purpose output 1
GPIO_0	28	28	n.a.	I/O	general purpose input/output
DAC_R	29	29	n.a.	AO	right channel audio output

Table 3. Pin description *...continued*

Symbol	TEF6686/ TEF6687	TEF6688/ TEF6689	Pull-up or pull-down[1]	Type[2]	Description
	Pin	Pin			
DAC_L	30	30	n.a.	AO	left channel audio output
VSS	31	31	n.a.	G	ground connection
XTAL_IN	32	32	n.a.	AI	crystal oscillator input

[1] D means internal weak pull-down of 50 kΩ; n.a. is non applicable.

[2] The pin types are defined in Table 4.

[3] Pins are either both inputs or both outputs.

Table 4. Pin type description

Type	Description
AI	analog input pin
AG	analog ground pin
AO	analog output pin
AP	analog power pin
AR	analog reference pin
G	ground pin
I	input
I/O	input or output
I^2C	I^2C-bus pin; 3.3 V tolerant
O	output
P	power supply pin

8. Functional description

8.1 FM front-end to IF ADC input

The RF input signal from the antenna is filtered by an external wideband band-pass RF filter. The RF filter passes the complete FM band of interest and provides impedance transformation for the antenna impedance matching.

The RF filter output signal is applied to the high dynamic range FM LNA. The LNA gain is controlled by the integrated AGC loop. The AGC range is seven steps of 6 dB. The input impedance of the LNA remains constant over the first five AGC steps and is reduced for the last two AGC steps.

The signal from the LNA is converted to a low IF using a complex mixer which includes image rejection. The IF signal from the mixer is amplified and filtered before the IF signal is digitized by the IF ADC.

8.2 AM front-end to IF ADC input

The RF input signal from the antenna is filtered by an external high-pass filter and an FM frequency band reject filter. The high-pass filter attenuates 50 Hz/60 Hz signals from power supply lines. The band reject filter or FM intrusion filter attenuates the FM signals before entering the AM LNA, preventing intermodulation from two FM signals degrading AM reception.

After filtering, the RF signal is applied to the AM LNA. The gain of the AM LNA can be controlled with up to ten 6 dB steps by the integrated AGC loop. The input capacitance of the AM LNA is constant over the first seven AGC steps and is reduced for the last three AGC steps.

In AM LW and MW mode, the LNA output signal is filtered before being applied to the IF ADC. The lack of frequency conversion eliminates performance limitations due to reception of image and harmonic LO frequencies.

In AM SW mode, the LNA output signal is filtered and applied to a complex image reject mixer for frequency conversion to low IF. This IF signal is amplified and filtered before it is digitized by the IF ADC.

8.3 Tuning system

The PLL tuning system provides the LO signal to drive the AM-SW and FM mixer for frequency conversion to low IF. The tuning system is capable of tuning to the US, European, Japanese, and OIRT FM bands and the full AM SW band. The tuning system combines low phase noise with fast tuning times.

8.4 IF ADC

The IF signal is digitized by a high dynamic range sigma-delta IF ADC. Due to the high dynamic range, there is no need for narrowband IF filtering. The IF ADC provides two bitstreams (I and Q data) to the radio processing block.

8.5 Radio processing

Radio processing performs the following functions:

- Decimation of the IF ADC bit streams
- Shift to baseband
- AGC compensation
- Linear AGC detection and control
- I/Q error detection and correction
- Interface to terrestrial digital radio processor for HD Radio or DRM reception (TEF6688 and TEF6689)
- Channel filtering
- AM/FM demodulation
- Ignition noise detection and correction
- FM stereo decoding with FMSI (TEF6687 and TEF6689)
- Programmable de-emphasis

- Quality detection
- Weak signal handling
- RDS/RBDS demodulation, decoding and error correction

The output of the radio processing block is a left and right digital audio signal.

8.5.1 AM mode features

Adjacent channels are rejected by the channel filter. The bandwidth of the channel filter can be programmed.

Ignition noise pulses are suppressed by the AM noise blanker, consisting of an IF noise blanker in front of the channel filter and an audio noise blanker after AM demodulation.

The following quality detectors are used to measure the quality of the signal reception:

- RSSI or field strength detection (level)
- Frequency offset detection
- AM modulation detection

The signal quality in weak reception conditions is improved by the AM weak signal handling consisting of:

- Soft mute controlled by level and modulation
- High-cut controlled by level and modulation

8.5.2 FM mode features

The TEF668X offers the high-end features Channel Equalizer and Improved Multipath Suppression. The Channel Equalizer improves multipath reception as well as weak signal reception by means of adaptive filtering.

The Improved Multipath Suppression algorithm reduces the audibility of multipath distortions.

The FMSI feature is available for the TEF6687 and TEF6689 and offers significant improved FM stereo performance. Conventional receivers blend from stereo to mono at medium signal levels of 40 dBμV to avoid the FM stereo noise being audible. With FMSI the stereo to mono blend is extended down to very weak signal levels of 10 dBμV without excessive stereo noise.

Adjacent channels are rejected by the channel filter. The bandwidth of the channel filter is variable and is dynamically controlled by the FM PACS algorithm. The bandwidth depends on the adjacent channel conditions and properties of the desired signal such as modulation and signal strength.

Ignition noise pulses are detected and suppressed by the noise blanker

The following quality detectors are used to measure the quality of the signal reception:

- RSSI or field strength detection (level)
- Frequency offset detection
- Multipath and adjacent channel detection by USN detection

- Multipath detection by WAM detection
- Frequency deviation by modulation detection
- Stereo pilot detection

The signal quality under weak signal and multipath conditions is improved by the FM weak signal handling, consisting of:

- Soft mute controlled by level, USN and WAM
- HighCut/LowCut controlled by level, USN, WAM and modulation
- Stereo blend controlled by level, USN, WAM and modulation
- Stereo HighBlend controlled by level, USN, WAM and modulation

8.5.3 RDS/RBDS

An RDS demodulator and RDS decoder processes the data received from RDS and RBDS transmissions with excellent RDS sensitivity.

8.5.3.1 RDS demodulator

The RDS demodulator includes optimized filtering and linear signal processing that allows very good RDS sensitivity. The MPX signal is filtered for selection of the 57 kHz RDS signal and data shaping. The RDS demodulator data is fed into the RDS decoder for further processing. To support available software stacks, the RDS demodulator data can also be read directly via the I^2C-bus or GPIO pins.

8.5.3.2 RDS decoder

The RDS decoder provides synchronization to the block and group structure of the demodulated RDS data stream. When synchronized, the decoder delivers data in a fixed ABCD group order for easy software handling. In the background, synchronization search continues for fast correction on bit slip or other synchronization errors. Extended error detection and correction are included.

An I^2C register indicates the availability of a new group. An interrupt signal ‘data available’ can be provided on a GPIO pin.

‘Data available’ is indicated whenever a new group is received (that is at reception of block D). For fast PI code reception, at synchronization start ‘data available’ is flagged on reception of the first PI code, such as block A or block C’.

8.5.4 Digital radio interface

For HD Radio and DRM reception (TEF6688 and TEF6689), the baseband signal is output to an external digital radio coprocessor, such as the NXP Semiconductors SAF356X or SAF360X. The baseband I^2S output includes a Bit ClocK (BCK), Word Select (WS) and the in-phase and quadrature-phase data signals (I-data and Q-data).

8.6 Audio input

One I^2S audio input is available supporting sample rates 44.1 kHz and 48 kHz.

8.7 Audio processing

The audio processing block has the following features:

- Volume control including mute
- HD Radio blending (TEF6688 and TEF6689)

8.8 Audio output

The audio output includes two mono DACs and one I²S audio output supporting sample rates 44.1 kHz and 48 kHz.

8.9 Crystal oscillator and external clock interface

In a stand-alone AM/FM application, the digital radio interface is not used. The crystal oscillator can be used with a fundamental mode crystal with a frequency of 4.000 MHz, 9.216 MHz or 12.000 MHz. In a system using digital radio coprocessor SAF356X or SAF360X, the crystal for the TEF6688 and TEF6689 must be 9.216 MHz or 12.000 MHz.

Instead of the stand-alone operation with a dedicated crystal, the TEF668X can also operate on an external supplied clock reference of 55.46667 MHz.

8.10 I²C-bus interface

The TEF668X is controlled by means of the I²C-bus interface. The I²C-bus interface supports the fast mode of 400 kbit/s in accordance with the I²C-bus specification.

The TEF668X I²C address selection is defined by the voltage levels on GPIO_2 pin during power up. The I²C address is C8h (default) or can be configured to be CAh. The I²C address selection table is defined in the application note Ref. 9

A logic 0 requires a 10 kΩ pull-down resistor to connect to ground. For a logic 1, the pin must be connected to the 3.3 V supply voltage by a 10 kΩ pull-up resistor.

9. I²C-bus protocol

The user manual Ref. 10 describes the software control interface for the TEF668X.

9.1 Write mode

Standard write transmissions to the TEF668X consist of an I²C-bus start condition and an 8-bit hardware device address for write as defined by the I²C-bus standard. Next, an 8-bit module identifier for FM, AM, audio, system and other parts. Control is indicated by an 8-bit command identifier and an 8-bit parameter index, followed by one or more 16-bit parameters.

Writing data to inactive modules is supported and this data is stored. Stored data is used upon activation of the module.

9.2 Read mode

Standard read transmissions from the TEF668X consist of writing a read request followed by the actual read transmission to obtain data.

Remark: The I²C-bus standard does not allow read addressing within a read transmission.

Received data or status information is read using special Get commands that include an index setting similar to Write definitions which are required for reading large data blocks and for future extendability.

A command with index 0 returns the module and command value. These commands are useful to allow for instances where requested data cannot be returned in time due to internal data handling delays.

In special cases, Get commands with index 0 or 1 require data to be read from the start. Read data with index is useful to read data blocks of a particular size, in case read buffers have limited size.

10. Overview of commands

Table 5. Write commands overview

Module	Command number	Command name	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5	Parameter 6	Parameter 7
FM/AM	1	Tune_To	mode	frequency (kHz)	-	-	-	-	-
FM	2	Set_Tune_Options	afu_bw mode	afu_bandw (kHz)	mute_time (ms)	sample_time (ms)	-	-	-
FM/AM	10	Set_Bandwidth	mode	bandwidth (kHz)	sensitivity (%)	lo_sensitivity (%)	-	-	-
FM/AM	11	Set_RFAGC	start (dBμV)	extension	-	-	-	-	-
AM	12	Set_Antenna	attenuation (dB)	-	-	-	-	-	-
FM	20	Set_MphSuppression	mode	-	-	-	-	-	-
FM	22	Set_ChannelEqualizer	mode	-	-	-	-	-	-
FM/AM	23	Set_NoiseBlanker	mode	sensitivity (%)	-	-	-	-	-
AM	24	Set_NoiseBlanker_Audio	mode	sensitivity (%)	-	-	-	-	-
FM/AM	30	Set_DigitalRadio[1]	mode (on/off)	-	-	-	-	-	-
FM	31	Set_Deemphasis	timeconstant (μs)	-	-	-	-	-	-
FM	32	Set_StereoImprovement[2]	mode	-	-	-	-	-	-
FM/AM	38	Set_LevelStep	step1 (dB)	step2 (dB)	step3 (dB)	step4 (dB)	step5 (dB)	step6 (dB)	step7 (dB)
FM/AM	39	Set_LevelOffset	offset (dB)	-	-	-	-	-	-
FM/AM	40	Set_SoftMute_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)	-	-	-
AM	41	Set_SoftMute_Mod	mode	start (mod %)	slope (mod %)	shift (control %)	-	-	-

Table 5. Write commands overview *...continued*

Module	Command number	Command name	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5	Parameter 6	Parameter 7
FM/AM	42	Set_SoftMute_Level	mode	start (dBμV)	slope (dB)	-	-	-	-
FM	43	Set_SoftMute_Noise	mode	start (%)	slope (%)	-	-	-	-
FM	44	Set_SoftMute_Mph	mode	start (%)	slope (%)	-	-	-	-
FM/AM	45	Set_SoftMute_Max	mode	limit (dB)	-	-	-	-	-
FM/AM	50	Set_HighCut_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)	-	-	-
FM/AM	51	Set_HighCut_Mod	mode	start (mod %)	slope (mod %)	shift (control %)	-	-	-
FM/AM	52	Set_HighCut_Level	mode	start (dBμV)	slope (dB)	-	-	-	-
FM	53	Set_HighCut_Noise	mode	start (%)	slope (%)	-	-	-	-
FM	54	Set_HighCut_Mph	mode	start (%)	slope (%)	-	-	-	-
FM/AM	55	Set_HighCut_Max	mode	limit (Hz)	-	-	-	-	-
FM/AM	56	Set_HighCut_Min	mode	limit (Hz)	-	-	-	-	-
FM/AM	57	Set_LowCut_Max	mode	limit (Hz)	-	-	-	-	-
FM/AM	58	Set_LowCut_Min	mode	limit (Hz)	-	-	-	-	-
FM/AM	59	Set_HighCut_Options	mode	-	-	-	-	-	-
FM	60	Set_Stereo_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)	-	-	-
FM	61	Set_Stereo_Mod	mode	start (mod %)	slope (mod %)	shift (control %)	-	-	-
FM	62	Set_Stereo_Level	mode	start (dBμV)	slope (dB)	-	-	-	-
FM	63	Set_Stereo_Noise	mode	start (%)	slope (%)	-	-	-	-
FM	64	Set_Stereo_Mph	mode	start (%)	slope (%)	-	-	-	-
FM	65	Set_Stereo_Max	mode	-	-	-	-	-	-
FM	66	Set_Stereo_Min	mode	limit (c.s. dB)	-	-	-	-	-
FM	70	Set_StHiBlend_Time	slow_attack (ms)	slow_decay (ms)	fast_attack (ms)	fast_decay (ms)	-	-	-
FM	71	Set_StHiBlend_Mod	mode	start (mod %)	slope (mod %)	shift (control %)	-	-	-
FM	72	Set_StHiBlend_Level	mode	start (dBμV)	slope (dB)	-	-	-	-
FM	73	Set_StHiBlend_Noise	mode	start (%)	slope (%)	-	-	-	-
FM	74	Set_StHiBlend_Mph	mode	start (%)	slope (%)	-	-	-	-

Table 5. Write commands overview *...continued*

Module	Command number	Command name	Parameter 1	Parameter 2	Parameter 3	Parameter 4	Parameter 5	Parameter 6	Parameter 7
FM	75	Set_StHiBlend_Max	mode	limit (Hz)	-	-	-	-	-
FM	76	Set_StHiBlend_Min	mode	limit (Hz)	-	-	-	-	-
FM/AM	80	Set_Scaler	gain (dB)	-	-	-	-	-	-
FM	81	Set_RDS	mode	restart	interface	-	-	-	-
FM/AM	82	Set_QualityStatus	mode	interface	-	-	-	-	-
FM/AM	83	Set_DR_Blend[1]	mode	in_time (ms)	out_time (ms)	gain (dB)	-	-	-
FM/AM	84	Set_DR_Options[1]	samplerate	mode	format	-	-	-	-
FM/AM	85	Set_Specials	ana_out	-	-	-	-	-	-
FM	90	Set_StBandBlend_Time[2]	attack	decay	-	-	-	-	-
FM	91	Set_StBandBlend_Gain[2]	band1	band2	band3	band4	-	-	-
FM	92	Set_StBandBlend_Bias[2]	band1	band2	band3	band4	-	-	-
AUDIO	10	Set_Volume	volume (dB)	-	-	-	-	-	-
AUDIO	11	Set_Mute	mode	-	-	-	-	-	-
AUDIO	12	Set_Input	source	-	-	-	-	-	-
AUDIO	13	Set_Output_Source	signal	source	-	-	-	-	-
AUDIO	21	Set_Ana_Out	signal	mode	-	-	-	-	-
AUDIO	22	Set_Dig_IO	signal	mode	format	operation	-	-	-
			samplerate	-	-	-	-	-	-
AUDIO	23	Set_Input_Scaler	source	gain (dB)	-	-	-	-	-
AUDIO	24	Set_WaveGen[3]	mode	offset	amplitude1	frequency1	-	-	-
			amplitude2	frequency2	-	-	-	-	-
APPL	1	Set_OperationMode	mode	-	-	-	-	-	-
APPL	3	Set_GPIO	pin	module	feature	-	-	-	-
APPL	4	Set_ReferenceClock	frequency_msb	frequency_lsb	type	-	-	-	-
APPL	5	Activate	mode	-	-	-	-	-	-

[1] TEF6688 and TEF6689 only.

[2] TEF6687 and TEF6689 only.

[3] For test purposes only.

Table 6. Read commands overview

Module	Command number	Command name	1	2	3	4
FM/AM	128	Get_Quality_Status	status	level	usn	warn
			offset	bandwidth	modulation	-
FM/AM	129	Get_Quality_Data	status	level	usn	warn
			offset	bandwidth	modulation	-
FM	130	Get_RDS_Status	status	a_block	b_block	c_block
			d_block	dec_error	-	-
FM	131	Get_RDS_Data	status	a_block	b_block	c_block
			d_block	dec_error	-	-
FM/AM	132	Get_AGC	input_att	feedback_att	-	-
FM/AM	133	Get_Signal_Status	status (stereo, digital)	-	-	-
FM/AM	134	Get_Processing_Status	softmute	highcut	stereo	sthiblend
			stband_1_2[1]	stband_3_4[1]	-	-
FM/AM	135	Get_Interface_Status[2]	samplerate	-	-	-
APPL	128	Get_Operation_Status	status	-	-	-
APPL	129	Get_GPIO_Status	status (pin state)	-	-	-
APPL	130	Get_Identification	device (type, variant)	hw_version (main, sub)	sw_version	-
APPL	131	Get_LastWrite	size/module	cmd/index	parameter	parameter
			parameter	parameter	parameter	parameter

[1] TEF6687 and TEF6689 only.

[2] TEF6688 and TEF6689 only.

11. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(RF)3V3}$	RF analog supply voltage (3.3 V)	on pin VDDA_RF		–0.5	+3.9	V
$V_{DDA(IF)3V3}$	IF analog supply voltage (3.3 V)	on pin VDDA_IFADC		–0.5	+3.9	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	on pin VDDD		–0.5	+3.9	V
$\Delta V_{DD(3V3-3V3)}$	supply voltage difference between two 3.3 V supplies	between pins VDDA_IFADC and VDDA_RF		–0.3	+0.3	V
V_n	voltage on any other pin			–0.5	$+V_{DDD(3V3)}$ + 0.3	V
I_{lu}	latch-up current	all supply voltages below the maximum value	[1]	–100	+100	mA
V_{lu}	latch-up voltage			-	$1.5 \times V_{DDD(3V3)}$	V
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			–40	+125	°C

Table 7. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	human body model	[2]	−2000	+2000	V
		charged-device model	[1]			
		corner pins		−750	+750	V
		other pins		−500	+500	V
P_{tot}	total power dissipation	$V_{DDA(RF)(3V3)}$ = 3.5 V; $V_{DDA(IF)(3V3)}$ = 3.5 V; $V_{DDD(3V3)}$ = 3.5 V		-	700	mW

[1] In accordance with AEC-Q100-004.

[2] In accordance with JESD22-A114 Class 2.

12. Thermal characteristics

Table 8. Thermal characteristics

The performance parameters are specified with center pin soldered to the board

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVQFN32 dual-layer board	[1]	50	K/W
		HVQFN32 four-layer board		30	K/W

[1] Simulation result assuming a dual layer board with a copper thickness of 35 µm; size: 50 mm × 50 mm; exposed die pad soldered to thermal landing pattern: thermal landing pattern connected to a large ground plane on the bottom layer by multiple thermal vias; copper coverages 25 % (top layer) and 90 % (bottom layer).

13. Static characteristics

Table 9. Voltage and current characteristics

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
$V_{DDA(RF)3V3}$	RF analog supply voltage (3.3 V)	on pin VDDA_RF	3.0	3.3	3.5	V
$V_{DDA(IF)3V3}$	IF analog supply voltage (3.3 V)	on pin VDDA_IFADC	3.0	3.3	3.5	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	on pin VDD_DIGITAL	3.0	3.3	3.5	V
Current in FM mode						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF	33	37	42	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC	81	94	110	mA
I_{DDD}	digital supply current	on pin VDDD	37	38	48	mA
Current in AM - MW/LW mode						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF	34	40	48	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC	63	74	86	mA
I_{DDD}	digital supply current	on pin VDDD	33	34	46	mA
Current in Standby mode						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF	0	0.3	2	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC	25	37	45	mA
I_{DDD}	digital supply current	on pin VDDD	15	24	35	mA

14. Dynamic characteristics

Table 10. Dynamic characteristics for audio processing and audio DAC

$V_{DDA(RF)(3V3)}$ = 3.3 V; $V_{DDA(IF)(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; f_s = 44.1 kHz; T_{amb} = 25 °C; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Audio processing						
G_{aud}	audio gain		–60	-	+24	dB
α_{mute}	mute attenuation		-	-	–80	dB
Audio DAC						
V_o	output voltage	at 0 dBFS digital input; R_L = 20 kΩ	870	910	950	mV
R_o	output resistance		-	-	1	kΩ
$\alpha_{o(unb)(ch-ch)}$	output unbalance between channels		–0.2	-	+0.2	dB
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	0 dBFS with unweighted 20 Hz to 20 kHz audio filter; R_L = 20 kΩ	-	-	–70	dB
		–60 dBFS with A-weighted audio filter; R_L = 20 kΩ	-	-	–27	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	in-band noise on idle channel, A-weighted	-	-	36	μV
α_{cs}	channel separation		70	-	-	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{supply(ripple)}/V_{audio(ripple)}$	50	-	-	dB
R_L	load resistance		20	-	-	kΩ
f_{resp}	frequency response	–3 dB corner frequency related to f_{AF} = 1 kHz	100	-	-	kHz
		low audio	-	-	20	Hz
		high audio	18	-	-	kHz

Table 11. Dynamic characteristics for tuning system

$V_{DDA(RF)(3V3)}$ = 3.3 V; $V_{DDA(IF)(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; all AC values are RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Crystal oscillator							
f_{nom}	nominal frequency	stand alone, digital radio interface not used		-	4.000	-	MHz
				-	9.216	-	MHz
				-	12.000	-	MHz
		digital radio interface enabled	[1]	-	9.216	-	MHz
			[1]	-	12.000	-	MHz
Clock interface							
$f_{clk(ext)}$	external clock frequency			-	55.46667	-	MHz
$V_{i(osc)}$	oscillator input voltage	peak-to-peak		200	400	-	mV

[1] Only applicable for TEF6688 and TEF6689.

Table 12. FM radio characteristics

f = 98.1 MHz, Δf = 22.5 kHz, f_{AF} = 1 kHz, 50 μs de-emphasis, IEC tuner filter 75 Ω/−6 dB dummy antenna, all signals in RMS at input dummy unless otherwise specified. Analog audio output at pins DAC_L and DAC_R.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	FM tuning range		65	-	108	MHz
$V_{i(sens)}$	input sensitivity voltage	$V_{i(RF)}$ for 26 dB SNR; channel equalizer on		-	−4	0	dBμV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 50 dBμV to 120 dBμV; mono		60	68	-	dB
		$V_{i(RF)}$ = 60 dBμV to 120 dBμV; stereo		56	60	-	dB
$\alpha_{sup(AM)}$	AM suppression	m = 30 %; f_{AF} = 1 kHz; $V_{i(RF)}$ = 40 dBμV to 120 dBμV		58	68	-	dB
THD	total harmonic distortion	f_{AF} = 1 kHz; $V_{i(RF)}$ = 20 dBμV to 120 dBμV					
		Δf = 75 kHz; mono		-	0.01	0.1	%
		Δf = 67.5 kHz; stereo; L_{out} only		-	0.1	0.3	%
S	selectivity	$V_{RF(wanted)}$ = 20 dBμV; Δf(wanted) = 22.5 kHz for 0 dB reference; $f_{AF(wanted)}$ = 1 kHz; $f_{RF(unw)} = f_{RF(wanted)} \pm \Delta f_{RF}$; Δf(unw) = 22.5 kHz; $f_{AF(unw)}$ = 1 kHz; increase $V_{RF(unw)}$ until SNR = 26 dB; $S = V_{RF(unw)} / V_{RF(wanted)}$; channel equalizer on					
		Δf_{RF} = 100 kHz		60	67	-	dB
		Δf_{RF} = 200 kHz		70	77	-	dB
IP3	third-order intercept point	$\Delta f_{RF(unw)1} = \pm$ 400 kHz; $\Delta f_{RF(unw)2} = \pm$ 800 kHz		115	120	-	dBμV
IP2	second-order intercept point	$f_{RF(unw)1}$ = 50 MHz; $f_{RF(unw)2}$ = 48 MHz		160	180	-	dBμV
$V_{i(RF)AGC(start)}$	start AGC RF input voltage	highest setting		-	92	-	dBμV
		lowest setting		-	84	-	dBμV
$\alpha_{cr(AGC)}$	AGC control range	internal AGC		-	40	-	dB
		external AGC		-	6	-	dB
α_{cs}	channel separation	Δf = 67.5 kHz; f_{AF} = 1 kHz; Δf_{pilot} = 7.5 kHz					
		$V_{i(RF)}$ = 20 dBμV	[1]	-	30	-	dB
		$V_{i(RF)}$ = 60 dBμV to 120 dBμV		45	-	-	dB
S_{RDS}	RDS sensitivity	Δf_{RDS} = 2 kHz; stereo; Δf_{FM} = 22.5 kHz; L = R; f_{AF} = 1 kHz					
		50 % correct blocks without error correction		-	15	19	dBμV
		95 % correct blocks without error correction		-	18	22	dBμV
V_o	output voltage	V_{RF} = 60 dBμV		-	120	-	mV
		DARC output; V_{RF} = 60 dBμV		-	150	-	mV

[1] Only applicable for TEF6687 and TEF6689.

Table 13. AM radio characteristics

f = 990 kHz; m = 30 %; f_{AF} = 1 kHz; IEC tuner filter 15 pF/60 pF dummy antenna; all signal levels in RMS at input dummy; unless otherwise specified. Analog audio output at pins DAC_L and DAC_R.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RF}	RF frequency	AM (LW) tuning range	144	-	288	kHz
		AM (MW) tuning range	522	-	1710	kHz
		AM (SW) tuning range	2.3	-	27.0	MHz
$V_{i(sens)}$	input sensitivity voltage	S/N = 26 dB; B_{aud} = 2 kHz; f_{RF} = 990 kHz; m = 30 %; f_{AF} = 400 kHz	-	32	36	dBµV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 74 dBµV	60	65	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 50 dBµV to 120 dBµV				
		f_{AF} = 1 kHz; m = 80 %	-	0.1	0.3	%
		f_{AF} = 400 Hz; m = 80 %	-	0.1	0.3	%
		f_{AF} = 100 Hz; m = 80 %	-	0.1	0.5	%
S_{stat}	static selectivity	single signal; Δf_{RF} = 10 kHz; $f_{tune} \pm 10$ kHz	70	80	-	dB
		single signal; Δf_{RF} = 20 kHz; $f_{tune} \pm 20$ kHz	80	-	-	dB
IP3	third-order intercept point	$\Delta f_{RF(unw)1}$ = 40 kHz; $\Delta f_{RF(unw)2}$ = 80 kHz	130	133	-	dBµV
		$\Delta f_{RF(unw)1}$ = 300 kHz; $\Delta f_{RF(unw)2}$ = 600 kHz	130	133	-	dBµV
IP2	second-order intercept point	$f_{RF(wanted)}$ = 1400 kHz; $f_{RF(unw)1}$ = 600 kHz; $f_{RF(unw)2}$ = 800 kHz	160	170	-	dBµV
V_o	output voltage	V_{RF} = 60 dBµV	-	100	-	mV

15. Application information

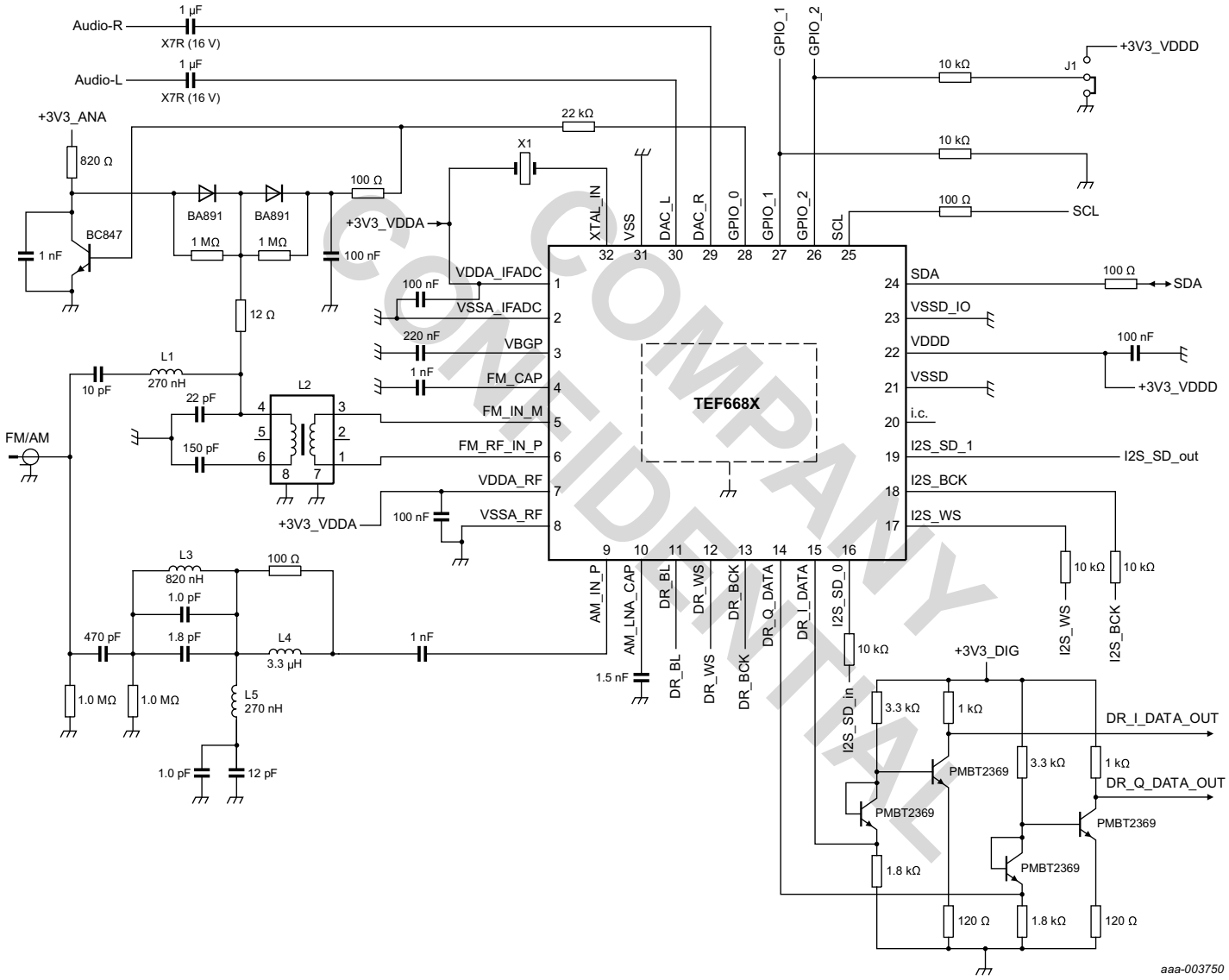


Fig 4. Schematic diagram

Table 14. List of components for Figure 4

Symbol	Type	Series	Manufacturer
L1	C2012C-R27J	C2012C	Sagami
L2	#A1313AN-0004GGH	5CCEG	Toko
L3	C2012C-R82J	C2012C	Sagami
L4	LLM2520-3R3K	LLM2520	Toko
L5	C2012C-R27J	C2012C	Sagami
X1	DSX530GA (9.216 MHz)	DSX530GA	KDS
	AS04000005 (4.000 MHz)	9B (HC-49S)	TXC
	AT040000xx (4.000 MHz)	9C (HC-49S SMD)	TXC
	AV12000003 (12.000 MHz)	AV	TXC

Table 15. DC operating points

$V_{DDA(RF)(3V3)}$ = 3.3 V; $V_{DDA(IF)(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
I2S_WS	17	-	0/3.3	-	-	0/3.3	-
I2S_BCK	18	-	0/3.3	-	-	0/3.3	-
I2S_SD_1	19	-	1.1	-	-	1.1	-
i.c.	20	-	0	-	-	0	-
GPIO_0	28	-	0/3.3	-	-	0/3.3	-
VSSA_RF	8	external GND			external GND		
AM_LNA_CAP	10	-	0	-	0.4	0.6	0.8
AM_IN_P	9	-	0	-	-	0.63	-
VSSA_IFADC	2	external GND			external GND		
VDDA_RF	7	external 3.3			external 3.3		
FM_IN_M	5	1.15	1.27	1.45	-	1.54	-
FM_IN_P	6	1.15	1.27	1.45	-	1.54	-
FM_CAP	4	-	1.27	-	-	1.54	-
XTAL_IN	32	-	2.8	-	-	2.8	-
VDDA_IFADC	1	external 3.3			external 3.3		
DAC_R	29	-	0.9	-	-	0.9	-
DAC_L	30	-	0.9	-	-	0.9	-
VSSD	21	external GND			external GND		
SCL	25	0/external I²C-bus voltage			0/external I²C-bus voltage		
SDA	24	0/external I²C-bus voltage			0/external I²C-bus voltage		
DR_Q_DATA[1]	14	-	0/3.3	-	-	0/3.3	-
DR_BCK[1]	13	-	0/3.3	-	-	0/3.3	-
I2S_SD_0	16	-	0/3.3	-	-	0/3.3	-
DR_I_DATA[1]	15	-	0/3.3	-	-	0/3.3	-
VDDD	22	external 3.3			external 3.3		
VBGP	3	2.42	2.55	2.67	2.42	2.55	2.67

Table 15. DC operating points *…continued*

$V_{DDA(RF)(3V3)}$ = 3.3 V; $V_{DDA(IF)(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
DR_BL[1]	11	-	0/3.3	-	-	0/3.3	-
VSS	31	external GND			external GND		
DR_WS[1]	12	-	0/3.3	-	-	0/3.3	-
VSSD_IO	23	external GND			external GND		
GPIO_2	26	-	0/3.3	-	-	0/3.3	-
GPIO_1	27	-	0/3.3	-	-	0/3.3	-

[1] This pin is internally connected for the TEF6686 and TEF6687. The function is only available in TEF6688 and TEF6689.

16. Test information

16.1 Quality information

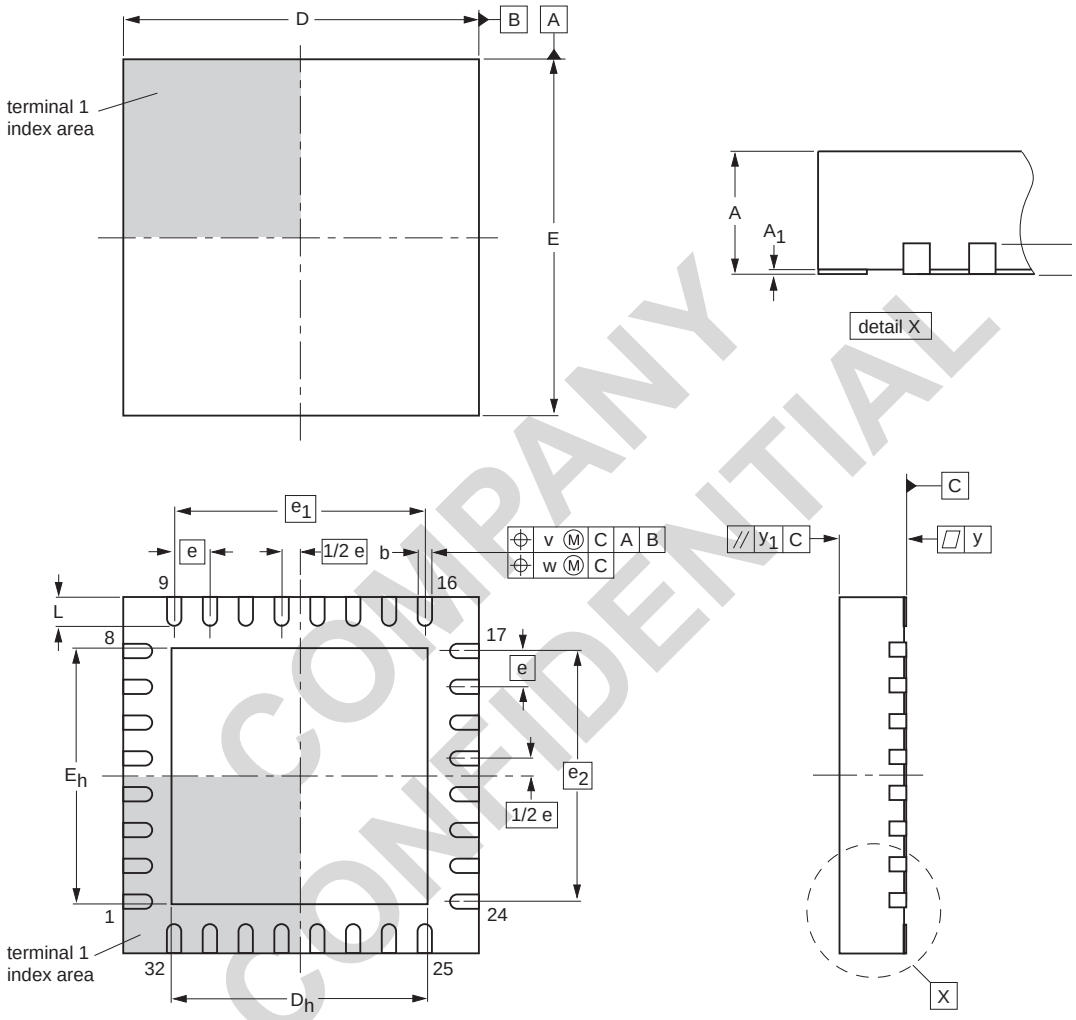
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

17. Package information

No tracks are permitted on the PCB top layer beneath the pin 1 marker. Refer to Ref. 9 for more detailed information with respect to package and PCB layout guidelines.

18. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit(1)		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.85	0.05	0.30	0.2	5.1	3.75	5.1	3.75	0.5	3.5	3.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

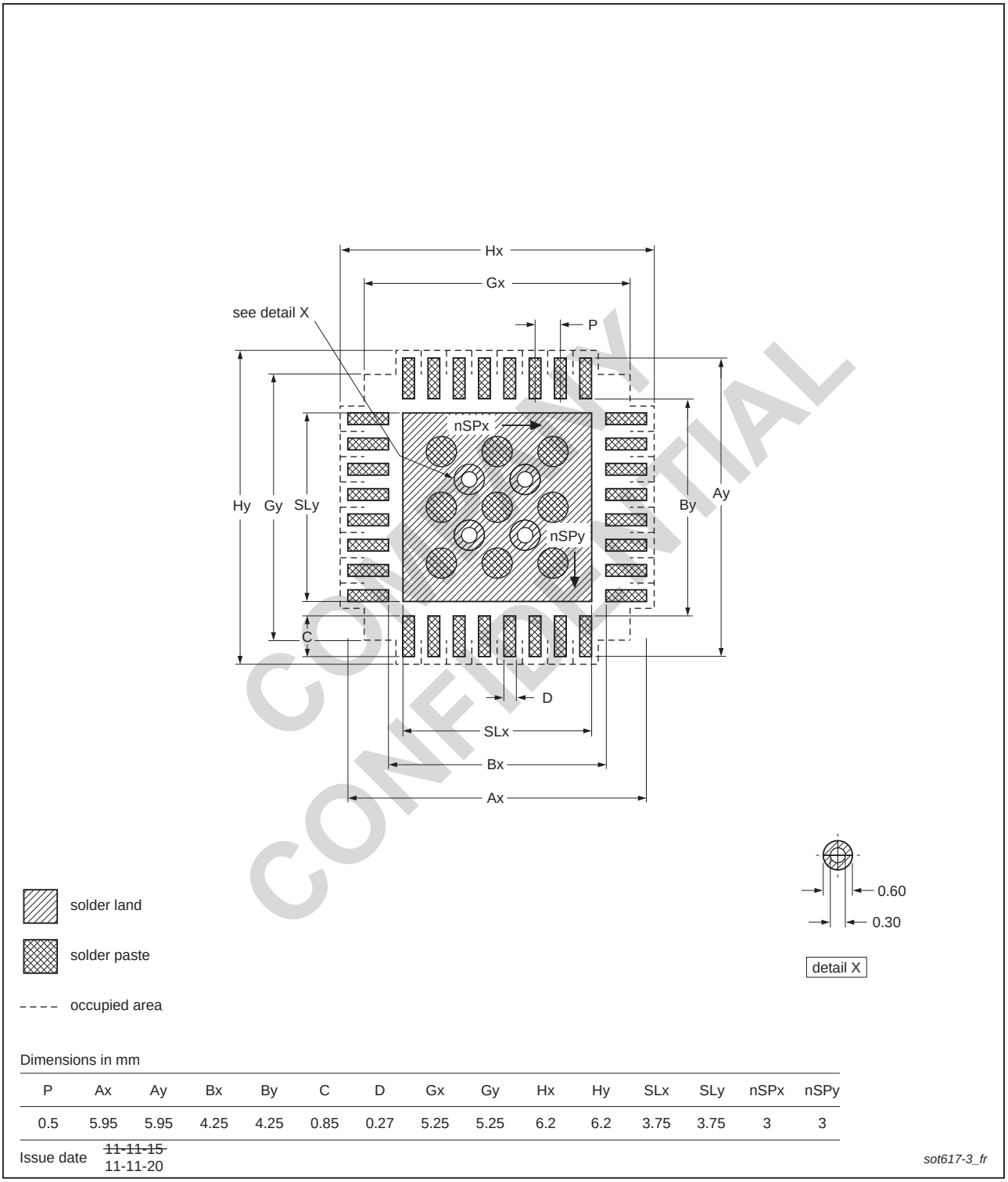
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 5. Package outline SOT617-3 (HVQFN32)

Footprint information for reflow soldering of HVQFN32 package **SOT617-3**



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

sot617-3_fr

Fig 6. Soldering footprint SOT617-3 (HVQFN32)

19. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 7) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020D)

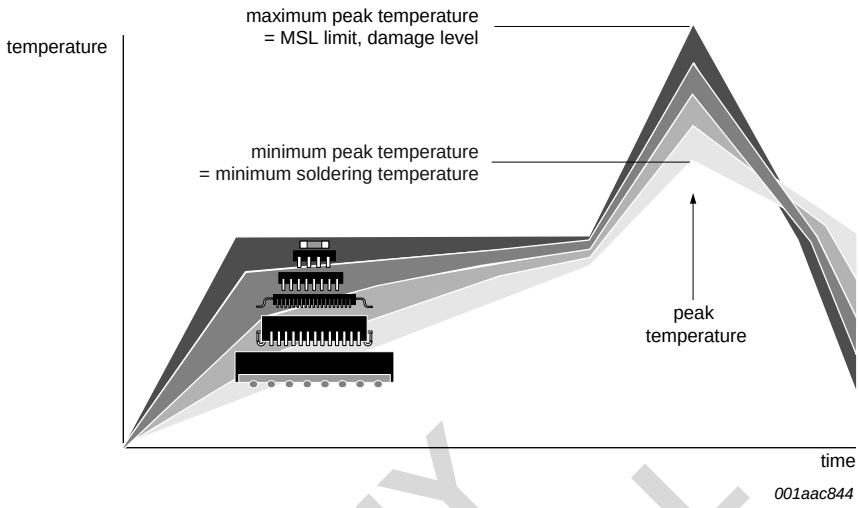
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 7.



MSL: Moisture Sensitivity Level

Fig 7. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

20. Abbreviations

Table 18. Abbreviations

Acronym	Description
AC	Alternating Current
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AGC	Automatic Gain Control
AM	Amplitude Modulation
BCK	Bit ClocK
DAC	Digital-to-Analog Converter
DARC	DAta Radio Channel
DRM	Digital Radio Mondiale
ESD	ElectroStatic Discharge
FM	Frequency Modulation
FMSI	FM Stereo Improvement
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^2C-bus	Inter-IC bus
I^2S	Inter-IC Sound
IC	Integrated Circuit
IF	Intermediate Frequency
I/O	Input/Output

Table 18. Abbreviations *...continued*

Acronym	Description
I/Q	In-phase/Quadrature phase
JEDEC	Joint Electron Device Engineering Council
LNA	Low-Noise Amplifier
LO	Local Oscillator
LW	Long Wave
MPX	FM-Multiplex Signal
MW	Medium Wave
OIRT	International Radio and Television Organisation (Organisation Internationale de Radiodiffusion et de Télévision)
PACS	Precision Adjacent Channel Suppression
PCB	Printed-Circuit Board
PI	Program Identification
PLL	Phase-Locked Loop
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RMS	Root-Mean-Square
RSSI	Received Signal Strength Indicator
SNR	Signal-to-Noise Ratio
SW	Short Wave
US	United States of America
USN	UltraSonic Noise
WAM	Wideband AM
WS	Word Select

21. Glossary

HD Radio™ — Technology upgrades broadcast radio from analog to digital

22. References

[1] **UM10204; I²C-bus specification and user manual - v.5 —** Official I²C Standard Document (available from NXP Semiconductors, International Marketing and Sales)

[2] **IEC 60134 —** Absolute Maximum Rating System

[3] **AEC - Q100-004 —** Automotive Electronics Council - IC Latch Up Test

[4] **AEC - Q100-002 —** Automotive Electronics Council - Human Body Model (HBM) Electrostatic Discharge (ESD) Test

[5] **AEC - Q100-011 —** Automotive Electronics Council - Charged Device Model (CDM) Electrostatic Discharge (ESD) Test

[6] **JESD22-A114 —** JEDEC Standard - Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-C101 —** JEDEC Standard - Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8] **Application note AN10365 —** Surface mount reflow soldering description

[9] **Application note AN11254 —** TEF668X Application Note

[10] **TEF668X User Manual —** Technical information

23. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEF668X v.4	20140115	Product data sheet	-	TEF668X v.3
Modifications:	• Type numbers TEF6687 and TEF6689 (FMSI) added • New Section added Section 17 “Package information” on page 22			
TEF668X v.3	20130730	Product data sheet	-	TEF668X v.2
Modifications:	• Preliminary data sheet changed to Product data sheet			
TEF668X v.2	20130709	Preliminary data sheet	-	TEF668X v.1
Modifications:	• Pins 12, 13, 14 and 15 changed • New text added to Section 17 “Package outline”			
TEF668X v.1	20130422	Preliminary data sheet	-	-

24. Legal information

24.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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25. Contact information

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