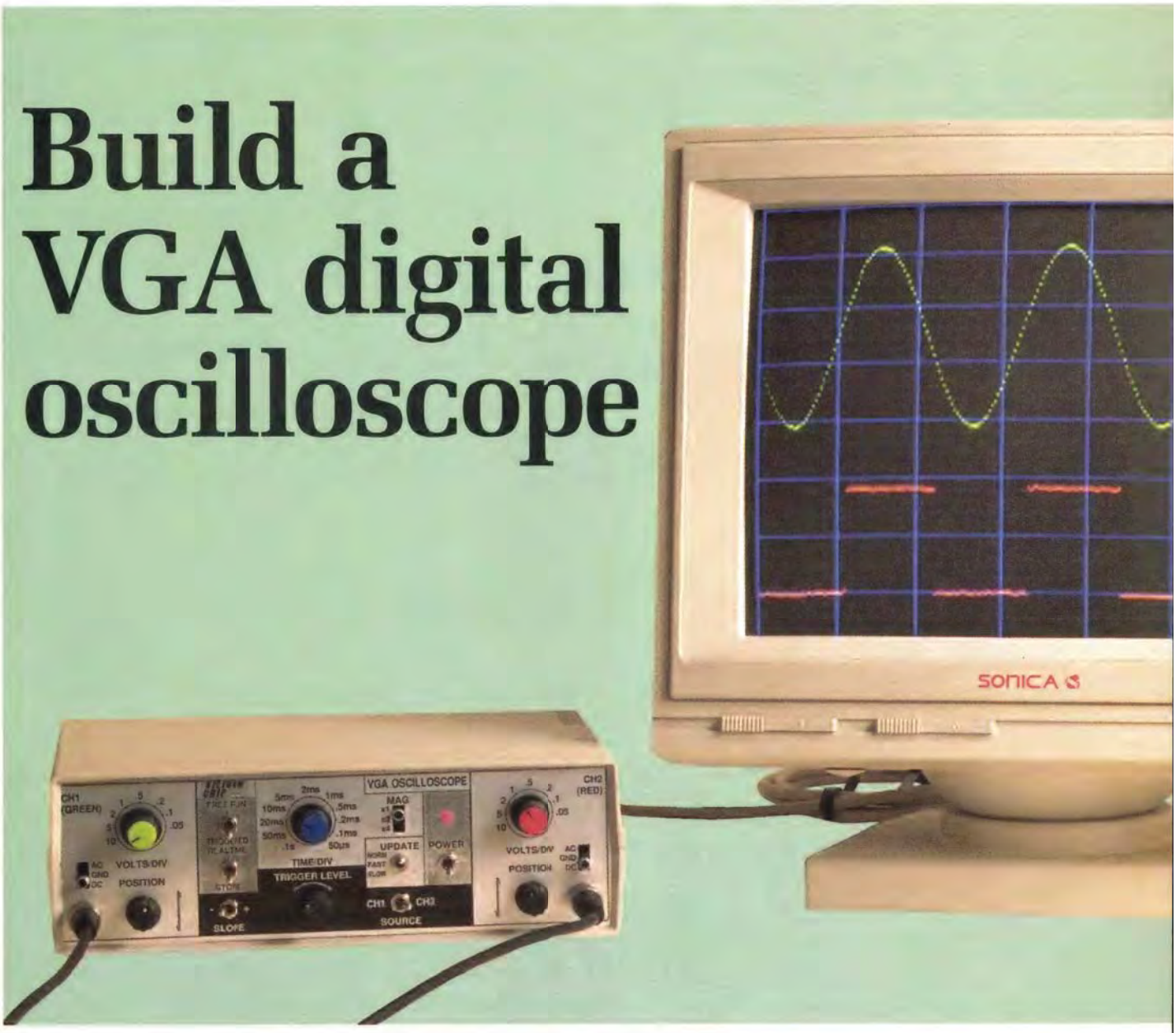
Build a VGA digital oscilloscope



How would you like a digital scope with a large screen? This one is based on a VGA monitor and displays two channels, one with a red trace and one with a green trace. At the same time, there is an electronically generated blue screen graticule to make measurements easy.

PART 1: By JOHN CLARKE

Many readers would like to have an oscilloscope but can't quite raise the $1000 or so you need for a fairly basic scope these days. However, many readers do have a spare VGA monitor and this can be pressed into useful service with our new VGA Oscilloscope. Apart from the need for a VGA monitor, it's a self-contained unit that doesn't tie up your computer.

No modifications are required to the VGA monitor itself – it just plugs into the VGA output on the test instrument which we'll call the Scope Adaptor for convenience. When you turn both the VGA monitor and the Scope Adaptor on, the screen displays a large blue graticule with seven divisions horizontally and eight vertically. Two traces are also displayed, one red and one green, for the two channel inputs.

The Scope Adaptor has knobs for vertical sensitivity & trace position on both channels, plus timebase and trigger level controls. There are also toggle switches for trigger source selection, AC/DC coupling, timebase magnification and a few others which we will discuss later.

Most importantly, the Scope Adaptor has two BNC sockets for the two channel inputs. These will accept nor-

Specifications

Bandwidth	useful up to 100kHz
Timebase	0.1s to 50µs per division in 11 ranges
Sensitivity	10V to 50mV per division in 8 ranges
Resolution	8-bit or 256 steps with 224 visible
Linearity	±1 LSB
Calibration Accuracy	vertical <5%; horizontal <10% (50µs position uncalibrated)
Input impedance	1MΩ

This photo shows the unit displaying a sinewave in one channel and a square wave in the other. Timebase speeds range from 100ms to 50µs/division.

mal 1:1 and 10:1 scope probes.

Using the VGA Oscilloscope is just like using any other scope. First, you connect the scope probes to the circuit to be measured and then adjust the vertical sensitivity controls on both channels to fill the screen. This done, you adjust the timebase control to give a reasonable number of signal cycles on the screen. Finally, you adjust the vertical position controls so that the two traces are comfortably separated (or overlapping if you wish).

To obtain a stable display, you will probably need to adjust the trigger level control and also select positive or negative edge triggering with the Slope switch. Or you can select between a triggered or free-running display. As we said above, driving the VGA Oscilloscope is little different from any other scope – up to a point.

Where the new VGA Oscilloscope does differ is that it also offers waveform storage, just like a digital storage oscilloscope – and that is exactly what it is. It works in much the same way as typical modern digital instruments such as the Hewlett-Packard HP 54600 series scopes or the Tektronix TDS 300 series. It converts the incoming analog signals into digital data and then stores them in RAM. The digital data is then processed in such a way as to generate a raster display on the VGA monitor.

Mind you, this VGA Oscilloscope does not have the extremely wide bandwidth of the commercial oscilloscopes mentioned above; nor does it have their price. However, it can be used to monitor signals up to 100kHz, making it a useful instrument for lots of applications. And unlike the commercial scopes, it does have that large VGA screen. To top it off, the display is in full colour! Few commercial scopes can boast a colour screen.

Some normal oscilloscope controls are not provided on the Scope Adaptor. No brightness controls are provided since these are on the VGA monitor. Focus is unnecessary since the trace thickness is set by the circuitry.

A MAGnification control expands the trace out by either a factor of two or four. This feature can be useful for high frequency signals above 20kHz where it is difficult to see each waveform cycle in the x1 magnification.

The screen is redrawn at a rate set by the UPDATE switch. The normal setting redraws the trace every second and this is seen on the screen as a momentary trace blanking. The other two positions of the switch are slow and fast. These are provided for low frequency signals and for displaying real time audio signals (music, speech, etc) respectively.

Waveform storage

A very useful feature of the VGA Oscilloscope is its ability to store a waveform and then display it indefinitely. This enables viewing of waveforms which cannot be readily seen on a normal oscilloscope. With the storage facility, you can capture momentary pulses in a circuit and view them at your leisure.

As noted above, the VGA Oscillo-

Features

- VGA display (no computer required)
- Dual trace
- 7 x 8 graticule
- Calibrated timebase and volts/division
- Timebase magnification (x2, x4)
- Free run and triggered display
- Storage facility
- Triggering on + or - slope and Channel 1 or Channel 2
- Trigger level control
- Vertical position for each trace
- AC/DC/GND input coupling

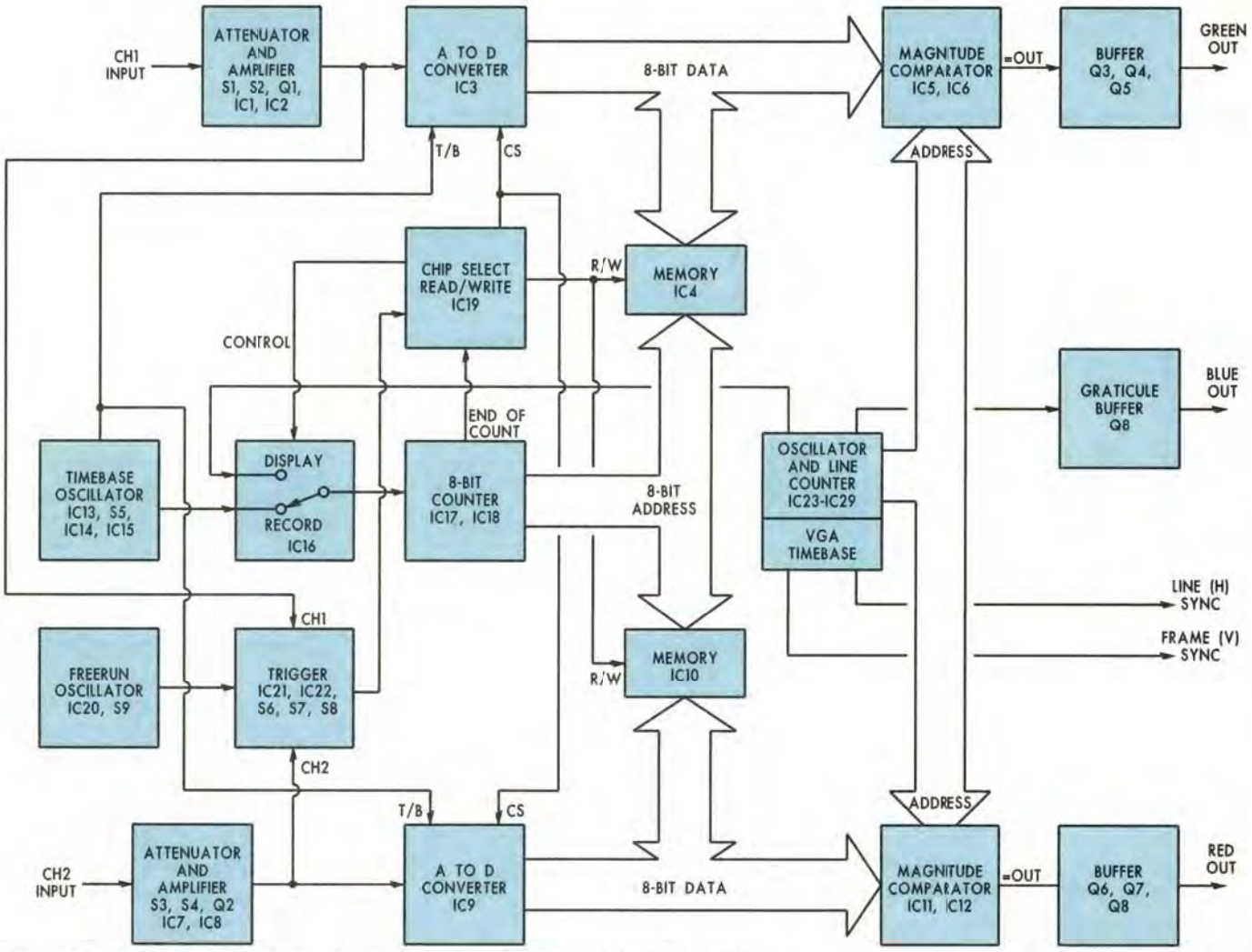


Fig.1: this block diagram shows the various signal processes inside the VGA Oscilloscope.

scope does not tie up your computer since it directly drives the VGA monitor. It operates best on a multisync monitor. With a standard VGA monitor, the extreme right hand graticule line may not displayed. This is, however, of little consequence.

Block diagram

Fig.1 shows the block diagram for the VGA Oscilloscope. In essence, signals for Channel 1 run along the top of the diagram while signals for Channel 2 run along the bottom of the diagram. Let's talk about Channel 1, on the assumption that all operations will be duplicated in Channel 2.

Channel 1 input signals are first passed into a switchable attenuator and amplifier (S1, S2, Q1, IC1 & IC2) which sets the amplitude to suit the following circuitry. The signals are then passed to an analog-to-digital (A-D) converter (IC3) which produces 8-bit data which is then stored in memory.

Initially, the A-D conversion operation is triggered either by the free run oscillator which periodically retriggers the oscilloscope or by a trigger signal from CH1 or CH2.

After each A-D conversion the new digital value is stored in the next memory address. The A-D conversion rate and memory address is under the control of the timebase oscillator (S5, 1C13, IC14, IC15) which clocks the 8-bit counter via the record switch in IC16. This counter increments the memory address.

256 memory locations are used to store all the data for one screen display. When all memory locations have been filled, the end of count signal (IC17, IC18) changes the chip select, read/write block to switch the memory to read mode. It also deselects the A-D converter and switches IC16.

During this conversion time the display trace is blanked. Note that the timebase oscillator frequency sets the rate of A-D conversions. At fast rates, high frequencies can be observed, while at slow conversion rates low frequency signals are accurately traced.

If we want to store and view one complete cycle of the input waveform, the timebase must operate 256 times faster than the input frequency. If the timebase is slower than this then more cycles will be seen. Conversely, if the timebase is faster, then only a portion of the full waveform will be observed.

When the memory is in the read mode, the 8-bit counter is clocked from the oscillator and line counter of the VGA timebase circuit. The display/record switch, IC16, performs this function. This clocking rate is exactly what is required for the memory contents to be displayed on the screen.

Screen display

In order to understand how the in-

formation stored in memory is displayed on the VGA screen, let us look at Fig.2. The display on a VGA monitor is made up of 480 horizontal lines which are scanned by the red, green and blue electron beams. A dot will appear each time one of the beams is is turned on for an instant. The respective beams are turned on by the R, G or B signals on the VGA connector.

For simplicity, Fig.2 only shows 11 horizontal scan lines instead of 480 but you get the general picture.

The position of any dot on the screen is dependent upon how long after the line sync pulse the red, green or blue gun is turned on and on what line is being scanned at the time.

Each horizontal line begins with a sync pulse and an entire set of lines is preceded by a frame sync pulse. This must be of sufficient duration for the electron beam to return from the bottom of the screen to the beginning of line 1. The time to scan one line is 32µs and to scan all 480 lines is 16.6ms. Thus, the horizontal scanning frequency is 31.25kHz and the frame rate is 60Hz.

This last frequency is called the refresh rate.

Making a picture

So how do we get the dots on the screen in order to make a picture which means something?

We have already stated that we have 256 memory locations which are scanned for each line of the screen. Each of these memory locations is 8-bits and therefore we can have a value stored in each location which ranges from 00000000 to 11111111; ie, 256 values.

Let us consider that the top of the screen corresponds to 11111111 and the bottom of the screen is 00000000. So as each line is scanned by the beam of the VGA monitor, simultaneously the 256 memory locations are being scanned. Now imagine that the top line is being scanned and we come to memory location 6 (actually address 00000101 when scanned from left to right) and the value stored just happens to be 11111111. Yippee, we get a dot on the screen which corresponds to that memory location (or address).

Next, consider line 2 and we scan across to memory location 5 and the value stored just happens to be 11111110. Again, we get a dot at that position. Further, as we scan further across the same line we come to location 7 and the value is also 11111110. Again, we got a dot on the screen.

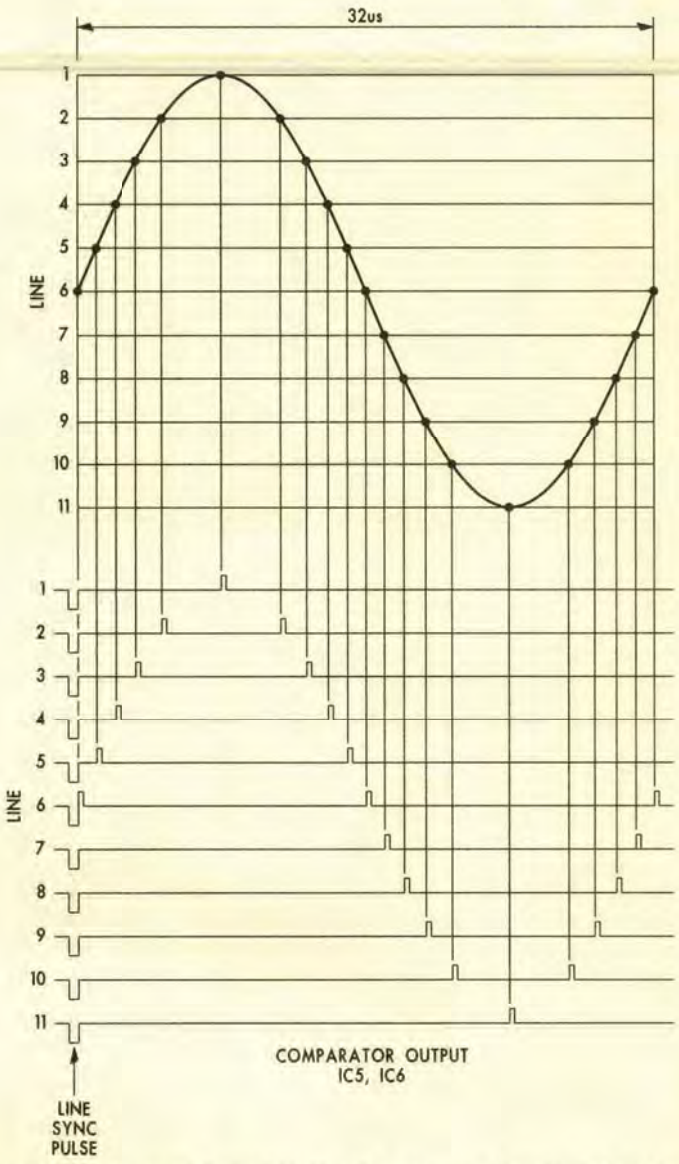


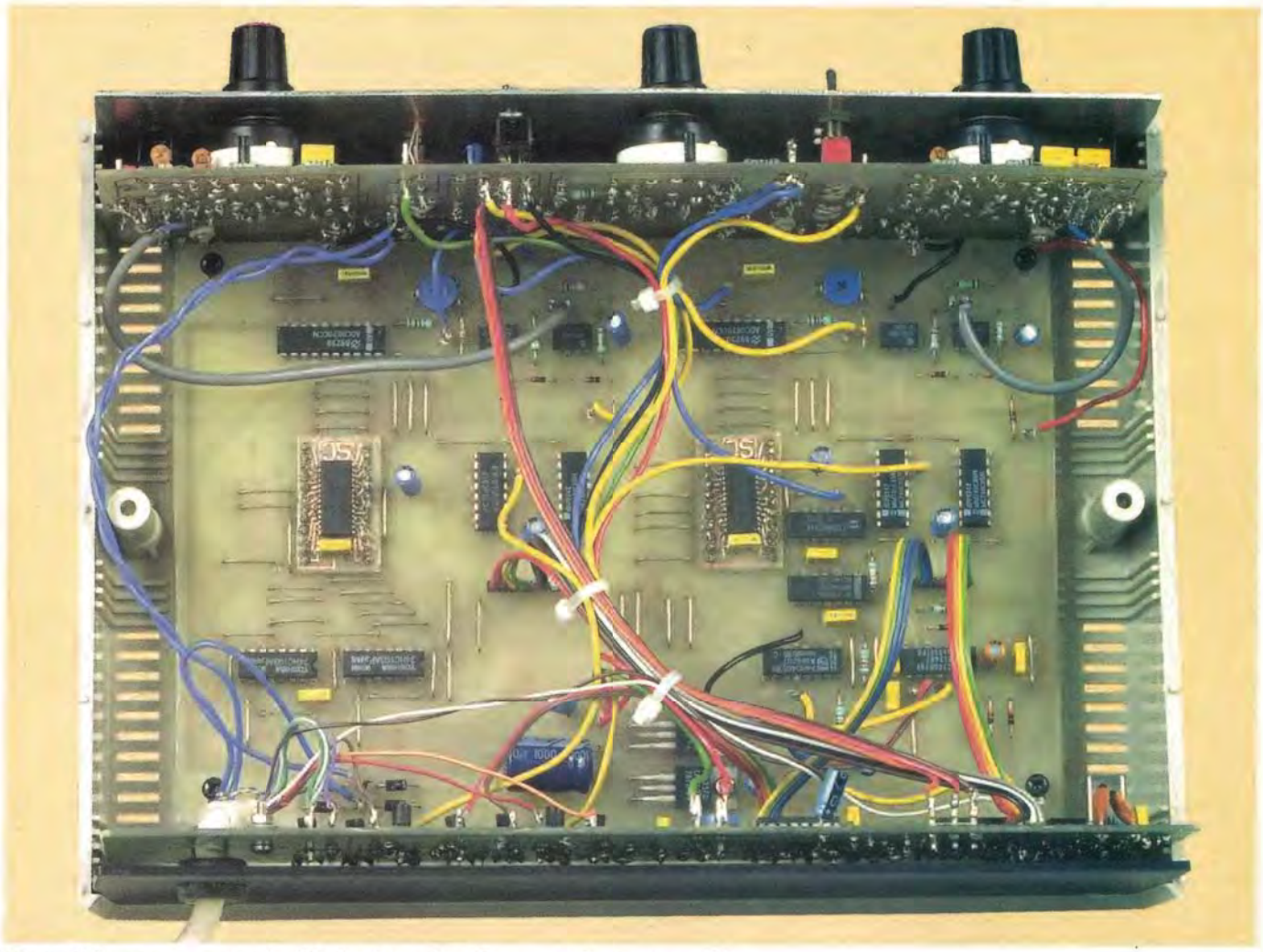
Fig.2: this diagram demonstrates the process of writing dots to the screen. There are 256 bytes of memory for each channel and each of the 256 lines on the screen corresponds to one of the possible values stored in each memory location.

Now we could go on and on with this process and talk about all 256 lines and 256 memory locations but you should be starting to get the picture. This is shown in abbreviated form in Fig.2. This shows only 11 lines and 21 memory locations but the principle is the same: if the value stored in a memory location corresponds with the line value we get a dot on the screen.

That's the principle but how is it done? Two magnitude comparators, IC5 & IC6, actually compare the data from each memory location with the line being scanned and its screen value; ie, the screen's 8-bit address which comes from the line counter.

If the line value equals the data value then a short pulse is produced from the output of the comparator and this is applied to the buffer (Q3, Q4 & Q5) which drives the green gun, for the Channel 1 trace.

Exactly the same process occurs for Channel 2 input signals except that they are stored in another 256 byte (8-



Most of the componentry inside the VGA Oscilloscope adaptor is readily available. The circuitry is mounted on three PC boards, with two small satellite boards used to accommodate the RAM chips.

The VGA Oscilloscope adaptor has most of the controls you would expect to find on a conventional oscilloscope. Vertical input sensitivity ranges from 50mV/div to 10V/div.

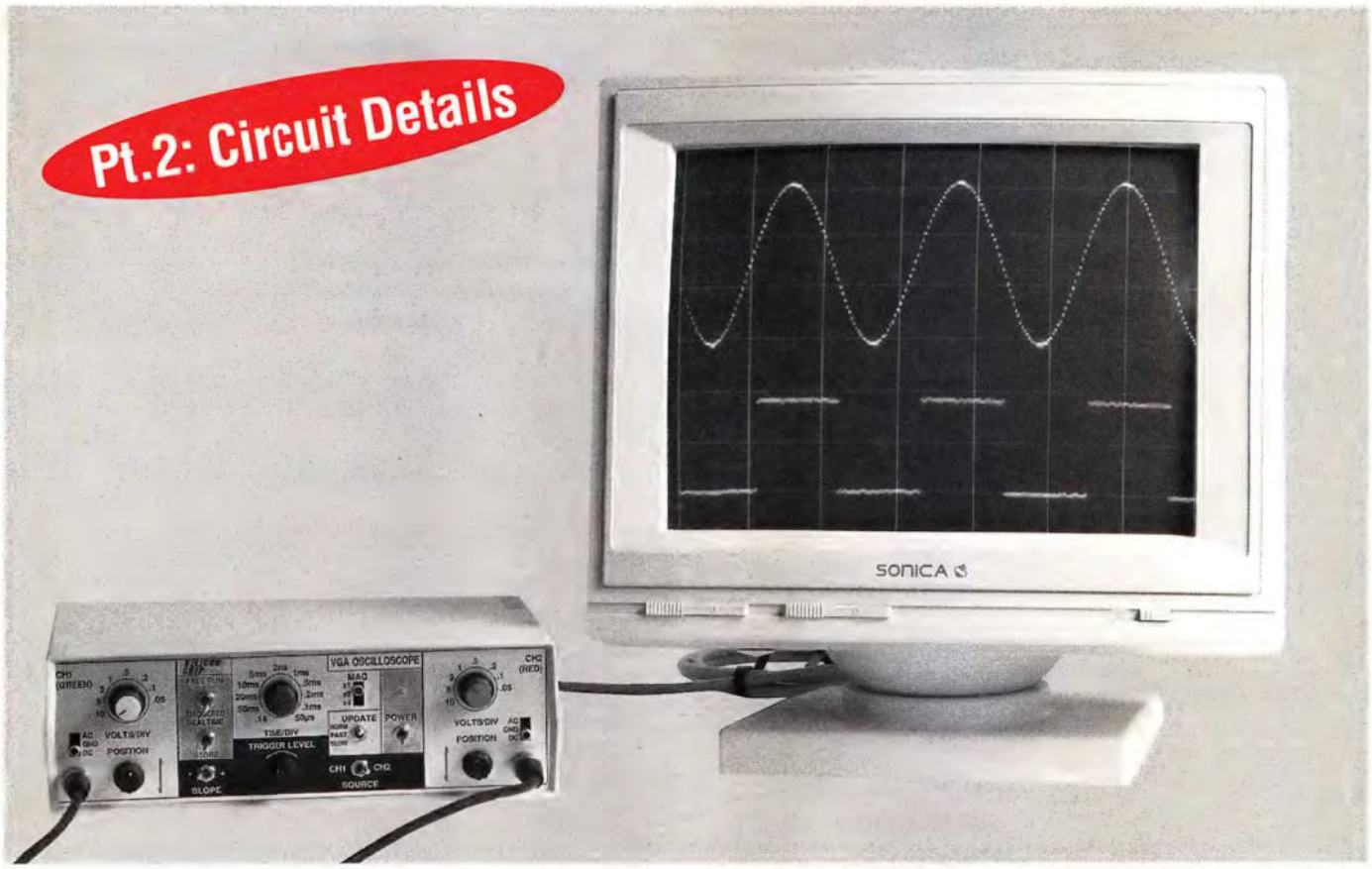
bit) memory. As the Channel 2 memory is clocked out, its values are compared by magnitude comparators IC11 and IC12 and dot signals are generated for the red gun, corresponding to the Channel 2 trace.

To recap, the analog input signals are converted to digital data and clocked into memory at a rate which is set by the timebase switch. The data is then read out of memory at a fixed rate, to suit the requirements of the VGA monitor.

The remainder of Fig.1 is devoted to the generation of VGA timebase signals (ie, line and frame sync pulses) and the graticule signal which drives the blue gun.

Next month

So far, we've given you the overall picture of how the VGA Oscilloscope works. The circuit details are just a teensy bit more complicated, as you might expect. We will discuss these next month and also publish the parts list. **SC**



Build a VGA digital oscilloscope

One of the real attractions of this digital scope, based on a VGA monitor, is that you don't have to peer at the display – it is large, bright and the different coloured traces and graticule make it easy to interpret what's happening. In this article we discuss the circuit details.

By JOHN CLARKE

To fully understand the discussion, it will be a help if you can refer to the block diagram presented on page 28 of last month's issue.

The circuit for the VGA Oscilloscope has been split into two sections. The main section is Fig.1, on pages 66 and 67, comprises most of the circuit while the timebase circuit, Fig.3, is shown on page 69.

28 ICs are used in the entire circuit. However, as we shall see, some of the circuit is repetitive (for the CH1 and CH2 inputs) and much of it involves timers and counters.

Looking at the top righthand corner of the two-page circuit, S1 is the AC/DC coupling switch for the Channel 1 input. S1 also has a GND setting to allow the trace to be positioned on the graticule as a ground (zero) reference point. Following S1, the input signal passes via the attenuator switch S2. This is essentially a string of resistors, with each one bypassed by a capacitor to improve high frequency response. Trimmer capacitor VC1 allows adjustment of the frequency compensation.

After the attenuator, the signal is applied to the gate of JFET Q1 which acts as a high impedance buffer. Its gate is protected from excessive signal excursion by two back-to-back LEDs. These begin to conduct for signals in excess of ±1.8V peak and

PARTS LIST

1 plastic case, 262 x 189 x 84mm, with metal panel
1 front panel label, 252 x 76mm
1 PC board, code 04307961, 252 x 75mm
1 PC board, code 04307962, 213 x 142mm
1 PC board, code 04307963, 252 x 75mm
2 PC boards, code 04307964, 20 x 32mm
3 2P3W slider switches (S1,S3,S11)
3 1-pole 12-way rotary switches (S2,S4,S5)
5 SPDT toggle switches (S6,S7,S8,S9,S12)
1 SPDT centre-off switch (S10)
2 10kΩ horizontal mount trimpots (VR1,VR3)
1 5kΩ horizontal trimpot (VR6)
2 500Ω linear pots (VR2,VR3)
1 5kΩ linear pot (VR5)
2 2-47pF miniature trim capacitors (VC1,VC2)
1 9-68pF miniature trim capacitor (VC3)
1 4MHz parallel resonant crystal (X1)
1 15-pin VGA line socket and lead
1 cable clamp
1 5mm rubber grommet
1 DC panel socket
2 BNC panel sockets
5 3mm LEDs (LEDs 1-5)
3 15mm OD black knobs
3 18mm OD knobs (1 green, 1 blue, 1 red)
92 PC stakes
2 8-way pin headers
1 1.8m length of 0.8mm tinned copper wire
1 150mm length of shielded cable
1 800mm length of 4-way rainbow cable
1 400mm length of red hookup wire
1 400mm length of green hookup wire
1 400mm length of blue hookup wire
1 400mm length of yellow hookup wire
1 400mm length of black hookup wire
3 3mm diameter x 6mm machine screws and nuts

Semiconductors
4 CA3140 op amps (IC1,IC2, IC7,IC8)
2 ADC0820CCN 8-bit A-D converters (IC3,IC9)
2 MCM6206DJ20 20ns 8-bit RAMs (IC4,IC10)
4 74HC85 4-bit magnitude comparators (IC5,IC6,IC11, IC12)
4 7555,TLC555CN CMOS timers (IC13,IC20,IC22,IC28)
4 74HC74 dual D-flipflops (IC14,IC19,IC26,IC27)
1 74HC86 quad EXOR gate (IC15)
1 74HC4053 analog CMOS switch (IC16)
2 74HC193 4-bit presettable counters (IC17,IC18)
1 LM319 dual comparator (IC21)
2 74HC00 quad NAND gates (IC23,IC29)
2 74HC4040 binary counters (IC24,IC25)
1 7812 12V regulator (REG1)
1 7805 5V regulator (REG2)
2 2N5484 JFETs (Q1,Q2)
3 BC338 NPN transistors (Q3,Q6,Q9)
2 BC548 NPN transistors (Q4,Q7)
2 BF199 NPN RF transistors (Q5,Q8)
21 1N914 signal diodes (D1-D16,D21-D25)
4 1N4004 diodes (D17-D20)
5 3mm red LEDs (LED1-5)

Capacitors
1 1000µF 16VW PC electrolytic
1 33µF 16VW PC electrolytic
15 10µF 16VW PC electrolytic
1 6.8µF 16VW PC electrolytic
1 1µF 16VW PC electrolytic
2 0.22µF MKT polyester
14 0.1µF MKT polyester
1 .047µF MKT polyester
4 .0039µF MKT polyester
2 .0015µF MKT polyester
5 .001µF MKT polyester
2 680pF MKT polyester or ceramic
1 560pF MKT polyester or ceramic
1 470pF MKT polyester or polystyrene
2 390pF ceramic
2 150pF ceramic
2 82pF ceramic
3 47pF ceramic
2 22pF ceramic
3 3-60pF trimmer capacitors (VC1-VC3)

Resistors (0.25W, 1%)

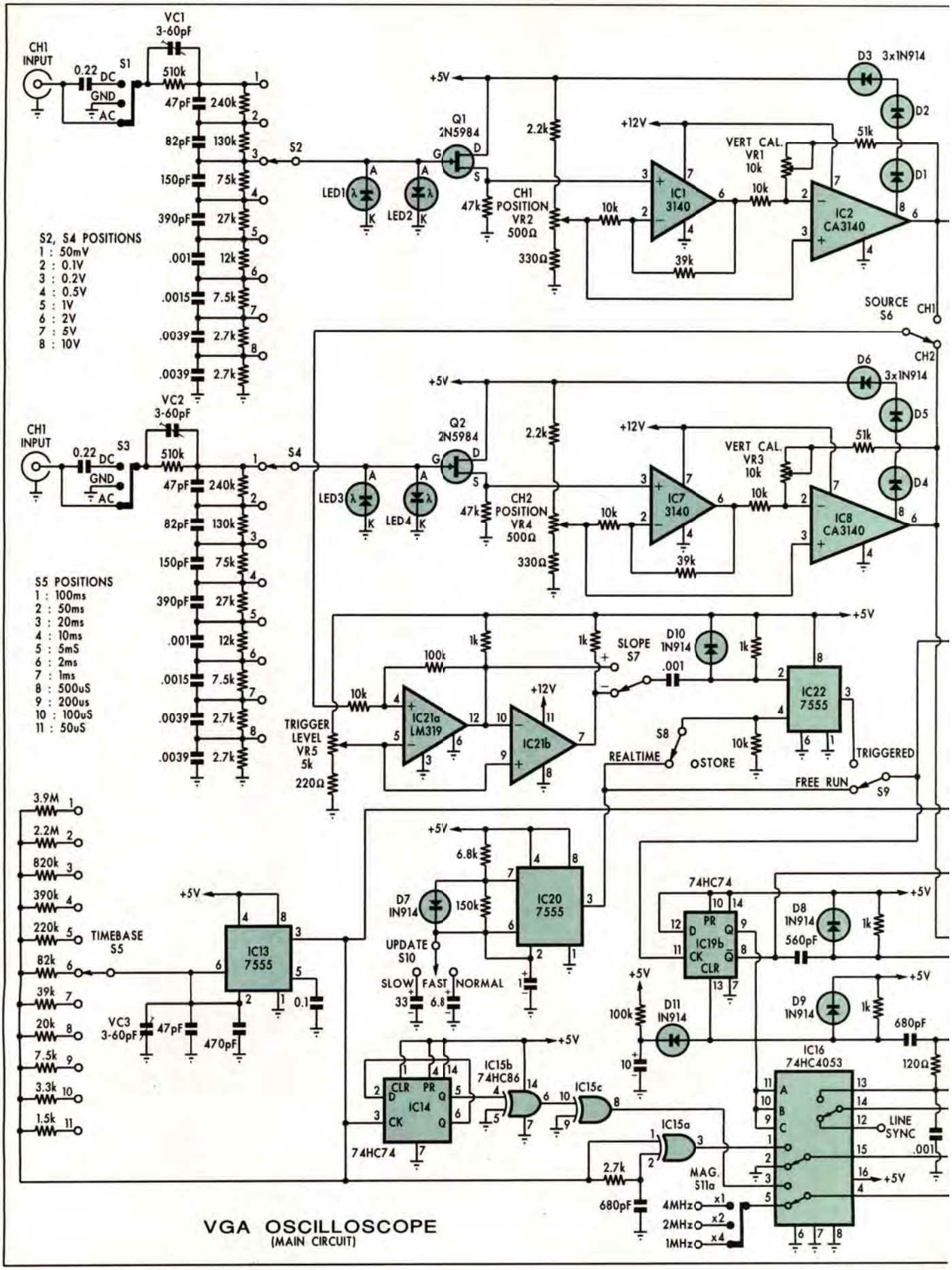
1 10MΩ	1 20kΩ
1 3.9MΩ	2 12kΩ
1 2.2MΩ	6 10kΩ
1 820kΩ	3 7.5kΩ
2 510kΩ	1 6.8kΩ
1 390kΩ	1 3.9kΩ
2 240kΩ	1 3.3kΩ
1 220kΩ	5 2.7kΩ
1 150kΩ	11 2.2kΩ
2 130kΩ	2 1.8kΩ
3 100kΩ	1 1.5kΩ
1 82kΩ	7 1kΩ
2 75kΩ	2 330Ω
2 51kΩ	1 220Ω
2 47kΩ	1 120Ω
3 39kΩ	3 75Ω
2 27kΩ	

Miscellaneous
Solder, four self-tapping screws, cable ties.

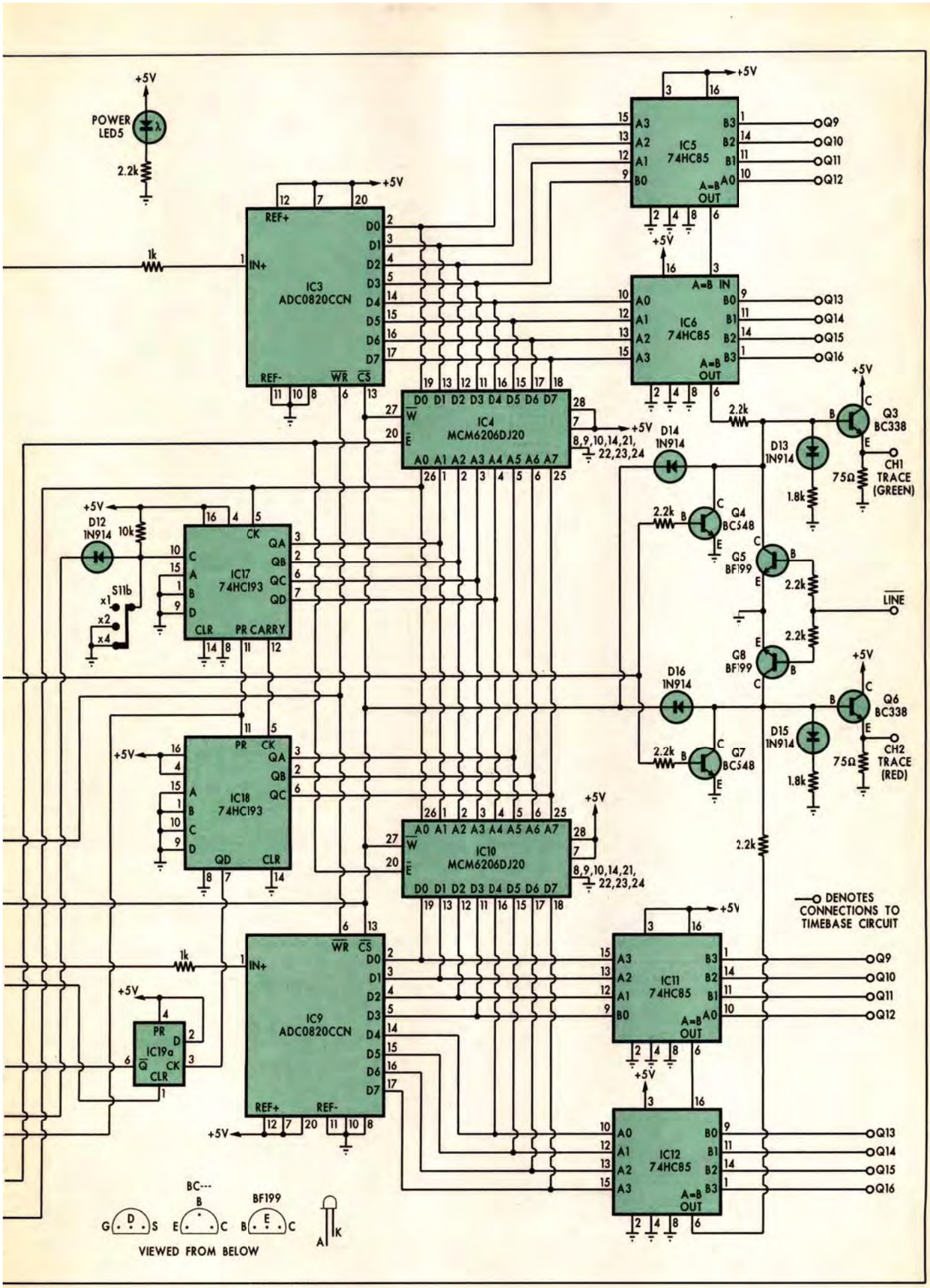
are there mainly to cater for the situation where the input attenuator is set too low for the size of the signal. Normally, if the attenuator is correctly set, the signal at the gate of Q1 will not exceed about ±200mV peak.

IC1 and IC2 invert and amplify the signal by about 25 times to produce sufficient level for the following A-D converter which requires 5V for full conversion. VR2 controls the DC output offset of IC1 and IC2 and thereby has the effect of shifting

Fig.1 (following page): the main circuit section for the VGA Oscilloscope. This comprises the input circuitry, A-D converters (IC3 & IC9), memory storage devices (IC4 & IC10) and the oscilloscope timebase circuitry (IC13-15, IC17 & IC18).



VGA OSCILLOSCOPE
(MAIN CIRCUIT)


+5V
POWER LED5
2.2k
IC3 ADC0820CCN
REF+
IN+
REF-
WR
CS
D0 D1 D2 D3 D4 D5 D6 D7
1k
IC5 74HC85
IC6 74HC85
A=B OUT
A3 A2 A1 A0
B3 B2 B1 B0
Q9 Q10 Q11 Q12
Q13 Q14 Q15 Q16
IC4 MCM6206DJ20
A0 A1 A2 A3 A4 A5 A6 A7
8,9,10,14,21, 22,23,24
D12 1N914
10k
IC17 74HC193
CK
QA QB QC QD
CLR
PR CARRY
S11b
x1
x2
x4
D14 1N914
D13 1N914
D16 1N914
D15 1N914
Q3 BC338
Q4 BC548
Q5 BF199
Q6 BC338
Q7 BC548
Q8 BF199
2.2k
1.8k
75Ω
CH1 TRACE (GREEN)
CH2 TRACE (RED)
LINE
IC18 74HC193
IC10 MCM6206DJ20
IC9 ADC0820CCN
IC11 74HC85
IC12 74HC85
IC19a
PR
CLR
DENOTES CONNECTIONS TO TIMEBASE CIRCUIT
BC---
BF199
VIEWED FROM BELOW

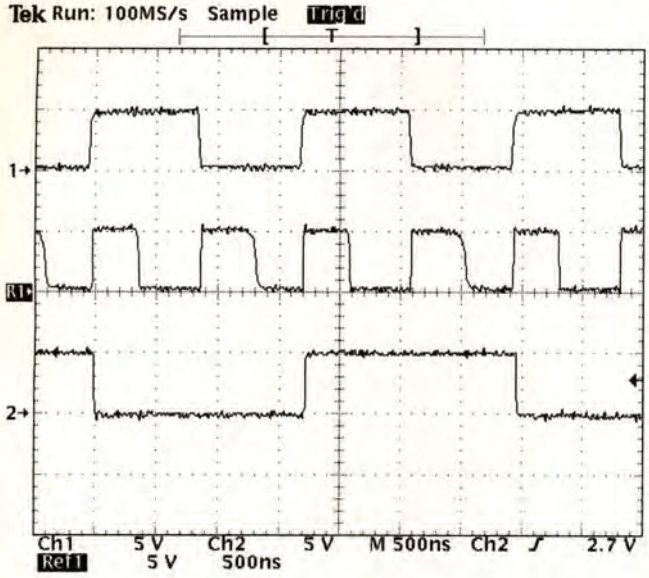


Fig.2: these oscilloscope waveforms show the timing for the record sequence. The top trace is the read/write input of the A-D converters, while the middle trace is the enable input for the memory. The lower trace is the clock input to counter IC17.

the signal trace up or down the VGA screen. VR1, in the feedback loop for IC2, changes the gain for the vertical calibration function.

Note that any change in the setting of VR2 will affect the overall gain of IC1 and IC2 since this is part of the gain setting resistance. However, the range over which the potentiometer is adjusted to set the waveform fully up or fully down on the screen is only a small percentage change compared to the overall resistance value. As a result, the gain change in not perceivable on the screen.

IC1 and IC2 are powered from 12V in order to ensure an output swing capability of more than 5V, while diodes D1-D3 clamp IC2's output to prevent overload in the following A-D converter.

IC3 is an 8-bit high speed A-D converter with an inbuilt sample and hold feature. It has a 4-bit flash converter which uses 32 comparators to speed up conversion and can convert an analog signal to an 8-bit digital code in a maximum of 1.5µs.

AD conversion is started by a low on the WR-bar input at pin 6 of IC3. This must be low for at least 600ns before going high and must remain high for a minimum of 800ns before the data is valid. The data output lines are connected to the RAM chip IC4. This is a 20ns access time high speed memory containing 32K bytes. We have only used 256 bytes and although this may seem wasteful, its selection was based on the high speed and cost. Paradoxically, larger memory can be less expensive than the less popular smaller RAM chips.

High speed RAM is paramount for this application. Remember that when the memory is called to cycle through each location when displaying the stored waveform on the screen, the allotted time per memory location is only 125ns (4MHz rate or 250ns period and 125ns per half cycle). This means that there are 20ns devoted to accessing the correct data and 105ns devoted to comparing this value with the line counter. Any standard 120ns memory would be lost trying to keep up this pace.

Channel 2 signals

The signal process for channel 2 is identical to that described above, the path being via attenuator switch S4, buffer Q2 and amplifiers IC7 and IC8. A-D conversion is in IC9 and the data is stored in RAM chip IC10.

IC17 and IC18, which are synchronous 4-bit preloadable counters, drive the address lines of IC4 & IC10. The clock input at pin 5 of IC17 (which is also the A0 input for IC4 and IC10) is from IC16 at pin 4. When the oscilloscope is in display mode the clock signal comes from the MAGnification selection at S11a via pin 5 of IC16 and is fed through to pin 4. When in the record mode, the clock is from IC15c at pin 3 of IC16. This indirectly obtains a clock signal from the timebase oscillator, IC13.

Triggering

The outputs of IC2 and IC8 connect to switch S6 and this selects the source of triggering from channel 1 or channel 2. Comparators IC21a and IC21b take the signal from S6 to generate the trigger signal. IC21a generates trigger signals for positive-going signals while IC21b acts as an inverter to generate trigger signals for negative-going inputs. The trigger threshold (level) is set by VR5. Positive or negative triggering is selected by switch S7.

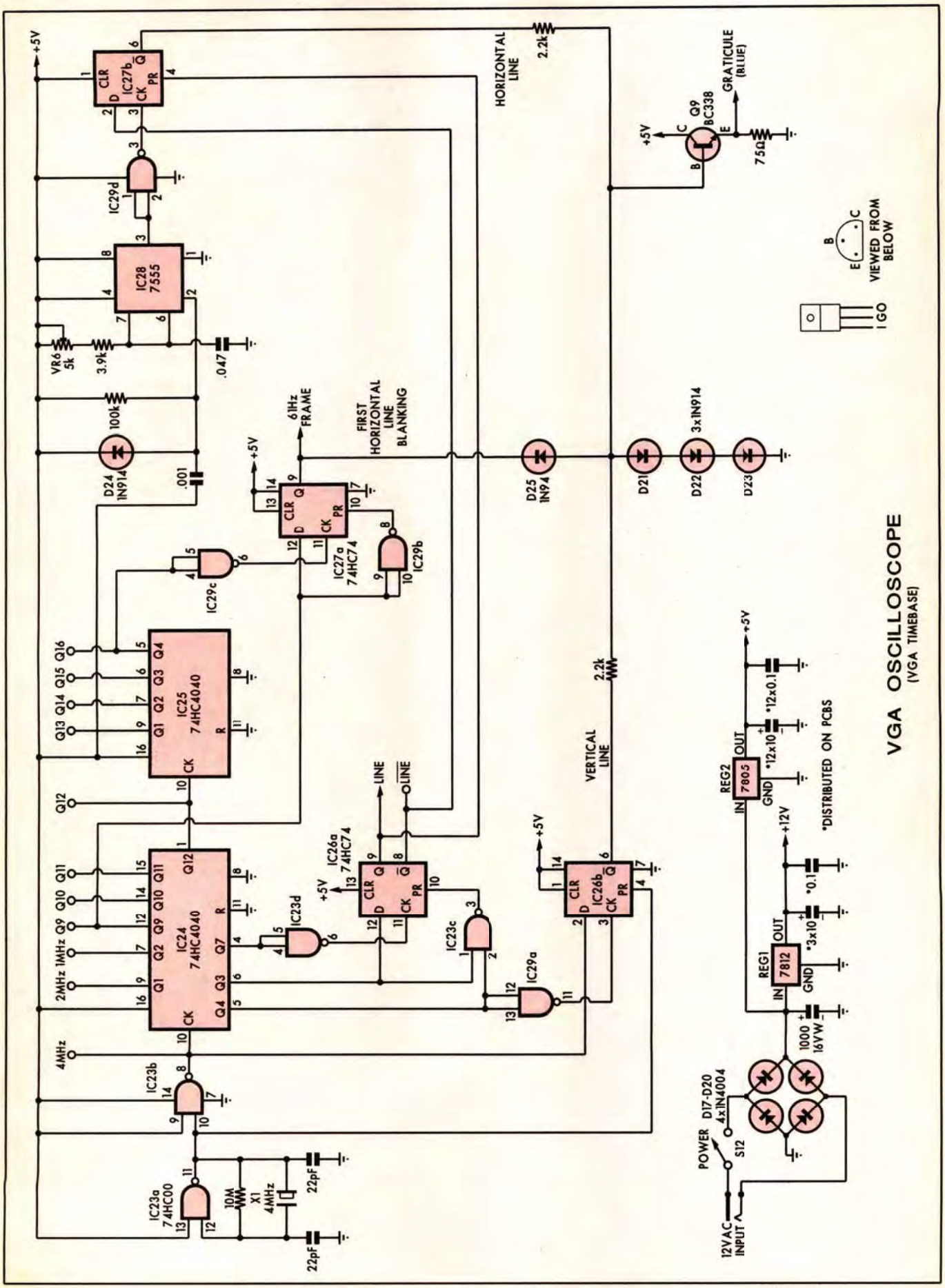
The comparator output selected by S7 triggers IC22 which is a 7555 timer set up as a one shot. When triggered, its output at pin 3 goes high and remains high until reset by the update oscillator IC20. This occurs when S8 is in the realtime position but IC22 remains set if left in the store position.

IC20 is another 7555 timer which operates as a free running oscillator. It charges the selected capacitor at pin 2 and 6 via a 6.8kΩ resistor and diode D7 and discharges it via the 150kΩ resistor. With this setup, its pin 3 output is high for a short time (to reset IC22) and low for a relatively long time to allow triggering from IC21.

Flipflop IC19b is triggered either by IC22 or IC20, depending on the setting of switch S9. In the free run position of S9, the display is updated at a regular interval set by the frequency of IC20. This means that the display will not be locked (ie, it will be moving) since a different part of the waveform will be stored at each trigger point. The triggered selection for S9 provides a static display since the waveform is stored at the same point in the waveform each time and only when the pin 3 output of IC20 is high.

IC19b is reset when power is first applied, due to the 10µF capacitor at the cathode of D11 being discharged. This pulls the CLR input (pin 13) low to reset the Q output low and the Q-bar output high. When

Fig.3 (right): the VGA timebase circuit. NAND gate IC23a and X1 form a master crystal oscillator, while binary counters IC24 & IC25 provide the 8-bit data signals for IC5, IC6, IC11 & IC12 (on Fig.1).


VGA OSCILLOSCOPE
(VGA TIMEBASE)
+5V
IC27b
IC29d
IC28 7555
VR4 5k
3.9k
.047
100k
D24 1N914
.001
61Hz FRAME
FIRST HORIZONTAL LINE BLANKING
IC27a 74HC74
IC29b
IC29c
IC25 74HC4040
IC24 74HC4040
Q16
Q15
Q14
Q13
Q12
Q11
Q10
Q9
Q7
Q4
Q3
Q2
Q1
2MHz
1MHz
4MHz
IC23a 74HC00
IC23b
IC23c
IC23d
IC29a
IC26a 74HC74
IC26b
LINE
VERTICAL LINE
2.2k
HORIZONTAL LINE
Q9 BC338
GRATICULE (BLUE)
75Ω
VIEWED FROM BELOW
I GO
D25 IN94
D21
D22
D23
3x1N914
REG2 7805
REG1 7812
IN
OUT
GND
*12x0.1
*12x10
*0.1
*3x10
1000 16VW
*DISTRIBUTED ON PCBS
D17-D20 4x1N4004
POWER
S12
12VAC INPUT
10M
X1 4MHz
22pF

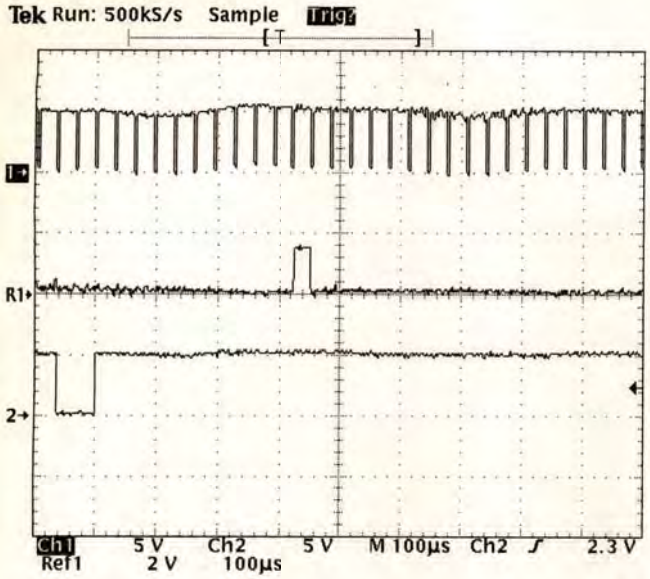


Fig.4: these oscilloscope waveforms show the line sync pulses (top) and the frame sync pulses (bottom). The centre trace is actually a horizontal line for the graticule.

IC19b is triggered, the Q output at pin 9 goes high and operates the three switches inside IC16 via the A, B and C inputs. This switches pin 4 to pin 3, pin 15 to pin 1 and pin 14 to pin 13. At the same time, the low output at pin 8 of IC19b (Q-bar) selects the ADC chips IC3 and IC9 (via their the CS inputs) and places IC4 and IC10 (RAM) in the write mode.

The low Q-bar output from pin 8 of IC19b also clears IC19a, via the 560pF capacitor connected to pin 1. This causes the Q-bar output of IC19a to go high. Before this happens, the previously low Q-bar output of IC19a presets IC17 and IC18, via IC16. Diode D12 holds the C preset input (pin 10) of IC17 low and so both counters are preset to 0000 0000. An RC delay from the Q-bar output of IC19a to pin 13 of IC16 is used to extend the preset time for IC17 and IC18.

The above sequence sets the circuit in the record mode. Timebase oscillator IC13 now controls the read/write inputs of A-D converters IC3 and IC9.

Fig.2 shows a screen printout of oscilloscope waveforms of the timing for the record sequence. The top trace is the read/write input of the A-D converters. When low, the A-D converter samples the data and flash converts the four most significant digits. 800ns after the rising edge of the read/write input, data from the A-D converter is valid.

The middle trace of the oscilloscope waveform is the enable input for the memory. It is derived from the timebase and passes through EXOR gate IC15a (IC15 is near the lower righthand corner of the circuit, Fig.1). IC15a has its pin 1 input directly connected to the timebase, while pin 2 is connected via an RC delay. Whenever the input to IC15a changes, pin 3 goes high for the delay period to disable the memory. This prevents any false data from the A-D converter being applied to the data inputs of the memory.

The lower trace on Fig.2 is the clock input to counter IC17 which is a divide-by-two timebase signal. The timebase clocks IC14, which is connected as a toggle flipflop. Its output is passed through two EXOR gates, IC15b & IC15c, wired as non-inverters to introduce a small amount of delay between the positive edge of the timebase and the change in the clock signal for IC17. This ensures that the memory is disabled via IC15a (middle trace) before the address is changed.

When counters IC17 & IC18 have reached a count of 256, the Q_D output at pin 7 of IC18 goes high and clocks D-flipflop, IC19a. This produces a low at the Q-bar (pin 6) output of IC19a and this presets IC17 & IC18. A low pulse to the CLR input of IC19b via the 680pF capacitor sets the Q output of IC19b low and Q-bar high. The high Q-bar output deselects A-D converters IC3 and IC9 and switches the IC4 and IC10 memories to read mode via the Write-bar inputs at pin 27.

The low Q output switches IC16 so that the clock input of IC17 and address line 0 of IC4 are controlled by the 4MHz to 1MHz inputs at pin 5. These inputs come from the timebase circuit (see Fig.3). Also the memories are permanently enabled via the now low E-bar inputs caused by pin 15 of IC16 connecting to the low pin 2. Counters IC17 and IC18 are now preset by the line sync signal now present at pin 14.

In addition, the low Q-bar output of IC19b clears IC19a via the 560pF capacitor connected to pin 1. Its Q-bar is high and so diode D12 connecting to the C input of IC17 is reverse biased. This input is pulled high via the 10kΩ resistor when S11b is in position 1. Preloading of IC17 now sets it to an initial count of 8. This may appear unusual, however it is used to move the oscilloscope trace along the screen so that the trigger point is exactly in line with the far left graticule vertical line.

Magnitude comparators

IC5 and IC6 (top righthand corner of Fig.1) are digital magnitude comparators with "less than", "greater than" and "equal-to" outputs. For our application we only use the "equal-to" output, pin 6, which turns on the display when the data from IC4 (channel 1 RAM) is identical to the line count from the VGA timebase circuitry. Pin 6 drives the base of transistor Q3 via a 2.2kΩ resistor. This is level-clamped using diode D13 and the 1.8kΩ resistor. The emitter follower configuration of Q3 drives the video input (green) of the VGA monitor via a 75Ω resistor. Thus the channel 1 trace is green.

Transistors Q4 and Q5 are for blanking the display when updating the A-D conversion and during the line sync pulse respectively. This prevents the trace from producing an unusual display or overscanning.

Q6, Q7 and Q8 operate in the same manner as above for the channel 2 trace; ie, Q6 drives the red gun of the VGA monitor, while Q7 & Q8 are for blanking. Q6 is driven by pin 6 of IC12. IC11 & IC12 are the digital magnitude comparators for channel 2.

Power

Power for the circuit is derived from a 12VAC plugpack which is rectified using D17-D20 and filtered

with a 1000µF capacitor. REG1 and REG2 provide the +12V and +5V supplies for the circuit. The 10µF capacitors at the output of each regulator prevent instability. There are also a number of 10µF and 0.1µF decoupling capacitors across the supply rails.

VGA timebase

The VGA timebase circuit is shown in Fig.3. NAND gate IC23a is the master crystal oscillator operating at 4MHz. A 10MΩ resistor between pins 11 and 12 biases the inverter into the linear mode. Crystal X1 oscillates across the inverter pins with the 22pF capacitors providing loading to prevent overtone oscillation.

IC23b inverts the clock signal and both this signal and the pin 11 output from IC23a is applied to the Data (pin 2) and the Preset (pin 4) inputs of flipflop IC26b. IC26b is a D-flipflop and the inverted level at the Data input is clocked through to the Q-bar output on the positive edge of the CK input at pin 3. When the preset is low, the Q-bar output is set low.

Graticule generation

IC24 is a binary counter with outputs from Q1-Q12. These are advanced on the negative transition of the clock input at pin 10. Its Q4 output runs at 250kHz and this is inverted with IC29a to clock IC26b.

When Q4 goes low and when the Preset input of IC26b is high, the Q-bar output of IC26b goes high. As soon as the Preset goes low again after 125ns the Q-bar output goes low again. This output produces a vertical graticule line signal 125ns wide and is repeated at a 250kHz rate or every 4µs.

This means that we have 8 vertical graticule lines in the allotted 32µs for each line.

The vertical line signal drives buffer transistor Q9 via a 1kΩ resistor. The three series diodes limit the base drive to 1.8V and the emitter to 1.2V.

The line sync pulses are derived using IC26a which works in the same manner as IC26b. When the Preset input at pin 10 is low, the Q output at pin 9 goes high when Q7 of IC24 goes low. The result is a 2µs (set by the Q3 output of IC24) low-going pulse at the Q output of IC26a. This occurs every 32µs as set by the Q7 output of IC24. Note that the use of IC23c to NAND the Q3 and Q4 outputs of IC24 before being applied to the Preset input of IC26a essentially shifts the line sync pulse so that it occurs before the first vertical graticule line.

IC25 is a second binary counter to give us the requisite Q13-Q16 outputs. Note also that Q9-Q16 are the line counter outputs used for comparators IC5 and IC6 and IC11 and IC12.

Similarly, the 4MHz, 2MHz and 1MHz outputs are used to clock the memories when in the playback mode, as selected by switch S11a.

Frame sync pulses

Frame sync pulses are derived in a similar way to the vertical graticule line and line sync pulses. Q16 from IC25 provides a 61Hz signal, while Q9 from IC24 gives a 64µs pulse width.

The oscilloscope waveforms in Fig.4 show the line sync pulses (top trace) and the frame sync pulse (bottom trace). The centre trace is actually a horizontal line for the graticule. Note that it occupies an entire line height from one line sync pulse to another.

IC28 is triggered by the Q13 output which occurs at eight times the frame frequency. This gives us a possible eight horizontal graticule lines. Unfortunately, this number does not result in a graticule in the centre of the screen. And a central graticule line is a very desirable oscilloscope feature.

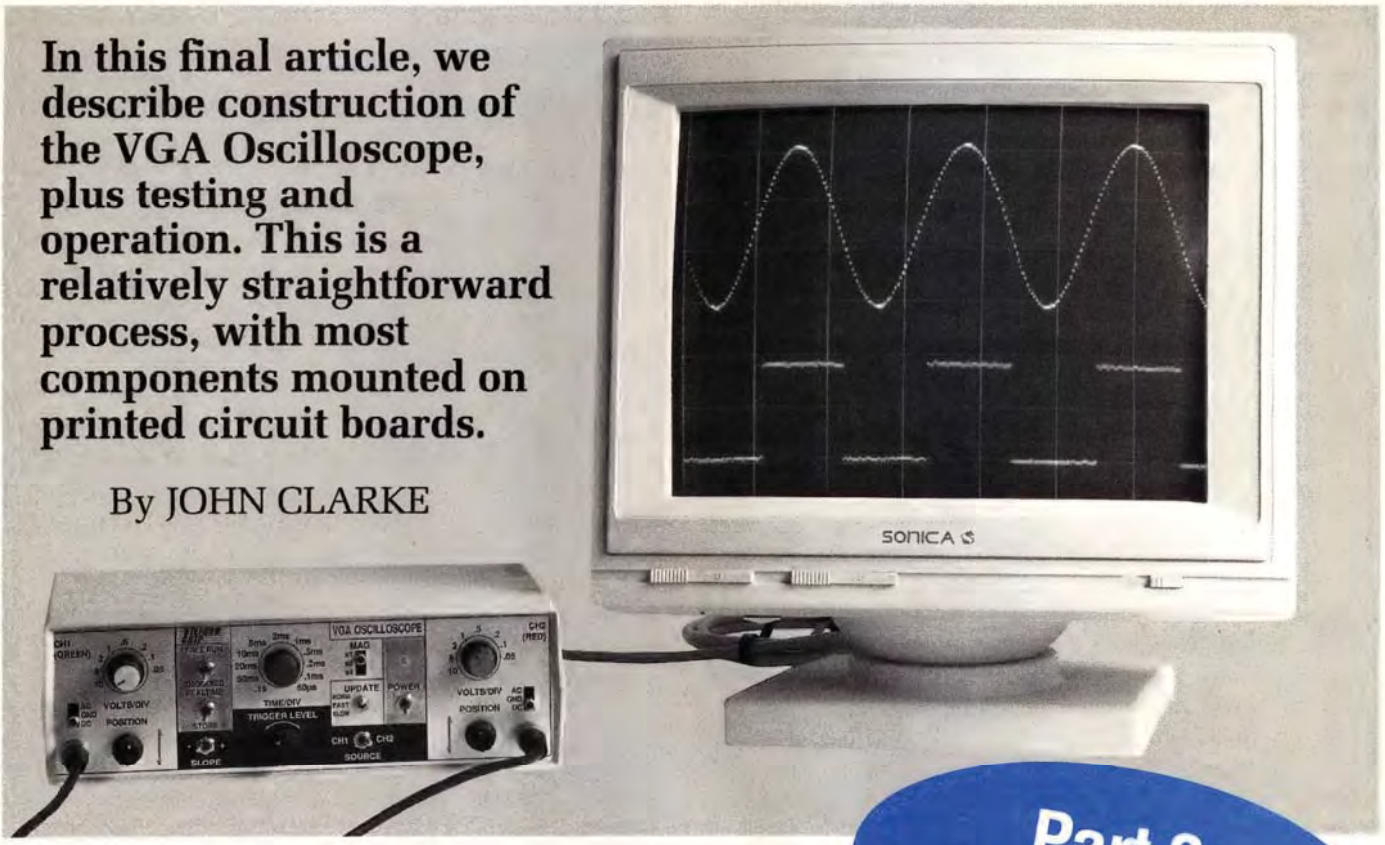
In order to obtain this, timer IC28 is used to delay the occurrence of each line so that one will actually be in the centre. The .047µF capacitor along with the 3.9kΩ resistor and trimpot VR6 set the delay at about 2048µs. The horizontal line signal from IC28 is inverted and clocked through IC27b for a horizontal line signal which is locked into the line sync pulse.

The horizontal graticule line is also buffered by Q9 before being applied to the blue gun input of the monitor.

This completes the circuit description. Next month we will present the construction details of the VGA Oscilloscope. **SC**

In this final article, we describe construction of the VGA Oscilloscope, plus testing and operation. This is a relatively straightforward process, with most components mounted on printed circuit boards.

By JOHN CLARKE



Part 3: Construction

Build a VGA digital oscilloscope

The VGA Oscilloscope is mounted in a plastic instrument case measuring 262 x 189 x 84mm. A Dynamark label measuring 252 x 76mm is fitted to the metal front panel. Most of the components are mounted on five PC boards and these are: the front panel PC board coded 04307961 and measuring 252 x 75mm; the main PC board coded 04307962, measuring 213 x 142mm; the rear timebase board coded 04307963 measuring 252 x 75mm and finally, two memory surface mount PC boards coded 04307964 and measuring 20 x 32mm.

Begin by checking the all the PC board patterns against the published artworks. Check for undrilled holes, broken tracks or shorts and fix these before proceeding. Also check that the front and rear boards fit neatly into the slots of the case and file the board edges to size if they are too large.

Memory boards

Work can start on the two small memory boards. These, for IC4 and IC10, are intended to be used with the copper side up, suitable for surface mount devices. The board overlay diagrams for both of these ICs are shown in Fig.1. For best results we recommend that pads for the ICs are pretinned using a fine tipped iron.

Once the pads are tinned, locate the IC in position, making sure it is oriented correctly and solder the four end pins in place using a minimal amount of solder. Now solder the remaining pins, taking care not to solder any two pins together.

Once done, you should check with your multimeter that each pin of the IC does in fact connect to the track, as shown on the published PC artwork. Also check that adjacent pins are not shorted except where the tracks on the overlay show that they are intended to connect.

Solder blobs between adjacent pins can be removed with solder wick and a soldering iron. After any repairs have been done, we recommend a thorough final check of the connections. Do not forget to install the 0.1uF capacitor from the copper side. In final assembly, the memory boards are attached to the main PC board using short lengths of tinned copper wire, soldered to the top side of the memory board and to the underside of the main board.

Main PC board

Now move on to the main PC board. Its component overlay is shown in

This photo shows the location of the various front panel controls. The vertical PC board behind the front panel supports all of these controls and associated components.

Fig.2. Insert all the links, using tinned copper wire, and solder them in place. All the ICs, with the exception of IC4 and IC10, can be inserted. Take care to install the correct type in each place and with the correct orientation. Now insert and solder the diodes and resistors in place. The accompanying resistor table gives the colour codes for each resistor value. It is also good practice to use a digital multimeter to verify each resistor value.

The voltage regulators (REG1 & REG2) are mounted horizontally and held in place with a screw and nut. Bend the regulator leads to insert them into the holes provided before installation. Make sure you place the 12V regulator (REG1) in the position closest to the PC board edge.

Capacitors can be mounted next. The 1000uF capacitor is placed on its side with the orientation shown. The remaining electrolytic capacitors also must be oriented with the correct polarity. 8-way header pins are installed in the positions adjacent to IC15, and near IC11 and IC12. Finally, insert the trimpots and PC stakes.

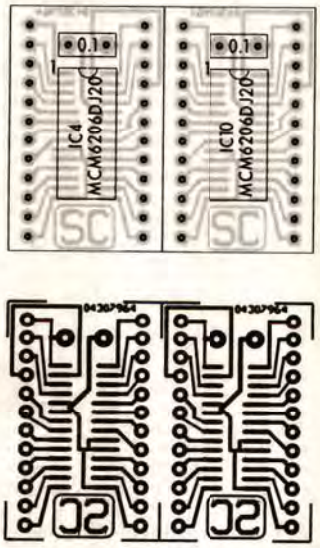
Timebase PC board

The component overlay for the timebase board is shown in Fig.3. Its assembly can proceed in the same order as the main board. Take care to orient the ICs and diodes with the polarity as shown. When installing the transistors, take care to place the BC338s in positions marked Q3, Q6 and Q9. The BC548's go in positions marked Q4 and Q7 while the BF199 devices are installed at Q5 and Q8.

Trimpot VR6 and the PC stakes are installed next. We did not use stakes in the two 4-way locations above IC24 and IC28.

Front panel board

The front panel PC board is shown in Fig.4. Carefully check out the board pattern as before and then install the links, resistors, diodes and capacitors, with the exception of the 0.22uF types. Note that LED1-LED4 are mounted flat



Two plug-in memory boards are used in the VGA Oscilloscope. The ICs on the boards are surface mount devices and require care when soldering. Fig.1 (above left) shows the PC board layouts and patterns, with a close-up photo of one assembled board at right.

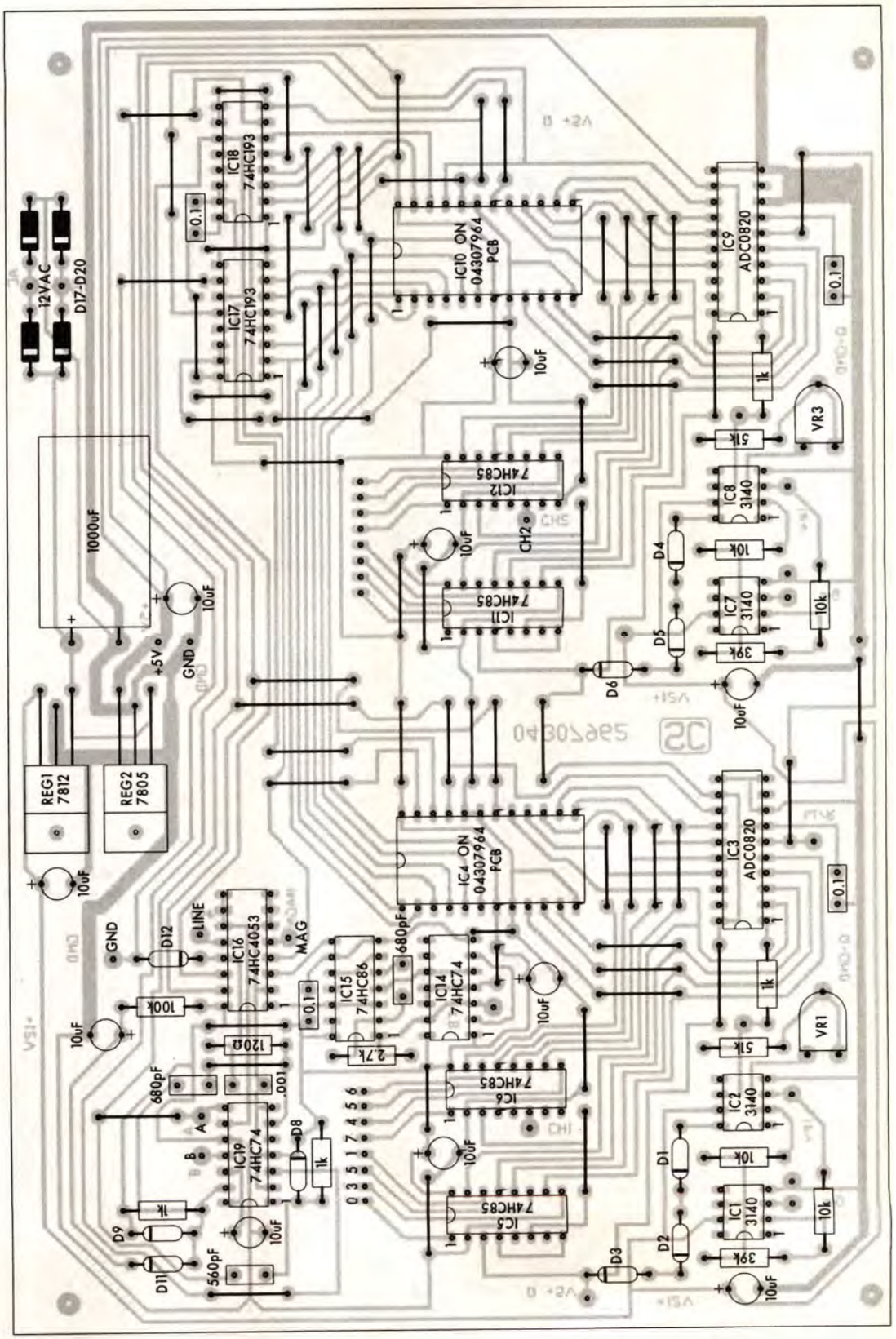


Fig.2: the parts layout for the main (horizontally mounted) printed circuit board. Solder in all of the wire links first, then proceed with the passive components and finally the diodes, transistors, regulators and finally the ICs. Opposite is the full-size main printed circuit board pattern.

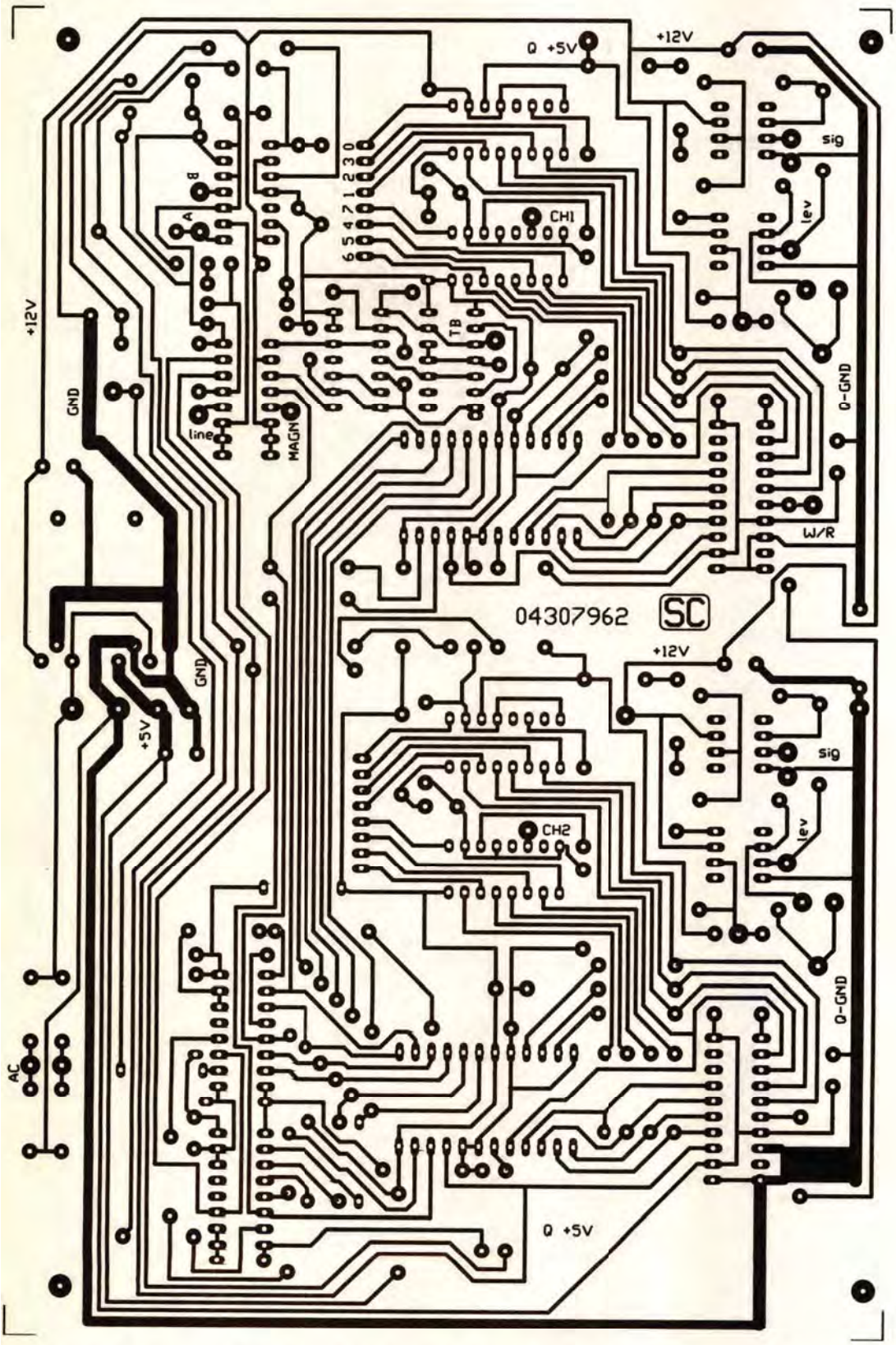
to the PC board with the cathode lead (the shortest one) bent sideways to fit into its hole. Do not shorten the leads for LED5. They need to be the full length so LED5 can reach the front panel. VC1-VC3 are mounted on the rear of the PC board for ease of adjustment later on.

Before installing any of the pots or rotary switches, cut their shafts to about 12mm long, so that the knobs will fit neatly in place. Switches S2, S5, S4, S6 - S10 and S12 are all soldered directly into the PC board. PC stakes are required to mount the slide switches S1, S3 and S11 and pots VR2, VR4 and VR5. The leads on the pots are bent over to solder to the top of the PC stakes.

Soldering in the slide switches S1, S3 and S11 requires a little more patience. The connecting lugs of each switch are inserted between the rows of PC stakes and carefully soldered in place. Check that the pins are connected by testing with a multimeter. Then solder in the 0.22uF capacitors and the PC stakes required for off-board connections.

The vertical attenuator switches S2 and S4 will be supplied as single-pole 12-position types and will need to be set to provide eight positions. This is done by rotating the switch fully clockwise and then lifting out the locking washer and repositioning it so that its tab sits in position 4. After this is done for S2 and S4, check that each switch will provide eight positions.

Switch S5 needs to be set to 11 positions. In this case the switch is rotated fully anticlockwise and the locking tab placed in position 11. Check that the switch rotates through 11 positions.



Before installing any of the boards in the case, it is best to drill the rear panel holes for the VGA lead and for the DC socket. These holes must line up with those on the rear panel PC board. The PC board hole for the socket is made large enough to accommodate the DC socket pins which will protrude through it when assembly is complete.

Fit a grommet into the rear panel for the VGA cord. Pull the VGA cord through the hole and secure it to the PC board using a cord clamp. Then fit the DC socket to the rear panel.

The front panel label can be affixed to the metal panel and drilled to accommodate the switches, pots and BNC sockets used for the input connections. The rectangular holes for the three slider switches are filed to shape after they have been drilled out.

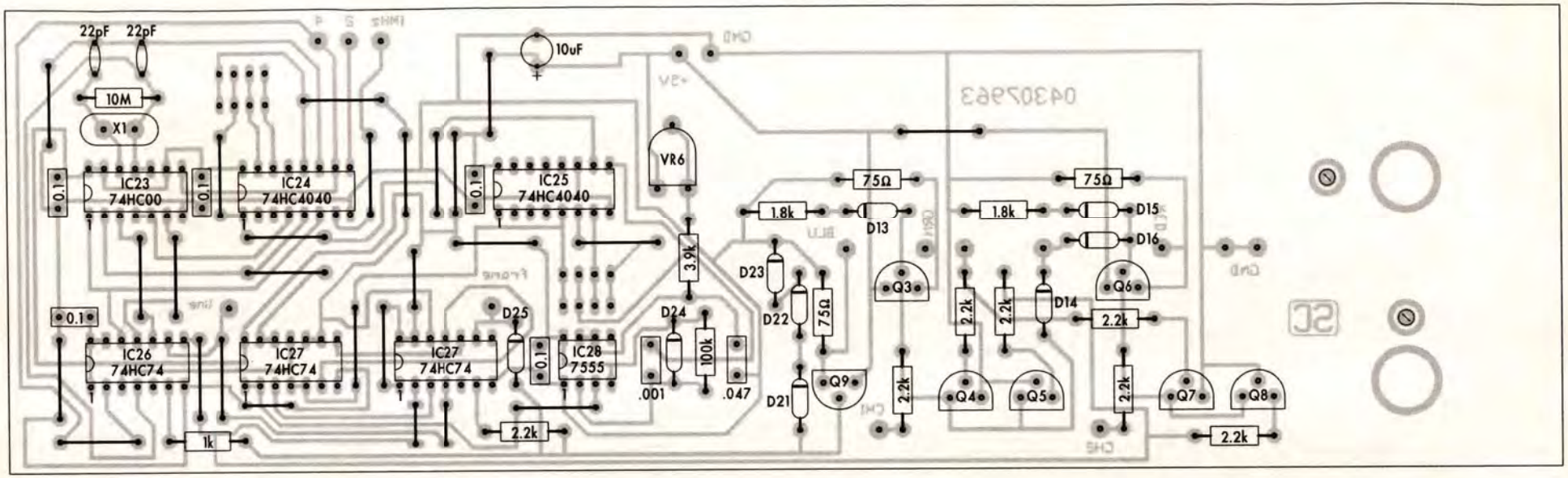
Then secure the BNC sockets to the front panel, using a star washer, nut and solder lug on each. The socket is connected to the front PC by soldering the centre pin to the PC stake and the earth connection via a short length of tinned copper wire to its GND PC stake.

Attach the front panel to the front PC board by securing it with the switch nuts. The pot nuts are not required. Fit all the knobs to the shafts of the pots and switches.

Before installing the main board in the case, it is necessary to shorten all the integral standoffs on the base. They should all be drilled off except for those at the outermost four corners. Also cut off the small upright spikes with side cutters. Then attach the main PC board in place, using self tappers into the four remaining integral standoffs. Slide the front and rear panel PC board assemblies into the case slots and the remaining wiring can be done.

Wiring

Fig.5 shows the wiring between the PC boards. Most of this is done with hookup wire. We used ribbon cable split into strips of four for connecting



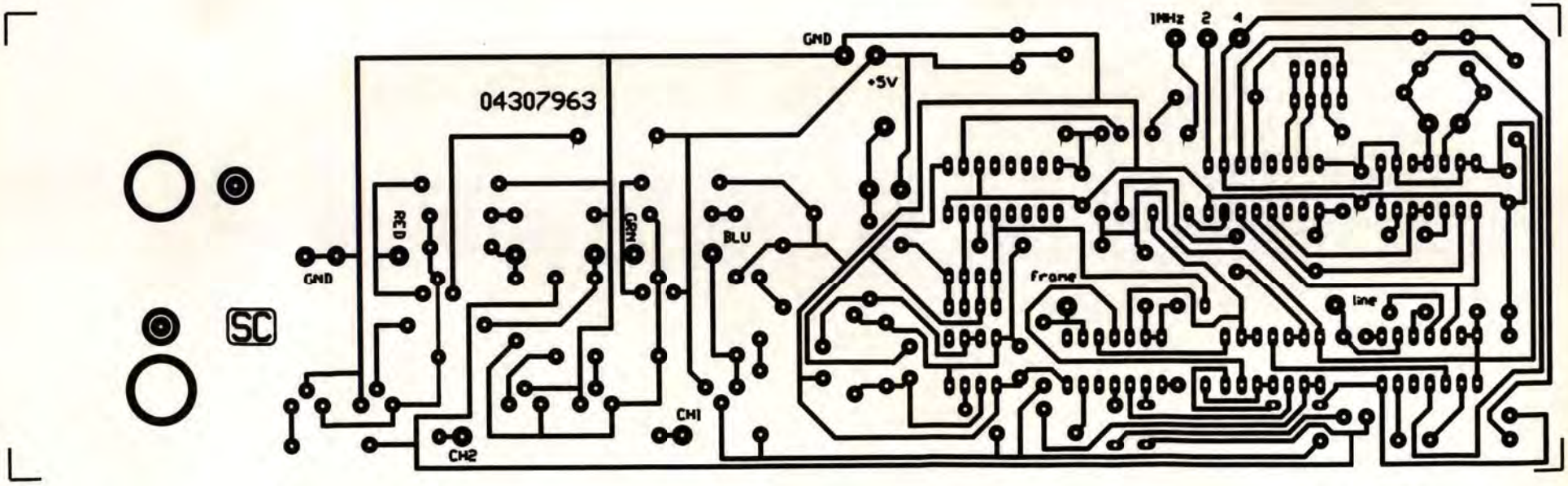


Fig.3 (top): the component layout for the timebase PC board, which mounts vertically at the rear of the case. Above is its associated PC board pattern, reproduced full size.

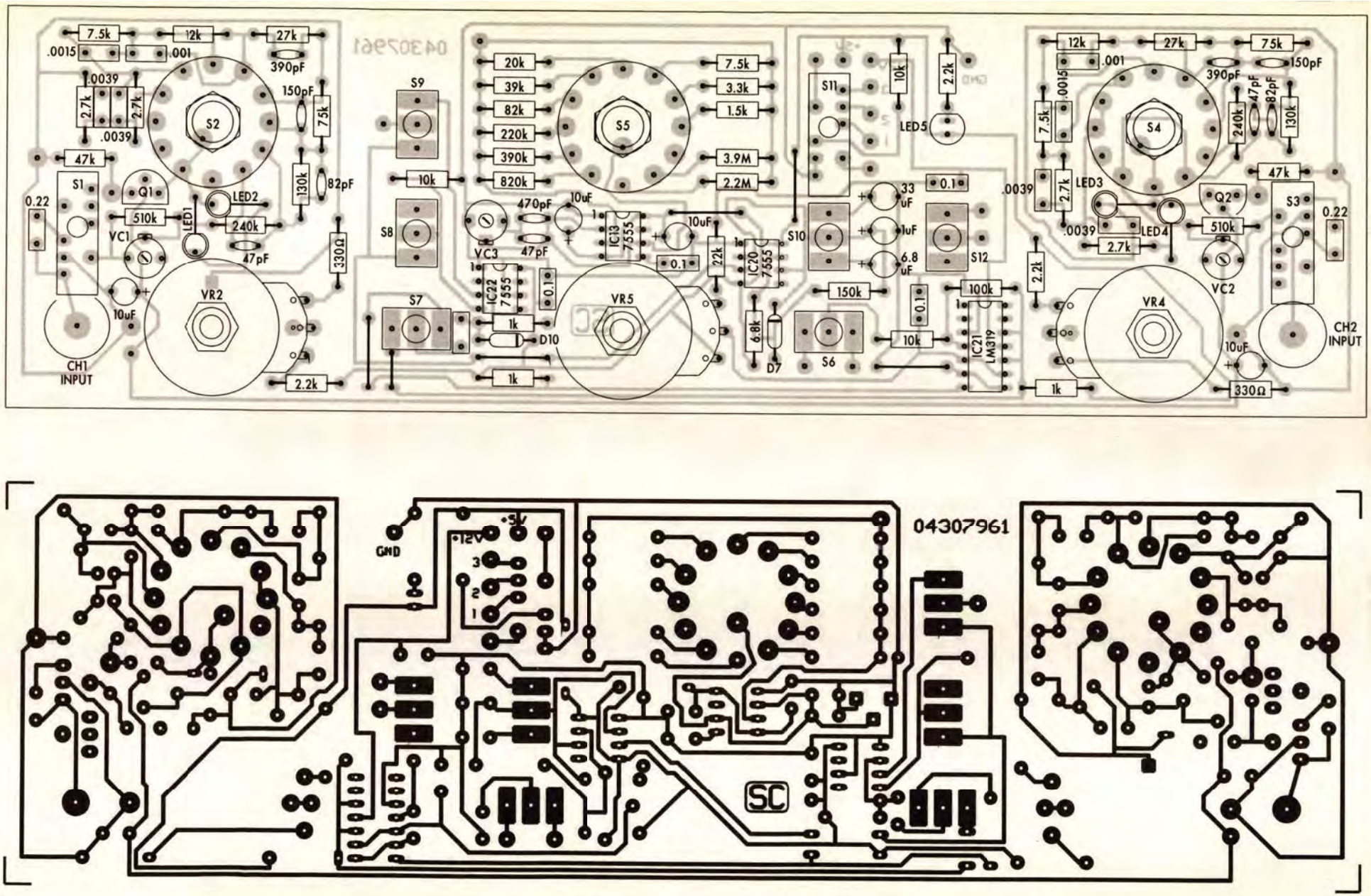
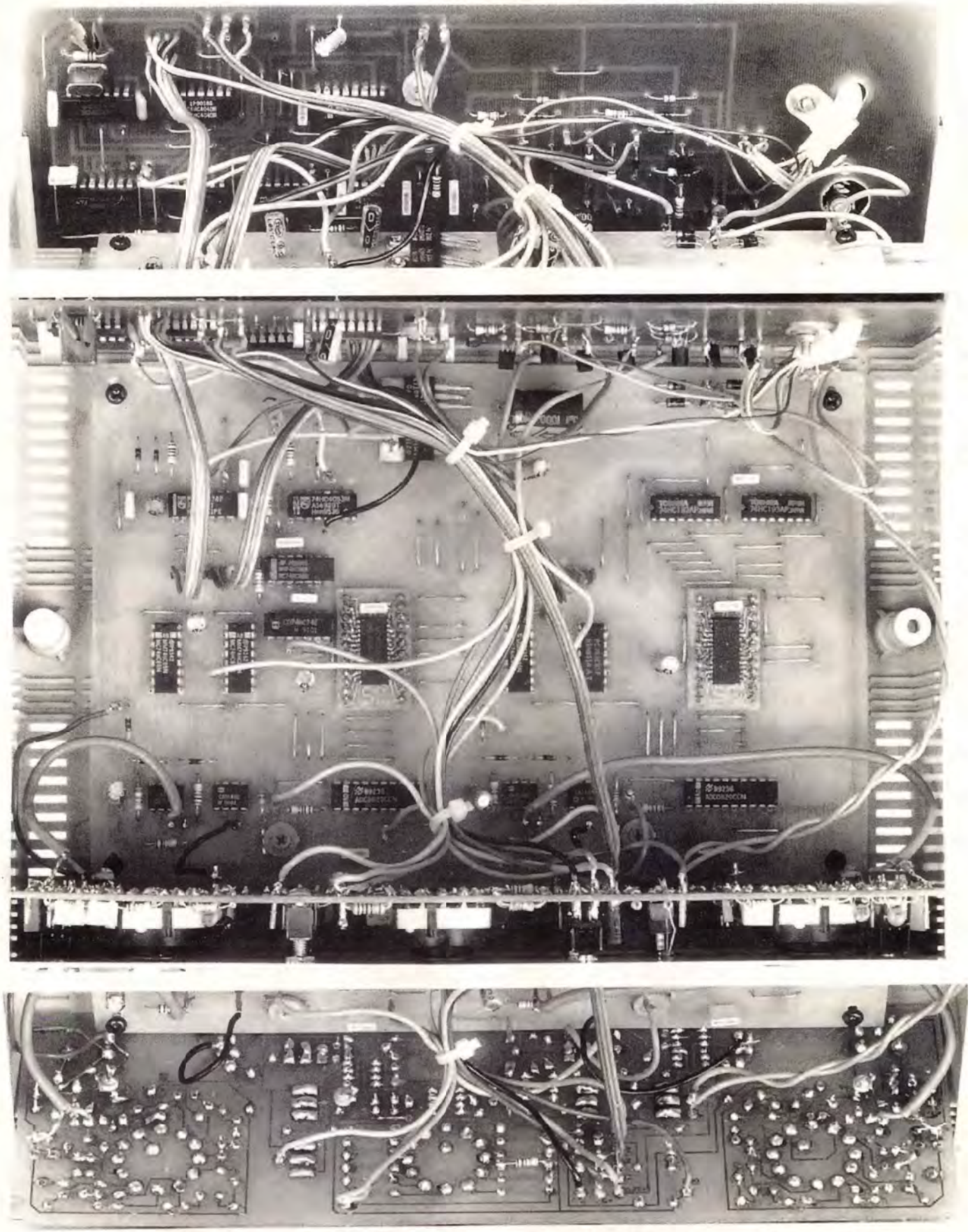


Fig.4 (top) : the component layout for the front panel (vertical) PC board, with its PC board pattern, reproduced full size.



The three photographs above are effectively an exploded view of the VGA Digital Oscilloscope, with the front and rear vertically mounted PC boards "folded out" from the main PC board similar to the component overlay diagram on the facing page. Both vertical boards mount in slots in the case with their components towards the front.

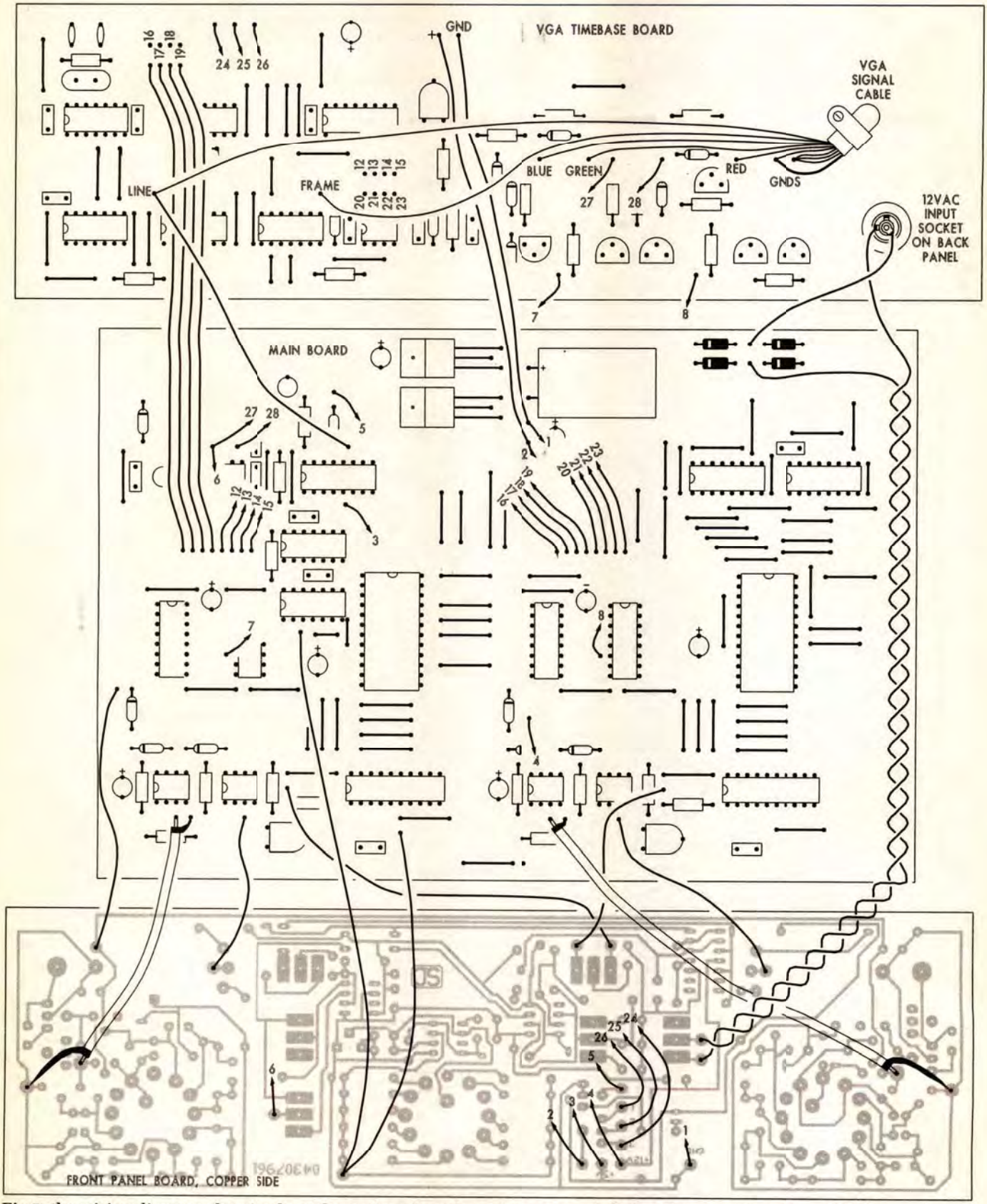


Fig.5: the wiring diagram showing how the various boards are interconnected. Use this in conjunction with the photographs on the opposite page along with the circuit diagram in last month's issue.

the 8-way pin headers on the main PC board to the rear panel board. Shielded cable is used to connect from the front panel to op amps IC1 and IC7.

The VGA cable is terminated onto the rear panel board at the positions indicated. Fig.6 shows the pin-out arrangement for a VGA socket. We purchased a VGA cable from Dick Smith

CAPACITOR MARKING CODES

	Value	IEC Code	EIA Code
❒	0.22µF	220n	224
❒	0.1µF	100n	104
❒	.047µF	47n	473
❒	.0039µF	3n9	392
❒	.0015µF	1n5	152
❒	.001µF	1n0	102
❒	680pF	680p	681
❒	560pF	560p	561
❒	470pF	470p	471
❒	390pF	390p	391
❒	150pF	150p	151
❒	47pF	47p	47
❒	22pF	22p	22

Electronics and it used white for the line sync, dark brown for frame sync, orange for the blue trace, red for the green trace, light brown for the red trace and purple, light blue, light green, dark green and un-insulated wire for the ground.

This may not be the same for your VGA cable so check this carefully with your multimeter.

When complete, tidy up all wiring with cable ties.

Testing

Before applying power, check your wiring carefully for errors. In particular, check that the positive and GND wires from the main PC board connect to the correct points on the front and rear PC board. Reverse polarity on a PC board may cause IC damage!

Apply power, check that the LED lights and that the regulators provide an output voltage of +12V from REG1 and +5V from REG2. Now you can check supply on all the ICs. Checking the front panel ICs can be done from the rear of this PC board.

IC1, IC2, IC7 & IC8 should have 12V between pins 7 and 4. IC3 & IC9 should have 5V between pins 20 and 8. IC4 & IC10 should have 5V between pins 14 and 28. IC5, IC6, IC11, IC12, IC16, IC17, IC18, IC24 & IC25 should have 5V between pins 8 and 16. IC13, IC20, IC22 & IC28 should have 5V between pins 8 and 1. IC14, IC15, IC19 IC23, IC26, IC27 & IC29 should have 5V between pins 7 and 14. IC21 should have 12V between pins 11 and 8.

If all voltages are correct you can test the oscilloscope using a VGA monitor. Turn all power off and connect the VGA lead to your monitor. Apply power to the oscilloscope first, then switch on the monitor. You should obtain at least steady blue vertical graticule lines on the screen. The horizontal graticule lines may not be present. If the graticule is broken up with rolling or with S-shaped patterns, then you have lost vertical or horizontal sync or the ground connections are disconnected.

Check wiring to the timebase and main boards for shorts, dry solder joints or discontinuities in tracks. Also recheck the VGA socket connections.

Select a timebase other than 50us and check that the red and green traces

RESISTOR COLOUR CODES

	No.	Value	4-Band Code (1%)	5-Band Code (1%)
❒	1	10MΩ	brown black blue brown	brown black black green brown
❒	1	3.9MΩ	orange white green brown	orange white black yellow brown
❒	1	2.2MΩ	red red green brown	red red black yellow brown
❒	1	820kΩ	grey red yellow brown	grey red black orange brown
❒	2	510kΩ	green brown yellow brown	green brown black orange brown
❒	1	390kΩ	orange white yellow brown	orange white black orange brown
❒	2	240kΩ	red yellow yellow brown	red yellow black orange brown
❒	1	220kΩ	red red yellow brown	red red black orange brown
❒	1	150kΩ	brown green yellow brown	brown green black orange brown
❒	2	130kΩ	brown orange yellow brown	brown orange black orange brown
❒	3	100kΩ	brown black yellow brown	brown black black orange brown
❒	1	82kΩ	grey red orange brown	grey red black red brown
❒	2	75kΩ	violet green orange brown	violet green black red brown
❒	2	51kΩ	green brown orange brown	green brown black red brown
❒	2	47kΩ	yellow violet orange brown	yellow violet black red brown
❒	3	39kΩ	orange white orange brown	orange white black red brown
❒	2	27kΩ	red violet orange brown	red violet black red brown
❒	1	20kΩ	red black orange brown	red black black red brown
❒	2	12kΩ	brown red orange brown	brown red black red brown
❒	8	10kΩ	brown black orange brown	brown black black red brown
❒	3	7.5kΩ	violet green red brown	violet green black brown brown
❒	1	6.8kΩ	blue grey red brown	blue grey black brown brown
❒	1	3.9kΩ	orange white red brown	orange white black brown brown
❒	1	3.3kΩ	orange orange red brown	orange orange black brown brown
❒	5	2.7kΩ	red violet red brown	red violet black brown brown
❒	10	2.2kΩ	red red red brown	red red black brown brown
❒	2	1.8kΩ	brown grey red brown	brown grey black brown brown
❒	1	1.5kΩ	brown green red brown	brown green black brown brown
❒	8	1kΩ	brown black red brown	brown black black brown brown
❒	2	330Ω	orange orange brown brown	orange orange black black brown
❒	1	220Ω	red red brown brown	red red black black brown
❒	1	120Ω	brown red brown brown	brown red black black brown
❒	3	75Ω	violet green black brown	violet green black gold brown

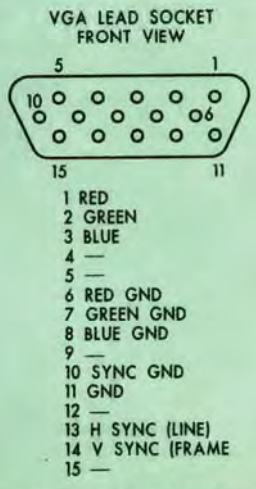


Fig.6 (above): the standard pin-outs for a VGA socket.

can be moved up and down the screen using the position controls. Note that if the traces are moved above the top of the screen they will produce a slanted two line trace on the lower screen portion. This is a sign of overrange. Signals brought to the bottom of the screen will flatten out to a straight line.

Several adjustments are required before the VGA oscilloscope is ready for use.

The first is to adjust VR6 to obtain the horizontal graticule lines. You will find that there are several settings for VR6 which will give the horizontal lines. Use the setting which centrally locates the graticule in the screen.

Check operation of the VGA oscilloscope by applying a square wave signal to the inputs and adjust the timebase and sensitivity for the best display. Note that you will need to select the Free run and Real time switch positions.

To trigger the trace, select the source (CH1 or CH2) the polarity and the Triggered position. Now adjust the trigger level so that the trace is triggered and is updated (as indicated by a momentary loss of display periodically). Use the update selection which best suits your purpose.

Check that the MAGnification switch provides an expanded timebase.

Adjust the trimmer capacitors VC1 and VC2 for best square wave response. This means that the waveform should be square without overshoot or rolloff at the rising and falling edges.

Adjust trimpots VR1 and VR3 for correct vertical calibration. If the peak-to-peak voltage of your signal is not known, measure the voltage of a battery using a multimeter. Then measure it on the VGA oscilloscope with the DC input selected. Now adjust the trimpot for a correct volts per division reading.

If the frequency of the oscillator is accurately known, check that the timebase calibration is correct. Now select the 50us timebase and adjust VC3 until the traces stop breaking up. In other words, adjust VC3 to set the maximum frequency before the A-D converters stop operating correctly. Incorrect A-D operation will be seen as many dots in a disjointed arrangement on the screen. When the frequency is adjusted so that the A-D converter operates correctly, the trace will appear normal with all dots following each other.

If correct adjustment is not possible, increase the 47pF value at pin 2 and 6 of IC13 to 56pF.

The VGA oscilloscope is now ready for use. Note that if GND input is selected, you will also need to switch to Free run triggering to obtain the update straight line on the screen. Any deviation from the straight line is due to noise and least significant digit error in the A-D conversion process. This is normal in a digital oscilloscope.

If the timebase selected is too slow for the signal being measured, a phenomenon called "aliasing" will occur. This happens since the sampling rate is not fast enough to obtain half a cycle of the waveform and a trace will be displayed which is of a much lower frequency than the incoming signal.

The problem is instantly recognised on the VGA oscilloscope since the waveform cannot be triggered correctly so that it remains steady. In most cases the waveform also shows as an envelope where two traces are evident with one being 180 degrees out of phase to the other.

If the oscilloscope is to be used to measure mains voltages take note of these precautions.

Set the volts per division switch to 10V. Use only a x10 probe and do not use the earth connection since you may incorrectly attach it to Active. The oscilloscope is earthed via the VGA monitor.

If the mains voltage is above 250VAC, the trace will overrange. To prevent this, the VR1 & VR3 calibration trimpots can be adjusted so that the trace level is reduced. This will uncalibrate the volts/division setting. SC

Fig.7: the front panel artwork for the VGA Digital Oscilloscope, reproduced full size.