

DATA SHEET

BFT46 N-channel silicon FET

Product specification
File under Discrete Semiconductors, SC07

December 1997

N-channel silicon FET

BFT46

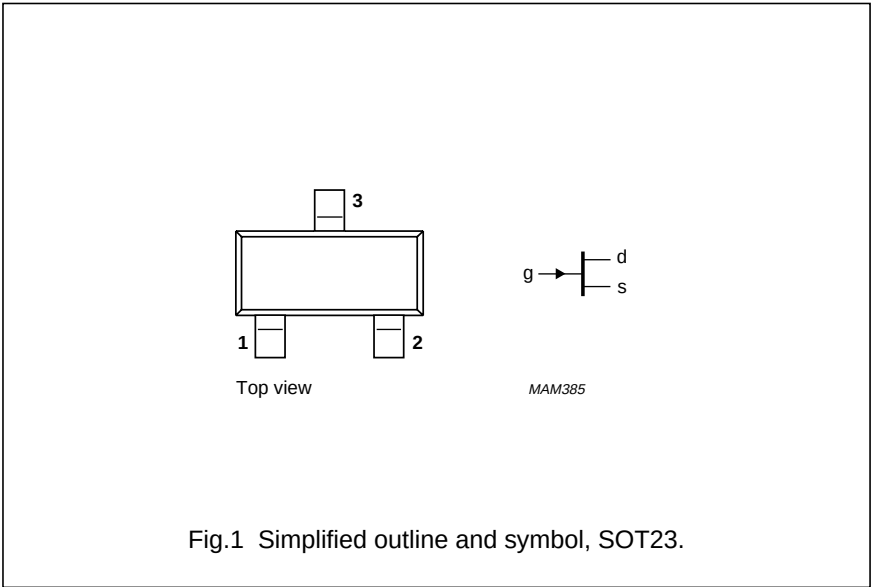
DESCRIPTION

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

PINNING

- 1 = drain
- 2 = source
- 3 = gate

Note : Drain and source are interchangeable.



Marking code

BFT46 = M3p

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to $T_{amb} = 40\text{ }^{\circ}\text{C}$	P_{tot}	max.	250 mW
Drain current			
$V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	>	0,2 mA
		<	1,5 mA
Transfer admittance (common source)			
$I_D = 0,2\text{ mA}; V_{DS} = 10\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	>	0,5 mS
Equivalent noise voltage			
$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A}; B = 0,6\text{ to }100\text{ Hz}$	V_n	<	0,5 μV

N-channel silicon FET

BFT46

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
Total power dissipation up to $T_{amb} = 40\text{ }^{\circ}\text{C}^{(1)}$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		-65 to +150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient ⁽¹⁾	$R_{th\ j-a}$	=	430 K/W
---	---------------	---	---------

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current			
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,2 nA
Drain current			
$V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	>	0,2 mA
		<	1,5 mA
Gate-source voltage			
$I_D = 50\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{GS}$	>	0,1 V
		<	1,0 V
Gate-source cut-off voltage			
$I_D = 0,5\text{ nA}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	<	1,2 V
y-parameters at $f = 1\text{ kHz}$;			
$V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$			
Transfer admittance	$ y_{fs} $	>	1,0 mS
Output admittance	$ y_{os} $	<	10 μS
$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A}; T_{amb} = 25\text{ }^{\circ}\text{C}$			
Transfer admittance	$ y_{fs} $	>	0,5 mS
Output admittance	$ y_{os} $	<	5 μS
Input capacitance at $f = 1\text{ MHz}$;			
$V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$	C_{is}	<	5 pF
Feedback capacitance at $f = 1\text{ MHz}$;			
$V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$	C_{rs}	<	1,5 pF
Equivalent noise voltage			
$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A}; T_{amb} = 25\text{ }^{\circ}\text{C}$			
$B = 0,6\text{ to }100\text{ Hz}$	V_n	<	0,5 μV

N-channel silicon FET

BFT46

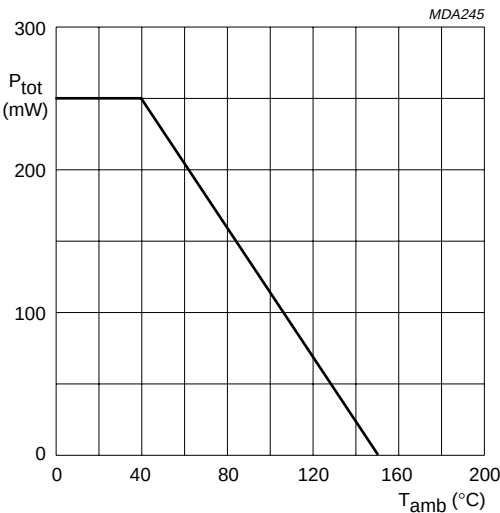


Fig.2 Power derating curve.

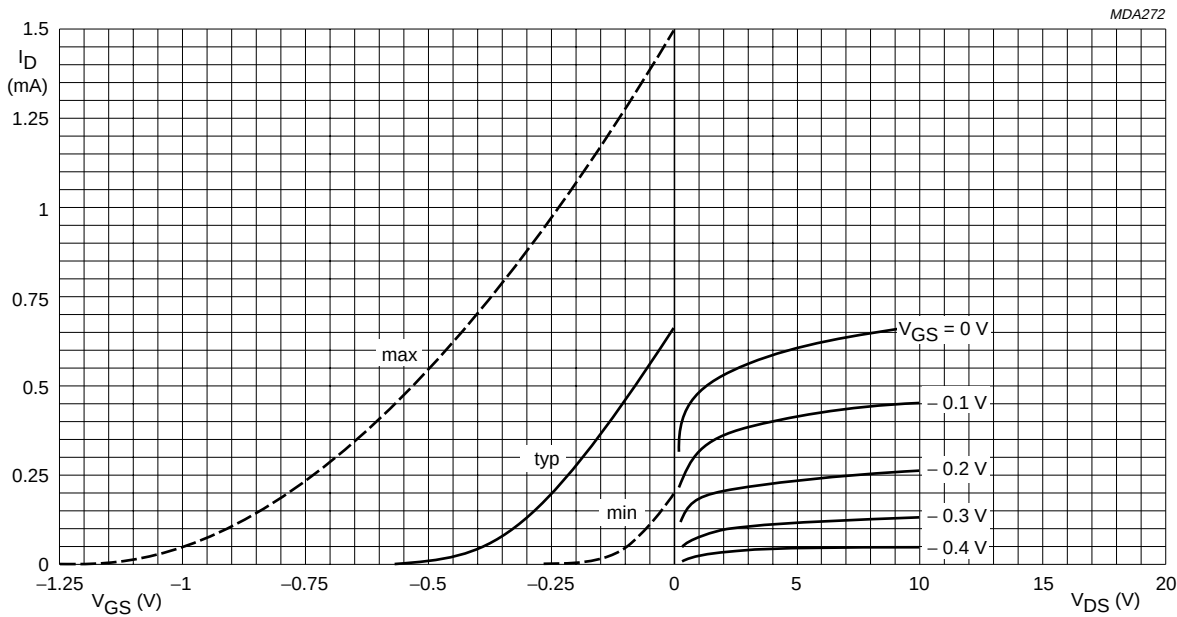


Fig.3 Typical values. $V_{DS} = 10$ V; $T_j = 25$ °C.

N-channel silicon FET

BFT46

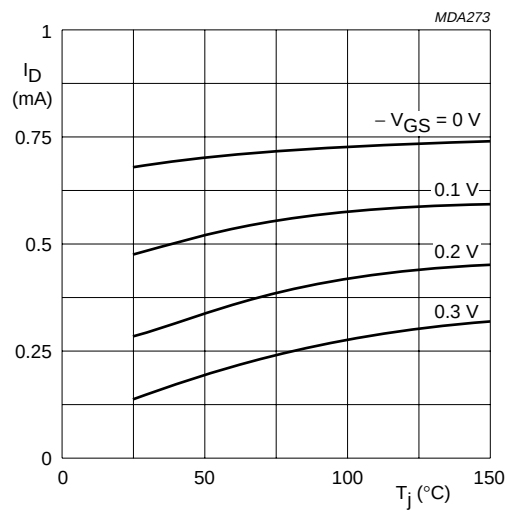


Fig.4 Typical values. $V_{DS} = 10\text{ V}$.

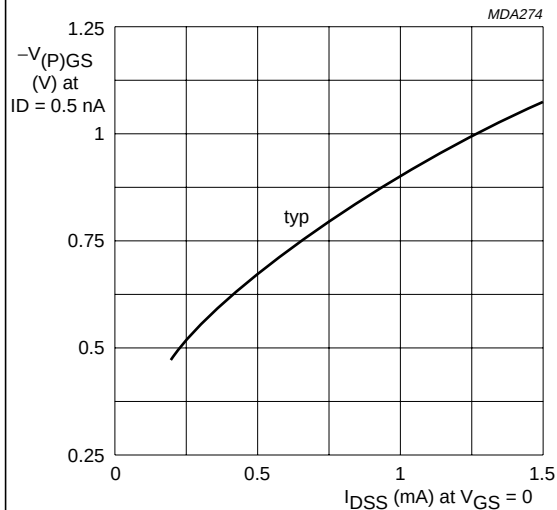


Fig.5 Correlation between $-V_{(P)GS}$ and I_{DSS} . $V_{DS} = 10\text{ V}$; $T_j = 25\text{ °C}$.

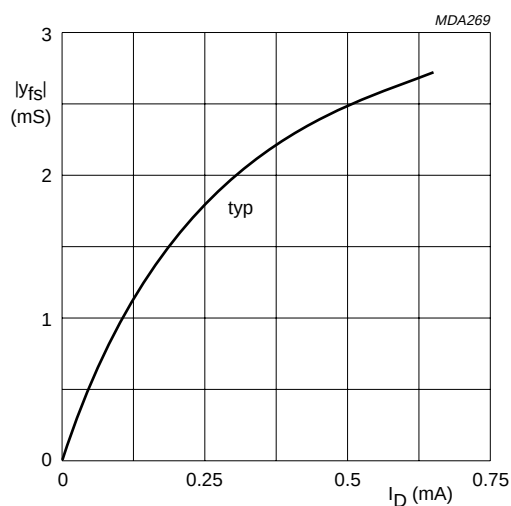


Fig.6 $|y_{fs}|$ versus I_D . $V_{DS} = 10\text{ V}$; $f = 1\text{ kHz}$; $T_{amb} = 25\text{ °C}$.

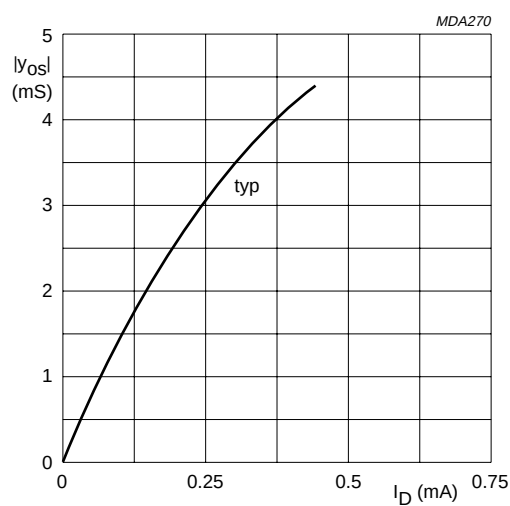


Fig.7 $|y_{os}|$ versus I_D . $V_{DS} = 10\text{ V}$; $f = 1\text{ kHz}$; $T_{amb} = 25\text{ °C}$.

N-channel silicon FET

BFT46

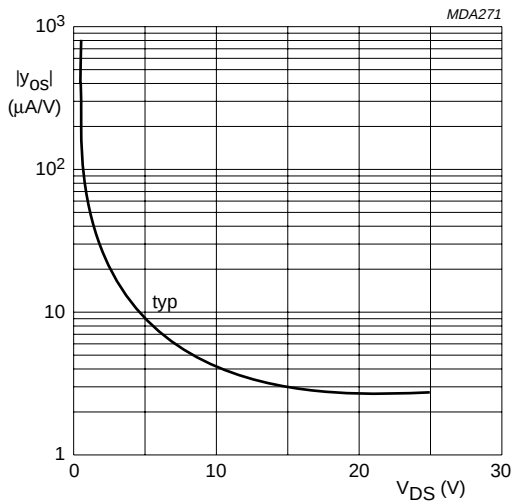


Fig.8 $|y_{os}|$ versus V_{DS} . $I_D = 0,4$ mA; $f = 1$ kHz; $T_{amb} = 25$ °C.

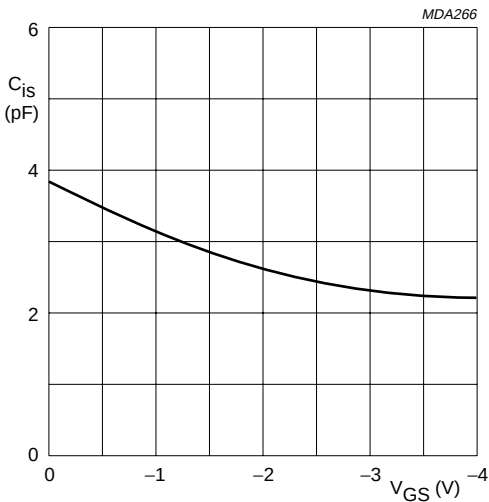


Fig.9 Typical values. $V_{DS} = 10$ V; $T_{amb} = 25$ °C.

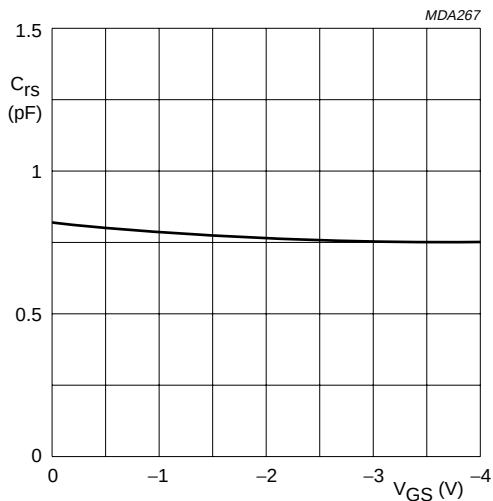


Fig.10 Typical values. $V_{DS} = 10$ V, $T_{amb} = 25$ °C.

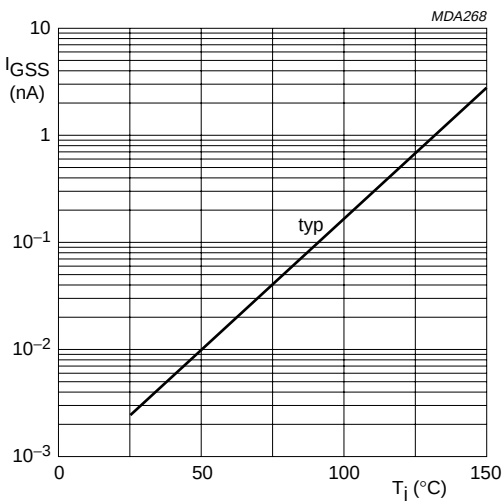
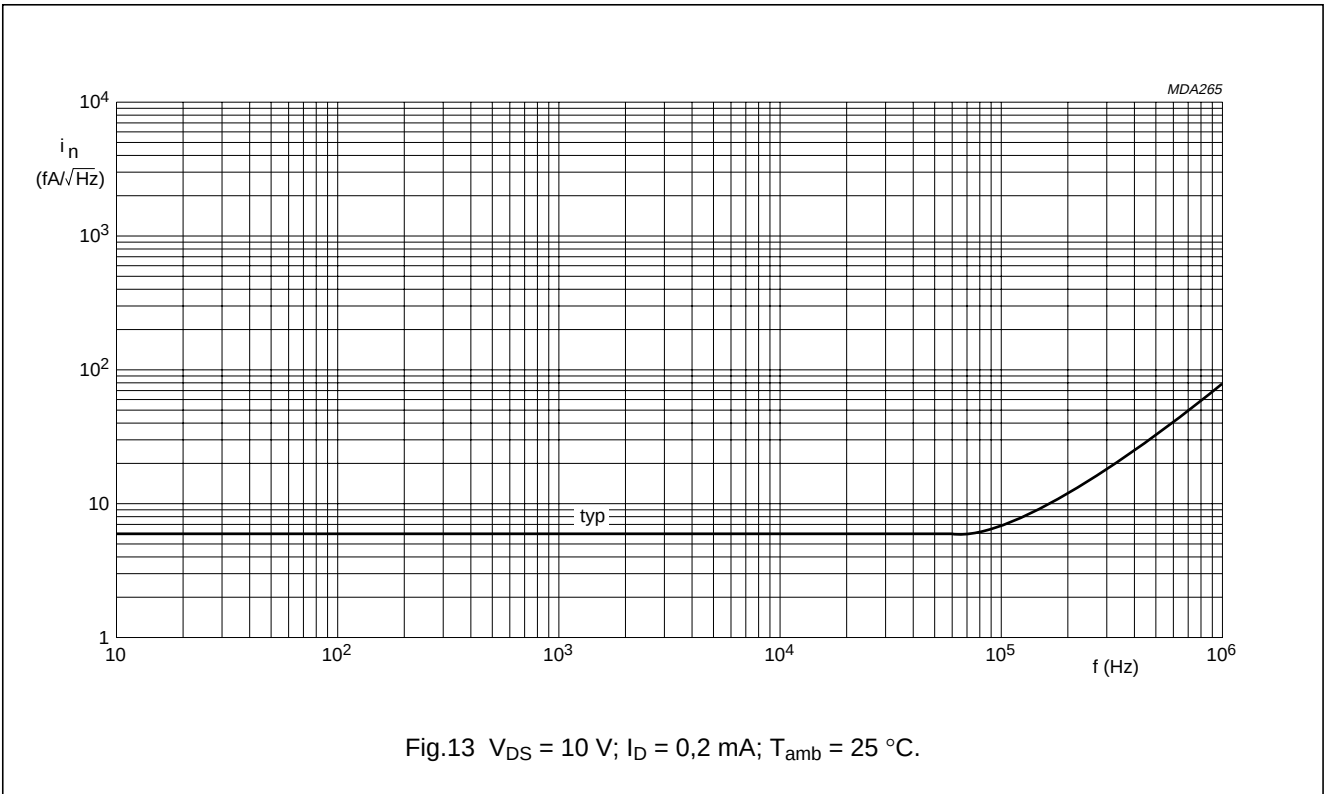
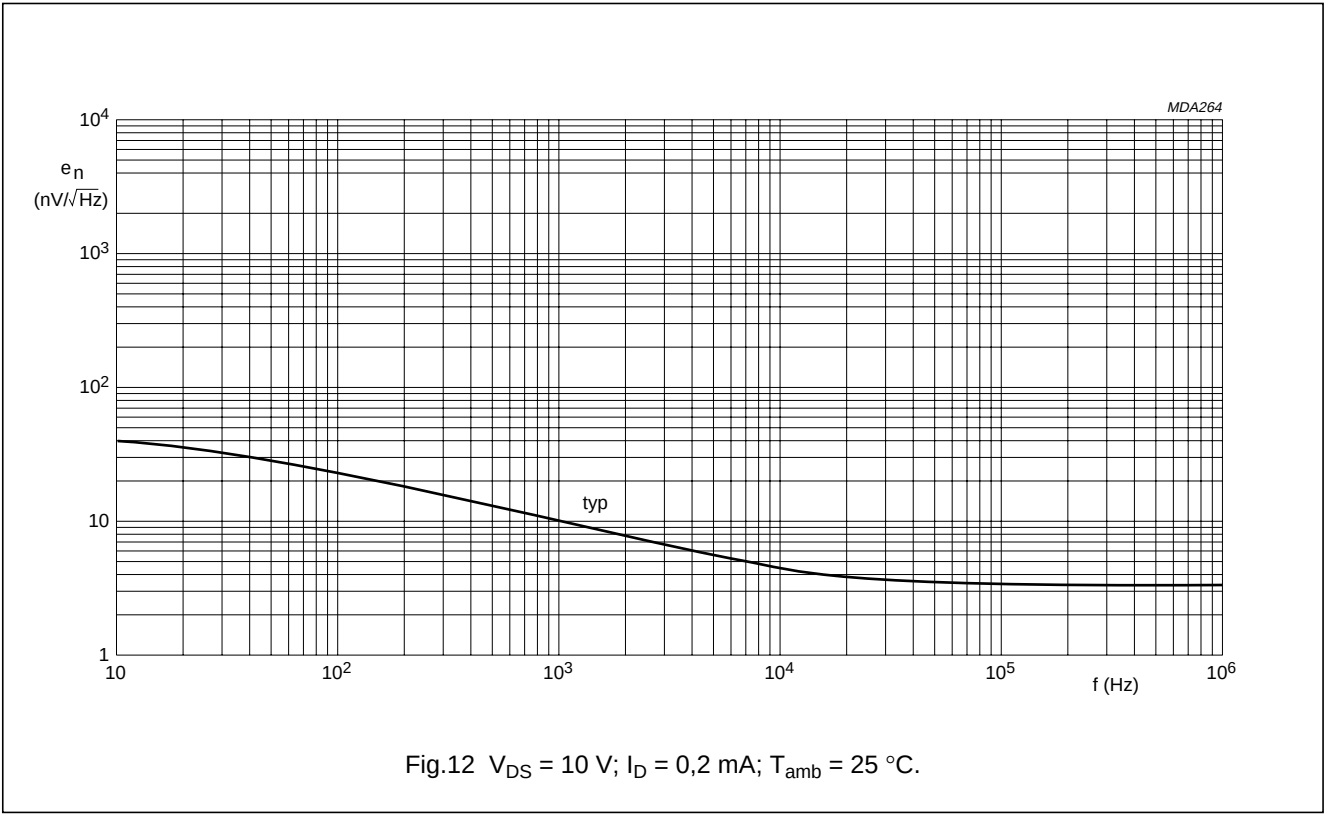


Fig.11 I_{GSS} versus T_j . $-V_{GSS} = 10$ V; $V_{DS} = 0$.

N-channel silicon FET

BFT46



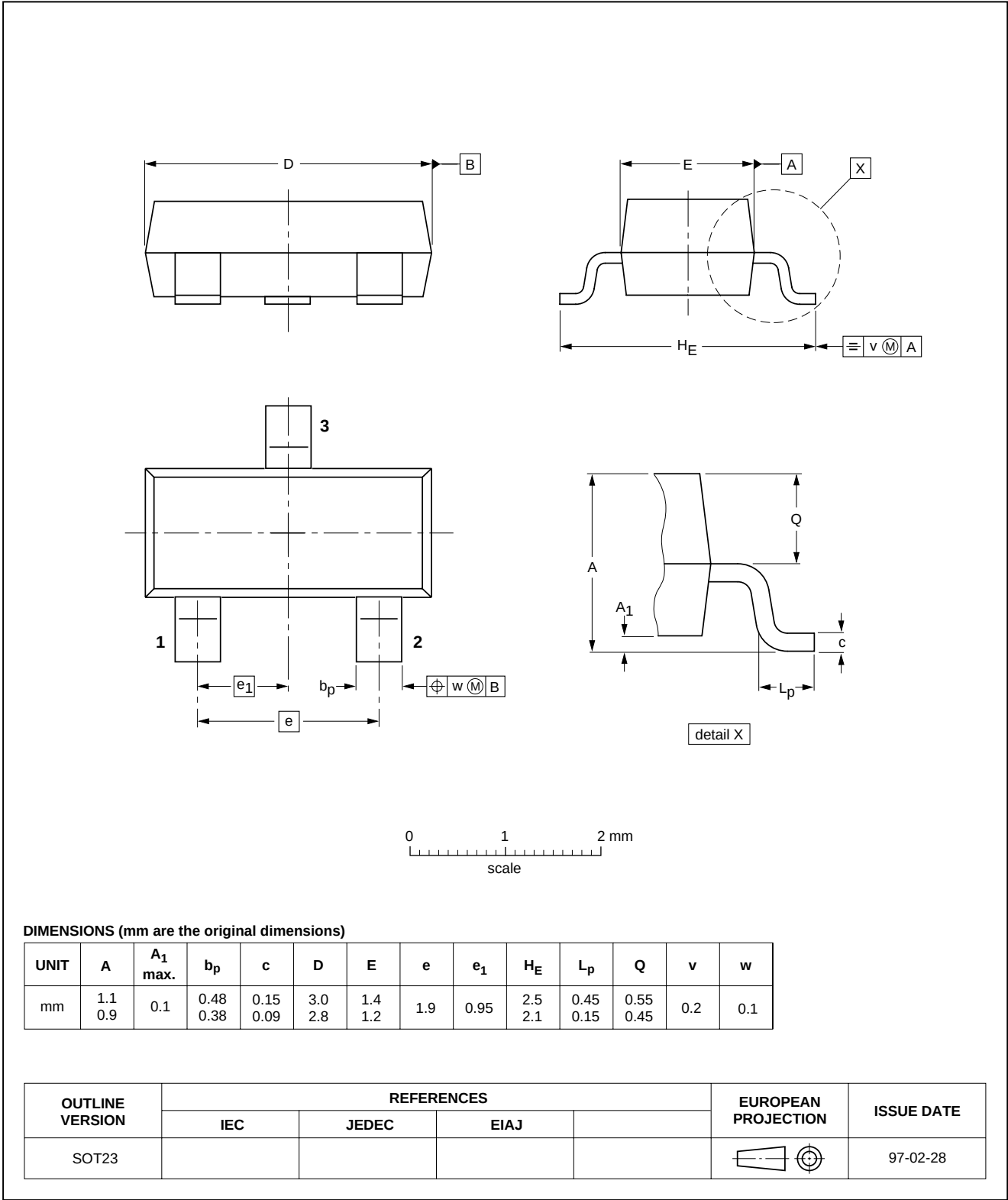
N-channel silicon FET

BFT46

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



N-channel silicon FET

BFT46

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.