1211EY1/1A, 1211EY2/2A

PUSH-PULL CONTROLLER FOR ELECTRONIC BALLASTS

GENERAL DESCRIPTION

The integrated circuit 1211EY1/2 represents the specialized controller electronic ballast for luminescent lamps. It is made on CMOS-technology.

FEATURES

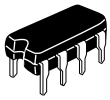
- Push-pull output with a pause between pulses
- Input of switching of frequency
- Compact case
- Minimum of external components
- Small power consumption
- Opportunity of application in output stages of powerful bipolar transistors (for 1211EY1/2A)
- Original topology

APPLICATION

- Controller ballast for compact luminescent lamps with a supply from an onboard network of a direct current 6...24 V
- Controller ballast for luminescent lamps with a supply from network of a active current 100...240 V
- DC-DC converters
- SMPS

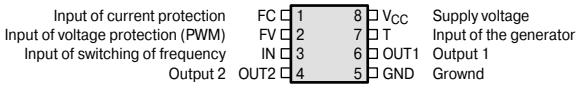
PIN CONFIGURATION AND PACKAGES

K1211EУ1P/2P **K1211EУ1T/2T**



Plastic DIP-8

Plastic SOP-8



MARKS

On the top side of the case of a integrated circuit it is represented: a trade mark of firm "DODECA-Electric", a full name of a standard rating (for example, KP1211EY1) and date of manufacturing. The reduced variant of marks is possible: a trade mark of firm "DODECA-Electric", the reduced record of the name of a standard rating (for example, EY1) and date of manufacturing.

STANDARD RATINGS

Old Type (for ГОСТ27394-87)	New Type (for ОСТ11073.915-2000)	Case (CIS)	Case (ISO)	Step (mm)	Factor of division K1	Factor of division K2	Power switch	Ability PWM
КР1211ЕУ1	К1211ЕУ1Р	2101.8-1	DIP-8	2,5	6 + 1	8 + 1	MOS	no
КР1211ЕУ1А	К1211ЕУ1АР	2101.8-1	DIP-8	2,5	2 + 1	3 + 1	Bi	no
ЭКР1211ЕУ1*	К1211ЕУ1Р1	2101.8-А	DIP-8	2,54	6 + 1	8 + 1	MOS	no
ЭКР1211ЕУ1А*	К1211ЕУ1АР1	2101.8-А	DIP-8	2,54	2 + 1	3 + 1	Bi	no
КФ1211ЕУ1	К1211ЕУ1Т	4303.8-1	SOP-8	2,5	6 + 1	8 + 1	MOS	no
ЭКФ1211ЕУ1*	К1211ЕУ1Т1	4303Ю.8-А	SOP-8	2,54	6 + 1	8 + 1	MOS	no
КФ1211ЕУ1А	К1211ЕУ1АТ	4303.8-1	SOP-8	2,5	2 + 1	3 + 1	Bi	no
ЭКФ1211ЕУ1А*	К1211ЕУ1АТ1	4303Ю.8-А	SOP-8	2,54	2 + 1	3 + 1	Bi	no
КР1211ЕУ2	К1211ЕУ2Р	2101.8-1	DIP-8	2,5	6 + 1	8 + 1	MOS	yes
КР1211ЕУ2А	К1211ЕУ2АР	2101.8-1	DIP-8	2,5	2 + 1	3 + 1	Bi	yes
ЭКР1211ЕУ2*	К1211ЕУ2Р1	2101.8-А	DIP-8	2,54	6 + 1	8 + 1	MOS	yes
ЭКР1211ЕУ2А*	К1211ЕУ2АР1	2101.8-А	DIP-8	2,54	2 + 1	3 + 1	Bi	yes
КФ1211ЕУ2	К1211ЕУ2Т	4303.8-1	SOP-8	2,5	6 + 1	8 + 1	MOS	yes
ЭКФ1211ЕУ2*	К1211ЕУ2Т1	4303Ю.8-А	SOP-8	2,54	6 + 1	8 + 1	MOS	yes
КФ1211ЕУ2А	К1211ЕУ2АТ	4303.8-1	SOP-8	2,5	2 + 1	3 + 1	Bi	yes
ЭКФ1211ЕУ2А*	К1211ЕУ2АТ1	4303Ю.8-А	SOP-8	2,54	2 + 1	3 + 1	Bi	yes
К1211ЕУ2*	К1211ЕУ2П	1102.8-1	SIP-8	2,5	6 + 1	8 + 1	MOS	yes
ЭК1211ЕУ2*	К1211ЕУ2П1	1106Ю.8-А	SIP-8	2,54	6 + 1	8 + 1	MOS	yes
К1211ЕУ2А*	К1211ЕУ2АП	1102.8-1	SIP-8	2,5	2 + 1	3 + 1	Bi	yes
ЭК1211ЕУ2А*	К1211ЕУ2АП1	1106Ю.8-А	SIP-8	2,54	2 + 1	3 + 1	Bi	yes

* manufactoring for special order

Note: The factor of division is specified in the periods of clock frequency, the first is duration of a pulse, the second - duration of a pause between pulses.

THE MAXIMAL VALUES OF PARAMETERS

Supply voltage V_{CC} ..... 12 V
Input voltage of high level V_{IN} H..... V_{CC} + 0.5 V
Input voltage of LOW level V_{IN} L ..... -0.5 V
Maximal output current I_{OUT} .....250 mA
Power supply P_D .....750 mW
The maximal capacity of loading C_L ..... 1000 pF

ELECTRIC CHARACTERISTICS

Supply voltage V_{CC}.....3...9 V
Input voltage of high level V_{IN} H.....no more $0.7V_{CC}$
Input voltage of low level V_{IN} L..... not less $0.2V_{CC}$
Average output current for each output $I_{OUT\ (av)}$..... 150 mA
Frequency of the specifying generator f_T ..no more than 5 MHz
Input current of high level I_{OUT} H.....no more than 1 μA
Input current of low level I_{OUT} L.....no more than 1 μA
Current of consumption at f_T = 0 .....no more than 10 μA

BLOCK DIAGRAM AND APPLICATION EXAMPLE

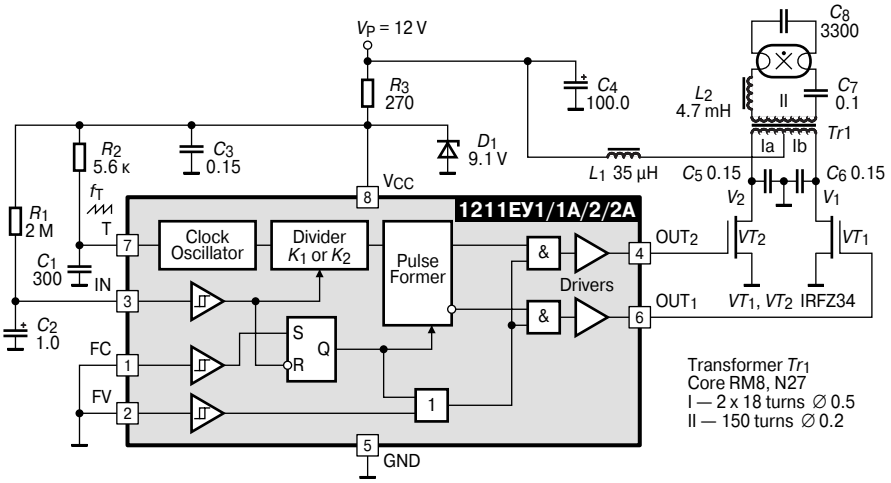


Fig. 1. Circuit ballast for a luminescent lamp power 9...15 W with switching at a zero voltage

DESCRIPTION

The block diagram of a integrated circuit 1211EY1/2A is given in a **Fig. 1**. The integrated circuit consists of the clock generator, a divider of frequency, the shaper of pulses and output amplifiers. Management of a integrated circuit is made through terminals IN, FC, FV. To terminals of management the integrated circuit connects the built - in threshold devices. Terminal IN switches a divider of frequency and resets the RS-trigger of blocking of the shaper of pulses and output amplifiers. At submission on terminal IN of a voltage of the low level the factor of division K_1 gets out and the RS-trigger is reset, at submission high - the factor of division K_2 gets out. Terminals FC and FV serve for construction of circuits of protection. Submission on terminal FV of a voltage of the high level causes deenergizing output amplifiers (on terminals OUT1 and OUT2 the voltage equal to zero) for a while while a voltage of the high level is established is kept on this terminal. Submission on terminal FC of a voltage of the high level causes setting of the RS-trigger and blocking of output amplifiers (on terminals OUT1 and OUT2 the voltage equal to zero) until on input IN is established will not be reset the *RC*-trigger.

Frequency of recurrence of pulses f_T, developed the clock generator, is set by *RC*-chain R_1C_1 connected to terminal T. Frequency of recurrence of pulses f_T can be calculated under the formula:

$$f(t) \approx \frac{0.07}{R_1 C_1} \qquad (1)$$

Dependence of stability of frequency of the generator on change of a supply voltage can be estimated under the diagram given in a **Fig. 3**. The current consumed by a integrated circuit, is increased with increase of frequency of the generator, as shown in a **Fig. 4**. The output of the generator is connected to a controlled divider of frequency from which output symmetric antiphase pulses act on an input of the shaper; the shaper provides a pause between them duration in one period of clock frequency, as shown in a **Fig. 2**.

The typical circuit of application of a integrated circuit 1211EY1/2A in ballast for a luminescent lamp is given in a **Fig. 1**. The circuit consists of a microcircuit 1211EY1/2A with timeset circuits and the push-pull transformer cascade which loading is oscillatory contour L_2C_8 with a luminescent lamp. After inclusion the circuit makes warming up of cathodes of a lamp by a voltage with frequency on 30 % above resonant, and then submits on it a high voltage with the frequency equal resonant, under which action a lamp begins to shine. Frequency of pulses, developed the generator, is selected such, that at the high level of a voltage on input IN (at the factor of division equal K_2) frequency of recurrence by it of pulses on an output of a integrated circuit it was equal to resonant frequency of an oscillatory contour. At submission of a supply voltage the current proceeding through resistor R_2 begins to charge capasity C_2 connected to terminal IN. The constant of time of *RC*-chain R_2C_2 determines time hiting cathodes of a lamp. Thus in time up to achievement of threshold value of a voltage on input IN warming up of cathodes of a lamp by frequency above resonant (factor of division K_1), and after achievement of threshold value - ignition and a luminescence of a lamp (factor of division K_2) is made.

For the given circuit resonant frequency of an oscillatory contour is equal 45 kHz, time of a charge of capasity C_2 – 2 seconds. Elements L_1, C_5 and C_6 provide change of a voltage on drains of transistors under the sine wave law. Transistors are switched at a zero voltage on a drain owing to what warming up of transistors decreases due to reduction of switching losses.

The integrated circuit 1211EY1/2A differs from 1211EY1/2 smaller values of both factors of division K_1 and K_2 (see the table of standard ratings) a divider of frequency that twice approximately allows to reduce frequency of the clock generator f_T. It is made that duration of a pause between the output pulses, equal to one period of clock frequency f_T, has increased also approximately twice, that effectively allows to use as swtches inexpensive bipolar transistors with big time of switching, than at what of field transistors.

Difference of integrated circuit 1211EY1 from 1211EY2 consists in various ways of blocking of outputs on input FV (pin 2). 1211EY1 blocks outputs at presence of potential of a high level on input FV (pin 2) for all time of action of this potential. 1211EY2 blocks an output on which at present there is an active high level front of a signal on input FV (pin 2) before the ending of the current pulse on an active output (OUT1 or OUT2), as shown in a **Fig. 2b** and **Fig. 2c**. Given property 1211EY2 allows to organize PWM-like control mode.

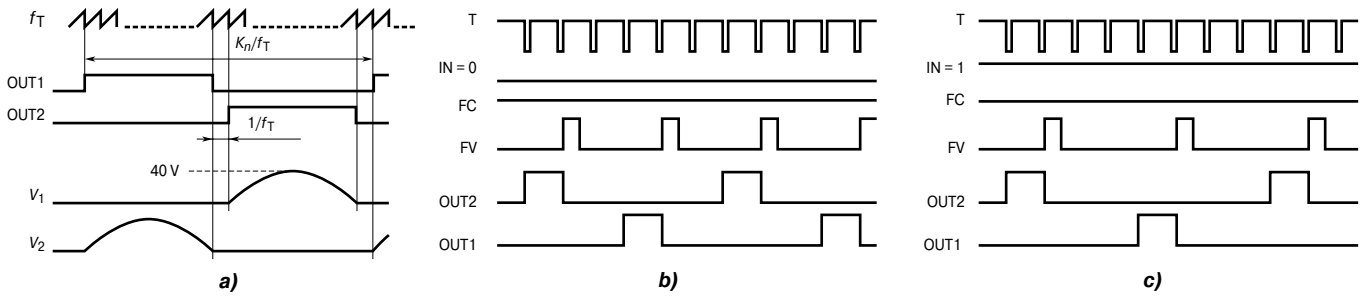


Fig. 2. Time diagrams

TYPICAL CHARACTERISTICS

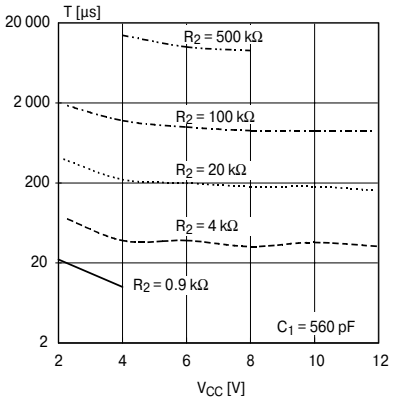


Fig. 3. Dependence of the period of following of pulses on an output of a microcircuit 1211EY1 from a supply voltage. The factor of division is equal 14

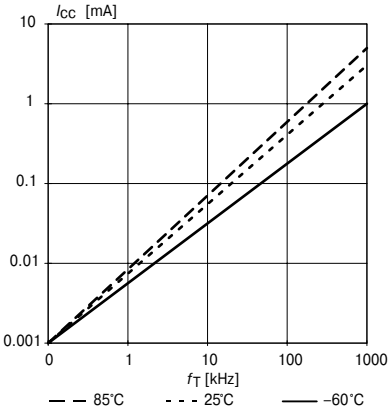


Fig. 4. Dependence of a current of consumption on frequency of the generator and temperatures

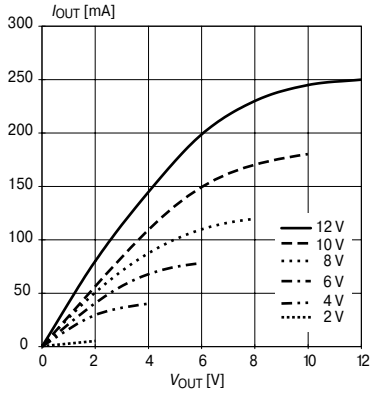


Fig. 5. Dependence of a output current on a output voltage (terminals 4, 6) at various supply voltage

REMARKS ON APPLICATION

At increase of a supply voltage the voltage brought to a lamp, and capacity, power dissipation is increased by a integrated circuit. To avoid failure as lamp, and power transistors, in ballast enter blocking on excess of a supply voltage and a consumed current. At increase of a supply voltage output stages are switched off with the help of terminal FV. At an output of a lamp the current consumed by transistors VT_1 and VT_2 out of operation is sharply increased. In this case output stages are disconnected with the help of terminal FC then work of a integrated circuit stops. The circuit of unit of blocking ballast on excess of a supply voltage is given in a **Fig. 6**. At increase of a supply voltage the voltage on input FV grows. At excess of a threshold of operation there is a blocking output stages of a integrated circuit (on terminals OUT1 and OUT2 the voltage equal to zero) is established. The level of operation of the circuit of protection (as much as possible allowable voltage $V_{P(max)}$, brought to the output stage) is determined by a choice of values of resistors R_1, R_2:

$$V_{P\,(max)} = \frac{0.6V_{CC}(R_1 + R_2)}{R_2} \qquad (2)$$

Resistance of resistor R_1 should be big enough to limit a current through the internal protective diode at the big throws of a supply voltage.

The circuit of unit of blocking ballast on excess of a current through a lamp is given in a **Fig. 7**. In case of an output of a lamp the current through a lamp that results in increase of a power failure at spirals of a lamp out of operation is sharply increased. This voltage is straightened by detector D_1C_1 and through divider R_1R_2 moves on input FC. For prevention of casual operation from handicapes in parallel resistor R_1 capasity C_1 is included. Divider R_1R_2 should be designed so that at as much as possible allowable current through a lamp the voltage on input FC has made $0.6V_{CC}$.

In a **Fig. 8** circuit ballast with protection of power keys is shown. This circuit is similar to the circuit in a **Fig. 1** and is added with units of protection. Additional resistors R_3, R_4 and crosspieces X_1, X_2 allow to reduce working frequency of the specifying generator by 5, 10 and 15%. Elements D_1 and R_5 provide protection against throws of a supply voltage. At increase of a supply voltage V_P up to 17 V stabilitron D_1 opens, the voltage on input FV will make 5 V, that meets to a threshold of operation of the circuit of protection. The voltage on terminals OUT1, OUT2 thus becomes equal to zero, transistors VT_1, VT_2 are closed. Resistor R6 limits a current on input FV at a level 5 mA at throws of a voltage up to 100 V. For this time the supply voltage of a microcircuit and frequency of work of the specifying generator should be established. Resistor R_{11} is the gauge of a current. The voltage from it acts on detector D_3C_8 and further on input FC. Selecting resistor R_{11}, establish threshold I_{MAX} of operation of protection on a current:

$$I_{MAX} = \frac{0.6V_{CC}}{R_{11}} \qquad (3)$$

If necessary this value can be counted in view of factor of transformation of transformer T_1 in a current of consumption from the power supply. Elements R_7, R_8, C_5 allow to limit emissions of a voltage on drains of field transistors VT_1, VT_2 at the moment of switching at a level $0.2V_P$ In a **Fig. 6** and a **Fig. 7** are shown possible variants of application of a integrated circuit for construction of pulse power supplies.

The loading characteristic of a integrated circuit is submitted in a **Fig. 8**.

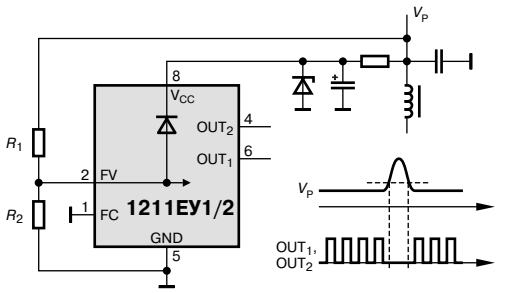


Fig. 6. The circuit of protection of the output stage on a voltage

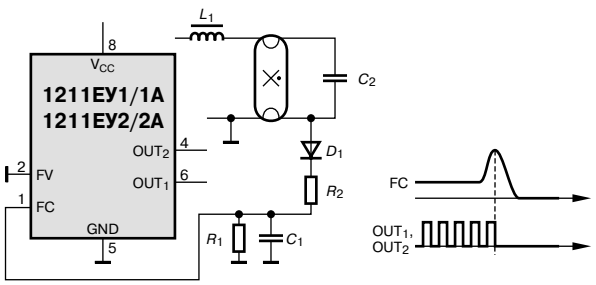


Fig. 7. The circuit of protection of the output stage on a current

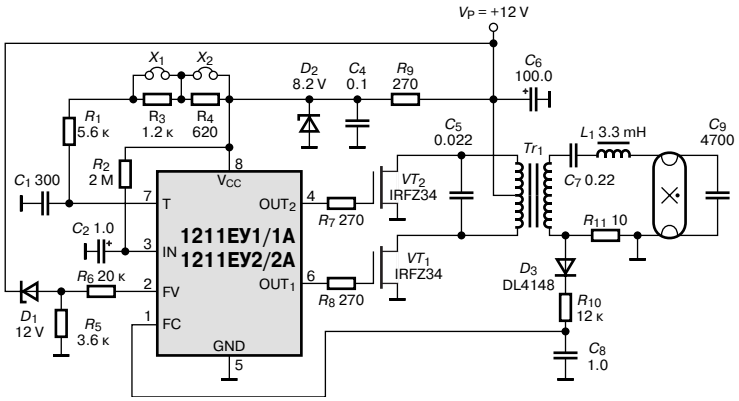


Fig. 8. Circuit ballast with protection of power keys

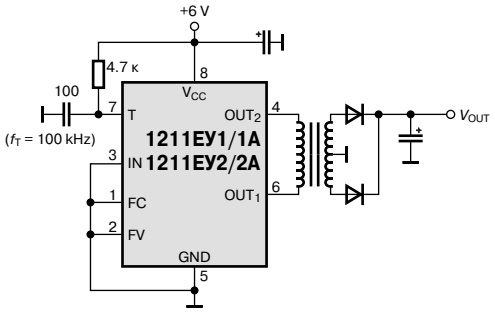


Fig. 9. The circuit of the pulse power supply 0.5 W

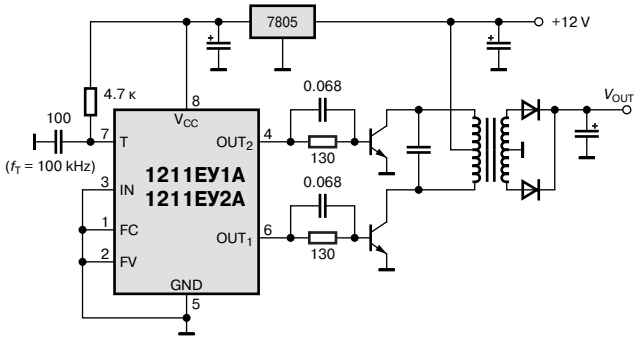


Fig. 10. The circuit of the converter of a voltage 15 W

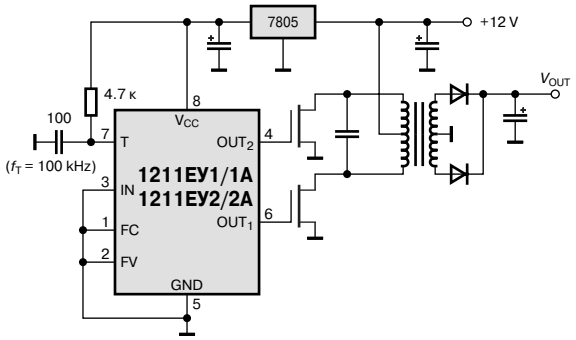


Fig. 11. The circuit of the converter of a voltage with use 1211EY1/2A and bipolar transistors