L2014

LIQUID CRYSTAL DISPLAY MODULE

USER'S MANUAL

CONTENTS

1. GENERAL

1.1 General

The L2014 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

1.2 Features

- 20-character, four-line liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

1.3 Block Diagram

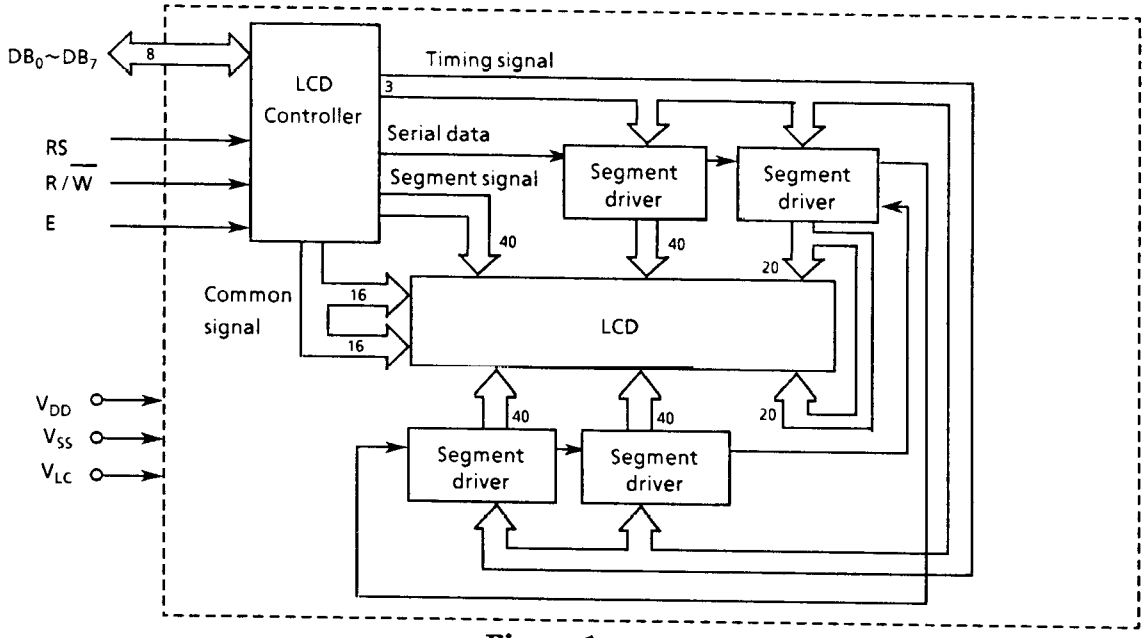


Figure 1

1.4 Absolute Maximum Ratings

1.4.1 TN LCD module (1/5 bias)

Vss = 0 V

Item	Symbol	Conditions	Standard	Unit
Power supply voltage	V_{DD}		− 0.3 to + 6.0	V
	V_{LC}		V_{DD} − 13.5 to V_{DD}	V
Input voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}		0 to + 50	°C
Storage temperature	T_{stg}	At 50% RH	− 20 to + 60	°C

1.4.2 New TN LCD module (1/4 bias)

Vss = 0 V

Item	Symbol	Conditions	Standard	Unit
Power supply voltage	V_{DD}		− 0.3 to + 6.5	V
	V_{LC}	$V_{LC} \geqq V_{SS}$	V_{DD} − 6.5 to V_{DD}	V
Input voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}		0 to + 50	°C
Storage temperature	T_{stg}	At 50% RH	− 20 to + 60	°C

1.5 Electrical Characteristics

1.5.1 TN LCD module (1/5 bias)

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{DD}-V_{LC}		4.0	—	11.0	V
* Input voltage	High	V_{IH}		2.2	—	V_{DD}	V
	Low	V_{IL}		0	—	0.6	V
** Output voltage	High	V_{OH}	$-I_{OH}$ = 0.205 mA	2.4	—	—	V
	Low	V_{OL}	I_{OL} = 1.2 mA	—	—	0.4	V
Current consumption		I_{DD}	Ta = 25°C, V_{DD} = 5 V, V_{LC} = 0.6 V	—	2.7	3.5	mA
		I_{LC}		—	1.0	2.0	mA
Clock oscillation frequency		f_{OSC}	Resistance oscillation	140	220	300	kHz

* Applied to DB_0 to DB_7, E, R/W, and RS ** Applied to DB_0 to DB_7

1.5.2 New TN LCD module (1/4 bias)

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{DD}-V_{LC}	$V_{LC} \geqq V_{SS}$	3.0	—	6.0	V
* Input voltage	High	V_{IH}		2.2	—	V_{DD}	V
	Low	V_{IL}		0	—	0.6	V
** Output voltage	High	V_{OH}	$-I_{OH}$ = 0.205 mA	2.4	—	—	V
	Low	V_{OL}	I_{OL} = 1.2 mA	—	—	0.4	V
Current consumption		I_{DD}	Ta = 25°C, V_{DD} = 5 V, V_{LC} = 0.4 V	—	2.9	4.0	mA
		I_{LC}		—	1.2	2.0	mA
Clock oscillation frequency		f_{OSC}	Resistance oscillation	140	220	300	kHz

* Applied to DB_0 to DB_7, E, R/W, and RS ** Applied to DB_0 to DB_7

Remark: Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.
The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

(1) TN LCD module

Temperature (°C)	0	25	50
V_{opr} (V)	4.65	4.4	4.1

$V_{opr} = V_{DD} - V_{LC}$

(2) New TN LCD module (Gray)

Temperature (°C)	0	25	50
V_{opr} (V)	5.0	4.75	4.5

$V_{opr} = V_{DD} - V_{LC}$

1.6 Timing Characteristics

1.6.1 Write operation

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Min.	Max.	Unit
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ → E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

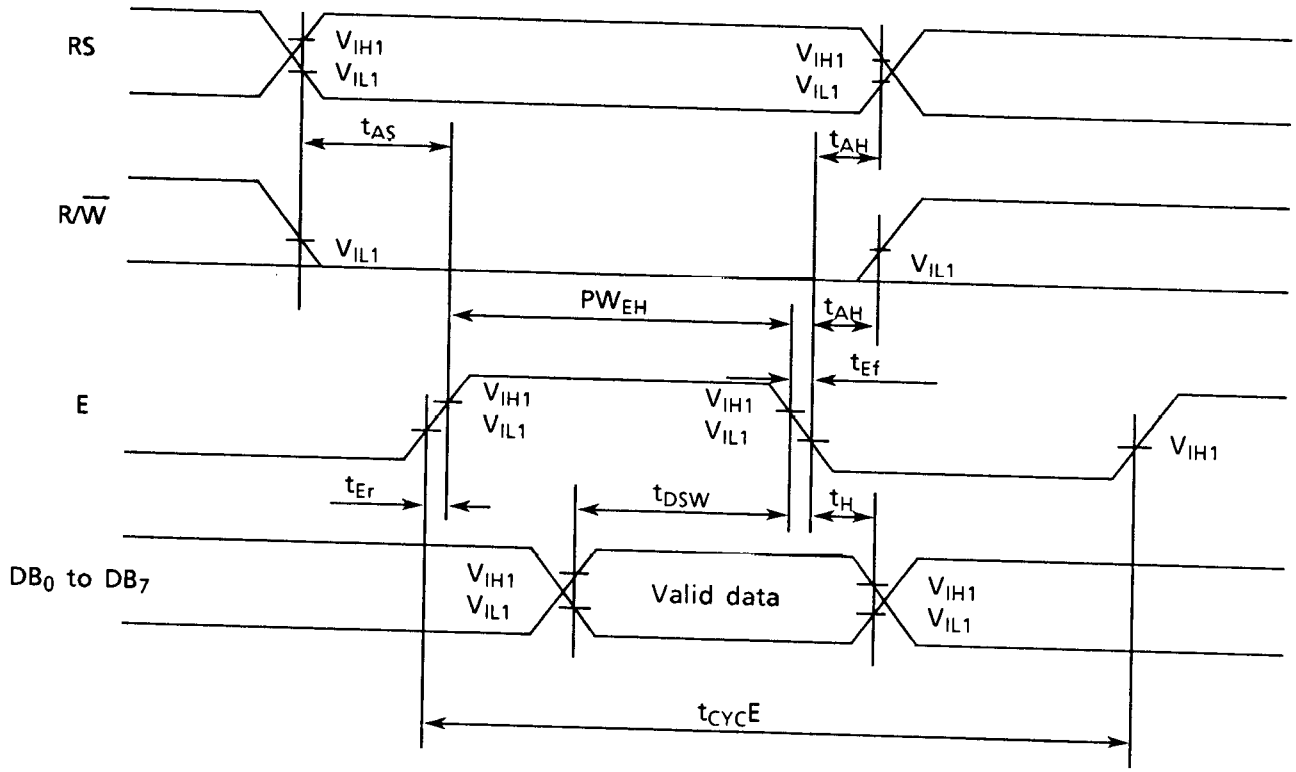


Figure 2 Data write from MPU to module

1.6.2 Read operation

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0°C to 50°C

Item		Symbol	Min.	Max.	Unit
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$→E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_H	20	–	ns

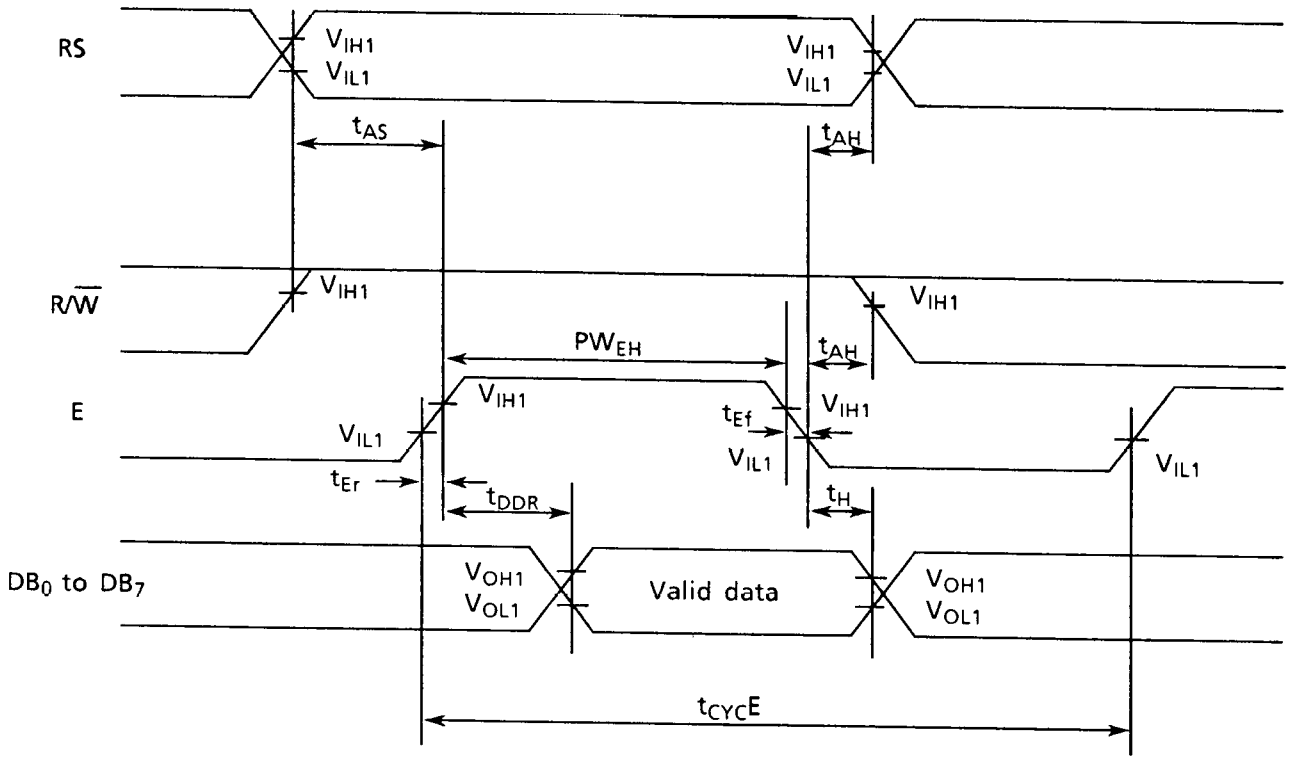


Figure 3 Data read from module to MPU

1.7 Optical Characteristics

1.7.1 TN LCD module

Viewing angle: 6 o'clock (Ø = 0°), Ta = 25°C, V_{opr} = 4.4 V

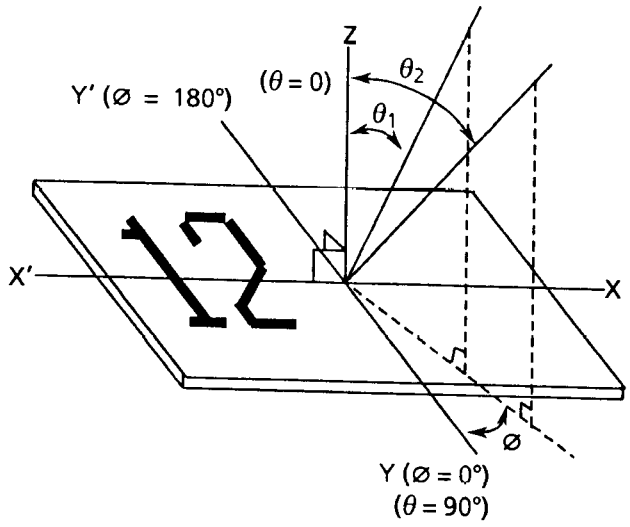
Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	$C \geqq 2.0$, Ø = 0°	35	–	–	Notes 1 & 2
Contrast	C	θ = 25°, Ø = 0°	5	8	–	Note 3
Response time (rise)	t_{on}	θ = 0°, Ø = 0°	–	40 ms	80 ms	Note 4
Response time (fall)	t_{off}	θ = 0°, Ø = 0°	–	120 ms	160 ms	Note 4

1.7.2 New TN LCD module (Gray)

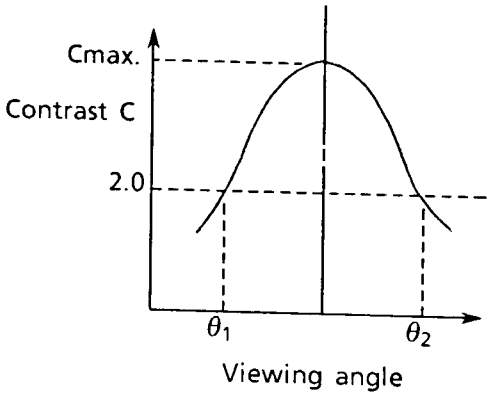
Viewing angle: 6 o'clock (Ø = 0°), Ta = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Reference
Viewing angle	$\theta_2 - \theta_1$	$C \geqq 2.0$, Ø = 0°	70	–	–	Notes 1 & 2
Contrast	C	θ = 25°, Ø = 0°	2	4	–	Note 3
Response time (rise)	t_{on}	θ = 0°, Ø = 0°	–	270 ms	400 ms	Note 4
Response time (fall)	t_{off}	θ = 0°, Ø = 0°	–	60 ms	100 ms	Note 4

Note 1: Definition of angles ø and θ

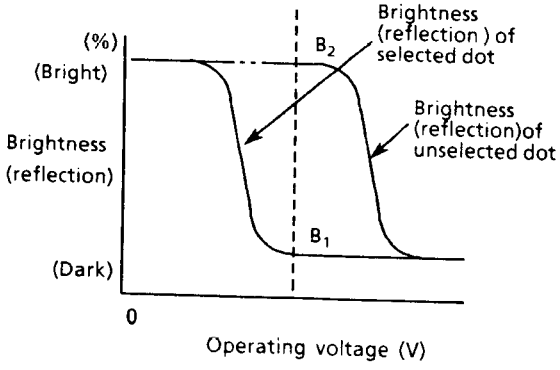


Note 2: Definition of viewing angles θ_1 and θ_2

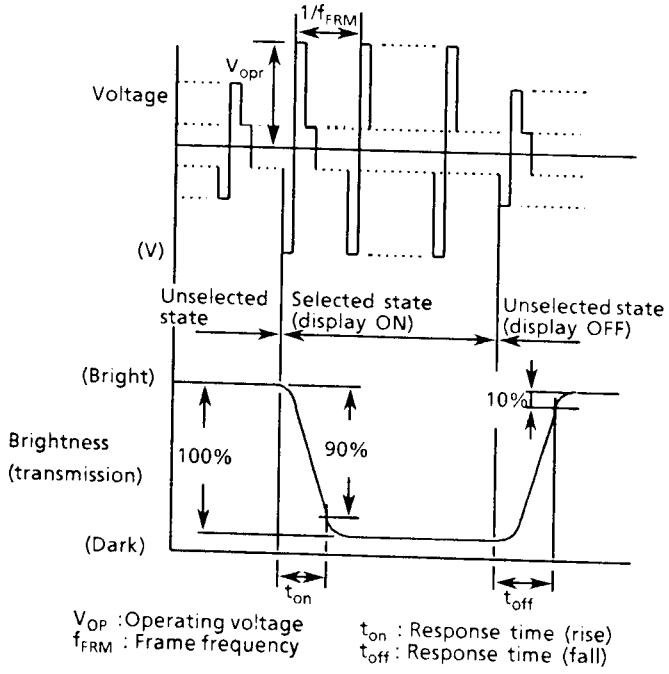


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

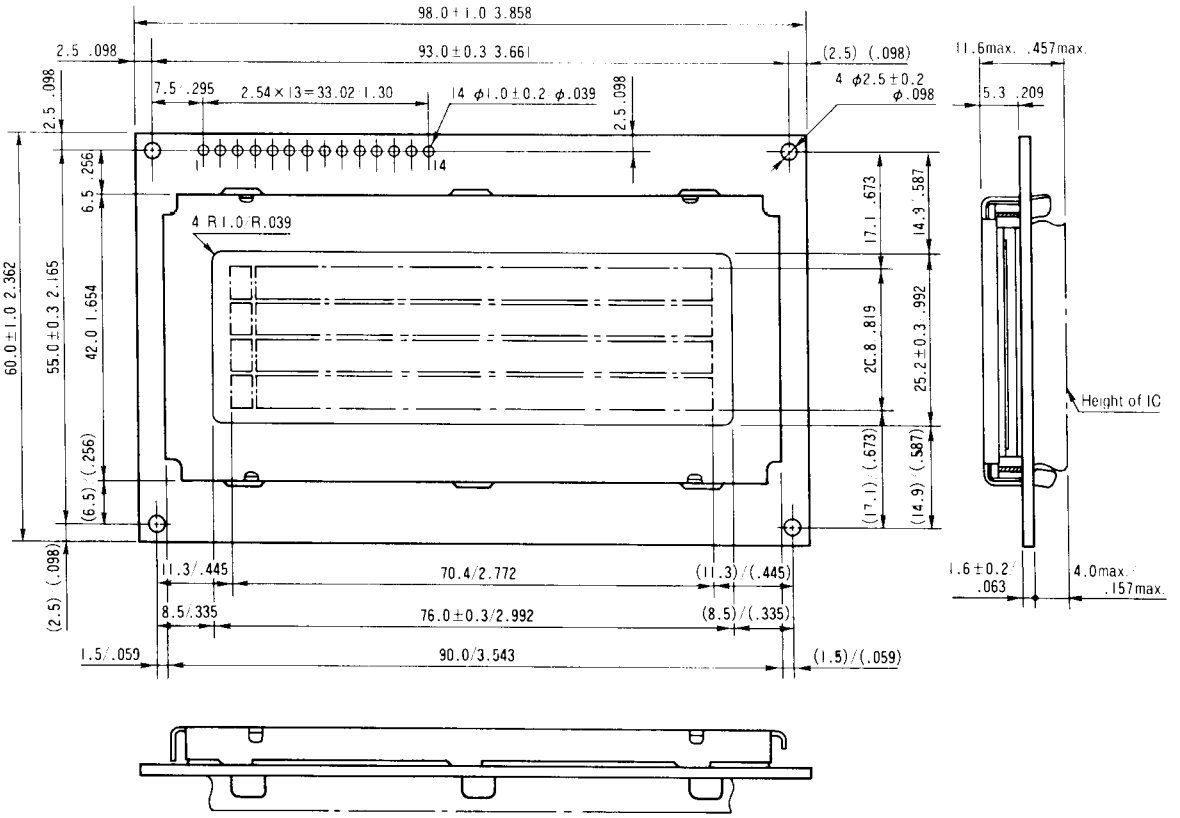


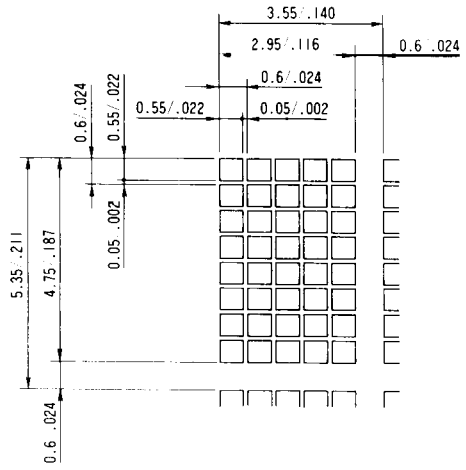
Note 4: Definition of response time



V_{OP} :Operating voltage
f_{FRM} : Frame frequency
t_{on} : Response time (rise)
t_{off} : Response time (fall)

1.8 Dimensions





Unit : mm/inch
General tolerance : ±0.5 mm

I/O terminal symbol

No.	Symbol
1	V_{SS}
2	V_{DD}
3	V_{LC}
4	RS
5	R/$\overline{W}$
6	E
7	DB_0
8	DB_1
9	DB_2
10	DB_3
11	DB_4
12	DB_5
13	DB_6
14	DB_7

Figure 4

2. OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB_0 to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_4 to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/$\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

2.2 Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	R/$\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and R/$\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

2.2.3 Address counter (AC)

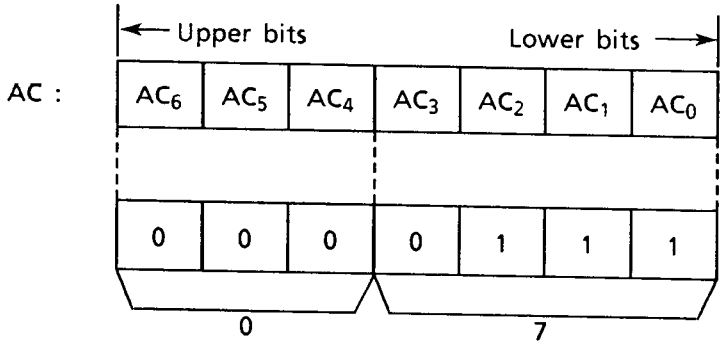
The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and R/$\overline{W}$ = 1.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



When display is not shifted, DD RAM addresses 00_H to 13_H are set in the line 1, 40_H to 53_H in the line 2, 14_H to 27_H in the line 3, and 54_H to 67_H in the line 4. Therefore, the line 1 end address and line 3 start address are consecutive, and the line 2 end address and line 4 start address are consecutive.

	1	2	3	4	5	6	- - -	15	16	17	18	19	20	Display digit
Line 1	00	01	02	03	04	05	- - -	0E	0F	10	11	12	13	DD RAM address
Line 2	40	41	42	43	44	45	- - -	4E	4F	50	51	52	53	
Line 3	14	15	16	17	18	19	- - -	22	23	24	25	26	27	
Line 4	54	55	56	57	58	59	- - -	62	63	64	65	66	67	

When display is shifted, DD RAM addresses 00_H to 27_H are displayed in the line 1 and in the line 3. DD RAM addresses 40_H to 67_H are displayed in the line 2 and in the line 4. The following figures are examples of display shifts.

Left shift

	1	2	3	4	5	6	- - -	15	16	17	18	19	20	Display digit
Line 1	01	02	03	04	05	06	- - -	0F	10	11	12	13	14	DD RAM address
Line 2	41	42	43	44	45	46	- - -	4F	50	51	52	53	54	
Line 3	15	16	17	18	19	1A	- - -	23	24	25	26	27	00	
Line 4	55	56	57	58	59	5A	- - -	63	64	65	66	67	40	

Right shift

	1	2	3	4	5	6	- - -	15	16	17	18	19	20	Display digit
Line 1	27	00	01	02	03	04	- - -	0D	0E	0F	10	11	12	DD RAM address
Line 2	67	40	41	42	43	44	- - -	4D	4E	4F	50	51	52	
Line 3	13	14	15	16	17	18	- - -	21	22	23	24	25	26	
Line 4	53	54	55	56	57	58	- - -	61	62	63	64	65	66	

2.2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

2.2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

Lower 4 bits \ Upper 4 bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)												
××××0001	(2)												
××××0010	(3)												
××××0011	(4)												
××××0100	(5)												
××××0101	(6)												
××××0110	(7)												
××××0111	(8)												
××××1000	(1)												
××××1001	(2)												
××××1010	(3)												
××××1011	(4)												
××××1100	(5)												
××××1101	(6)												
××××1110	(7)												
××××1111	(8)												

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data)	CG RAM address		Character pattern (CG RAM data)
7 6 5 4 3 2 1 0 ← Upper bit Lower bit →	5 4 3 ← Upper bit	2 1 0 Lower bit →	7 6 5 4 3 2 1 0 ← Upper bit Lower bit →
0 0 0 0 * 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * 0 0 0 0 0
0 0 0 0 * 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	* * * 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * 0 0 0 0 0
		0 0 0 0 0 1	* * *
0 0 0 0 * 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1	* * *

Example of character pattern (R)

← Cursor position

Example of character pattern (¥)

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.
- The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

2.3 Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time#
	RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
(1) Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
(4) Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
(6) Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), the duty ratio (N), and character fonts (F)	40 µs
(7) CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
(8) DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
(9) BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
(10) Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
(11) Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

* : Invalid bit
A_{CG} : CG RAM address
A_{DD} : DD RAM address
AC : Address counter

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

N = 1 : 1/16 duty
N = 0 : 1/8 or 1/11 duty

F = 1 : 5×10 dot matrix
F = 0 : 5×7 dot matrix

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

\# An execution time indicates maximum value when f_{osc} is 250 kHz. It changes at the inverse proportion of f_{osc}.

2.4 Instruction Details

(1) Display Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0). Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

(2) Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* : Don't care bit

Cursor Home returns cursor to home position (address 0).
DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

(3) Entry Mode Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

(4) Display ON/OFF Control

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

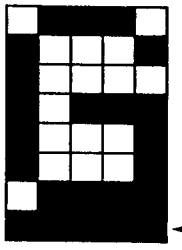
Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

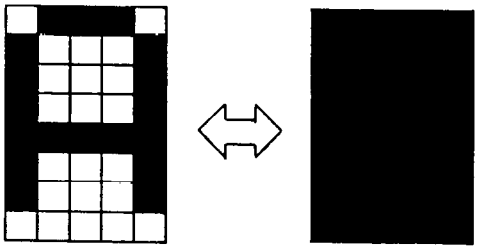
C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.
The cursor is displayed in the dot line below the character fonts.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.
For blinking, all-black dots and the character are switched about every 0.4 seconds when f_{osc} is 250 kHz. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display)



B = 1 (blinking)



(5) Cursor/Display Shift

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* : Don't care bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.
The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character by two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2.
Displays of lines 1, 2, 3 and 4 are shifted at the same time. The display pattern of line 1 or 3 is not shifted to line 2 or 4, and that of line 2 or 4 is not shifted to line 1 or 3. See 2.2.4 Display data RAM on page 10.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

Note: If only display shift is done, the AC contents do not change.

(6) Function Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* : Don't care bit

Function Set sets the interface data length, the duty ratio, and the character font.

DL : Interface data length
When DL = 1, the data length is set at eight bits (DB_7 to DB_0).
When DL = 0, the data length is set at four bits (DB_7 to DB_4).
The upper four bits are transferred first, then the lower four bits follow.

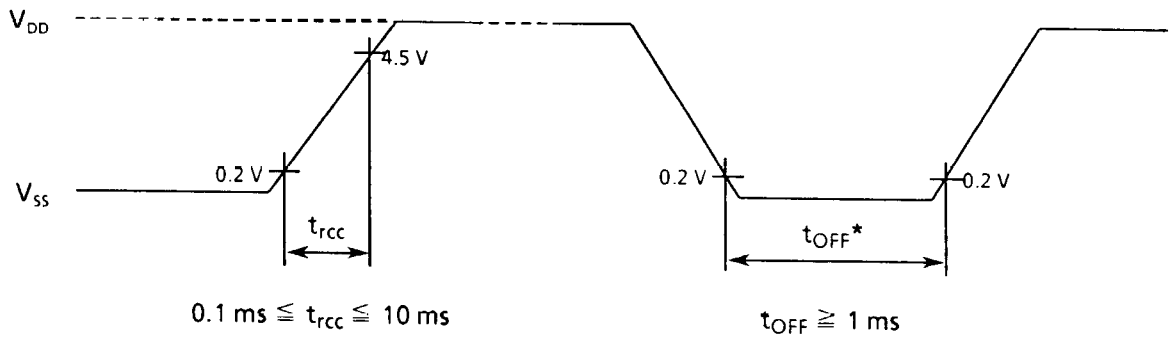
N : Duty ratio
When N = 1, the duty ratio is set to 1/16.
When N = 0, the duty ratio is set to 1/8 or 1/11.
For L2014, set N to 1.

F : Character font
When F = 1, the character font is set to 5×10 dot matrix.
When F = 0, the character font is set to 5×7 dot matrix.
If N is set to 1, F becomes "Don't care bit". For L2014, set F to 0 or 1.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

1. Automatic initialization
   The system is automatically initialized at power-on if the following power supply conditions are satisfied.



0.1 ms ≦ t_{rcc} ≦ 10 ms

t_{OFF} ≧ 1 ms

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

The following instructions are executed for initialization.

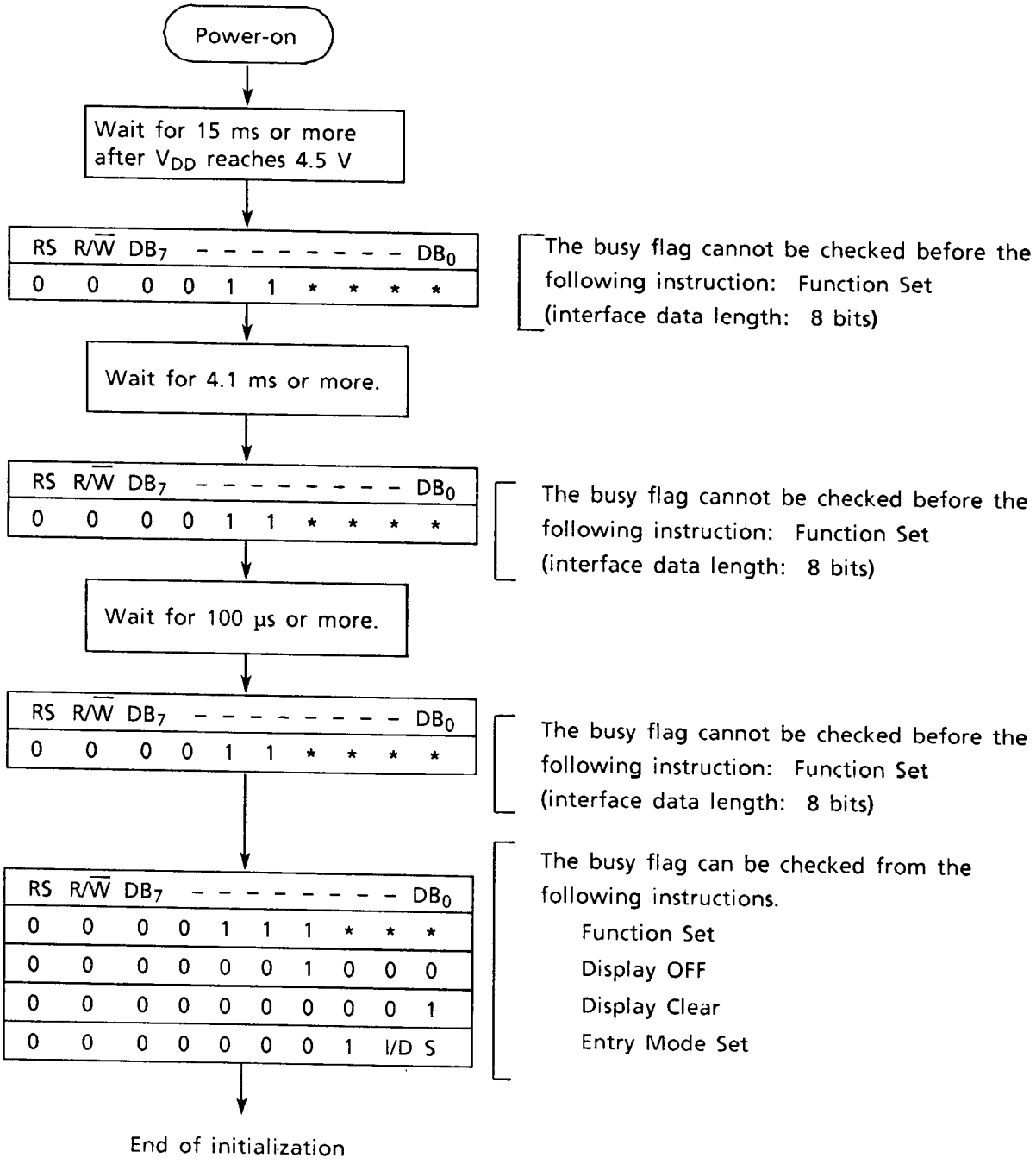
- Display Clear
- Function Set — DL = 1: Interface data length: Eight bits
  N=0: 1/8 duty
  F=0: Character font: 5×7 dot matrix
- Display ON/OFF Control — D = 0: Display OFF
  C = 0: Cursor OFF
  B = 0: Blink OFF
- Entry Mode Set — I/D = 1: Increment
  S = 0: No display shift

Since the condition is not suitable for the L2014, further Function Set instruction is necessary. See 2. 4. (6) Function Set on page 17.

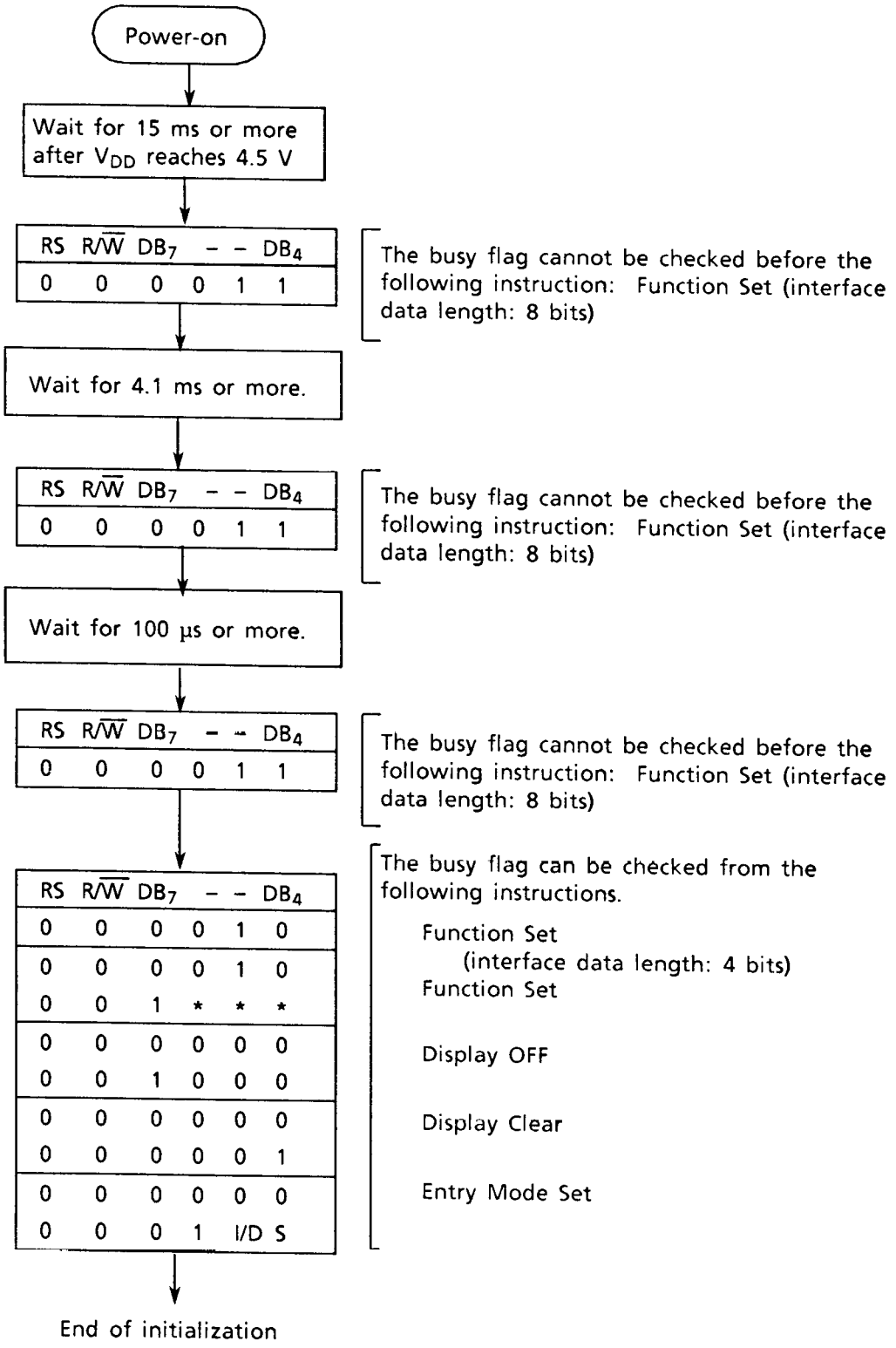
2. Initialization by instructions

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the following instructions. Since it is unknown whether the interface data length is set to eight bits or four bits at power on, execute Function Set twice to set the interface data length to eight bits. And then for setting the required interface data length execute further Function Set instruction.

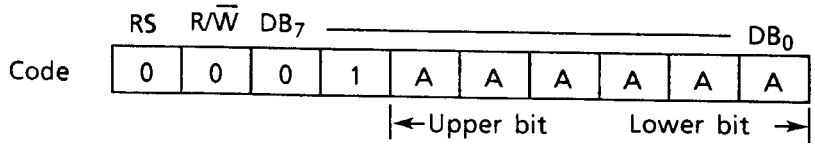
(a) Interface data length : Eight bits



(b) Interface data length: Four bits

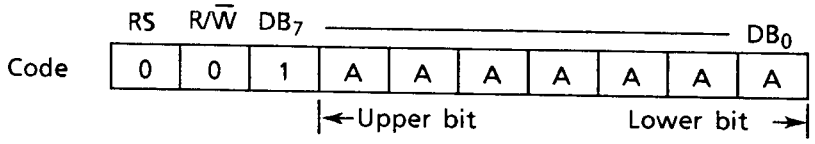


(7) CG RAM Address Set



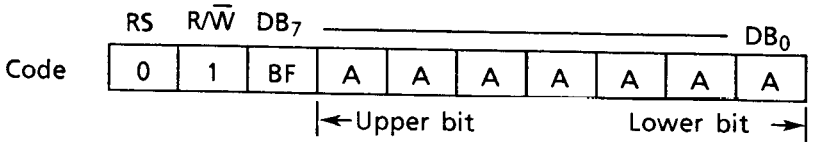
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

(8) DD RAM Address Set



DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 and line 3 (AAAAAAA) are 00_H to 27_H and those for line 2 and line 4 (AAAAAAA) are 40_H to 67_H.

(9) Busy Flag/Address Read



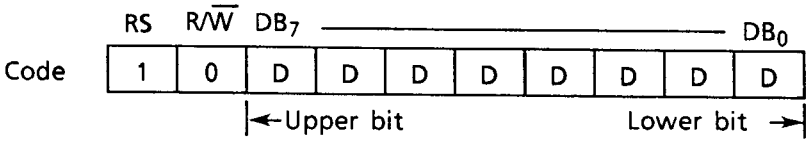
The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

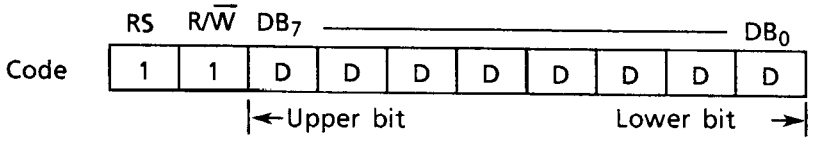
Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

(10) Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

(11) Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

2.5 Examples of Instruction Use

2.5.1 Interface data length: Eight bits

No.	Instruction	Display	Operation
1	Power-on RS: —, R/W: —, DB_7 —— DB_0: —		The built-in reset circuit initializes the module.
2	Function Set RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
3	Display ON/OFF Control RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
4	Entry Mode Set RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
5	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
6	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 0 0 1 1	LC_	C is written.
7	⋮	⋮	
8	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 1 0 0	LCD ----- L2014 _	4 is written in digit 20. Cursor appears at digit 1 of line 3.

No.	Instruction	Display	Operation
9	DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 1 0 0 0 0 0 0	LCD ------ L2014 _	RAM address is set so that the cursor is positioned at digit 1 of line 2.
10	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 1 0	LCD ------ L2014 2_	2 is written.
11	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 0 0	LCD ------ L2014 20_	0 is written.
12	⋮	⋮	
13	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 1 0 0 1 1	LCD ------ L2014 20 ----- 4 LINES _	S is written in digit 20. Cursor appears at digit 1 of line 4.
14	DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 0 0 1 0 1 0 0	LCD ------ L2014 20 ----- 4 LINES _	RAM address is set so that the cursor is positioned at digit 1 of line 3.
15	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 0 0 0	LCD ------ L2014 20 ----- 4 LINES H_	H is written.
16	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 0 0 1	LCD ------ L2014 20 ----- 4 LINES HI_	I is written.
17	⋮	⋮	

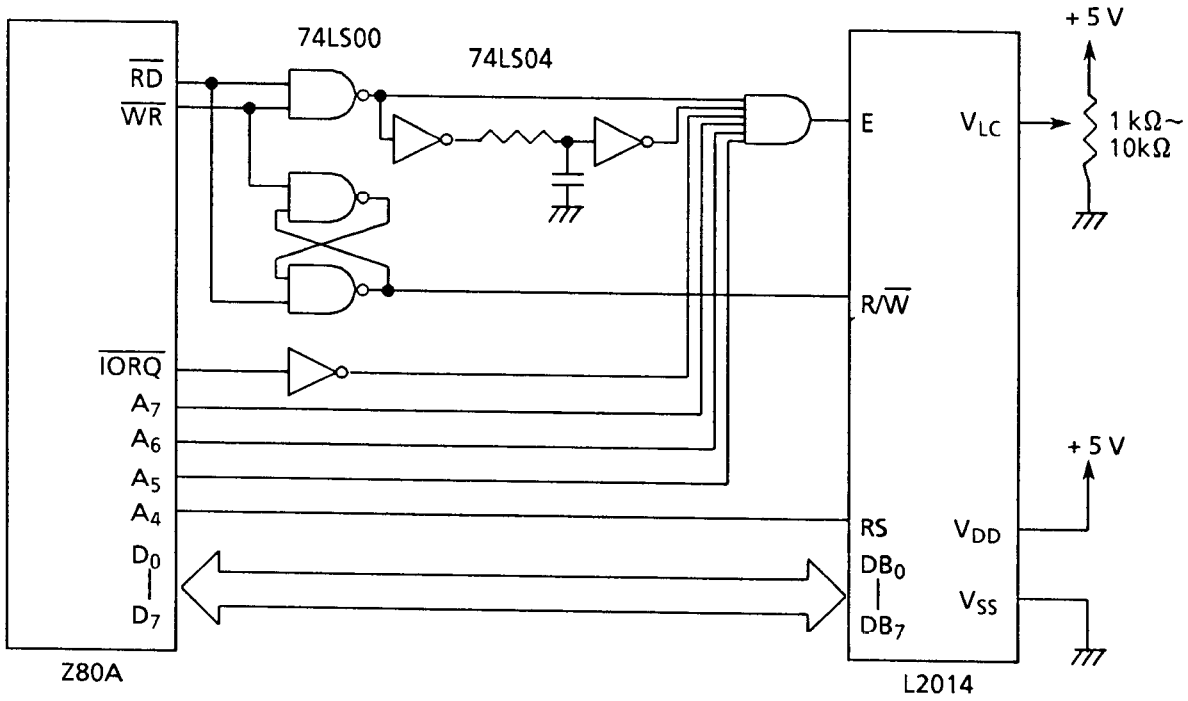
No.	Instruction	Display	Operation
18	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 1 0 1 0 0	LCD ------ L2014 20 ----- 4 LINES HIGH CONTRAST_	T is written.
19	DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 1 0 1 0 1 0 0	LCD ------ L2014 20 ----- 4 LINES HIGH CONTRAST _	RAM address is set so that the cursor is positioned at digit 1 of line 4.
20	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 1 0 1 1 1	LCD ------ L2014 20 ----- 4 LINES HIGH CONTRAST W_	W is written.
21	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 0 0 1	LCD ------ L2014 20 ----- 4 LINES HIGH CONTRAST WI_	I is written.
22	⋮	⋮	
23	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 0 1 0 1	LCD ------ L2014 20 ----- 4 LINES HIGH CONTRAST WIDE --- ANGLE_	E is written.
24	DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 0 0 0 0 0 0 0	LCD ------ L2014 20 ----- 4 LINES HIGH CONTRAST WIDE --- ANGLE	The cursor returns to the home position.
25	Display clear RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
26	⋮	⋮	

2.5.2 Interface data length: Four bits

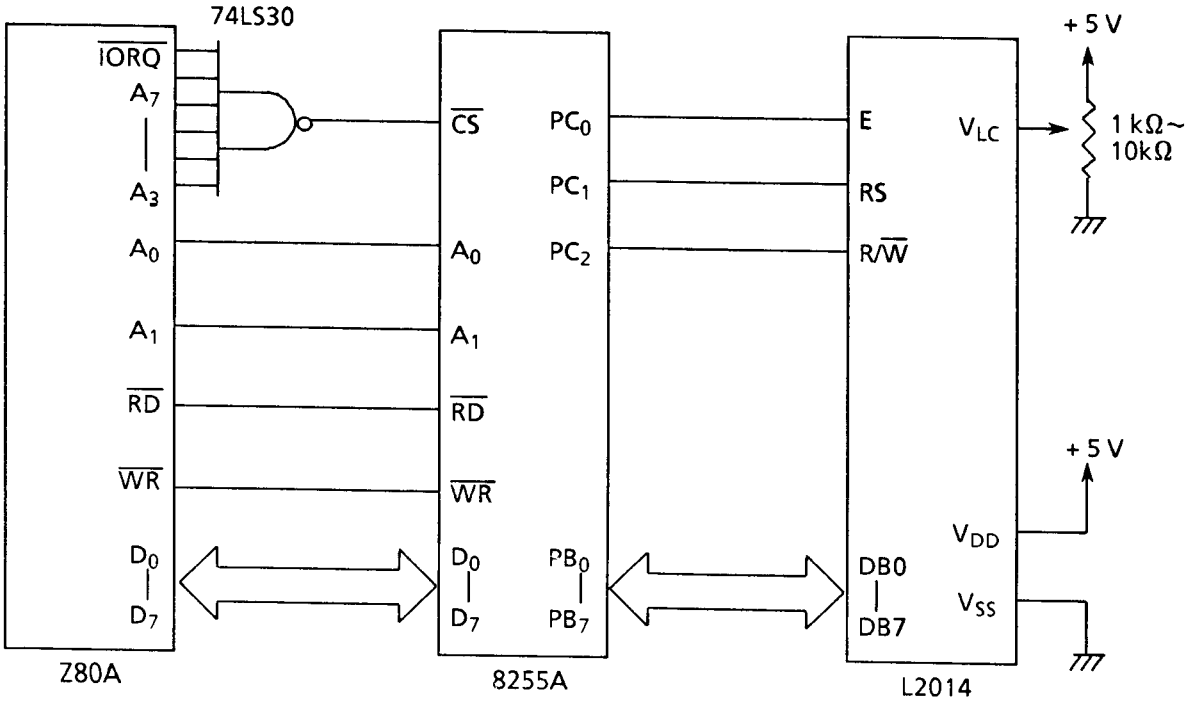
No.	Instruction	Display	Operation
1	Power-on RS | R/W | DB7 — DB4		The built-in reset circuit initializes the module.
2	Function Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 1 0		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
3	Function Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 1 0 0 | 0 | 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
4	Display ON/OFF Control RS | R/W | DB7 — DB4 0 | 0 | 0 0 0 0 0 | 0 | 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
5	Entry Mode Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 0 0 0 | 0 | 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
6	Write to CG RAM or DD RAM RS | R/W | DB7 — DB4 1 | 0 | 0 1 0 0 1 | 0 | 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
7	⋮	⋮	

2.6 MPU Connection Diagrams

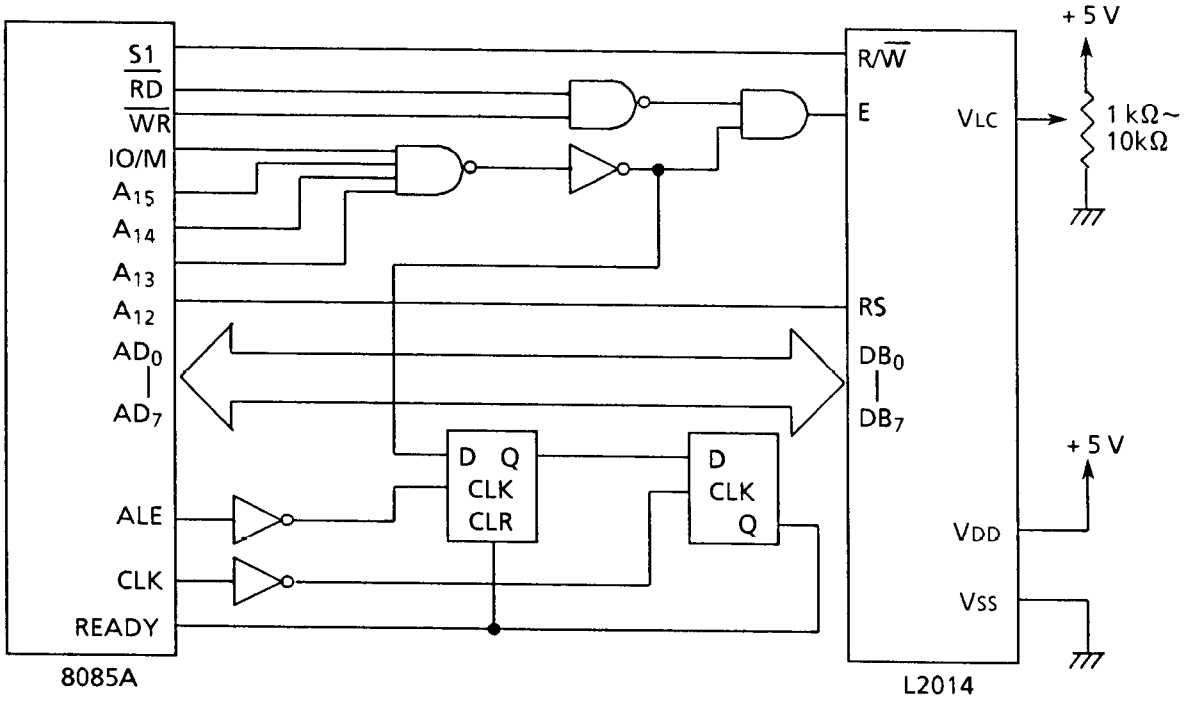
2.6.1 Z80A



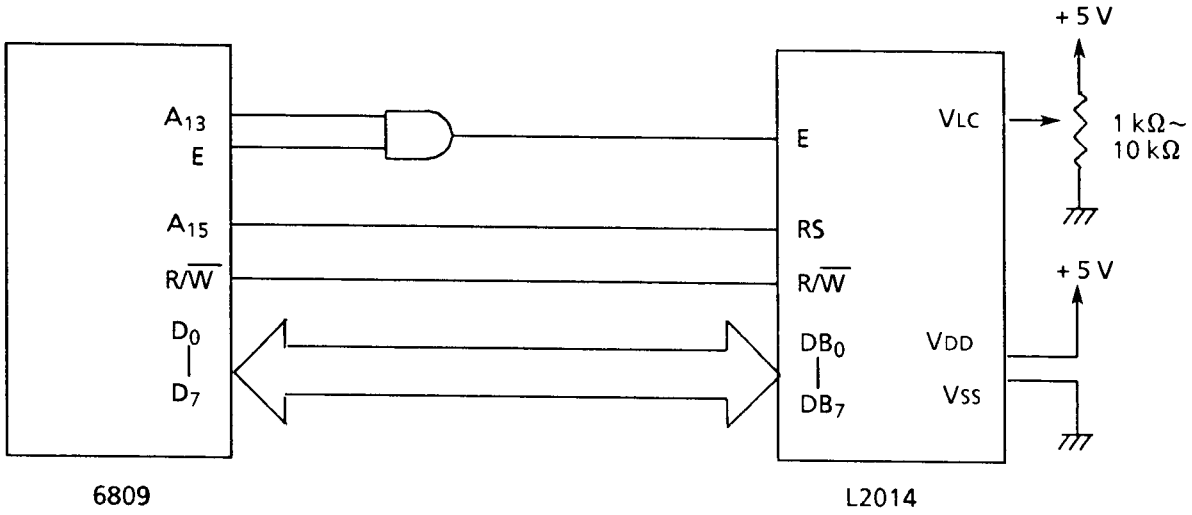
2.6.2 Z80A and 8255A



2.6.3 8085A



2.6.4 6809



3.NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

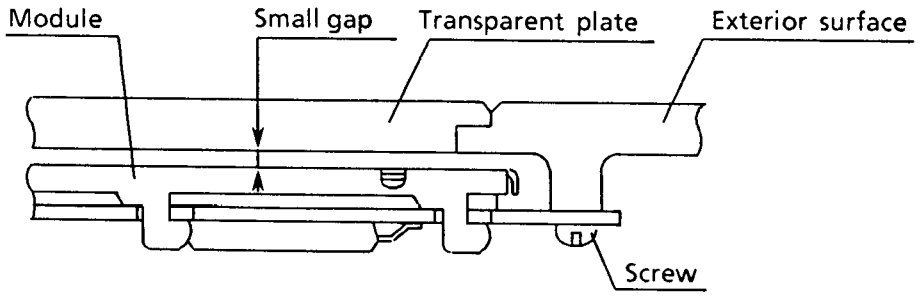
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizer of the display is very fragile; handle it very carefully.

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- Connect a 10-μF capacitor between the power supply terminals to eliminate noise.
- To protect the module from external pressure, place a transparent plates (e.g. acrylic or glass), leaving a small gap, over the display surface, frame, and polarizer.

☆Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- To store the module for a long time, a dark place where the temperature is 25°C ±10°C and the humidity below 65% RH is recommendable.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

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