64Mbit IoT RAM

64Mbit SQPI PSRAM Data Sheet

Version 0.71

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2 Introduction

This document defines “64Mbit IoT RAM”, which is 64 Mbit of SPI/QPI (serial/quad parallel interface) Pseudo−SRAM device. This RAM is configurable as 1 bit Input and Output separate or 4 bit I/O common interface.

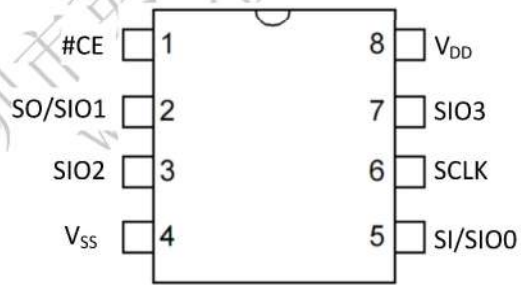
The Linear Burst can cross page boundary within tCEM(max.) . 32 bytes wrap burst mode is also available. The linear and wrap burst mode is selectable by "Burst mode toggle command”.

This device also has Pseudo-SRAM features. All of necessary Refresh operation is taken care by device itself.

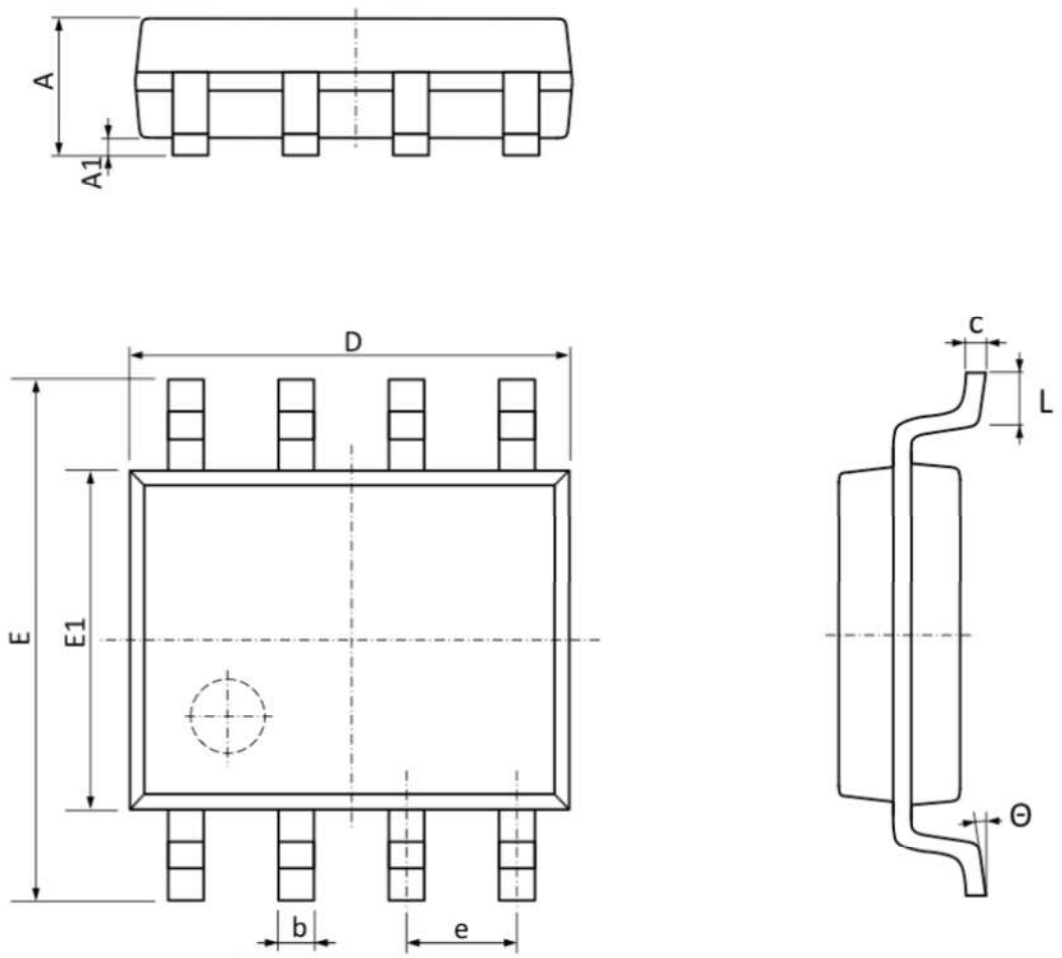
3 Package Information

The IPS6404L−SQ is available in standard package in 8−lead SOP−8 (150mil)

SOP 8(150mil) pin order



4 Package Dimension SOP8 (150mil)



unit : mm (except Θ)

Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.15	0.25
D	4.75	5.05
E1	3.80	4.00
E	5.80	6.20
e	1.27(TYP.)	
L	0.40	0.80
Θ	0°	8°

5 Ordering Information

Table 1 : Ordering information

Ordering Part number	Operational Voltage	Maximum Frequency	Temperature Range	Minimum Order Quantity
IPS6404L-SQ-SPN	2.7V ~ 3.6V	104Mhz	-25°C to +85°C	4Kunits
IPS6404L-SQL-SPN	1.62V ~ 1.98V	133Mhz		

6 Signal description

Table 2 : Signal description

Symbol	Signal Type	SPI Mode	QPI Mode
VDD	Power	Core Power Supply	
VSS	Ground	Core Supply Ground	
CE#	Input	Chip select signal, Active Low. When CE# input is High, memory will be in Standby state	
CLK	Input	Clock Signal	
SI/SIO[0]	I/O	Serial Input	I/O[0]
SO/SIO[1]	I/O	Serial Output	I/O[1]
SIO[3:2]	I/O	(I/O[3:2]*)	I/O[3:2]

*: Fast read Quad access and Quad Write access in SPI Mode use SIO[3:2].
Recommend to pull down to GND if no use of SIO[3:2] in SPI mode.

7 Power up initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at or above minimum VDD, the device will require 150µs to complete its self-initialization process. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track VDD within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the 150µs period the device requires initialization command sequence as it's shown in Figure 2, and then the device is ready for normal operation.

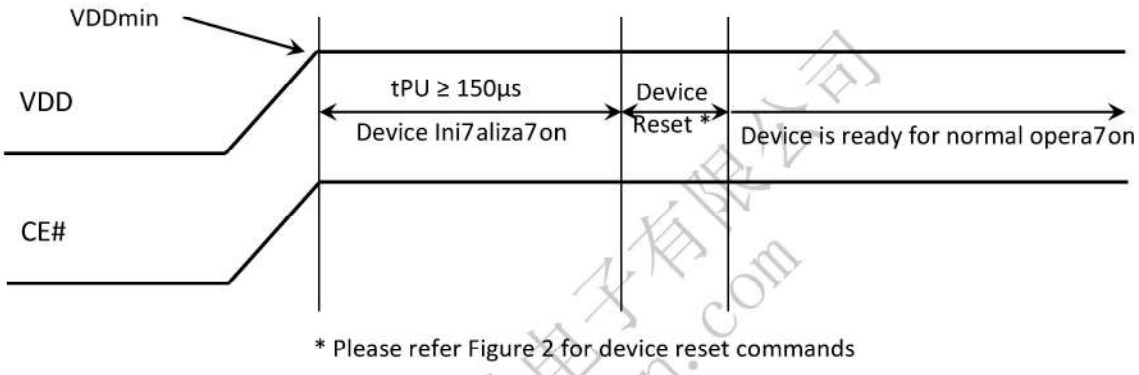


Figure 1 : Power-Up Initialization Timing

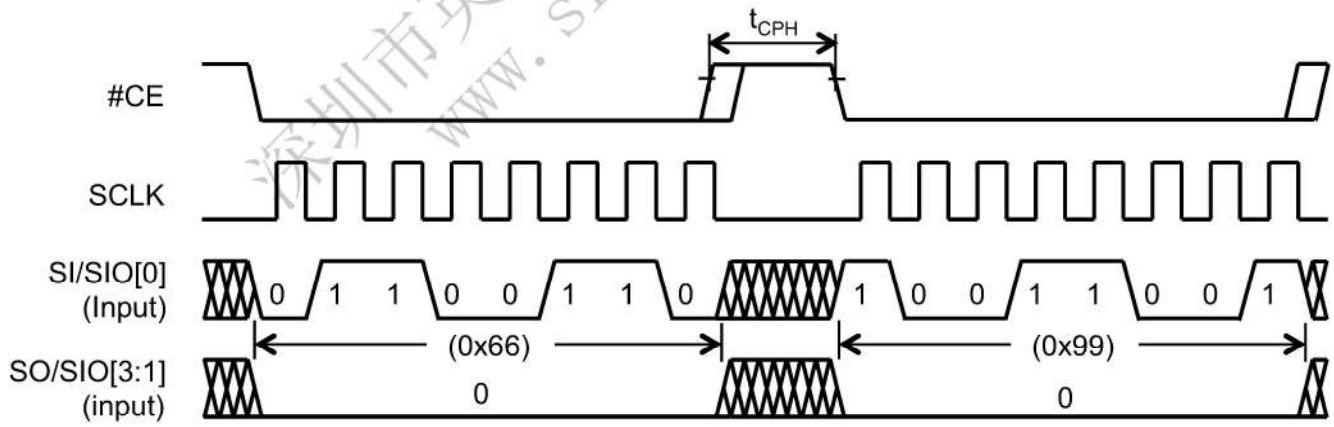


Figure 2 : Reset command sequence for Device Initialization

8 Interface Description

8.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 64M device is addressed with A[22:0].

8.2 Page Length

The page size is 1K Bytes. Read and write operations are always linear address space. The Linear Burst can cross page boundary under following conditions.

- Operative Clock frequency ≤ 84Mhz
- CE# low pulse width ≤ tCEM(max.)

The wrap 32 burst mode can be set by "Burst mode toggle commend" optionally. There is no page boundary crossing function supported on wrap 32 burst mode.

8.3 Drive Strength

The device powers up in 50Ω.

8.4 Power-on Status

The device powers up in SPI Mode.

It is required to have CE# high before beginning any operations.

8.5 Command/Address Latching Truth

The device recognizes the following commands specified by the various input methods

		SPI Mode					QPI Mode				
Command	Code	Cmd	Addr	Wait Cycle	DIO	Max Freq.	Cmd	Addr	Wait Cycle	DIO	Max Freq.
Read	0x03	S	S	0	S	33	N.A.				
Fast Read	0x0B	S	S	8	S	*84/133(104)	N.A.				
Fast Read Quad	0xEB	S	Q	6	Q	*84/133(104)	Q	Q	6	Q	*84/133(104)
Write	0x02	S	S	0	S	*84/133(104)	Q	Q	0	Q	*84/133(104
Quad Write	0x38	S	Q	0	Q	*84/133(104)	same as 0x02				
Enter Quad Mode	0x35	S	-	-	-	133(104)	N.A.				
Exit Quad Mode	0xF5	N.A.					Q	-	-	-	133(104)
Reset Enable	0x66	S	-	-	-	133(104)	Q	-	-	-	133(104)
Reset	0x99	S	-	-	-	133(104)	Q	-	-	-	133(104)
Burst mode toggle	0xC0	S	-	-	-	133(104)	Q	-	-	-	133(104)
Read ID	0x9F	S	S	0	S	133(104)	N/A				

Remark: S = Serial IO, Q = Quad IO, 133(104) = 133Mhz @ 1.8V and 104Mhz @ 3.3V

*Note: 84Mhz is maximum operative clock frequency allows to across the page boundary access.

8.6 Command termination

All Reads & Writes must be completed by raising CE# LOW to HIGH immediately afterwards in order to terminate the active command and set the device in to standby.

Not doing so will block internal refresh operations and leads to memory failure.

Command termination operation is necessary not only for Reads & Write operation and also any command operation, such as Enter Quad mode command and Reset commands.

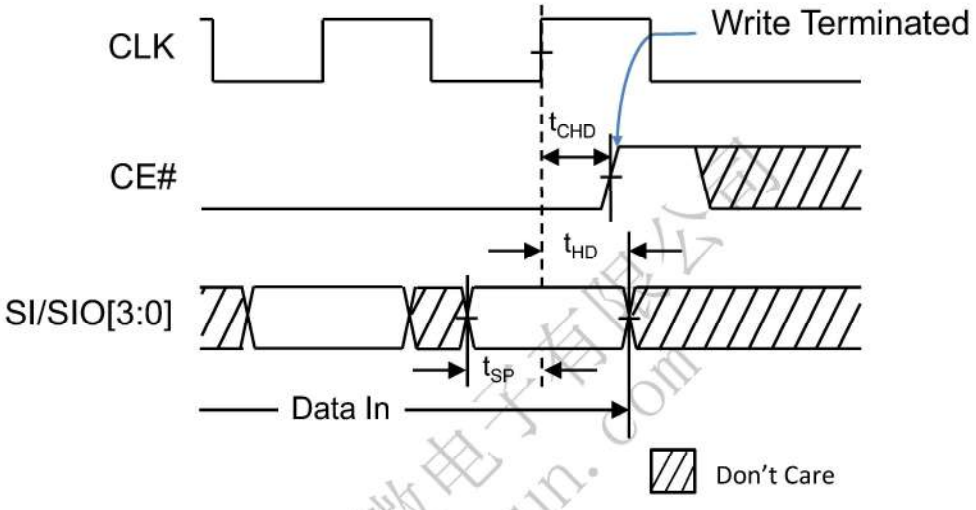


Figure 3 : Write Command Termination

For a memory controller to correctly latch the last piece of the data to read termination, it is recommended to provide a longer CE# hold time (tCHD > tACLK+ tCLK) for a sufficient data window.

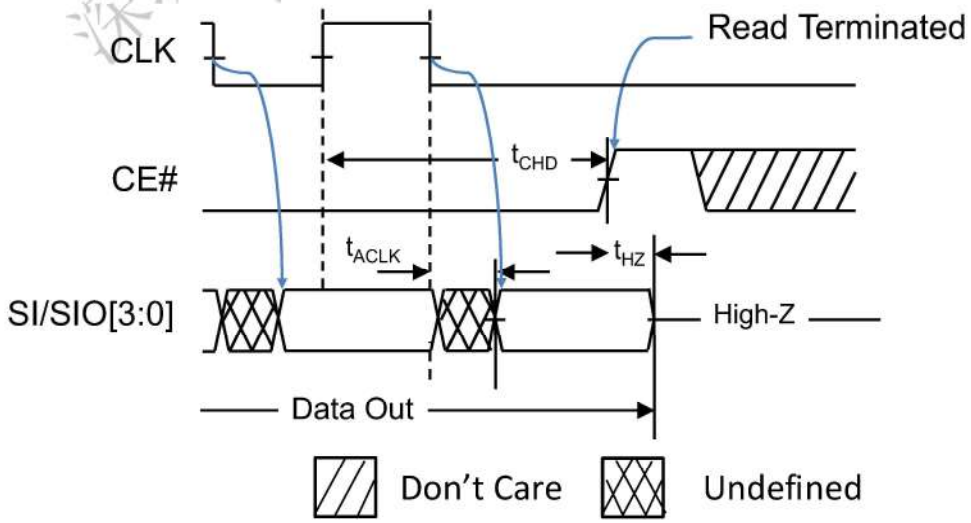


Figure 4 : Read Command Termination

9 Linear and Wrap "Burst mode toggle command" operation

The device allows linear burst operation to burst through page boundary (Page boundary is 1Kbyte page size) within tCEM(Max.). In this linear mode, the memory page boundary becomes invisible to the memory controller and runs maximum CLK frequency up to 84Mhz. Default setting is Linear Burst mode.

The 32 Bytes Wrap burst mode is also available for a certain application.

This Burst mode toggle command switches the device's burst mode operation between Linear burst mode and Wrap burst mode.

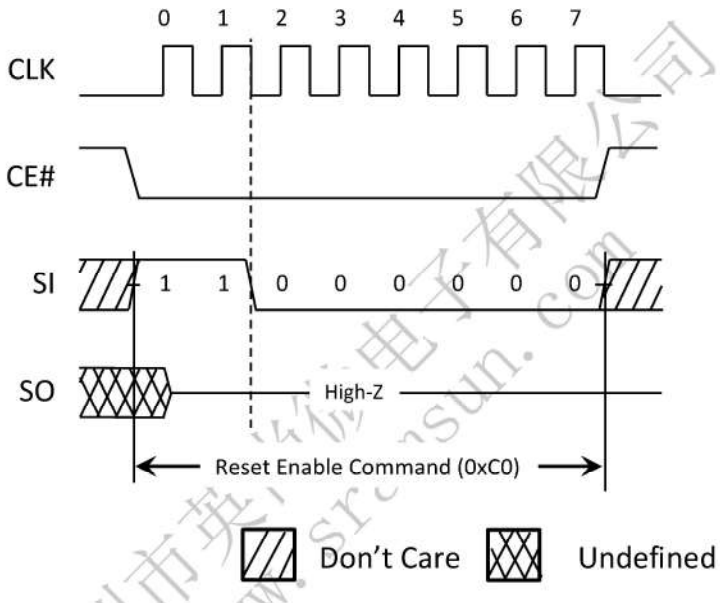


Figure 5 : SPI Burst Mode toggle command "0xC0"

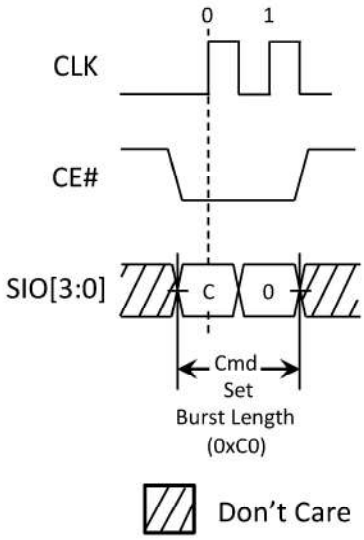


Figure 6 : QSPI Burst Mode toggle command "0xC0"

10 SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

10.1 SPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

SPI Reads can be done in three ways:

1. 0x03: Serial CMD, Serial IO, slow frequency
2. 0x0B: Serial CMD, Serial IO, fast frequency
3. 0xEB: Serial CMD, Quad IO, fast frequency

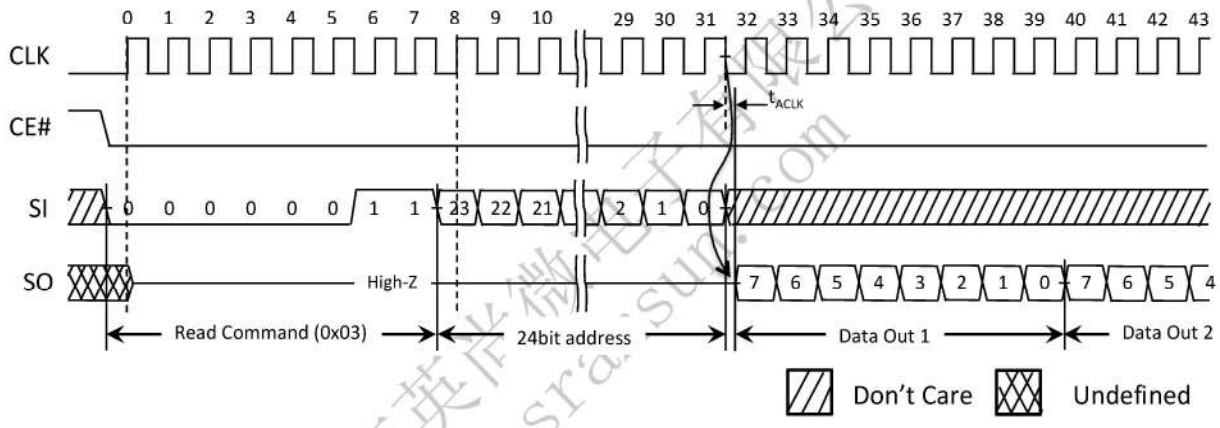


Figure 7 : SPI Read 0x03 (max frequency @ 33MHz)

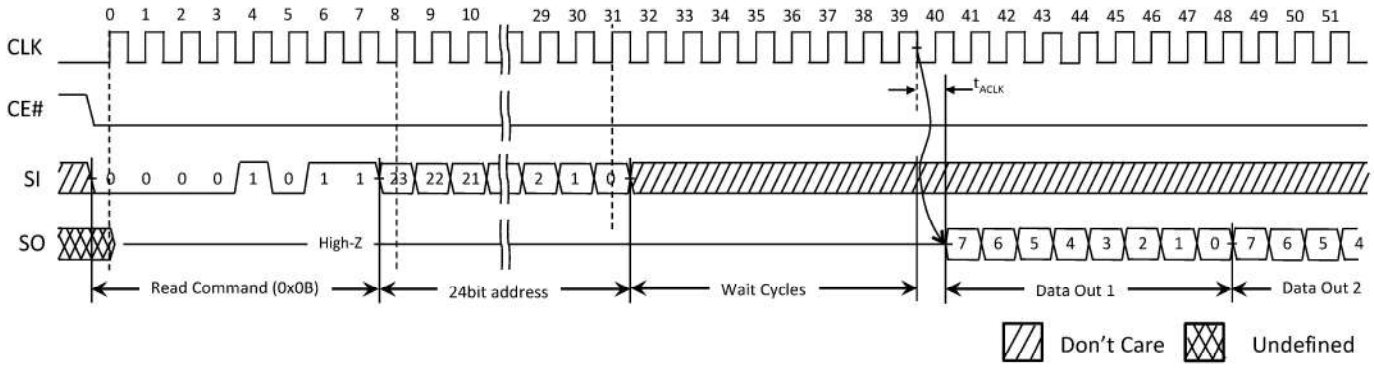


Figure 8 : SPI Read 0x0B (max frequency @ *104/133MHz) ***84Mhz for Page Boundary Crossing**

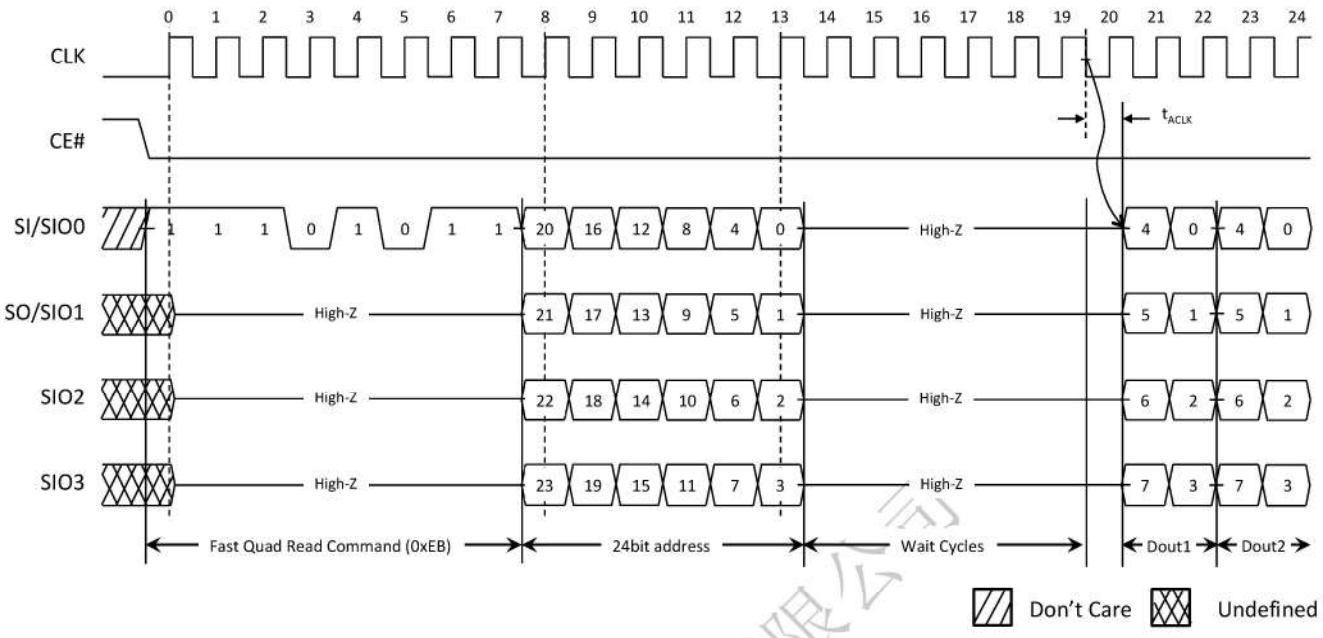


Figure 9 : SPI Fast Quad Read 0xEB (max frequency @ *104/133MHz) *84Mhz for Page Boundary Crossing

10.2 SPI Write Operations

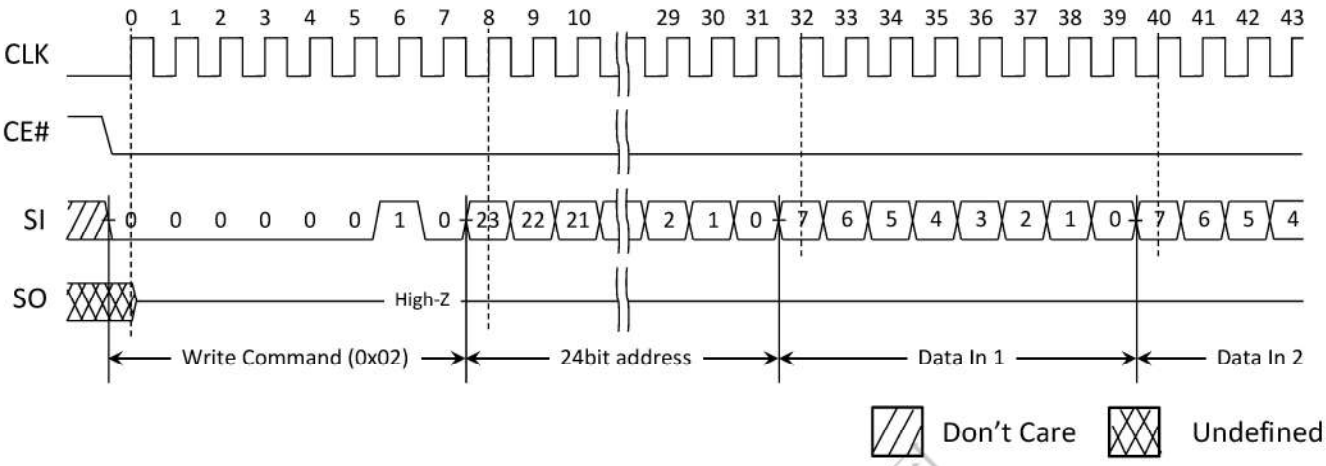


Figure 10 : SPI Write 0x02(max frequency @ *104/133MHz) *84Mhz for Page Boundary Crossing

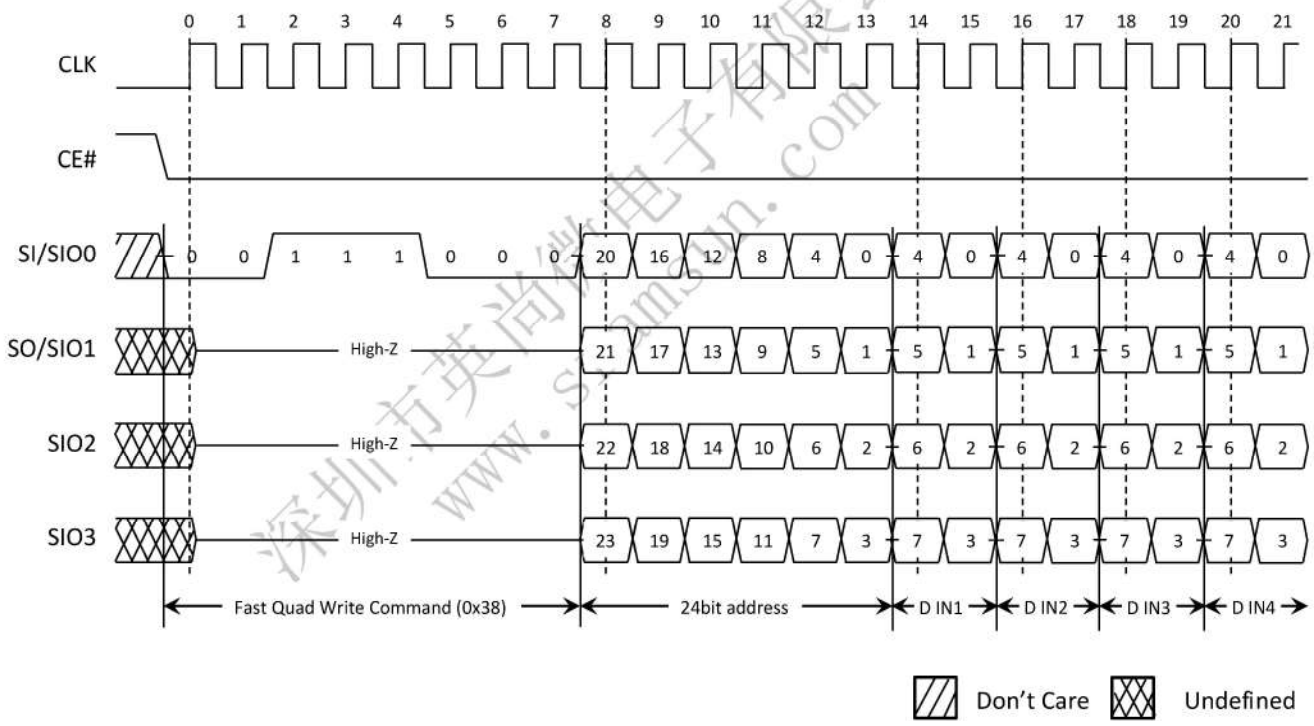


Figure 11 : SPI Write 0x38(max frequency @ *104/133MHz) *84Mhz for Page Boundary Crossing

10.3 SPI to QPI Mode Enable Operation

This command switches the device into QPI mode.

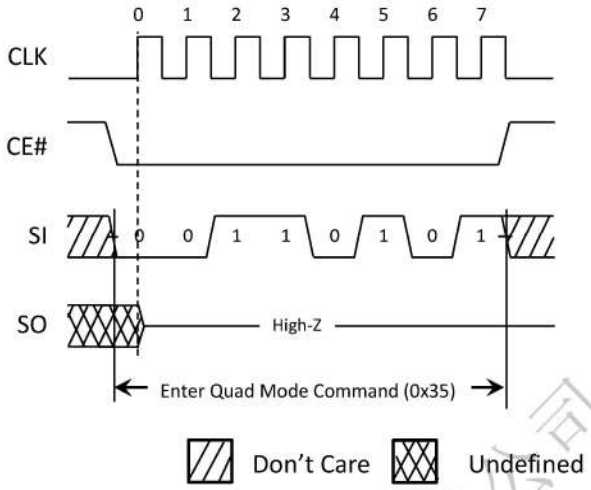


Figure 12 : Quad Mode Enable 0x35

10.4 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

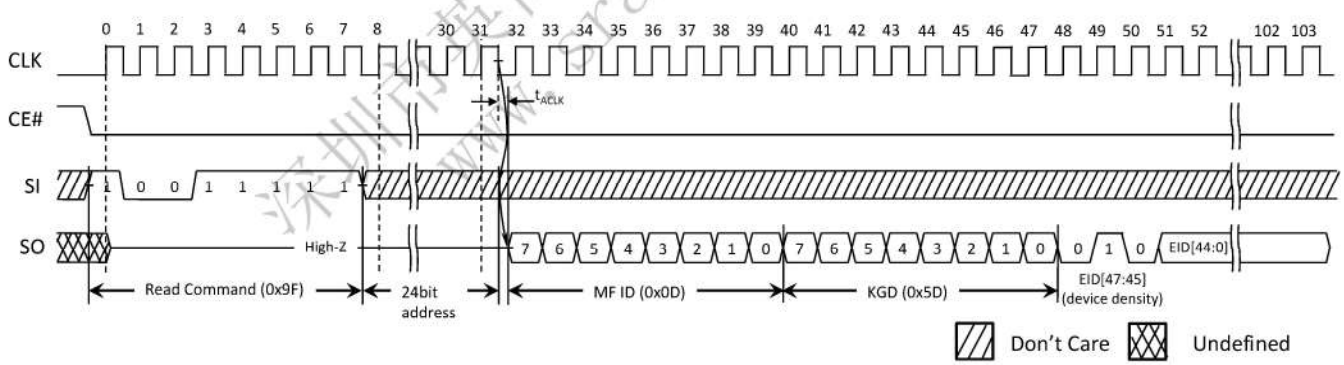


Figure 13 : SPI Read ID 0x9F (available only in SPI mode)

Table 3: Known Good Die (KGD)

KGD [7:0]	Known Good Die Register
0x5D	Pass
0x55	Fail

*Note: Default value on this register is (0x55=fail). After the all tests passed then programed as (0x5D= PASS) in manufacturing process.

11 QPI Mode Operations

11. 1 QPI Read Operations

For Fast Quad read (0xEB) , data will be available t_{ACLK} after the falling edge of CLK.

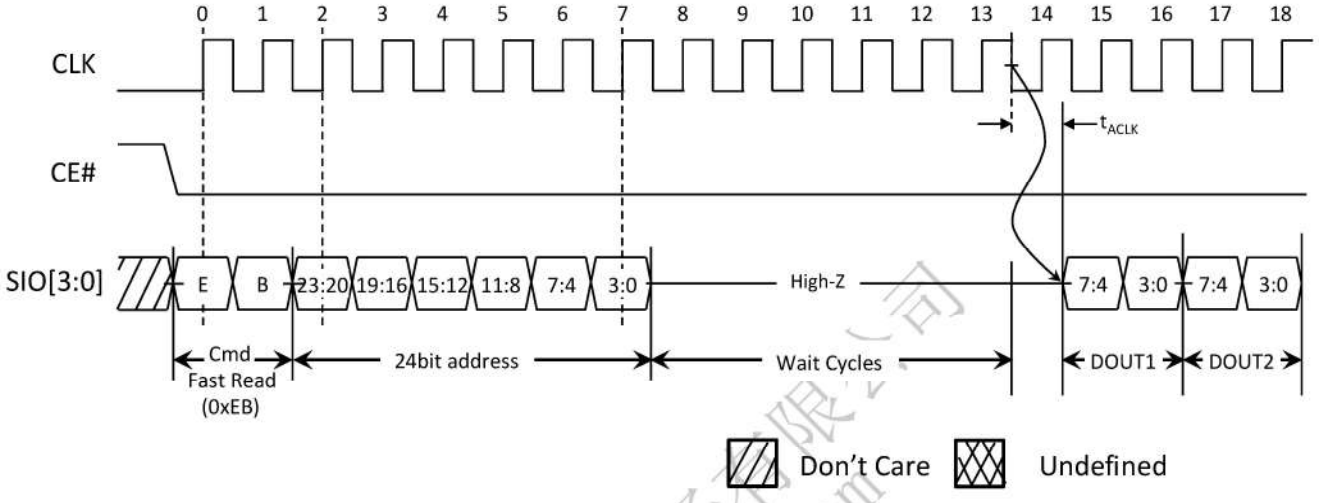


Figure 14 : QPI Fast Read 0xEB (max frequency *104/133MHz) ***84Mhz for Page Boundary Crossing**

11.2 QPI Write Operations

QPI write command can be input as 0x02 or 0x38. It does not matter Clock frequency.

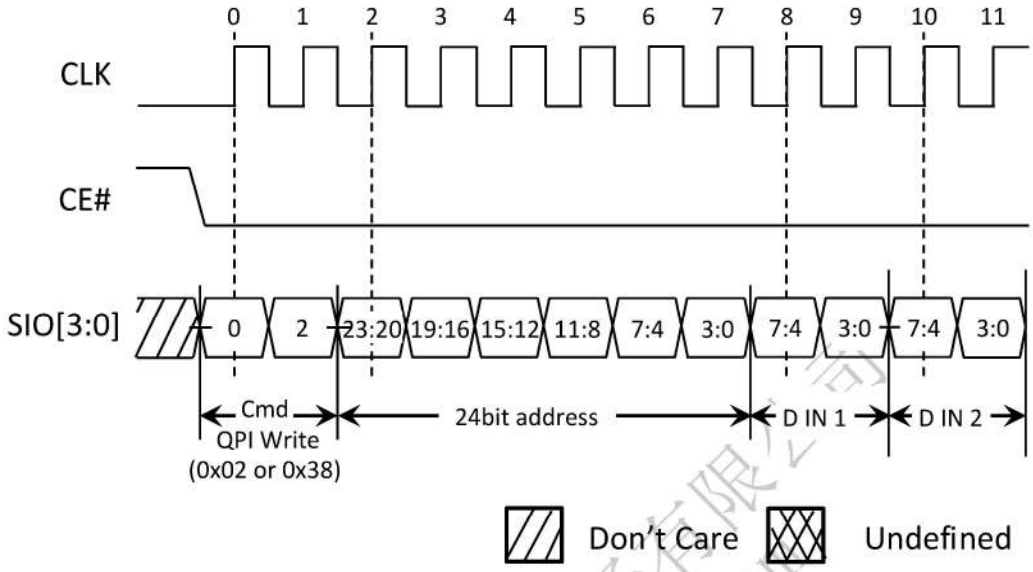


Figure 15 : QPI Write 0x02 or 0x38
(max frequency *104/133MHz) *84Mhz for Page Boundary Crossing

11.3 QPI Quad Mode Exit Operation

This command will switch the device back into SPI mode.

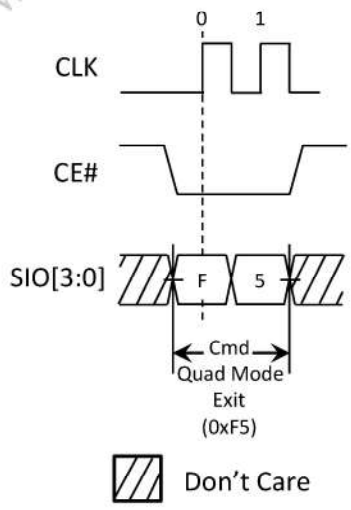


Figure 16 : Quad Mode Exit 0xF5 (Only available in QPI mode)

12 Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power up. This operation consists of two commands: Reset Enable (RSTEN) and Reset (RST).

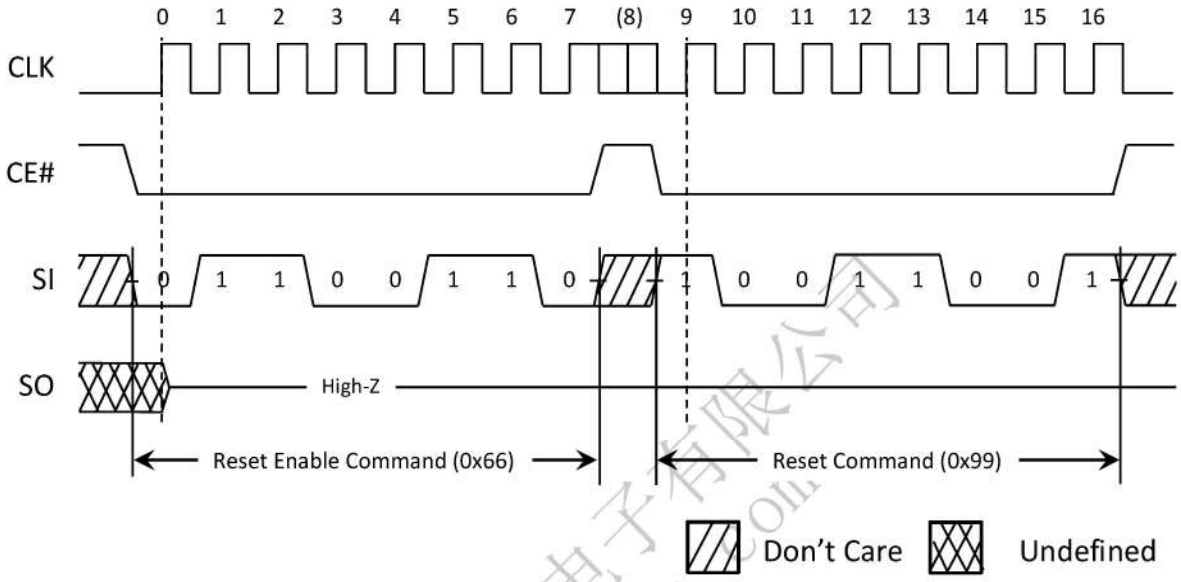


Figure 17 : SPI Reset

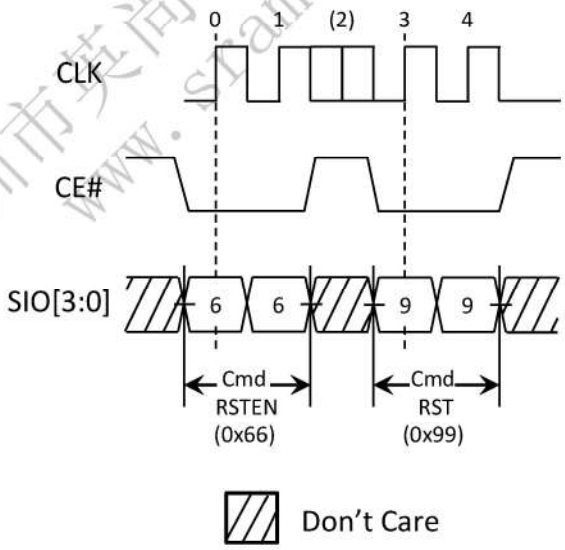


Figure 18 : QPI Reset

The Reset operation requires the Reset Enable command followed by the Reset command. Any command other than the Reset command after the Reset Enable command will disable the Reset Enable procedure.

13 Input / Output Timing

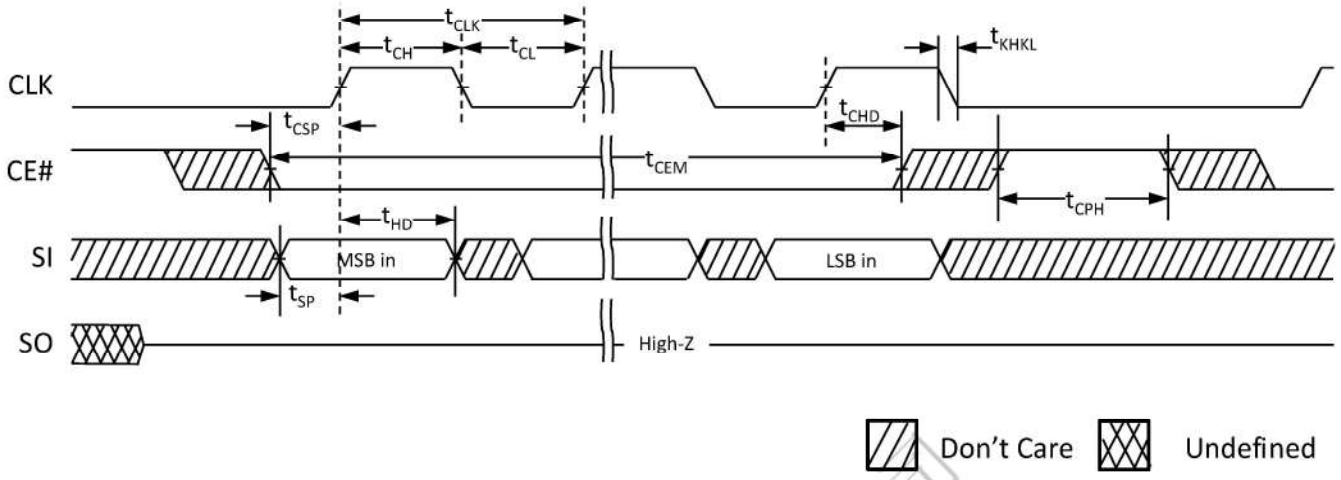


Figure 20: Input Timing

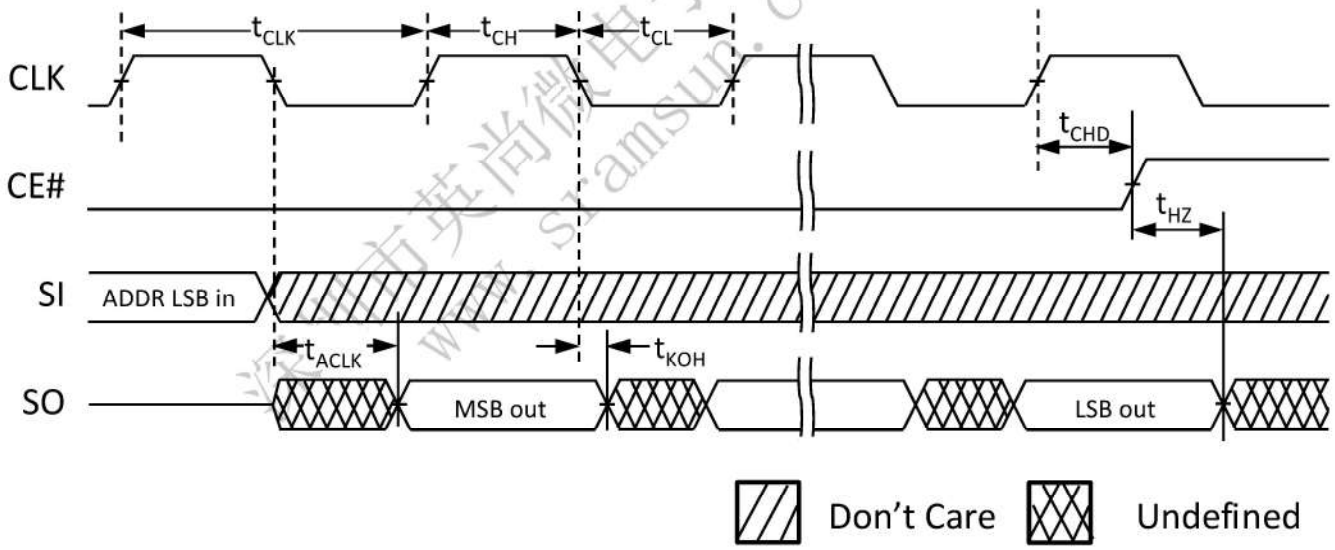


Figure 21: Output Timing

14 Electrical Specifications:

14.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit	Notes
Voltage to any ball except V_{DD} relative to V_{SS}		VT	−0.3 to V_{DD}+0.3	V	
Voltage on V_{DD} supply relative to V_{SS}	IPS6404L-SQ	V_{DD}	−0.2 to +4.10	V	
	IPS6404L-SQL		−0.2 to +2.45	V	
Storage Temperature		T_{STG}	−55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

14.2 Operating Conditions

Table 5: Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (standard)	-25	85	°C	

14.3 DC Characteristics

Table 6: DC Characteristics

Symbol	Parameter		Min	Max	Unit	Notes
VDD	Supply Voltage	IPS6404L-SQ	2.70	3.60	V	
		IPS6404L-SQL	1.62	1.98	V	
VIH	Input high voltage		VDD−0.4	VDD+0.2	V	
VIL	Input low voltage		−0.2	0.4	V	
VOH	Output high voltage (IOH=−0.2mA)		0.8 VDD		V	
VOL	Output low voltage (IOL=+0.2mA)			0.2 VDD	V	
ILI	Input leakage current			1	µA	
ILO	Output leakage current			1	µA	
ICC	Read/Write	IPS6404L-SQ		TBD	mA	
		IPS6404L-SQL		TBD	mA	
ISB	Standby current	IPS6404L-SQ		150	µA	
		IPS6404L-SQL		150	µA	

14.4 AC Characteristics

Table 7: READ/WRITE Timing

Symbol	Parameter	3.3V-104Mhz		1.8V-133Mhz		Unit	Notes
		Min	Max	Min	Max		
t_{CLK}	CLK period – SPI Read (0x03)	30.3		30.3		ns	33MHz
	CLK period – all other operations	9.6		7.5			104/133MHz
t_{CH}/t_{CL}	Clock high/low width	0.45	0.55	0.45	0.55	t_{CLK}	
t_{KHKL}	CLK rise or fall time		1.5		1.5	ns	
t_{CPH}	CE# HIGH between subsequent burst operations	18.0		18.0		ns	
t_{CEM}	CE# low pulse width		8		8	μs	
t_{CSP}	CE# setup time to CLK rising edge	3		2.5		ns	
t_{CHD}	CE# hold time from CLK rising edge	3		2.5			
t_{SP}	Setup time to active CLK edge	2.5		2.0		ns	
t_{HD}	Hold time from active CLK edge	2		2		ns	
t_{HZ}	Chip disable to DQ output high-Z		7		6	ns	
t_{ACLK}	CLK to output delay	2	7	2	6	ns	
t_{KOH}	Data hold time from clock falling edge	1.5		1.5		ns	

15 Version History

Version 0.1	Mar 15th, 2017	Initial Version
Version 0.2	April 14th, 2017	Update initialization command sequence Vdd range changed in to two product categories Update DC parameter table Correct Device ID value on Fig 9
Version 0.3	April 28th, 2017	Adding note on SIO[3:2] in SPI mode
Version 0.4	May 31st, 2017	Simplify ordering part number and update AC parameter by frequency. Add 84Mhz limitation for Page boundary crossing
Version 0.5	Jun 23rd, 2017	Add Read/write command termination figures Add Burst mode toggle command and figures Add tCHD in AC parameters table
Version 0.6	July 4th ,2017	Version for internal use
Version 0.7	July 12th, 2017	Correct Typo on Fig 4 Read command termination. Delete P.16 figure QPI Fast Read 0x0B (max 84Mhz). Revise tCPH (min.) = 9.6 ns to 18ns Correct total page number
Version 0.71	Sep 19th, 2017	Fix Absolute Maximum ratings