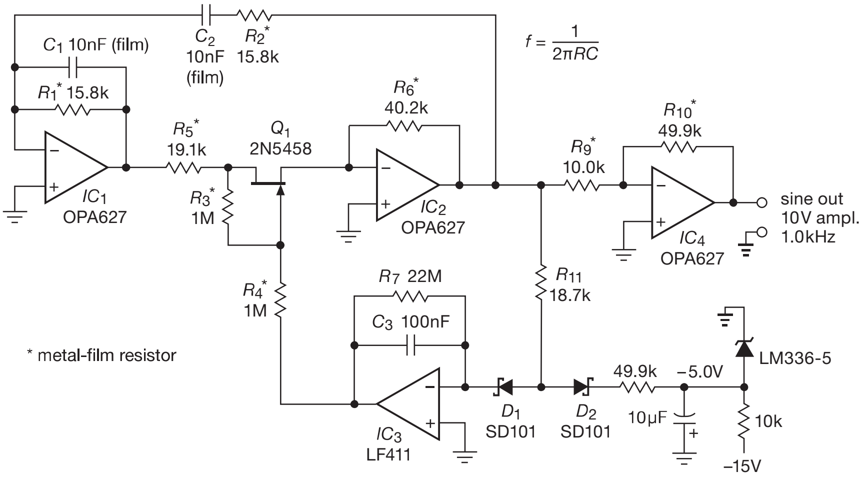

Figure 7.22. Wien-bridge (1 kHz) oscillator with unusually low distortion (<0.001%). To obtain best performance, include a trimmer in R_5, adjusted to optimize the controlled value of the JFET's resistance.

For this configuration, sustained oscillation occurs when IC_2's voltage gain is −2.00. We chose R_5 to be 5% smaller than critical, with the series JFET providing the adjustable 1k (nominal) additional resistance. That puts a 100 mV (peak-to-peak) sinewave across the JFET, which we judged small enough for good linearity, especially with the linearizing divider R_3R_4 (see §3.2.7A). Amplitude control is provided by integrator IC_3, which receives pulses of input current (via the divider to a stable −5 V reference) when the sinewave output of IC_2 reaches 2 V amplitude: its negative-going output back-biases the JFET's gate, relative to the source at virtual ground, raising the JFET's resistance and thus lowering the gain of IC_2 to maintain this output amplitude.[28] For the values shown, the JFET's minimum R_{ON} (i.e., at V_{GS}=0) must be less than 1k, which requires a minimum g_m of 1 mS (see §3.2.7); the 2N5458 specifies a minimum g_m of 1.5 mS, so the circuit is guaranteed to start up. We tacked on an inverting gain-of-5 stage to produce a healthy 10 V amplitude output.

The circuit worked "out of the box" – correct frequency and amplitude (1 kHz, 10 V) and a good-looking sinewave. The measured total harmonic distortion (THD) was an admirable 0.002%.[29] Before celebrating, though, we tried some variations: (a) Replacing the film capacitors with ceramic ("X7R" type) raised the distortion[30] a hundred-fold, to 0.22%! (b) Dropping the swing across the JFET to 50 mVpp (by raising R_5 to 19.6k) halved the distortion, to 0.001%; from here on we stuck with this smaller JFET swing. (c) Next we trimmed the ratio of R_3/R_4 slightly, to minimize the (dominantly second harmonic) distortion, achieving a final THD figure of 0.0002%; that's −114 dB down from the signal, a mere 2 parts per million! (d) Finally, to see the effect of the linearizing gate divider, we omitted R_4, which raised the distortion 50-fold, to 0.01%.

Some important lessons from this exercise, if you want the lowest distortion, are (a) avoid inexpensive ceramic capacitors, (b) use the gate-linearizing trick (subtracting $V_{DS}/2$ from V_{GS}), and (c) keep the swing small across JFETs being used as resistors, preferably less than 100 mV (which, however, causes a rather lengthy amplitude settling time). Because JFET nonlinearity dominated the distortion, even when trimmed, we could have reduced the distortion still further by running the oscillator at lower amplitude, say 0.5 V, at the expense of added broadband noise produced by the fixed noise contribution of the op-amps.[31]

C. *RC* phase-shift oscillator

Unlike the relaxation oscillator (where an *RC* time constant is combined with voltage thresholds to make an

[28] We chose the integrator gain to put the unity-gain frequency of the control loop roughly at 50 Hz.

[29] Almost entirely second harmonic.

[30] Now dominated by third harmonic.

[31] Better yet, use a photoresistive gain control, as in Figure 7.21. Jim Williams did this, and he also added a lowpass filter between IC_3 and R_4 to attenuate the integrator's small cycle-by-cycle error-correcting waveform, achieving a measured distortion below 3 ppm; see LTC app-note AN132.