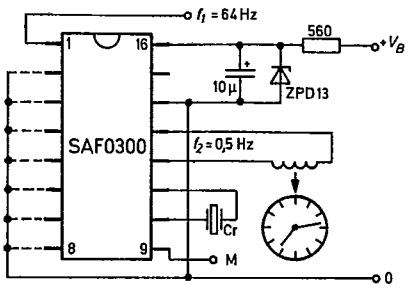
INTEGRATED CIRCUITS FOR ELECTRONIC CLOCKS

SAF0300 Car Clock IC with Digital Adjustment, 0.5 Hz Output and Additional 64 Hz Signal (16-Pin Plastic Package)

CMOS circuit for crystal-controlled analog car clocks with 12 V (6... 16.5 V) supply voltage having an additional 64 Hz push-pull output supplying a time base signal e. g. for recording speedometers. The SAF0300 consists of an oscillator circuit, a fixed 4 : 1 frequency divider, an adjustable frequency divider which is variable in 127 steps and covering the range from 2^{14} : 1 to $(2^{14} + 2^2)$: 1, a motor driver stage in bridge configuration and the 64 Hz push-pull output.

Apart from the crystal the oscillator does not require any additional components. The correct output frequency may be set by seven adjustment terminals with an accuracy of 10^{-6}. At 4.194 812 MHz oscillator frequency the bridge output (pins 12/13) supplies a squarewave signal of 0.5 s pulse duration and 0.5 Hz frequency if the adjustable frequency divider is set to the center position. In the motor coil flows each second a current pulse of alternate direction. Output 1 (pin 1) supplies the additional 64 Hz squarewave signal with a pulse duty factor of 0.5.



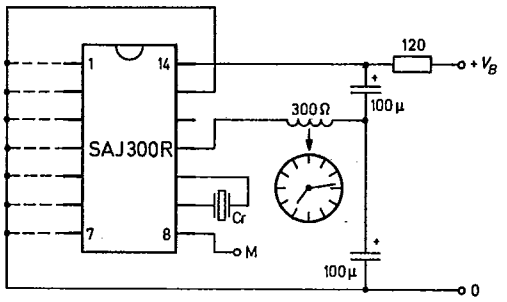
SAF0300 Application Circuit

The adjustable frequency divider has been designed so that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. Pin 8 gives the smallest adjustment step of 1.9 ppm. Pin 7 offers the nextlarger step of 3.8 ppm and so forth, up to pin 2 which enables an adjustment step of 122 ppm to be obtained. If all adjustment terminals are grounded, the output frequency is reduced by 242 ppm.

SAJ300R Car Clock IC with Digital Adjustment and 0.5 Hz Output (14-Pin Plastic Package TO-116)

CMOS circuit for use in crystal-controlled analog car clocks operating on 12 V (6...16,5 V) supply voltage. The SAJ300R contains an oscillator circuit, a fixed 4 : 1 frequency divider, an adjustable frequency divider and a motor driver stage. The adjustable frequency divider of the SAJ300R has an adjustment range from 2^{21} : 1 to $(2^{21} + 2^9)$: 1.

Except for the crystal, the oscillator requires no additional components. The trimmer capacitor previously needed for frequency adjust-ment has been taken over by the variable frequency divider. Seven adjustment pins are provided. They are used to set the divider ratio to the required value with an accuracy of 10^{-6}. With an oscillator frequency of 4.194 812 MHz the series-connected push-pull output stage supplies a symmetrical squarewave signal with a pulse duty factor of 0.5. The frequency of this output signal is 0.5 Hz if the variable frequency divider is set to the center.



SAJ300R Application Circuit

Due to the differentiating effect of the motor capacitors pulses of alternate direction occur in the motor coil.

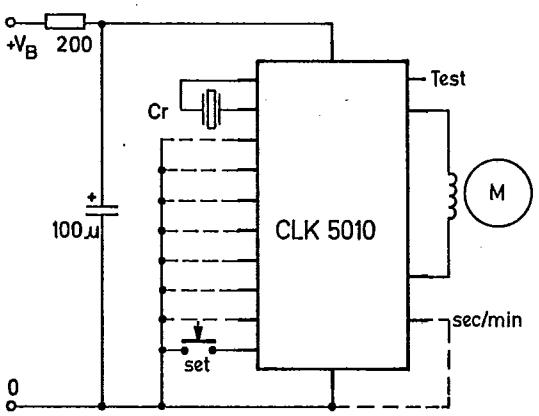
The adjustable frequency divider has been designed so that the maximum output frequency is set when all adjustment pins are either open circuit or connected to pin 14. If one or more adjustment pins are grounded (taken to pin 13) the output frequency decreases. Pin 7 gives the smallest adjustment of 1.9 ppm. Pin 6 affords the nextlarger step of 3.8 ppm and so forth, up to pin 1 which enables an adjustment step of 122 ppm to be obtained.

CLK5010 Car Clock IC with Electrical Setting (16-Pin Plastic Package)

CMOS circuit for crystal-controlled analog car clocks operating on 12 V supply, having optional 0.5 Hz or 1/120 Hz output frequency for driving either clocks with second-hands or without. With the minutes output frequency chosen, electrical setting of the clock by pushing the "set" button is provided. When the button is released, the seconds' counter is reset, so that the clock is synchronized to the full minute. If the seconds' option is chosen, the clock must be set mechanically.

The CLK5010 Car Clock IC is equipped with digital adjustment of the output frequency. By means of seven adjustment pins, the correct output frequency may be set to an accuracy of ±0.95 ppm.

At 4.194812 MHz oscillator frequency and the adjustable divider set to the center position, the motor driver stage in bridge configuration supplies a squarewave signal of 125 ms pulse duration and either 0.5 Hz frequency or 1/120 Hz frequency respectively. This means an output pulse of alternate direction flowing through the motor coil every second or every minute.



CLK5010 Application Circuit