High: > 2 CPU clock cycles for f_{ck} < 12MHz, 3 CPU clock cycles for f_{ck} ≥ 12MHz

31.9.1. SPI Serial Programming Algorithm

When writing serial data to the ATmega128A, data is clocked on the rising edge of SCK.

When reading data from the ATmega128A, data is clocked on the falling edge of SCK. Refer to Figure 31-8 Serial Programming Waveforms on page 398 for timing details.

To program and verify the ATmega128A in the SPI Serial Programming mode, the following sequence is recommended (See four byte instruction formats in Figure 31-8 Serial Programming Waveforms on page 398):

1. Power-up sequence:
   Apply power between VCC and GND while $\overline{\text{RESET}}$ and SCK are set to “0”. In some systems, the programmer can not guarantee that SCK is held low during power-up. In this case, $\overline{\text{RESET}}$ must be given a positive pulse of at least two CPU clock cycles duration after SCK has been set to “0”.

   As an alternative to using the RESET signal, $\overline{\text{PEN}}$ can be held low during Power-on Reset while SCK is set to “0”. In this case, only the $\overline{\text{PEN}}$ value at Power-on Reset is important. If the programmer cannot guarantee that SCK is held low during power-up, the $\overline{\text{PEN}}$ method cannot be used. The device must be powered down in order to commence normal operation when using this method.
2. Wait for at least 20ms and enable SPI Serial Programming by sending the Programming Enable serial instruction to pin MOSI.
3. The SPI Serial Programming instructions will not work if the communication is out of synchronization. When in sync. the second byte (0x53), will echo back when issuing the third byte of the Programming Enable instruction. Whether the echo is correct or not, all 4 bytes of the instruction must be transmitted. If the 0x53 did not echo back, give $\overline{\text{RESET}}$ a positive pulse and issue a new Programming Enable command.
4. The Flash is programmed one page at a time. The page size is found inPage Size on page 386. The memory page is loaded one byte at a time by supplying the 7 LSB of the address and data together with the Load Program Memory Page instruction. To ensure correct loading of the page, the data low byte must be loaded before data high byte is applied for given address. The Program Memory Page is stored by loading the Write Program Memory Page instruction with the 9MSB of the address. If polling is not used, the user must wait at least t_{WD_FLASH} before issuing the next page. (See Table 31-14 Minimum Wait Delay Before Writing the Next Flash or EEPROM Location, VCC = 5V ± 10% on page 398).
   Note: 1. If other commands than polling (read) are applied before any write operation (Flash, EEPROM, Lock bits, Fuses) is completed, may result in incorrect programming.
5. The EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. If polling is not used, the user must wait at least t_{WD_EEPROM} before issuing the next byte. (See Table 31-14 Minimum Wait Delay Before Writing the Next Flash or EEPROM Location, VCC = 5V ± 10% on page 398). In a chip erased device, no 0xFFs in the data file(s) need to be programmed.
6. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO.
7. At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):
   - Set $\overline{\text{RESET}}$ to “1”.
   - Turn VCC power off.