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S1D13774B02B WVGA LCD Controller

Hardware Functional Specification

Document Number: X85A-A-003-01

Status: Revision 1.5 - EPSON CONFIDENTIAL

Issue Date: 2008/07/02

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13774 LCD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Operational Overview

The S1D13774 is a low cost, low power LCD Controller providing multiple LCD support for embedded and mobile products requiring up to WVGA resolution. The Video Input interface and optional TV-Out support, via an external NTSC/PAL encoder, enhance the capabilities of the S1D13774 to meet a wide variety of applications. Supporting up to three display layers, the S1D13774 provides the Host processor with flexibility in handling multiple image sources.

The S1D13774 feature set includes independent resizing of PIP window image data using the bi-cubic scaler, rotation and mirror functions, alpha blending and transparency, image scrolling for each layer, and LCD output manipulation such as gamma control and optional dithering. The Auto Movie Enhancement (AME) feature allows independent chroma, contrast, and gamma adjustments of the image data in a selected PIP window. The combination of these features allows the Host processor to provide image data, but off-loads the image processing requirements from the Host.

The S1D13774 contains 1280K bytes of embedded DRAM which is used to store image data for up to three layers. This feature set provides a low cost, low power single chip solution to meet the demands of embedded markets requiring up to WVGA resolution, such as Mobile Communications devices.

1.3 Abbreviations and Acronyms

The following abbreviations and acronyms are used in this document:

All numbers are in decimal unless marked otherwise (b for binary, h for hexadecimal)
k = 2^{10} = 1024 when used with regards to memory
b = bit
B = Byte
bpp = bits-per-pixel
msb = Most Significant bit
lsb = Least Significant bit
IO = Input/Output
LUT = Look-Up Table
NC = No Connection
YYC = YUV to YUV Converter
YRC = YUV to RGB Converter
RYC = RGB to YUV Converter
VDP = Vertical Display Period
VNDP = Vertical Non-display Period
DDS = Digital Direct Synthesis
POUT = PLL Output

2 Features

2.1 Display Buffer

- Embedded 1280k bytes of DRAM can be used for:
  - Main Window frame buffer
  - PIP1 Window frame buffer
  - PIP2 Window frame buffer
- Supports eco Image Codec (eIC)

2.2 Registers

- Registers are memory mapped
- Asynchronous/Synchronous registers (asynchronous registers are accessible when power save modes are enabled)

2.3 Host Interface

- Types of Host interface:
  - 18-bit Indirect Interface
  - I2C Slave

2.4 Video Input Interface

- 8-bit YUV interface, 12-bit RGB interface

2.5 Input Data Formats

- Image data can be input as:
  - YUV 4:2:2
  - YUV 4:2:0
  - RGB 5:6:5
  - RGB 6:6:6
  - RGB 8:8:8

2.6 LCD Interface

- Supports up to two panels:
  - LCD1 can be:
    - 18/24-bit RGB Interface
  - LCD2 can be:
    - Parallel Interface (MPU Interface)
    - Serial Interface

2.7 External NTSC/PAL Encoder Interface

- Hsync & Field Interface (Interlace)
- ITU-R BT656 Interface (Interlace)
- Parallel Interface (MPU Interface) (Non-Interlace)

2.8 Display Features

- Picture in Picture, Transparency, Alpha Blending
- Image Rotation (90°, 180°, 270°) and Mirroring
- Scroll Assist
- AME (Auto Movie Enhancement)
- Supports up to three layers:
  - Main Window:
    - RGB 8:8:8, RGB 6:6:6, RGB 5:6:5
    - Image Doubling
  - PIP1 Window:
    - RGB 8:8:8, RGB 6:6:6, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0
    - Bi-Cubic Scaling (1/2x ~ 8x)
    - Over/Down Sampling Scaling (1/8x ~ 8x)
    - Edge Enhancement
  - PIP2 Window:
    - RGB 8:8:8, RGB 6:6:6, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0
    - Bi-Cubic Scaling (1/2x ~ 8x)
    - Over/Down Sampling Scaling (1/8x ~ 8x)
    - Edge Enhancement

2.9 Miscellaneous

- Internal PLL or digital clock input (CLKI)
- Software initiated Power Save Mode
- Available general purpose IO pins
- Package:
  - VFBGA 161-pin: 7x7mm, Ball pitch 0.5mm, Thickness 1.0mm

3 Block Diagrams

3.1 Typical System Implementations

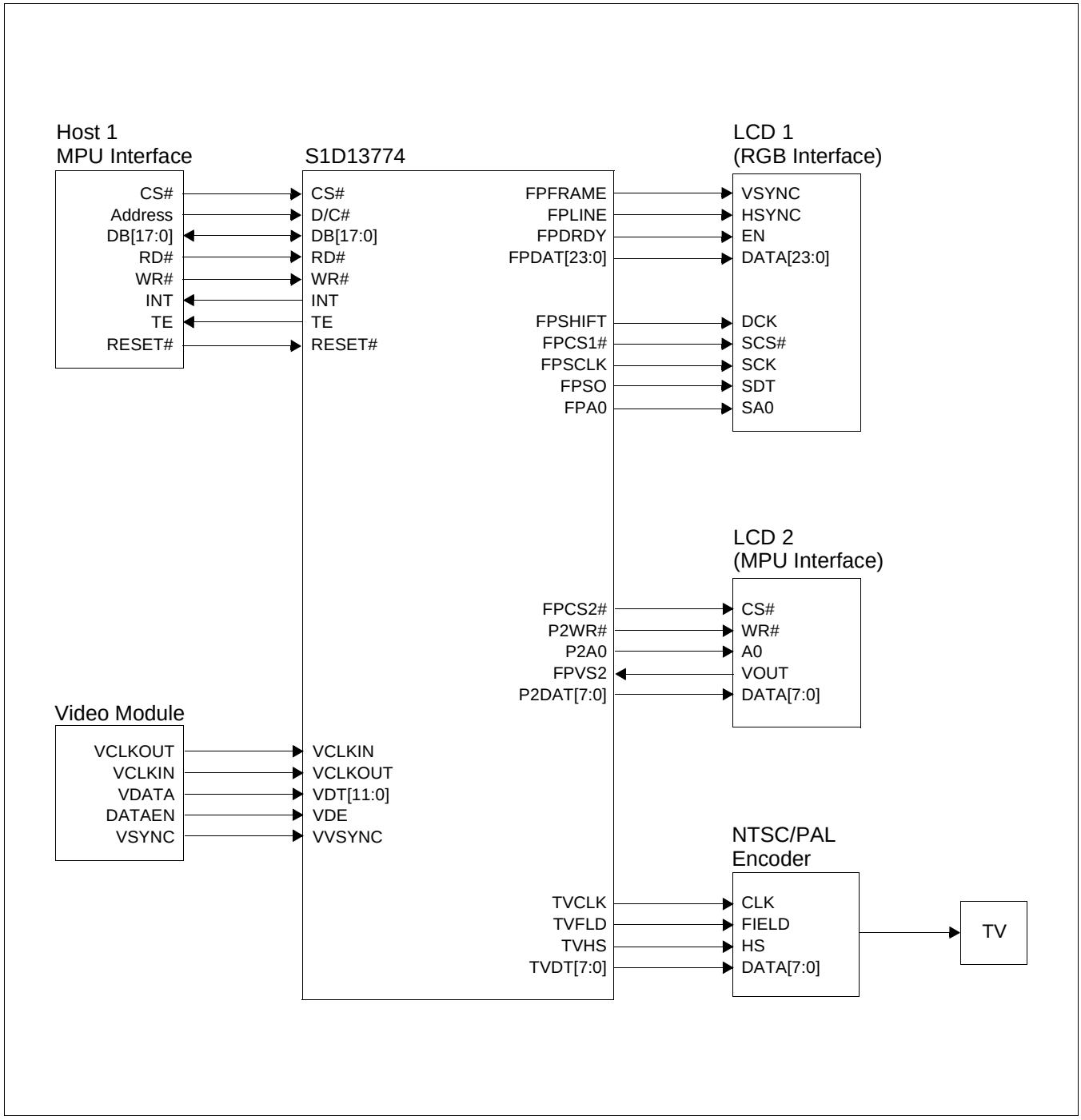


Figure 3-1: Example System Block Diagram 1

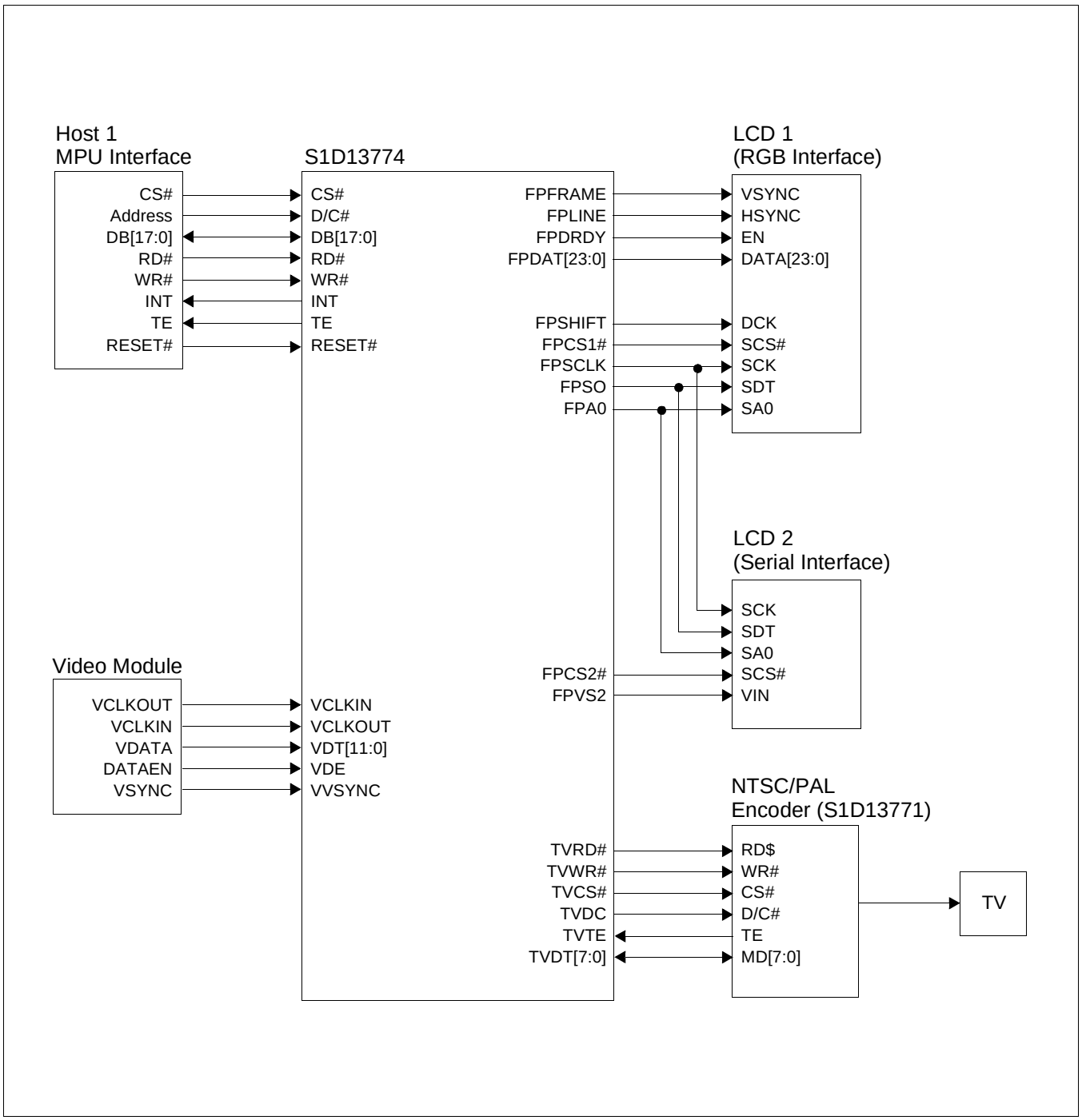


Figure 3-2: Example System Block Diagram 2

3.2 System Block Diagram

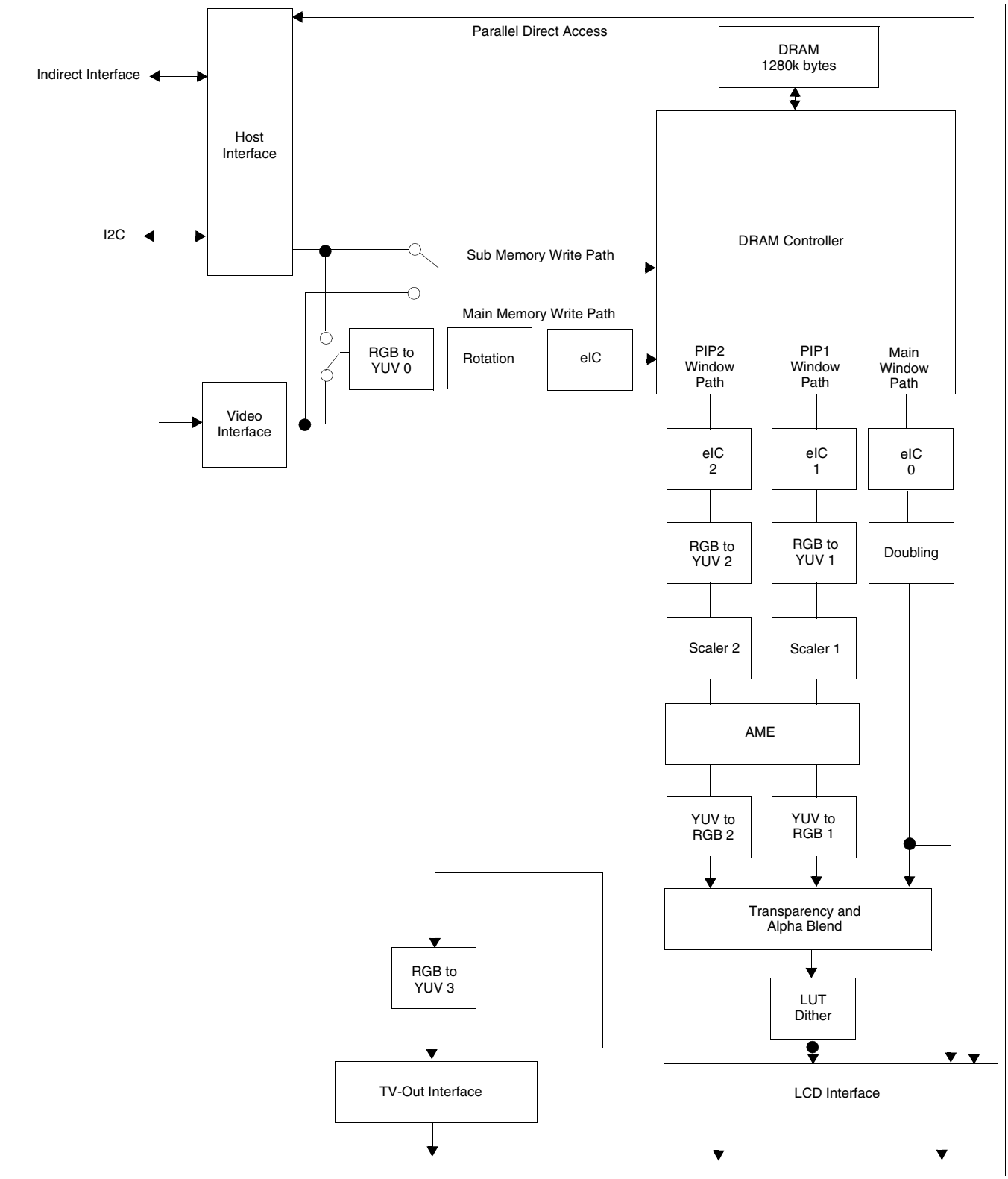


Figure 3-3: S1D13774 Block Diagram

4 Pins

4.1 Pinout Diagram

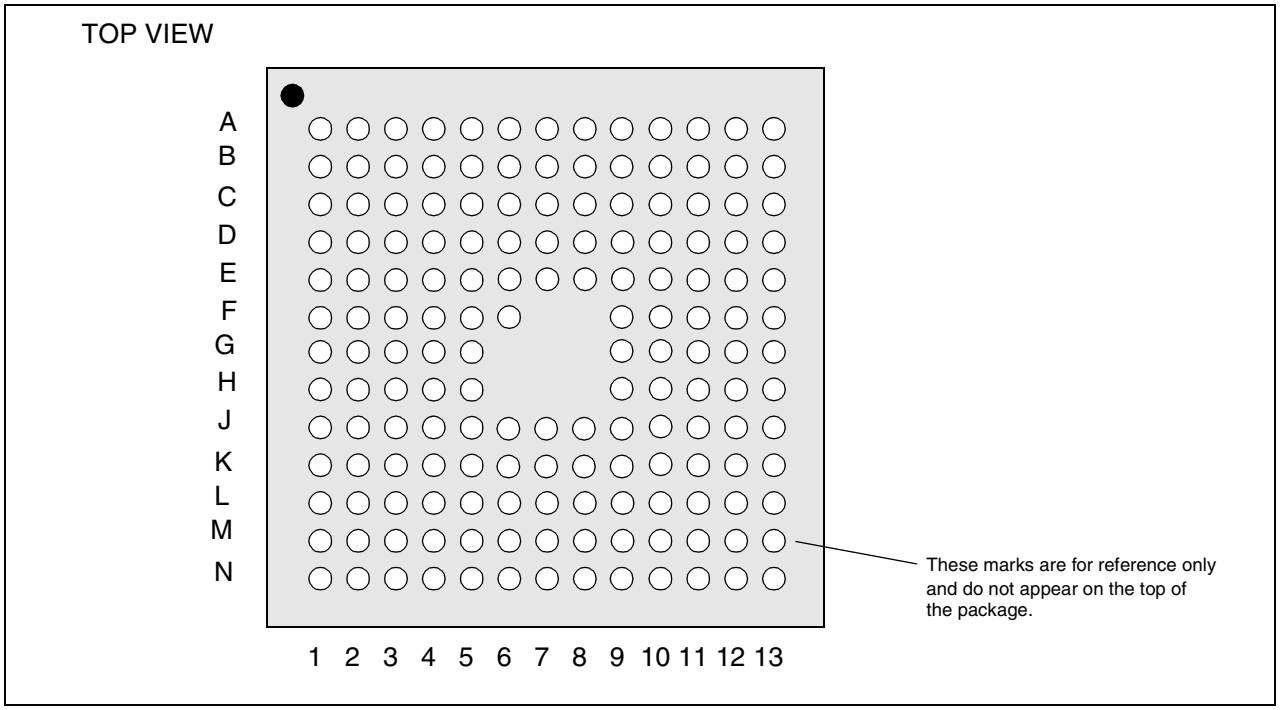


Figure 4-1: S1D13774 VFBGA7HX 161-pin Pin Mapping (Top View)

Table 4-1: S1D13774 VFBGA7HX 161-pin Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	NC	GPIOH8	GPIOH2	COREVDD	VDT9	VDT7	SDA	SCL	GPIOH23	CLKI	PLPAV	PLP	NC	A
B	GPIOH9	GPIOH6	GPIOH3	VSS	VDT8	VDT6	GPIOH0	VDT1	TE	VSS	PLLVSS	PLLVDD	OSCO	B
C	GPIOH12	GPIOH7	GPIOH4	VDT10	GPIOH22	VDT5	GPIOH1	VDT0	GPIOH20	HIOVDD	VSS	OSCVDD	OSCI	C
D	GPIOH15	GPIOH14	GPIOH5	VDT11	GPIOH21	VDT4	VDT3	VDT2	VSS	I2CEN	COREVDD	CORE18VDD	MTEST3	D
E	VCLKIN	GPIOH17	GPIOH10	GPIOH11	HIOVDD	COREVDD	VSS	HIOVDD	HIOVDD	COREVDD	VSS	MDREF	MTEST2	E
F	GPIOH18	COREVDD	GPIOH16	GPIOH13	VXSD	NC			VSS	FPDAT10	COREVDD	COREVDD	MTEST1	F
G	VCLKOUT	VVSYNC	VSS	VDE	VRESET				VSS	PIOVDD	FPDAT11	VSS	MTEST0	G
H	DRAMVDD	DRAMVDD	DRAMVSS	GPIOH19	TESTEN				PIOVDD	FPDAT16	FPDAT8	FPDAT9	PIOVDD	H
J	DRAMVCC	DRAMVCC	DRAMVSS	DRAMVSS	CNF3	CNF1	CNF2	CNF0	SRESET	FPCS2#	FPDAT14	FPDAT17	FPDAT7	J
K	HIOVDD	COREVDD	DRAMVSS	PIOVDD	VSS	GPIOP11	COREVDD	PIOVDD	FPDAT0	FPSO	COREVDD	VSS	FPDAT15	K
L	INT	VSS	COREVDD	GPIOP14	GPIOP8	GPIOP7	FPFRAME	VSS	FPCS1#	GPIOP4	FPA0	FPDAT12	FPDAT13	L
M	RESET#	CRES	GPIOP13	GPIOP9	GPIOP6	VSS	FPLINE	FPDAT1	FPDAT3	FPDAT6	GPIOP3	GPIOP1	FPSCK	M
N	NC	RRES	GPIOP12	GPIOP10	GPIOP5	FPSHIFT	FPDRDY	FPDAT2	FPDAT4	FPDAT5	GPIOP2	GPIOP0	NC	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

4.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
AP	=	Analog Power pin
G	=	Ground
AG	=	Analog Ground

RESET# / Power Save Status

H	=	High level output
L	=	Low level output
Hi-Z	=	High Impedance

Table 4-2 Cell Descriptions

Item	Description
LI	LVCMOS Input Buffer
LIS	LVCMOS Schmitt Input Buffer
LIU	LVCMOS Input Buffer with pull-up resistor
LID	LVCMOS Input Buffer with pull-down resistor
LIDS	LVCMOS Schmitt Input Buffer with pull-down resistor
LO	LVCMOS Output buffer
LO_DSEL	LVCMOS Output Buffer with Drive Selector. The driving capability can be controlled using REG[0018h].
LB_DSEL	LVCMOS Bidirectional Buffer with Drive Selector. The driving capability can be controlled using REG[0018h].
LBU_DSEL	LVCMOS Bidirectional Buffer with Drive Selector and pull-up resistor. The driving capability can be controlled using REG[0018h].
LBD_DSEL	LVCMOS Bidirectional Buffer with Drive Selector and pull-down resistor. The driving capability can be controlled using REG[0018h].
ABBMD	Analog Bi-directional Buffer
AIBMD	Analog Input Buffer
AOBMD	Analog Output Buffer
AIBP	Analog Input Buffer for PLL
AOBP	Analog Output Buffer for PLL
OIB	Oscillator Input Buffer
OOB	Oscillator Output Buffer

LVCMOS is Low Voltage CMOS (see Section 5, “D.C. Characteristics” on page 40).

4.2.1 Host Interface

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
INT	O	L1	LO_DSEL	HIOVDD	L	Interrupt output. When an internal interrupt occurs, this output pin is driven high. If the Host CPU clears the internal interrupt, this pin is driven low.
RESET#	I	M1	LIS	HIOVDD	Input	This active low input sets all internal registers to the default state and forces all signals to their inactive states. Minimum low pulse width is 200ns.
CRES	I	M2	LIS	HIOVDD	Input	This input pin is used for noise rejection on the RESET# pin and should be connected through a capacitor to VSS. For details, see Section 19, “RESET# Glitch Rejection” on page 404. When unused, CRES should be connected to VSS.
RRES	O	N2	LO	HIOVDD	RESET#	This output pin is used for noise rejection on the RESET# pin and should be connected through a resistor to the CRES pin. For details, see Section 19, “RESET# Glitch Rejection” on page 404. When unused, RRES should be left unconnected.
TE	O	B9	LO_DSEL	HIOVDD	L	This output pin is the Tearing Effect pin which reflects the FPFRAME (VSYNC) signal for the host interface. It can be used to indicate when it is safe to write new data from the Host in order to prevent visual tearing of an image. For further information on configuring this pin, refer to the register descriptions for REG[0400h] bit 15 and REG[0404h]. For further information on using TE, see Section 14.4, “Host Interface VSYNC Output (Tearing Effect)” on page 361.
SCL	IO	A8	LB_DSEL	HIOVDD	Input	This input/output pin is the I2C bus serial clock. When the I2C Interface is not used, this pin must be connected to VSS.
SDA	IO	A7	LB_DSEL	HIOVDD	Input	This pin is the I2C bus data Input/output. When the I2C Interface is not used, this pin must be connected to VSS.
I2CEN	I	D10	LID	HIOVDD	Input with Pull-Down	This input pin is the I2C CLK Enable and can be used to enable the I2C module at chip initialization. When this pin is high, the clock specified by CNF1 (OSC or CLKI) is supplied to the I2C module. This pin is ORed with the I2C Quick Enable bit (REG[030h] bit 0), so that the I2C module can be enabled using either hardware (I2CEN pin) or software (REG[0030h] bit 0). If the I2C interface is enabled after initialization, the I2C Enable bit (REG[0B04h] bit 0) should be used and the source clock is derived from SYSCLK. For further details on the I2C Clock, see Section 8, “Clocks” on page 88.

4.2.2 Video Input Interface

Table 4-3: Video Input Interface Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
VDT[11:0]	IO	D4,C4,A5,B5, A6,B6,C6,D6, D7,D8,B8,C8	LBD_DSEL	HIOVDD	Input with Pull-Down	These input/output pins are the Video Input Data pins 11-0.
VVSYNC	I	G2	LIU	HIOVDD	Input with Pull-Up	This input pin is the Video Vsync.
VDE	I	G4	LID	HIOVDD	Input with Pull-Down	This input pin is the Video Data Enable.
VCLKIN	I	E1	LIDS	HIOVDD	Input with Pull-Down	This input pin is the Video Clock In.
VCLKOUT	O	G1	LBD_DSEL (see Note)	HIOVDD	L	This output pin is the Video Clock Out.

Note

The Bi-directional IO is used for test production only.

4.2.3 LCD Interface

Table 4-4: LCD Interface Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
FPDAT[17:0]	O	J12,H10,K13, J11,L13,L12, G11,F10, H12,H11,J13, M10,N10,N9, M9,N8,M8,K9	LB_DSEL (see Note)	PIOVDD	L	These output pins are the LCD interface data pins 17-0. They have multiple functions depending on the configuration of the LCD and TV-Out Interfaces. For details, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.
FPFRAME	O	L7	LB_DSEL (see Note)	PIOVDD	L	This output pin has multiple functions depending on the configuration of the LCD and TV-Out Interfaces. For details, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.
FPLINE	O	M7	LB_DSEL (see Note)	PIOVDD	L	This output pin has multiple functions depending on the configuration of the LCD and TV-Out Interfaces. For details, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.
FPSHIFT	O	N6	LB_DSEL (see Note)	PIOVDD	L	This output pin has multiple functions depending on the configuration of the LCD and TV-Out Interfaces. For details, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.
FPDRDY	O	N7	LB_DSEL (see Note)	PIOVDD	L	This output pin has multiple functions depending on the configuration of the LCD and TV-Out Interfaces. For details, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.
FPCS1#	O	L9	LB_DSEL (see Note)	PIOVDD	H	This output pin is Chip Select for the LCD1 serial interface.
FPCS2#	O	J10	LB_DSEL (see Note)	PIOVDD	H	This output pin is Chip Select for the LCD2 serial/parallel interface. For panel modes 3-2 and 3-3, GPIOH23 is used instead of this pin.
FPSCK	O	M13	LB_DSEL (see Note)	PIOVDD	H	This output pin is the clock for the LCD1/LCD2 serial interface.
FPA0	O	L11	LB_DSEL (see Note)	PIOVDD	L	This output pin is the Command/Parameter select for the LCD1/LCD2 serial interface.
FPSO	O	K10	LB_DSEL (see Note)	PIOVDD	L	This pin is the Data output for the LCD1/LCD2 serial interface.

Note
The Bi-directional IO is used for test production only.

4.2.4 GPIO

The functionality of the GPIO pins is controlled by the configuration of the LCD and TV-Out interfaces. For a summary of GPIO functionality, refer to Section 4.7, "GPIO Pin Mapping" on page 38

Table 4-5: GPIO Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
GPIOP0	IO	N12	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD1 data output pin. (FPDAT18) • LCD2 data output pin. (P2DAT0) • TV-Out data output pin. (TVDT0)
GPIOP1	IO	M12	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD1 data output pin. (FPDAT19) • LCD2 data output pin. (P2DAT1) • TV-Out data output pin. (TVDT1)
GPIOP2	IO	N11	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD1 data output pin. (FPDAT20) • LCD2 data output pin. (P2DAT2) • TV-Out data output pin. (TVDT2)
GPIOP3	IO	M11	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD1 data output pin. (FPDAT21) • LCD2 data output pin. (P2DAT3) • TV-Out data output pin. (TVDT3)
GPIOP4	IO	L10	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD1 data output pin. (FPDAT22) • LCD2 data output pin. (P2DAT4) • TV-Out data output pin. (TVDT4)
GPIOP5	IO	N5	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD1 data output pin. (FPDAT23) • LCD2 data output pin. (P2DAT5) • TV-Out data output pin. (TVDT5)
GPIOP6	IO	M5	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD2 data output pin. (P2DAT6) • TV-Out data output pin. (TVDT6)
GPIOP7	IO	L6	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD2 data output pin. (P2DAT7) • TV-Out data output pin. (TVDT7)

Table 4-5: GPIO Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
GPIOP8	IO	L5	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD2 A0 output pin. (P2A0) • TV-Out Hsync output pin. (TVHS) • TV-Out A0 output pin. (TVDC)
GPIOP9	IO	M4	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • LCD2 Write Enable output pin. (P2WR#) • TV-Out Field output pin. (TVFLD) • TV-Out Write Enable output pin. (TVWR#)
GPIOP10	IO	N4	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • TV-Out CLK output pin. (TVCLK) • TV-Out Read Enable output pin. (TVRD#)
GPIOP11	IO	K6	LBU_DSEL	PIOVDD	Input with Pull-Up	This pin has multiple functions. • GPIO input/output pin • TV-Out Chip Select input pin. (TVCS#)
GPIOP12	IO	N3	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • TV-Out TE input pin. (TVTE)
GPIOP13	IO	M3	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin •
GPIOP14	IO	L4	LBD_DSEL	PIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • VIN/VOUT for the LCD2. (FPVS2)
GPIOH0	IO	B7	LBD_DSEL	HIOVDD	Input with Pull-Down	This pin has multiple functions. • GPIO input/output pin • TV-Out TE input pin. (TVTE)
GPIOH1	IO	C7	LBU_DSEL	HIOVDD	Input with Pull-Up	This pin has multiple functions. • GPIO input/output pin • TV-Out Chip Select input pin. (TVCS#)
GPIOH2	IO	A3	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin • TV-Out data output pin (TVDT0) When CNF0 = H • Data pin for the Indirect Host Interface (DB0)

Table 4-5: GPIO Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
GPIOH3	IO	B3	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin • TV-Out data output pin (TVDT1) When CNF0 = H • Data pin for the Indirect Host Interface (DB1)
GPIOH4	IO	C3	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin • TV-Out data output pin (TVDT2) When CNF0 = H • Data pin for the Indirect Host Interface (DB2)
GPIOH5	IO	D3	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out data output pin. (TVDT3) When CNF0 = H • Data pin for the Indirect Host Interface. (DB3)
GPIOH6	IO	B2	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out data output pin. (TVDT4) When CNF0 = H • Data pin for the Indirect Host Interface. (DB4)
GPIOH7	IO	C2	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down. When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out data output pin. (TVDT5) When CNF0 = H • Data pin for the Indirect Host Interface. (DB5)
GPIOH8	IO	A2	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out data output pin. (TVDT6) When CNF0 = H • Data pin for the Indirect Host Interface. (DB6)

Table 4-5: GPIO Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
GPIOH9	IO	B1	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out data output pin. (TVDT7) When CNF0 = H • Data pin for the Indirect Host Interface. (DB7)
GPIOH10	IO	E3	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out data output pin. (TVHS) • TV-Out A0 output pin. (TVDC) When CNF0 = H • Data pin for the Indirect Host Interface. (DB8)
GPIOH11	IO	E4	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out Field output pin. (TVFLD) • TV-Out Write output pin. (TVWR#) When CNF0 = H • Data pin for the Indirect Host Interface. (DB9)
GPIOH12	IO	C1	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • TV-Out CLK output pin. (TVCLK) • TV-Out Read output pin. (TVRD#) When CNF0 = H • Data pin for the Indirect Host Interface. (DB10)
GPIOH13	IO	F4	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT0) When CNF0 = H • Data pin for the Indirect Host Interface. (DB11)
GPIOH14	IO	D2	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT1) When CNF0 = H • Data pin for the Indirect Host Interface. (DB12)

Table 4-5: GPIO Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
GPIOH15	IO	D1	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT2) When CNF0 = H • Data pin for the Indirect Host Interface. (DB13)
GPIOH16	IO	F3	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT3) When CNF0 = H • Data pin for the Indirect Host Interface. (DB14)
GPIOH17	IO	E2	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT4) When CNF0 = H • Data pin for the Indirect Host Interface. (DB15)
GPIOH18	IO	F1	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT5) When CNF0 = H • Data pin for the Indirect Host Interface. (DB16)
GPIOH19	IO	H4	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT6) When CNF0 = H • Data pin for the Indirect Host Interface. (DB17)
GPIOH20	IO	C9	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 data output pin. (P2DAT7) When CNF0 = H • Data/Command Select input pin for the Indirect Host Interface. (D/C#)

Table 4-5: GPIO Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
GPIOH21	IO	D5	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 A0 output pin. (P2A0) When CNF0 = H • Read Enable input pin for the Indirect Host Interface. (RD#)
GPIOH22	IO	C5	LBD_DSEL	HIOVDD	When CNF0=L, Input with Pull-Down When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 Write Enable output pin. (P2WR#) When CNF0 = H • Write Enable input pin for the Indirect Host Interface. (WR#)
GPIOH23	IO	A9	LBU_DSEL	HIOVDD	When CNF0=L, Input with Pull-Up When CNF0=H, Input	This pin has multiple functions. When CNF0 = L • GPIO input/output pin. • LCD2 Chip Select output pin. (P2CS#) When CNF0 = H • Chip Select input pin for the Indirect Host Interface. (CS#)

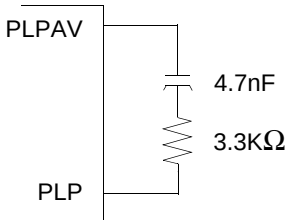
4.2.5 Clock

Table 4-6: Clock Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
CLKI	I	A10	LIS	HIOVDD	Input	This input clock has multiple functions. • When the internal PLL is used, this pin is the input reference clock for the internal PLL. • When the PLL is bypassed, this pin is the digital clock input for the system clock (SYSCLK).
OSCO	O	B13	OOB	OSCVDD	When OSCI=H, OSCO is Low output. When OSCI=L, OSCO is High output.	This pin, along with OSCI, is the 2-terminal crystal interface. When the internal oscillator is not used, this pin should be left unconnected.
OSCI	I	C13	OIB	OSCVDD	Input	This pin, along with OSCO, is the 2-terminal crystal interface. When the internal oscillator is not used, this pin should be connected to OSCVDD.

4.2.6 Miscellaneous

Table 4-7: Miscellaneous Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	IO Voltage	RESET# State	Description
CNF[3:0]	I	J5,J7,J6,J8	LI	HIOVDD	Input	These input pins are used for configuring the S1D13774 and must be connected to either HIOVDD or VSS. The states of these pins are latched at RESET#. For a summary of configuration options, see Section 4.3, “Summary of Configuration Options” on page 31.
MDREF	O	E12	AOBMD	CORE18VDD	L	This pin is a production test pin and must be left unconnected for normal operations.
PLP	O	A12	AOBP	PLLVDD	H	This pin is the output node for the PLL Charge Pump circuit and should be connected to the Low Pass Filter.
PLPAV	I	A11	AIBP	PLLVDD	H	This input pin is the Analog Power Supply for the Low Pass Filter and should be connected to the Low Pass Filter as shown. 
TESTEN	I	H5	LID	HIOVDD	Input with pull-down	This pin is a Test Enable input and is used for production test only. This pin should be left unconnected for normal operation.
SRESET	O	J9	LO	PIOVDD	H	This pin is a production test pin and must be left unconnected for normal operations.
VRESET	O	G5	LB_DSEL (see Note)	HIOVDD	L	This pin is a production test pin and must be left unconnected for normal operations.
VXSD	O	F5	LB_DSEL (see Note)	HIOVDD	L	This pin is a production test pin and must be left unconnected for normal operations.
MTEST3	I	D13	AIBMD	CORE18VDD	Input	This pin is a production test pin and must be connected to VSS.
MTEST2	I	E13	AIBMD	CORE18VDD	Input	This pin is a production test pin and must be connected to VSS.
MTEST1	IO	F13	ABBMD	CORE18VDD	Input	This pin is a production test pin and must be connected to VSS.
MTEST0	IO	G13	ABBMD	CORE18VDD	Input	This pin is a production test pin and must be connected to VSS.

Note

The Bi-directional IO is used for test production only.

4.2.7 Power and Ground

Table 4-8: Power and Ground Pin Descriptions

Pin Name	Type	Pin # 161-pin	Cell	Description
COREVDD	P	A4,D11,E6, E10,F2,F11,F12, K2,K7,K11,L3	P	Core power supply (1.5V)
HIOVDD	P	C10,E5,E8,E9,K1	P	IO power supply for the host interface
PIOVDD	P	G10,H9,H13,K4,K8	P	IO power supply for the LCD interface
VSS	G	B4,B10,C11,D9,E7, E11,F9,G3,G9,G12, K5,K12,L2,L8,M6	P	GND
DRAMVDD	P	H1,H2	P	1.5V DRAM Core power supply
DRAMVCC	P	J1,J2	P	2.5V DRAM Interface power supply
DRAMVSS	G	H3,J3,J4,K3	P	GND for DRAM
CORE18VDD	AP	D12	P	Core power supply (1.8V)
PLLVDD	AP	B12	P	PLL power supply
PLLVSS	AG	B11	P	GND for PLL
OSCVDD	P	C12	P	IO power supply for the Oscillator (2.5V)

4.3 Summary of Configuration Options

These pins are used for configuration of the S1D13774 and must be connected to either HIOVDD or VSS. The states of these pins are latched at RESET#. When the states of CNF[3:0] are changed, RESET# must be asserted before the change has an effect.

Table 4-9: Summary of Power-On Configurations

CNF[3:0] Input	Power-On/Reset State	
	1 (connected to VDD)	0 (connected to VSS)
CNF3	Reserved	Connect to VSS for normal operation
CNF2	Reserved	Connect to VSS for normal operation
CNF1	2-Terminal Crystal used as I2C clock when I2CEN pin = High. (OSCI, OSCO pins)	Oscillator used as I2C clock when I2CEN pin = High. (CLKI pin)
CNF0	Connect to VDD for normal operation	Reserved

4.4 Indirect Host Interface Pin Mapping

Table 4-10: Indirect Host Interface Pin Mapping

Pin Name	Indirect Host Interface	Description
GPIOH2	DB0 (input/output)	Data 0
GPIOH3	DB1 (input/output)	Data 1
GPIOH4	DB2 (input/output)	Data 2
GPIOH5	DB3 (input/output)	Data 3
GPIOH6	DB4 (input/output)	Data 4
GPIOH7	DB5 (input/output)	Data 5
GPIOH8	DB6 (input/output)	Data 6
GPIOH9	DB7 (input/output)	Data 7
GPIOH10	DB8 (input/output)	Data 8
GPIOH11	DB9 (input/output)	Data 9
GPIOH12	DB10 (input/output)	Data 10
GPIOH13	DB11 (input/output)	Data 11
GPIOH14	DB12 (input/output)	Data 12
GPIOH15	DB13 (input/output)	Data 13
GPIOH16	DB14 (input/output)	Data 14
GPIOH17	DB15 (input/output)	Data 15
GPIOH18	DB16 (input/output)	Data 16 (see Note)
GPIOH19	DB17 (input/output)	Data 17 (see Note)
GPIOH20	D/C# (input)	Data/Command select (H:Data L: Command)
GPIOH21	RD# (input)	Read enable
GPIOH22	WR# (input)	Write enable
GPIOH23	CS# (input)	Chip select

Note

When a write to memory is performed using RGB 6:6:6 Format 5 (REG[0400h] bits 6-4 = 100b), DB[17:16] are used.

4.5 Video Interface Pin Mapping

Table 4-11: Video Interface Pin Mapping

Pin Name	8-bit YUV 4:2:2 Interface	12-bit RGB Interface
VDT0	VDT0 (input)	VDT0 (input)
VDT1	VDT1 (input)	VDT1 (input)
VDT2	VDT2 (input)	VDT2 (input)
VDT3	VDT3 (input)	VDT3 (input)
VDT4	VDT4 (input)	VDT4 (input)
VDT5	VDT5 (input)	VDT5 (input)
VDT6	VDT6 (input)	VDT6 (input)
VDT7	VDT7 (input)	VDT7 (input)
VDT8	—	VDT8 (input)
VDT9	—	VDT9 (input)
VDT10	—	VDT10 (input)
VDT11	—	VDT11 (input)
VVSYNC	VVSYNC (input)	VVSYNC (input)
VDE	VDE (input)	VDE (input)
VCLKIN	VCLKIN (input)	VCLKIN (input)
VCLKOUT	VCLKOUT (output)	VCLKOUT (output)

4.6 LCD and TV-out Interface Pin Mapping

When REG[0104h] bits 1-0 = 00b.

Table 4-12: LCD and TV-Out Interface Pin Mapping Mode 1

Pin Name	Mode 1-1					Mode 1-2				
	LCD1 RGB I/F	LCD2 Serial I/F	TV-Out I/F			LCD1 RGB I/F	LCD2 Serial I/F	TV-Out I/F		
			HS&FD I/F	BT656 I/F	MPU I/F			HS&FD I/F	BT656 I/F	MPU I/F
FPCS1#	SCS1	—	—	—	—	SCS1	—	—	—	—
FPCS2#	—	SCS2	—	—	—	—	SCS2	—	—	—
FPSCLK	SCK	SCK	—	—	—	SCK	SCK	—	—	—
FPSA0	SA0	SA0	—	—	—	SA0	SA0	—	—	—
FPSO	SDO	SDO	—	—	—	SD0	SDO	—	—	—
FPFRAME	VSYNC	—	—	—	—	VSYNC	—	—	—	—
FPLINE	HSYNC	—	—	—	—	HSYNC	—	—	—	—
FPSHIFT	DCK	—	—	—	—	DCK	—	—	—	—
FPDRDY	ENAB	—	—	—	—	ENAB	—	—	—	—
FPDAT0	R7	—	—	—	—	R7	—	—	—	—
FPDAT1	R6	—	—	—	—	R6	—	—	—	—
FPDAT2	R5	—	—	—	—	R5	—	—	—	—
FPDAT3	G7	—	—	—	—	G7	—	—	—	—
FPDAT4	G6	—	—	—	—	G6	—	—	—	—
FPDAT5	G5	—	—	—	—	G5	—	—	—	—
FPDAT6	B7	—	—	—	—	B7	—	—	—	—
FPDAT7	B6	—	—	—	—	B6	—	—	—	—
FPDAT8	B5	—	—	—	—	B5	—	—	—	—
FPDAT9	R4	—	—	—	—	R4	—	—	—	—
FPDAT10	R3	—	—	—	—	R3	—	—	—	—
FPDAT11	R2	—	—	—	—	R2	—	—	—	—
FPDAT12	G4	—	—	—	—	G4	—	—	—	—
FPDAT13	G3	—	—	—	—	G3	—	—	—	—
FPDAT14	G2	—	—	—	—	G2	—	—	—	—
FPDAT15	B4	—	—	—	—	B4	—	—	—	—
FPDAT16	B3	—	—	—	—	B3	—	—	—	—
FPDAT17	B2	—	—	—	—	B2	—	—	—	—
FPDAT18 (GPIOP0)	—	—	TVDT0	TVDT0	TVDT0	R1	—	—	—	—
FPDAT19 (GPIOP1)	—	—	TVDT1	TVDT1	TVDT1	R0	—	—	—	—
FPDAT20 (GPIOP2)	—	—	TVDT2	TVDT2	TVDT2	G1	—	—	—	—
FPDAT21 (GPIOP3)	—	—	TVDT3	TVDT3	TVDT3	G0	—	—	—	—
FPDAT22 (GPIOP4)	—	—	TVDT4	TVDT4	TVDT4	B1	—	—	—	—
FPDAT23 (GPIOP5)	—	—	TVDT5	TVDT5	TVDT5	B0	—	—	—	—
GPIOP6	—	—	TVDT6	TVDT6	TVDT6	—	—	—	—	—
GPIOP7	—	—	TVDT7	TVDT7	TVDT7	—	—	—	—	—
GPIOP8	—	—	TVHS	—	TVDC	—	—	—	—	—
GPIOP9	—	—	TVFLD	—	TVWR#	—	—	—	—	—
GPIOP10	—	—	TVCLK	TVCLK	TVRD#	—	—	—	—	—
GPIOP11	—	—	—	—	TVCS#	—	—	—	—	—
GPIOP12	—	—	—	—	TVTE	—	—	—	—	—
GPIOP13	—	—	—	—	—	—	—	—	—	—
GPIOP14	—	FPVS2 (in)	—	—	—	—	FPVS2 (in)	—	—	—
GPIOH0	—	—	—	—	—	—	—	—	—	TVTE
GPIOH1	—	—	—	—	—	—	—	—	—	TVCS#
GPIOH2	—	—	—	—	—	—	—	TVDT0	TVDT0	TVDT0
GPIOH3	—	—	—	—	—	—	—	TVDT1	TVDT1	TVDT1
GPIOH4	—	—	—	—	—	—	—	TVDT2	TVDT2	TVDT2
GPIOH5	—	—	—	—	—	—	—	TVDT3	TVDT3	TVDT3
GPIOH6	—	—	—	—	—	—	—	TVDT4	TVDT4	TVDT4
GPIOH7	—	—	—	—	—	—	—	TVDT5	TVDT5	TVDT5
GPIOH8	—	—	—	—	—	—	—	TVDT6	TVDT6	TVDT6
GPIOH9	—	—	—	—	—	—	—	TVDT7	TVDT7	TVDT7
GPIOH10	—	—	—	—	—	—	—	TVHS	—	TVDC
GPIOH11	—	—	—	—	—	—	—	TVFLD	—	TVWR#
GPIOH12	—	—	—	—	—	—	—	TVCLK	TVCLK	TVRD#
GPIOH13-23	—	—	—	—	—	—	—	—	—	—

Note

In Mode 1-2, when Indirect Host interface is used, TV-out cannot be used.

When REG[0104h] bits 1-0 = 01b.

Table 4-13: LCD and TV-Out Interface Pin Mapping Mode 2

Pin Name	Mode 2-1					Mode 2-2				
	LCD1 RGB I/F	LCD2 Parallel I/F	TV-Out I/F			LCD1 RGB I/F	LCD2 Parallel I/F	TV-Out I/F		
			HS&FD I/F	BT656 I/F	MPU I/F			HS&FD I/F	BT656 I/F	MPU I/F
FPCS1#	SCS1	—	—	—	—	SCS1	—	—	—	—
FPCS2#	—	P2CS#	—	—	—	—	P2CS#	—	—	—
FPSCLK	SCK	—	—	—	—	SCK	—	—	—	—
FPSA0	SA0	—	—	—	—	SA0	—	—	—	—
FPSO	SDO	—	—	—	—	SD0	—	—	—	—
FPFRAME	VSYNC	P2WR#	—	—	—	VSYNC	P2WR#	—	—	—
FPLINE	HSYNC	P2A0	—	—	—	HSYNC	P2A0	—	—	—
FPSHIFT	DCK	—	—	—	—	DCK	—	—	—	—
FPDRDY	ENAB	—	—	—	—	ENAB	—	—	—	—
FPDAT0	R7	P2DAT0	—	—	—	R7	P2DAT0	—	—	—
FPDAT1	R6	P2DAT1	—	—	—	R6	P2DAT1	—	—	—
FPDAT2	R5	P2DAT2	—	—	—	R5	P2DAT2	—	—	—
FPDAT3	G7	P2DAT3	—	—	—	G7	P2DAT3	—	—	—
FPDAT4	G6	P2DAT4	—	—	—	G6	P2DAT4	—	—	—
FPDAT5	G5	P2DAT5	—	—	—	G5	P2DAT5	—	—	—
FPDAT6	B7	P2DAT6	—	—	—	B7	P2DAT6	—	—	—
FPDAT7	B6	P2DAT7	—	—	—	B6	P2DAT7	—	—	—
FPDAT8	B5	P2DAT8	—	—	—	B5	P2DAT8	—	—	—
FPDAT9	R4	P2DAT9	—	—	—	R4	P2DAT9	—	—	—
FPDAT10	R3	P2DAT10	—	—	—	R3	P2DAT10	—	—	—
FPDAT11	R2	P2DAT11	—	—	—	R2	P2DAT11	—	—	—
FPDAT12	G4	P2DAT12	—	—	—	G4	P2DAT12	—	—	—
FPDAT13	G3	P2DAT13	—	—	—	G3	P2DAT13	—	—	—
FPDAT14	G2	P2DAT14	—	—	—	G2	P2DAT14	—	—	—
FPDAT15	B4	P2DAT15	—	—	—	B4	P2DAT15	—	—	—
FPDAT16	B3	P2DAT16	—	—	—	B3	P2DAT16	—	—	—
FPDAT17	B2	P2DAT17	—	—	—	B2	P2DAT17	—	—	—
FPDAT18 (GPIOP0)	—	—	TVDT0	TVDT0	TVDT0	R1	P2DAT18	—	—	—
FPDAT19 (GPIOP1)	—	—	TVDT1	TVDT1	TVDT1	R0	P2DAT19	—	—	—
FPDAT20 (GPIOP2)	—	—	TVDT2	TVDT2	TVDT2	G1	P2DAT20	—	—	—
FPDAT21 (GPIOP3)	—	—	TVDT3	TVDT3	TVDT3	G0	P2DAT21	—	—	—
FPDAT22 (GPIOP4)	—	—	TVDT4	TVDT4	TVDT4	B1	P2DAT22	—	—	—
FPDAT23 (GPIOP5)	—	—	TVDT5	TVDT5	TVDT5	B0	P2DAT23	—	—	—
GPIOP6	—	—	TVDT6	TVDT6	TVDT6	—	—	—	—	—
GPIOP7	—	—	TVDT7	TVDT7	TVDT7	—	—	—	—	—
GPIOP8	—	—	TVHS	—	TVDC	—	—	—	—	—
GPIOP9	—	—	TVFLD	—	TVWR#	—	—	—	—	—
GPIOP10	—	—	TVCLK	TVCLK	TVRD#	—	—	—	—	—
GPIOP11	—	—	—	—	TVCS#	—	—	—	—	—
GPIOP12	—	—	—	—	TVTE	—	—	—	—	—
GPIOP13	—	—	—	—	—	—	—	—	—	—
GPIOP14	—	FPVS2 (IO)	—	—	—	—	FPVS2 (IO)	—	—	—
GPIOH0	—	—	—	—	—	—	—	—	—	TVTE
GPIOH1	—	—	—	—	—	—	—	—	—	TVCS#
GPIOH2	—	—	—	—	—	—	—	TVDT0	TVDT0	TVDT0
GPIOH3	—	—	—	—	—	—	—	TVDT1	TVDT1	TVDT1
GPIOH4	—	—	—	—	—	—	—	TVDT2	TVDT2	TVDT2
GPIOH5	—	—	—	—	—	—	—	TVDT3	TVDT3	TVDT3
GPIOH6	—	—	—	—	—	—	—	TVDT4	TVDT4	TVDT4
GPIOH7	—	—	—	—	—	—	—	TVDT5	TVDT5	TVDT5
GPIOH8	—	—	—	—	—	—	—	TVDT6	TVDT6	TVDT6
GPIOH9	—	—	—	—	—	—	—	TVDT7	TVDT7	TVDT7
GPIOH10	—	—	—	—	—	—	—	TVHS	—	TVDC
GPIOH11	—	—	—	—	—	—	—	TVFLD	—	TVWR#
GPIOH12	—	—	—	—	—	—	—	TVCLK	TVCLK	TVRD#
GPIOH13-23	—	—	—	—	—	—	—	—	—	—

Note

In Mode 2-2, when Indirect Host interface is used, TV-Out cannot be used.

When REG[0104h] bits 1-0 = 10b.

Table 4-14: LCD and TV-Out Interface Pin Mapping Mode 3

Pin Name	Mode 3-1					Mode 3-2					Mode 3-3				
	LCD1 RGB	LCD2	TV-Out I/F			LCD1 RGB	LCD2	TV-Out I/F			LCD1 RGB	LCD2	TV-Out I/F		
	I/F	Parallel I/F	HS&FD I/F	BT656 I/F	MPU I/F	I/F	Parallel I/F	HS&FD I/F	BT656 I/F	MPU I/F	I/F	Parallel I/F	HS&FD I/F	BT656 I/F	MPU I/F
FPCS1#	SCS1	—	—	—	—	SCS1	—	—	—	—	SCS1	—	—	—	—
FPCS2#	—	P2CS#	—	—	—	—	—	—	—	—	—	—	—	—	—
FPSCLK	SCK	—	—	—	—	SCK	—	—	—	—	SCK	—	—	—	—
FPSA0	SA0	—	—	—	—	SA0	—	—	—	—	SA0	—	—	—	—
FPSO	SDO	—	—	—	—	SD0	—	—	—	—	SD0	—	—	—	—
FPFRAME	VSYNC	—	—	—	—	VSYNC	—	—	—	—	VSYNC	—	—	—	—
FPLINE	HSYNC	—	—	—	—	HSYNC	—	—	—	—	HSYNC	—	—	—	—
FPSHIFT	DCK	—	—	—	—	DCK	—	—	—	—	DCK	—	—	—	—
FPDRDY	ENAB	—	—	—	—	ENAB	—	—	—	—	ENAB	—	—	—	—
FPDAT0	R7	—	—	—	—	R7	—	—	—	—	R7	—	—	—	—
FPDAT1	R6	—	—	—	—	R6	—	—	—	—	R6	—	—	—	—
FPDAT2	R5	—	—	—	—	R5	—	—	—	—	R5	—	—	—	—
FPDAT3	G7	—	—	—	—	G7	—	—	—	—	G7	—	—	—	—
FPDAT4	G6	—	—	—	—	G6	—	—	—	—	G6	—	—	—	—
FPDAT5	G5	—	—	—	—	G5	—	—	—	—	G5	—	—	—	—
FPDAT6	B7	—	—	—	—	B7	—	—	—	—	B7	—	—	—	—
FPDAT7	B6	—	—	—	—	B6	—	—	—	—	B6	—	—	—	—
FPDAT8	B5	—	—	—	—	B5	—	—	—	—	B5	—	—	—	—
FPDAT9	R4	—	—	—	—	R4	—	—	—	—	R4	—	—	—	—
FPDAT10	R3	—	—	—	—	R3	—	—	—	—	R3	—	—	—	—
FPDAT11	R2	—	—	—	—	R2	—	—	—	—	R2	—	—	—	—
FPDAT12	G4	—	—	—	—	G4	—	—	—	—	G4	—	—	—	—
FPDAT13	G3	—	—	—	—	G3	—	—	—	—	G3	—	—	—	—
FPDAT14	G2	—	—	—	—	G2	—	—	—	—	G2	—	—	—	—
FPDAT15	B4	—	—	—	—	B4	—	—	—	—	B4	—	—	—	—
FPDAT16	B3	—	—	—	—	B3	—	—	—	—	B3	—	—	—	—
FPDAT17	B2	—	—	—	—	B2	—	—	—	—	B2	—	—	—	—
FPDAT18 (GPIOP0)	—	P2DAT0	—	—	—	R1	—	—	—	—	—	—	TVDT0	TVDT0	TVDT0
FPDAT19 (GPIOP1)	—	P2DAT1	—	—	—	R0	—	—	—	—	—	—	TVDT1	TVDT1	TVDT1
FPDAT20 (GPIOP2)	—	P2DAT2	—	—	—	G1	—	—	—	—	—	—	TVDT2	TVDT2	TVDT2
FPDAT21 (GPIOP3)	—	P2DAT3	—	—	—	G0	—	—	—	—	—	—	TVDT3	TVDT3	TVDT3
FPDAT22 (GPIOP4)	—	P2DAT4	—	—	—	B1	—	—	—	—	—	—	TVDT4	TVDT4	TVDT4
FPDAT23 (GPIOP5)	—	P2DAT5	—	—	—	B0	—	—	—	—	—	—	TVDT5	TVDT5	TVDT5
GPIOP6	—	P2DAT6	—	—	—	—	—	—	—	—	—	—	TVDT6	TVDT6	TVDT6
GPIOP7	—	P2DAT7	—	—	—	—	—	—	—	—	—	—	TVDT7	TVDT7	TVDT7
GPIOP8	—	P2A0	—	—	—	—	—	—	—	—	—	—	TVHS	—	TVDC
GPIOP9	—	P2WR#	—	—	—	—	—	—	—	—	—	—	TVFLD	—	TVWR#
GPIOP10	—	—	—	—	—	—	—	—	—	—	—	—	TVCLK	TVCLK	TVRD#
GPIOP11	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TVCS#
GPIOP12	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TVTE
GPIOP13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GPIOP14	—	FPVS2 (IO)	—	—	—	—	FPVS2 (IO)	—	—	—	—	FPVS2 (IO)	—	—	—
GPIOH0	—	—	—	—	TVTE	—	—	—	—	TVTE	—	—			
GPIOH1	—	—	—	—	TVCS#	—	—	—	—	TVCS#	—	—			
GPIOH2	—	—	TVDT0	TVDT0	TVDT0	—	—	TVDT0	TVDT0	TVDT0	—	—			
GPIOH3	—	—	TVDT1	TVDT1	TVDT1	—	—	TVDT1	TVDT1	TVDT1	—	—			
GPIOH4	—	—	TVDT2	TVDT2	TVDT2	—	—	TVDT2	TVDT2	TVDT2	—	—			
GPIOH5	—	—	TVDT3	TVDT3	TVDT3	—	—	TVDT3	TVDT3	TVDT3	—	—			
GPIOH6	—	—	TVDT4	TVDT4	TVDT4	—	—	TVDT4	TVDT4	TVDT4	—	—			
GPIOH7	—	—	TVDT5	TVDT5	TVDT5	—	—	TVDT5	TVDT5	TVDT5	—	—			
GPIOH8	—	—	TVDT6	TVDT6	TVDT6	—	—	TVDT6	TVDT6	TVDT6	—	—			
GPIOH9	—	—	TVDT7	TVDT7	TVDT7	—	—	TVDT7	TVDT7	TVDT7	—	—			
GPIOH10	—	—	TVHS	—	TVDC	—	—	TVHS	—	TVDC	—	—			
GPIOH11	—	—	TVFLD	—	TVWR#	—	—	TVFLD	—	TVWR#	—	—			
GPIOH12	—	—	TVCLK	TVCLK	TVRD#	—	—	TVCLK	TVCLK	TVRD#	—	—			
GPIOH13	—	—	—	—	—	—	P2DAT0	—	—	—	—	P2DAT0	—	—	—
GPIOH14	—	—	—	—	—	—	P2DAT1	—	—	—	—	P2DAT1	—	—	—
GPIOH15	—	—	—	—	—	—	P2DAT2	—	—	—	—	P2DAT2	—	—	—
GPIOH16	—	—	—	—	—	—	P2DAT3	—	—	—	—	P2DAT3	—	—	—
GPIOH17	—	—	—	—	—	—	P2DAT4	—	—	—	—	P2DAT4	—	—	—
GPIOH18	—	—	—	—	—	—	P2DAT5	—	—	—	—	P2DAT5	—	—	—
GPIOH19	—	—	—	—	—	—	P2DAT6	—	—	—	—	P2DAT6	—	—	—
GPIOH20	—	—	—	—	—	—	P2DAT7	—	—	—	—	P2DAT7	—	—	—
GPIOH21	—	—	—	—	—	—	P2A0	—	—	—	—	P2A0	—	—	—
GPIOH22	—	—	—	—	—	—	P2WR#	—	—	—	—	P2WR#	—	—	—
GPIOH23	—	—	—	—	—	—	P2CS#	—	—	—	—	P2CS#	—	—	—

Note

1. In Mode 3-1, when Indirect Host interface is used, TV-Out cannot be used.
2. In Mode 3-2, when Indirect Host interface is used, LCD2 / TV-Out cannot be used.
3. In Mode 3-3, when Indirect Host interface is used, LCD2 cannot be used.
4. For Mode 3-2 or Mode 3-3, the FPCS2# pin (which is unused) will toggle during LCD2 activity.

4.7 GPIO Pin Mapping

When the GPIOP[14:0] and GPIOH[23:0] pins are not used as their alternate functions, the pins are available as general purpose IO pins.

Table 4-15: GPIOP Pin Mapping

Pin Name	REG[0104h] bit 5 = 1b	REG[0104h] bit 5 = 0b				REG[018Ch] bit 13 = 1b
		REG[0200h] bits 1-0 = 01b & REG[0200h] bit 2 = 0b	REG[0200h] bits 1-0 = 10b & REG[0200h] bit 2 = 0b	REG[0200h] bits 1-0 = 11b & REG[0200h] bit 2 = 0b	REG[0104h] bits 1-0 = 10b & REG[0104h] bit 2 = 0b	
GPIOP0	R1	TVDT0	TVDT0	TVDT0	P2DAT0	—
GPIOP1	R0	TVDT1	TVDT1	TVDT1	P2DAT1	—
GPIOP2	G1	TVDT2	TVDT2	TVDT2	P2DAT2	—
GPIOP3	G0	TVDT3	TVDT3	TVDT3	P2DAT3	—
GPIOP4	B1	TVDT4	TVDT4	TVDT4	P2DAT4	—
GPIOP5	B0	TVDT5	TVDT5	TVDT5	P2DAT5	—
GPIOP6	—	TVDT6	TVDT6	TVDT6	P2DAT6	—
GPIOP7	—	TVDT7	TVDT7	TVDT7	P2DAT7	—
GPIOP8	—	TVHS	TVDC	—	P2A0	—
GPIOP9	—	TVFLD	TVWR#	—	P2WR#	—
GPIOP10	—	TVCLK	TVRD#	TVCLK	—	—
GPIOP11	—	—	TVCS#	—	—	—
GPIOP12	—	—	TVTE	—	—	—
GPIOP13	—	—	—	—	—	—
GPIOP14	—	—	—	—	—	FPVS2

Table 4-16: GPIOH Pin Mapping

Pin Name	CNF0 = H	CNF0 = L			
		REG[0200h] bits 1-0 = 01b & REG[0200h] bit 2 = 1b	REG[0200h] bits 1-0 = 10b & REG[0200h] bit 2 = 1b	REG[0200h] bits 1-0 = 11b & REG[0200h] bit 2 = 1b	REG[0104h] bits 1-0 = 10b & REG[0104h] bit 2 = 1b
GPIOH0	—	—	TVTE	—	—
GPIOH1	—	—	TVCS#	—	—
GPIOH2	DB0	TVDT0	TVDT0	TVDT0	—
GPIOH3	DB1	TVDT1	TVDT1	TVDT1	—
GPIOH4	DB2	TVDT2	TVDT2	TVDT2	—
GPIOH5	DB3	TVDT3	TVDT3	TVDT3	—
GPIOH6	DB4	TVDT4	TVDT4	TVDT4	—
GPIOH7	DB5	TVDT5	TVDT5	TVDT5	—
GPIOH8	DB6	TVDT6	TVDT6	TVDT6	—
GPIOH9	DB7	TVDT7	TVDT7	TVDT7	—
GPIOH10	DB8	TVHS	TVDC	—	—
GPIOH11	DB9	TVFLD	TVWR#	—	—
GPIOH12	DB10	TVCLK	TVRD#	TVCLK	—
GPIOH13	DB11	—	—	—	P2DAT0
GPIOH14	DB12	—	—	—	P2DAT1
GPIOH15	DB13	—	—	—	P2DAT2
GPIOH16	DB14	—	—	—	P2DAT3
GPIOH17	DB15	—	—	—	P2DAT4
GPIOH18	DB16	—	—	—	P2DAT5
GPIOH19	DB17	—	—	—	P2DAT6
GPIOH20	D/C#	—	—	—	P2DAT7
GPIOH21	RD#	—	—	—	P2A0
GPIOH22	WR#	—	—	—	P2WR#
GPIOH23	CS#	—	—	—	P2CS#

5 D.C. Characteristics

5.1 Absolute Maximum Ratings

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
COREVDD	Core Supply Voltage	-0.3 ~ 2.5	V
DRAMVDD	DRAM Supply Voltage	-0.3 ~ 2.5	V
DRAMVCC	DRAM Supply Voltage	-0.3 ~ 3.5	V
PLLVDD	PLL Supply Voltage	-0.3 ~ 2.5	V
CORE18VDD	Core Supply Voltage (1.8V)	-0.3 ~ 3.5	V
HIOVDD	Host IO Supply Voltage	-0.3 ~ 3.5	V
PIOVDD	Panel IO Supply Voltage	-0.3 ~ 3.5	V
OSCVDD	OSC Supply Voltage	-0.3 ~ 3.5	V
Vin_io	Digital Input Signal Voltage	-0.3 ~ HIOVDD + 0.3 -0.3 ~ PIOVDD + 0.3	V
Iin_io	Digital Input Signal Current	±10	mA
Vout_io	Digital Output Signal Voltage	-0.3 ~ HIOVDD + 0.3 -0.3 ~ PIOVDD + 0.3	V
Iout_io	Digital Output Signal Current	±30	mA
Tstg	Storage Temperature	-65 ~ 150	°C

5.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
COREVDD	Core Supply Voltage (1.5V)	VSS=0V	1.40	1.50	1.60	V
DRAMVDD	DRAM Supply Voltage	VSS=0V	1.40	1.50	1.60	V
DRAMVCC	DRAM Supply Voltage	VSS=0V	2.30	2.50	2.70	V
PLLVDD	PLL Supply Voltage	VSS=0V	1.40	1.50	1.60	V
CORE18VDD	Core Supply Voltage (1.8V)	VSS=0V	1.70	1.80	1.90	V
HIOVDD	Host IO Supply Voltage	VSS=0V	1.70	1.80	1.90	V
			2.30	2.50	2.70	
PIOVDD	Panel IO Supply Voltage	VSS=0V	1.70	1.80	1.90	V
			2.30	2.50	2.70	
OSCVDD	OSC Supply Voltage	VSS=0V	2.30	2.50	2.70	V
Vin	Input Voltage	VSS=0V	VSS	—	HIOVDD PIOVDD	V
Topr	Operating Temperature	VSS=0V	-20	25	85	°C

5.3 Electrical Characteristics

Table 5-3: Electrical Characteristics for Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
IQ_CORE	Core Quiescent Current	Quiescent Condition	—	22.2	—	µA
IQ_DRAMVDD	DRAMVDD Quiescent Current	Quiescent Condition	—	3.9	—	µA
IQ_DRAMVCC	DRAMVCC Quiescent Current	Quiescent Condition	—	1.8	—	µA
IQ_PLL	PLLVDD Quiescent Current	Quiescent Condition	—	1.2	—	µA
IQ_CORE18	CORE18VDD Quiescent Current	Quiescent Condition	—	0.1	—	µA
IQ_IO	HIOVDD + PIOVDD Quiescent Current	Quiescent Condition	—	0.4	—	µA
IQ_OSC	OSCVDD Quiescent Current	Quiescent Condition	—	0.1	—	µA
I_CORE	COREVDD Operational Current	Note 1	—	11.0	—	mA
I_DRAMVDD	DRAMVDD Operational Current	Note 1	—	1.6	—	mA
I_DRAMVCC	DRAMVCC Operational Current	Note 1	—	0.5	—	mA
I_PLL	PLLVDD Operational Current	PLL output clock frequency (fck) = 71MHz	—	1.8	—	mA
I_CORE18	CORE18VDD Operational Current	Note 1	—	0.1	—	µA
I_OSC	OSCVDD Operational Current	OSC clock frequency = 27MHz	—	2.6	—	mA
I_IZ	Input Leakage Current	Vin = VDD or Vin = VSS	-10	—	10	µA
I_OZ	Output Leakage Current	Vin = VDD or Vin = VSS	-10	—	10	µA
HIOVOH	High Level output voltage1	HIOVDD=min	(0.8 HIOVDD)	—	—	V
PIOVOH	High Level output voltage1	HIOVDD=min	(0.8 PIOVDD)	—	—	V
HIOVOL	High Level output voltage1	HIOVDD=min	-	—	(0.2 HIOVDD)	V
PIOVOL	High Level output voltage1	PIOVDD=min	-	—	(0.2 PIOVDD)	V
HIOVIH	High Level input voltage	CMOS input	(0.7 HIOVDD)	—	—	V
PIOVIH	High Level input voltage	CMOS input	(0.7 PIOVDD)	—	—	V
HIOVIL	Low Level input voltage	CMOS input	—	—	(0.3 HIOVDD)	V
PIOVIL	Low Level input voltage	CMOS input	—	—	(0.3 PIOVDD)	V
HIOVT+	Positive Trigger voltage	CMOS Schmitt (Note 2)	—	1.4	—	V
HIOVT-	Negative Trigger voltage	CMOS Schmitt (Note 2)	—	1.0	—	V
HIOVH	Hysteresis Voltage	CMOS Schmitt (Note 2)	—	0.4	—	V

Table 5-3: Electrical Characteristics for Recommended Operating Conditions

Rpu	Pull-up Resistance	Vi=VSS (PIOVDD, HIOVDD = 2.5V)	10	—	200	KΩ
		Vi=VSS (PIOVDD, HIOVDD = 1.8V)	20	—	210	
Rpd	Pull-down Resistance	Vi=VDD (PIOVDD, HIOVDD = 2.5V)	10	—	200	KΩ
		Vi=VDD (PIOVDD, HIOVDD = 1.8V)	20	—	210	
Cio	Pin Capacitance	f=1MHz, VDD=0V	—	3.8	—	pF

Note

1. 480x800 24-bit TFT Panel
   System Clock = 71MHz
   Pixel Clock = System Clock / 3
   RGB 8:8:8, Main Window Path
2. The Schmitt characteristics are effective only at HIOVDD=2.5V.

6 A.C. Characteristics

Conditions for HIOVDD = PIOVDD = 1.70 ~ 1.90V
T_A = -20 to 85 °C
CL = 30pF (Host Interface, LCD Interface, GPIO Interface)

Conditions for HIOVDD = PIOVDD = 2.30 ~ 2.70V
TA = -20 to 85 °C
CL = 30pF (Host Interface, LCD Interface, GPIO Interface)

Note

For the Indirect Host, LCD, TV-Out, and Video Input interface timing, the transition point between logic high and logic low is one half (1/2) of IOVDD.

6.1 Output Signal Rise/Fall Timing

Multi-drive IO cells (LO_DSEL, LB_DSEL, LBU_DSEL, and LBD_DSEL) have the following rise/fall timing. For more information on IO cells, see Section 4.2, "Pin Descriptions" on page 18.

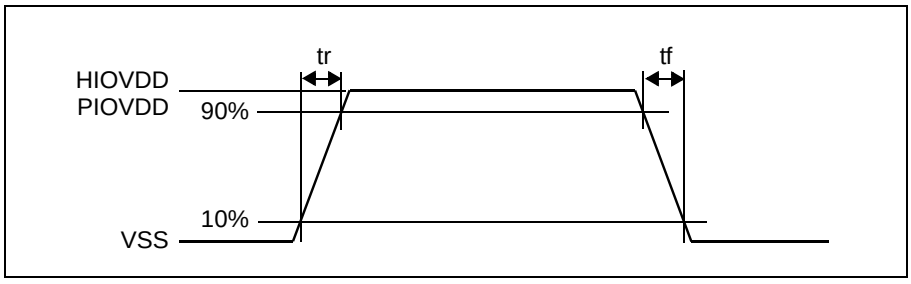


Figure 6-1: Output Signal Rise/Fall Timing

Table 6-1: Output Signal Rise/Fall Timing

Symbol	Parameter	Condition Output Drive Level (REG[0018h])	IOVDD = 1.8V		IOVDD = 2.5V		Units
			Typ	Max	Typ	Max	
tr	Output rise time (10%-90%)	11b (max)	3.2	7.4	2.6	4.8	ns
		10b	4.0	9.2	3.2	6.6	ns
		01b	8.8	20.0	6.4	14.0	ns
		00b (min)	18.0	42.0	12.6	28.0	ns
tf	Output fall time (10%-90%)	11b (max)	2.8	7.4	2.4	4.6	ns
		10b	3.6	9.2	2.8	5.6	ns
		01b	9.8	26.0	7.4	16.0	ns
		00b (min)	19.6	52.0	14.0	32.0	ns

1. CL = 30pF. Values in the table scale linearly based on the load capacitance. For example, when CL is 15pF, tr and tf will be one half (1/2) of the value in the table.

6.2 Clock Timing

6.2.1 CLKI Input Timing (PLL Used)

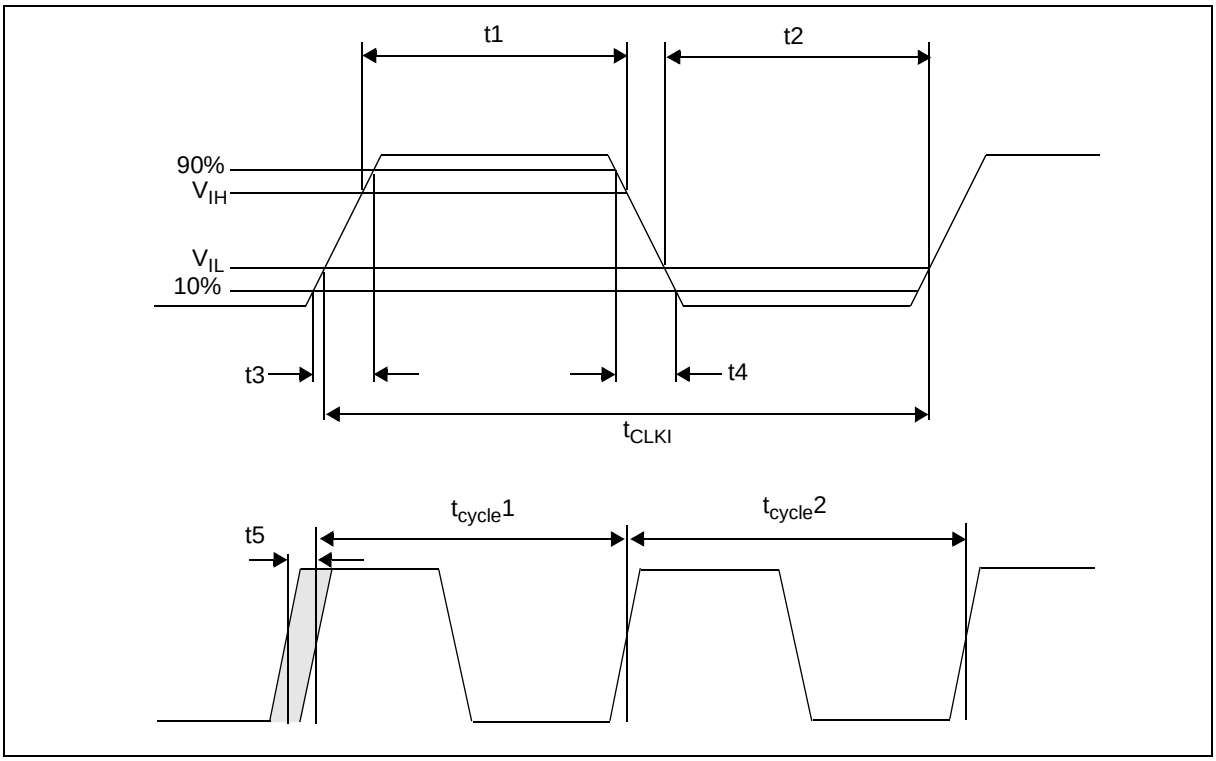


Figure 6-2 Clock Input Requirements (CLKI when PLL used)

Table 6-2: Clock Input Requirements (CLKI when PLL used)

Symbol	Parameter	Min	Typ	Max	Units
Fclki	Input Clock Frequency	1	27	40	MHz
Tclki	Input Clock Period	—	1/Fclki	—	ns
t1	Input Clock Pulse Width high	0.4 Fclki	—	0.6 Fclki	ns
t2	Input Clock Pulse Width Low	0.4 Fclki	—	0.6 Fclki	ns
t3	Input Clock rise time (10%-90%)	—	—	5.0	ns
t4	Input Clock fall time (90%-10%)	—	—	5.0	ns
t5	Input Clock Period Jitter	-400	—	400	ps
t6	Input Clock Cycle Jitter	-400	—	400	ps

1. Input Clock comes from the external Oscillator (CLKI).
2. t5 and t6 are requirements for PLL input and are not required when the PLL is not used.
3. t6 = tcycle1 - tcycle2
4. Input Duty cycle is not critical and can be 40/60.
5. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
6. The input clock cycle jitter is the difference in period between adjacent cycles.
7. The jitter characteristics must satisfy both the t5 and t6 characteristics.
8. When the TV-Out interface is HSYNC & FIELD or ITU-R BT656 (REG[0200h] bits 1-0 =01b, 11b), it is necessary to input 27MHz frequency to CLKI or OSCI/OSCO.

6.2.2 CLKI Input Timing (PLL Bypassed)

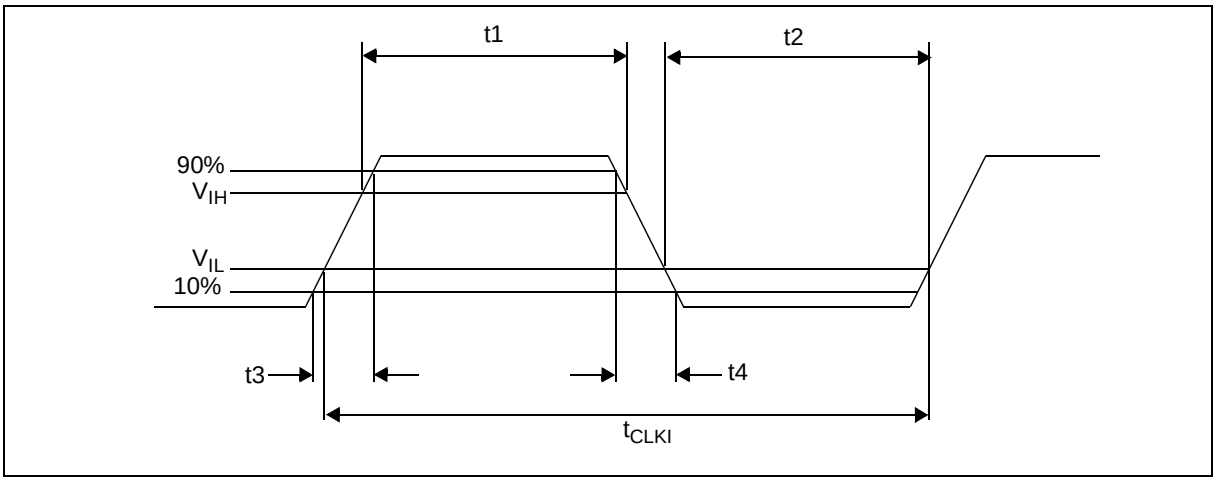


Figure 6-3 Clock Input Requirements (CLKI when PLL bypassed)

Table 6-3: Clock Input Requirements (CLKI when PLL bypassed)

Symbol	Parameter	Min	Typ	Max	Units
Fclki	Input Clock Frequency	40	—	71	MHz
Tclki	Input Clock Period	—	1/Fclki	—	ns
t1	Input Clock Pulse Width high	0.4 Fclki	—	0.6 Fclki	ns
t2	Input Clock Pulse Width Low	0.4 Fclki	—	0.6 Fclki	ns
t3	Input Clock rise time (10%-90%)	—	—	5.0	ns
t4	Input Clock fall time (90%-10%)	—	—	5.0	ns

1. Input Clock comes from the external Oscillator (CLKI).
2. Input Duty cycle is not critical and can be 40/60.
3. When the TV-Out interface is HSYNC & FIELD or ITU-R BT656 (REG[0200h] bits 1-0 = 01b, 11b), PLL bypass mode is not supported.

6.2.3 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

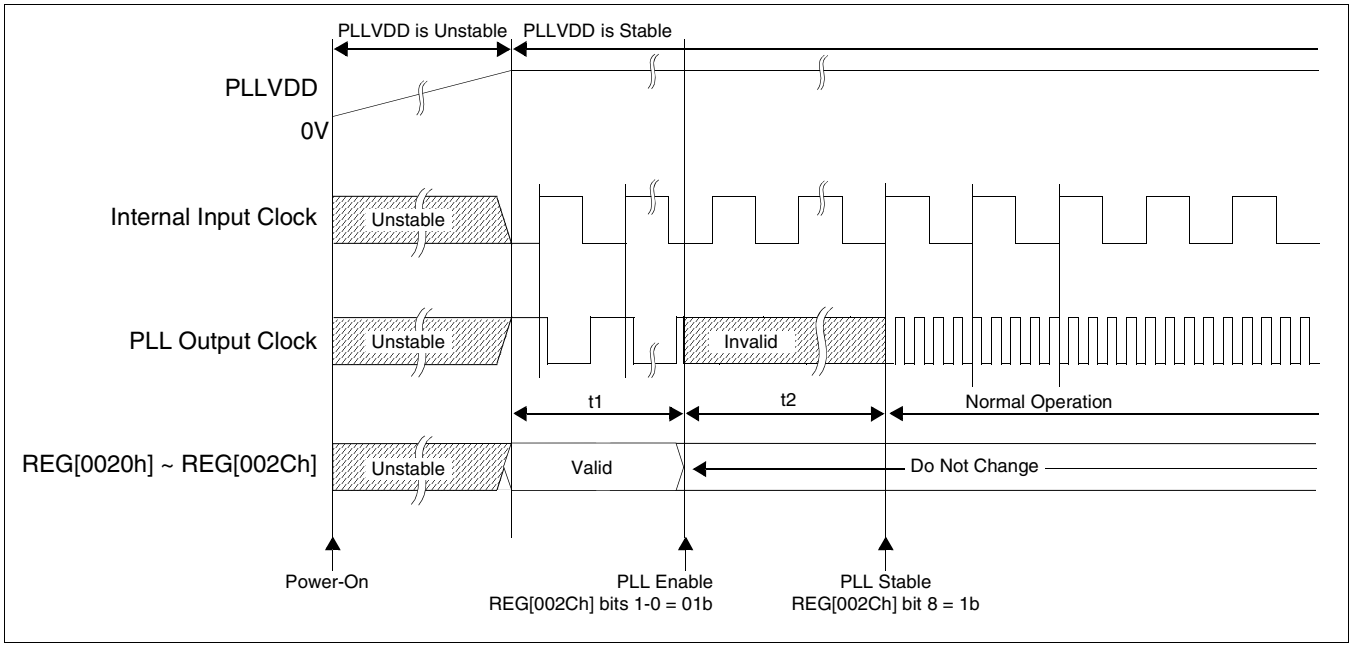


Figure 6-4: PLL Start-up

Table 6-4: PLL Start-up

Symbol	Parameter	Min	Typ	Max	Units
t1	PLL Bypass / PLL register programming for initialization	—	—	Note	—
t2	PLL Lock time	—	—	1.5	ms
Fckout	PLL Output Clock Frequency	40	—	71	MHz
Jperiod	PLL Output Clock Period Jitter (Note 2)	-400	—	400	ps

1. t1 is determined by the Host Interface cycle time required to program the PLL registers.
2. The PLL output clock period jitter is the displacement relative to the center period. The center period is set using the PLL setting registers (REG[0020h] ~ REG[0024h]) and has the same frequency tolerance as the input clock (CLKI or OSCI/OSCO).

6.3 Power Supply Sequence

6.3.1 Power-On Sequence

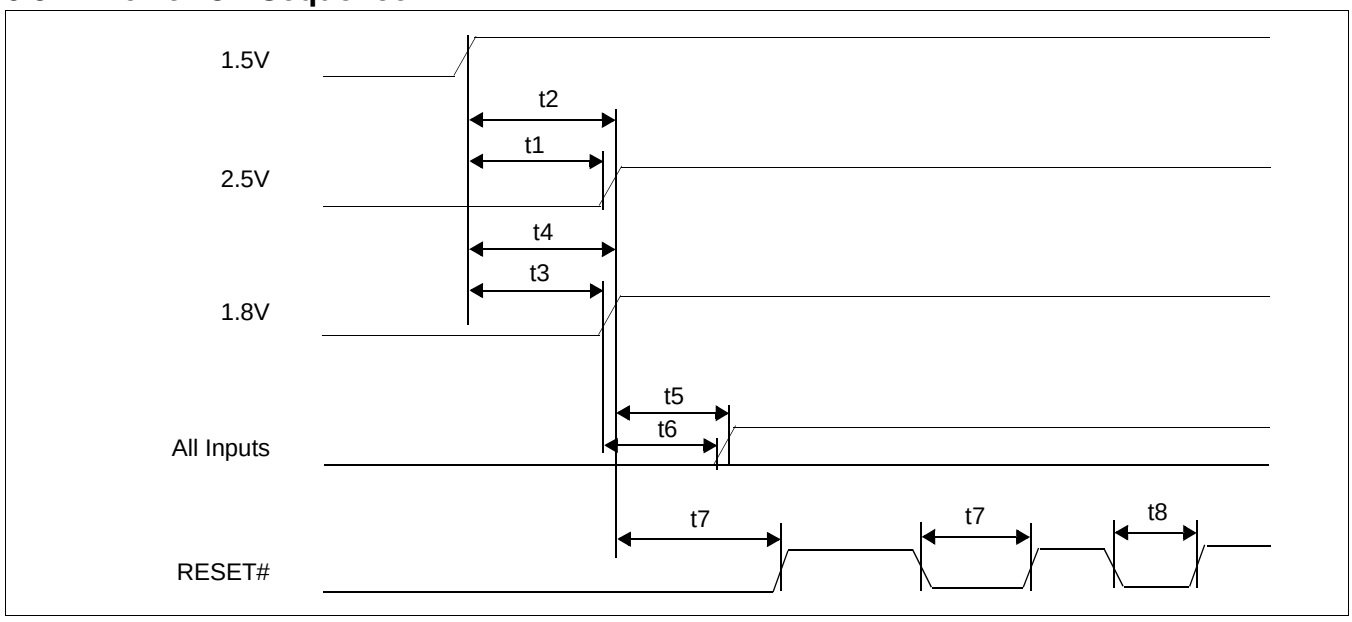


Figure 6-5: Power-On Sequence

Table 6-5: Power-On Sequence

Symbol	Parameter	Min	Typ	Max	Units
t1	1.5V_VDD rise (1.2V) to 2.5V_VDD rise (0.25V)	0 (Note 1)	—	—	ms
t2	1.5V_VDD rise (1.2V) to 2.5V_VDD rise (2.0V)	—	—	100 (Note 2)	ms
t3	1.5V_VDD rise (1.2V) to 1.8V_VDD rise (0.18V)	0 (Note 1)	—	—	ms
t4	1.5V_VDD rise (1.2V) to 1.8V_VDD rise (1.44V)	—	—	100 (Note 2)	ms
t5	When PIOVDD/HIOVDD = 1.8V , 1.8V_VDD rise (0.36V) to All inputs rise (0.36V)	0 (Note 1)	—	—	ms
	When PIOVDD/HIOVDD= 2.5V , 2.5V_VDD rise (0.50V) to All inputs rise (0.50V)				
t6	When PIOVDD/HIOVDD = 1.8V , 1.8V_VDD rise (1.44V) to All inputs rise (1.44V)	0 (Note 1)	—	—	ms
	When PIOVDD/HIOVDD = 2.5V , 2.5V_VDD rise (2.00V) to All inputs rise (2.00V)				
t7	Active RESET# Pulse Width	Note 3	—	—	—
t8	RESET# Pulse Width to be ignored	—	—	Note 3	—

1. If the time is less than 0 ms, there will be shoot-through current. If the time is less than -1 ms, it will affect long term reliability.
2. During the time, there will be shoot-through current in the level shifter. If the time is longer than 100 ms, it will affect long term reliability.
3. These timings are controlled by external components. If no glitch rejection is required, the RRES pin should be left unconnected and CRES pin should be connected to VSS. In this case the RESET# line should be held low longer than 200ns to guarantee reset.

6.3.2 Power-Off Sequence

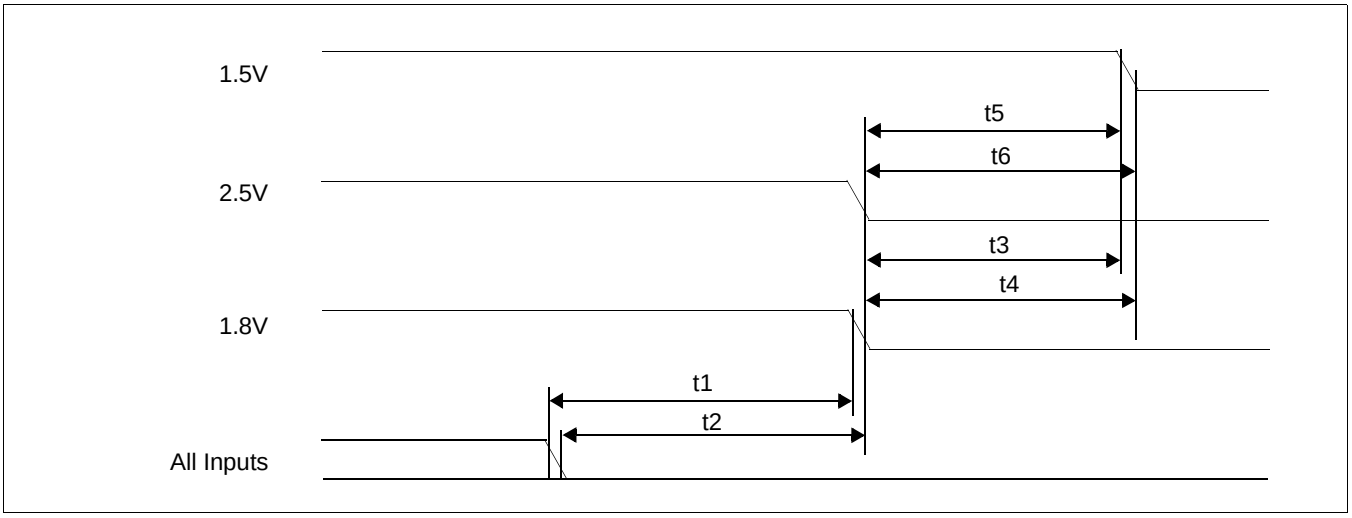


Figure 6-6: Power-Off Sequence

Table 6-6: Power-Off Sequence

Symbol	Parameter	Min	Typ	Max	Units
t1	When PIOVDD/HIOVDD = 1.8V, All inputs fall (1.44V) to 1.8V fall (1.44V)	0 (Note 1)	—	—	ms
	When PIOVDD/HIOVDD = 2.5V, All inputs fall (2.00V) to 2.5V fall (2.00V)				
t2	When PIOVDD/HIOVDD = 1.8V, All inputs fall (0.36V) to 1.8V fall (0.36V)	0 (Note 1)	—	—	ms
	When PIOVDD/HIOVDD = 2.5V, All inputs fall (0.50V) to 2.5V fall (0.50V)				
t3	1.8V_VDD fall (VSS) to 1.5V_VDD fall (1.2V)	0 (Note 1)	—	—	ms
t4	1.8V_VDD fall (VSS) to 1.5V_VDD fall (VSS)	—	—	100 (Note 2)	ms
t5	2.5V_VDD fall (VSS) to 1.5V_VDD fall (1.2V)	0 (Note 1)	—	—	ms
t6	2.5V_VDD fall (VSS) to 1.5V_VDD fall (VSS)	—	—	100 (Note 2)	ms

1. If the time is less than 0 ms, there will be shoot-through current. If the time is less than -1 ms, it will affect long term reliability.
2. During the time, there will be shoot-through current in the level shifter. If the time is longer than 100 ms, it will affect long term reliability.

6.4 Indirect Host Interface Timing

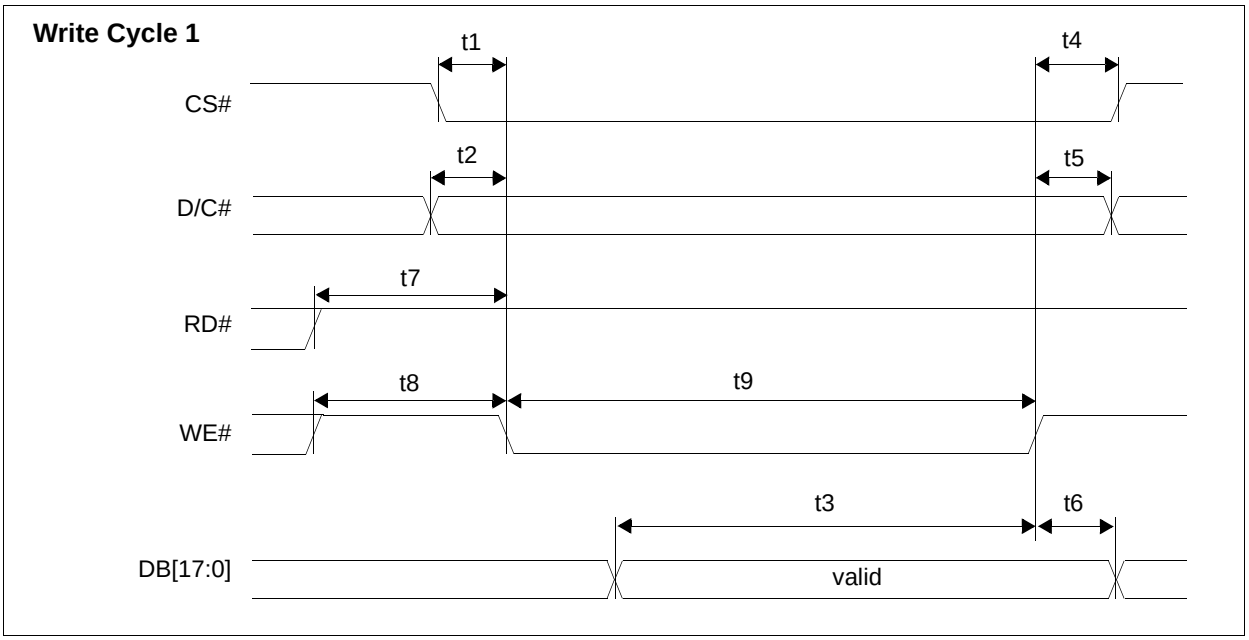


Figure 6-7: Indirect Interface Write Cycle 1

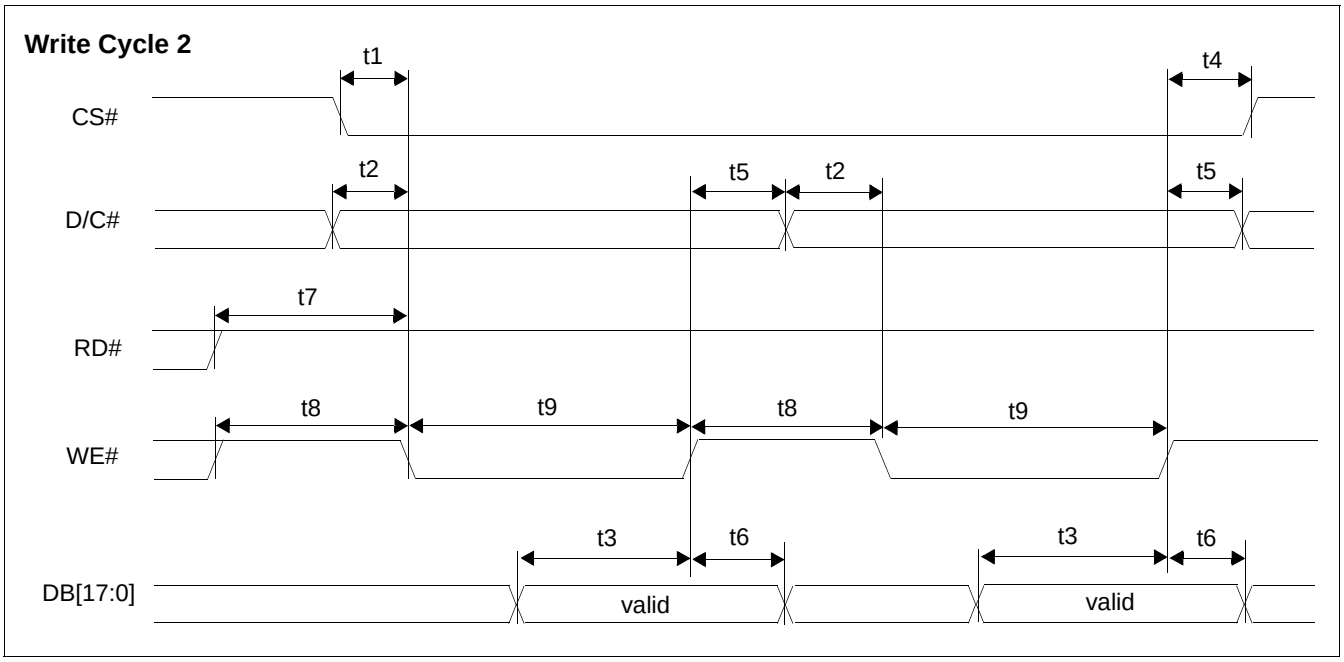


Figure 6-8: Indirect Interface Write Cycle 2

Table 6-7: Indirect Interface Write Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.5V		Units
		Min	Max	Min	Max	
t1	CS# setup time	2	—	2	—	ns
t2	D/C# setup time	2	—	2	—	ns
t3	DB[17:0] setup time	2	—	2	—	ns
t4	CS# hold time from WE# rising edge	2	—	2	—	ns
t5	D/C# hold time from WE# rising edge	2	—	2	—	ns
t6	DB[17:0] hold time from WE# rising edge	4	—	4	—	ns
t7	RD# rising edge to WE# falling edge	1	—	1	—	Ts (Note 1)
t8	WE# high width	1	—	1	—	Ts
t9	WE# low width	2	—	2	—	Ts

1. Ts = System Clock Period

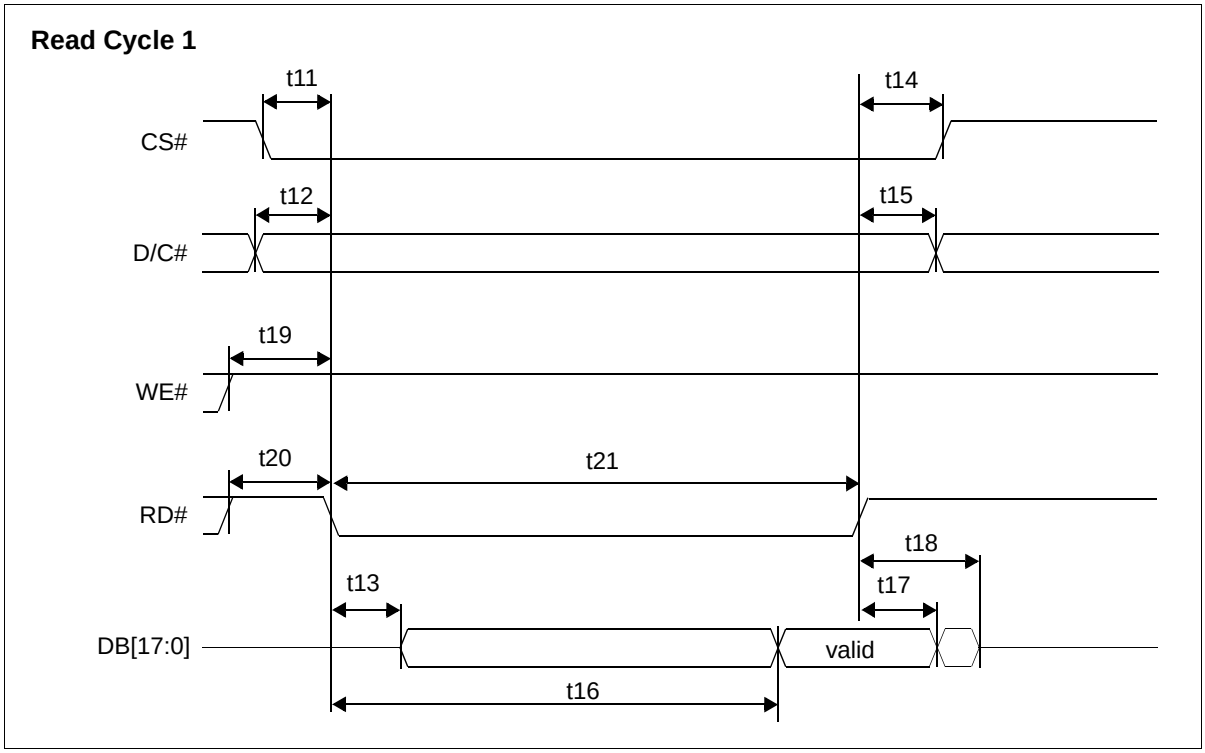


Figure 6-9: Indirect Interface Read Cycle 1

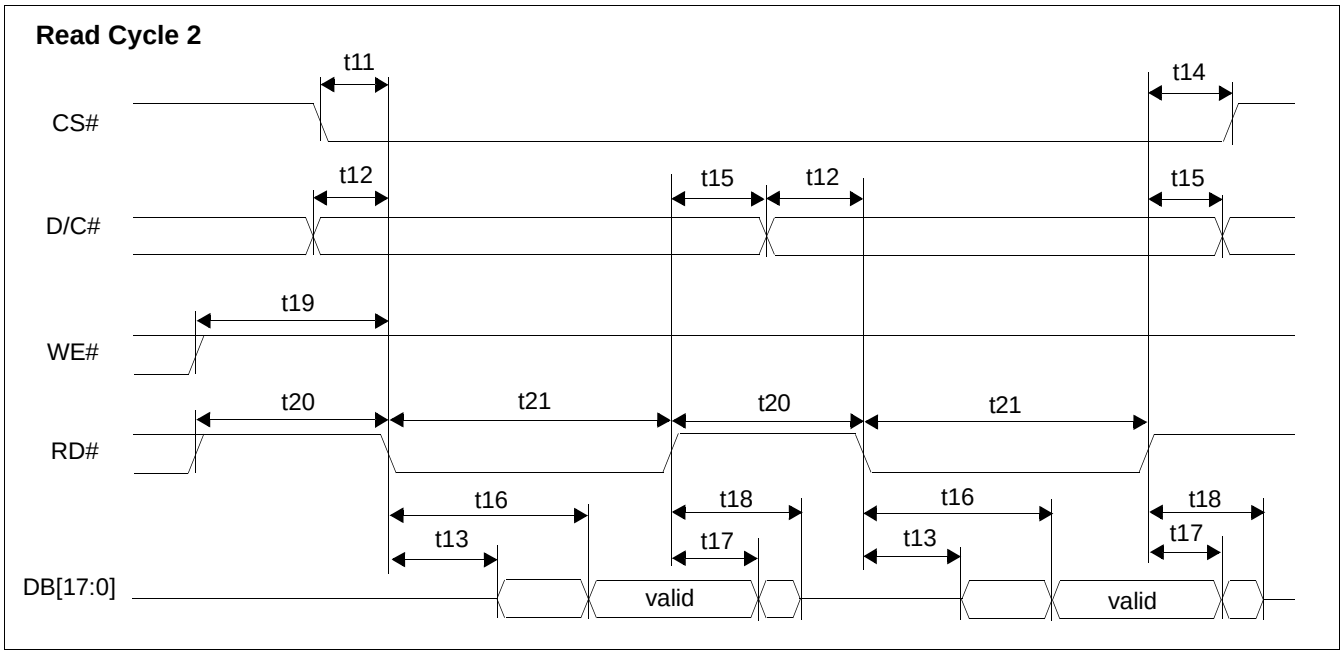


Figure 6-10: Indirect Interface Read Cycle 2

Table 6-8: Indirect Interface Read Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.5V		Units
		Min	Max	Min	Max	
t11	CS# setup time	2	—	2	—	ns
t12	D/C# setup time	2	—	2	—	ns
t13	RD# falling edge to DB[17:0] driven	2	—	2	—	ns
t14	CS# hold time from RD# rising edge	2	—	2	—	ns
t15	D/C# hold time from RD# rising edge	2	—	2	—	ns
t16	RD# falling edge to valid Data: for REG[0018h] bits 1-0 = 00b	—	32	—	23	ns
	for REG[0018h] bits 1-0 = 01b	—	23	—	16	ns
	for REG[0018h] bits 1-0 = 10b	—	16	—	12	ns
	for REG[0018h] bits 1-0 = 11b	—	15	—	11	ns
t17	DB[17:0] hold time from RD# rising edge	2	—	2	—	ns
t18	RD# rising edge to DB[17:0] release	—	11	—	9	ns
t19	WE# rising edge to RD# falling edge	1	—	1	—	Ts (Note 1)
t20	RD# high width	1	—	1	—	Ts
t21	RD# low width	2	—	2	—	Ts

1. Ts = System Clock Period

6.5 I2C Interface Timing

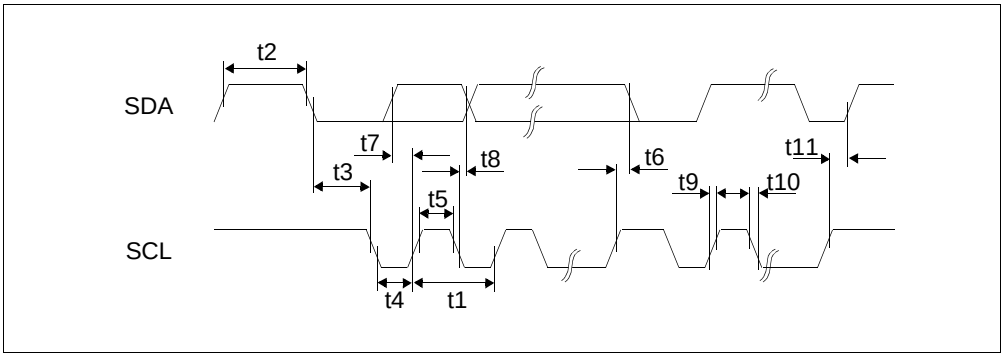


Figure 6-11: I2C Interface Timing

Table 6-9: I2C Interface Timing

Symbol	Parameter	HIOVDD=1.8V HIOVDD=2.5V		Units
		Min	Max	
t1	SCL Frequency	—	400	KHz
t2	Bus Free time between a STOP and START condition	1.3	—	µs
t3	Hold time for a START Condition	0.6	—	µs
t4	SCL Low Width	1.3	—	µs
t5	SCL High Width	0.6	—	µs
t6	Setup time for a repeated START Condition	0.6	—	µs
t7	SDA setup time from SCL Rising	100	—	ns
t8	SDA hold time to SCL Falling	0 (Note 1)	—	µs
t9	Rise Time of both SCL and SDA	—	300	ns
t10	Fall Time of both SCL and SDA	—	300	ns
t11	Setup time for a STOP Condition	0.6	—	µs

1. The I2C specification specifies a SDA hold time of 300ns. However, the S1D13774 I2C interface does not require a 300ns hold time.

6.6 Video Interface Timing

6.6.1 12-bit RGB Video Interface Timing

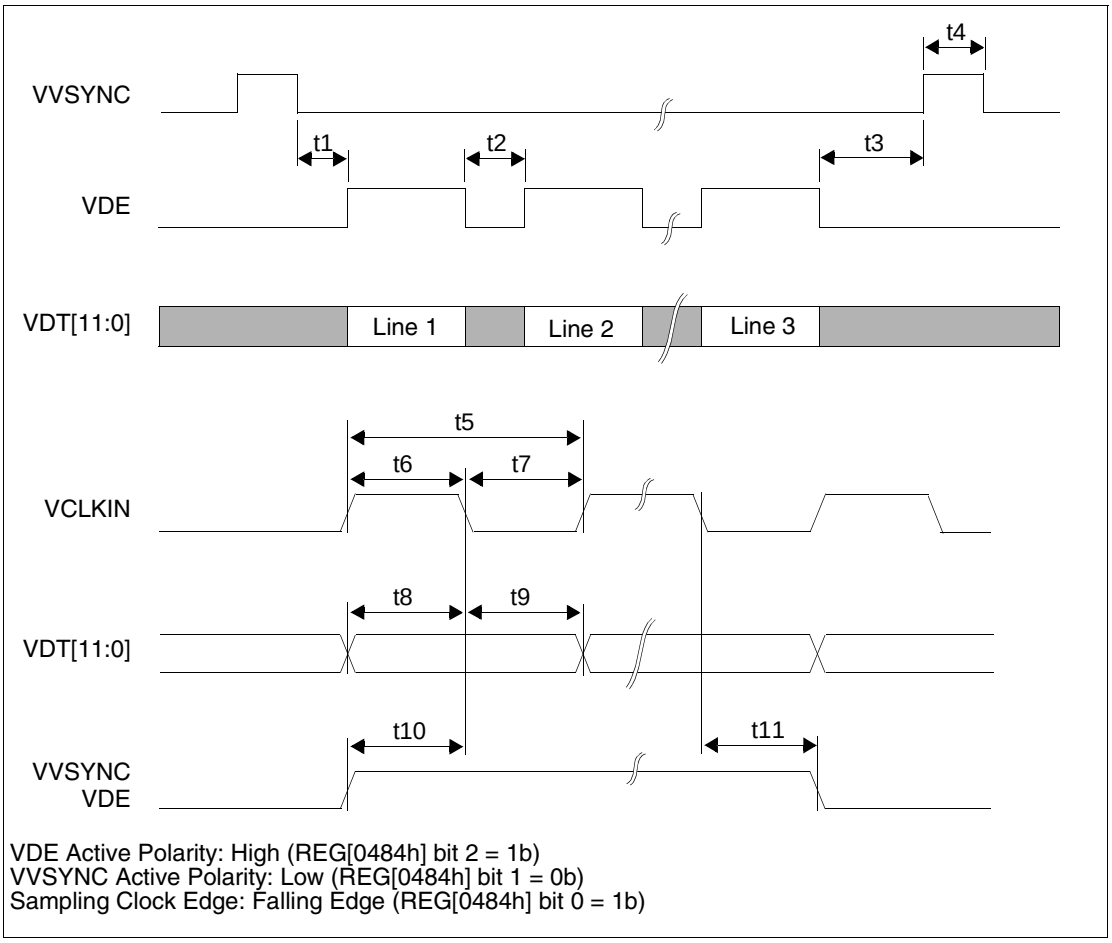


Figure 6-12: 12-bit RGB Video Interface Timing

Table 6-10: 12-bit RGB Video Interface Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.5V		Units
		Min	Max	Min	Max	
t1	VVSYNC falling edge to VDE rising edge	0	—	0	—	Tv (Note 1)
t2	Horizontal blank period	4	—	4	—	Tv
t3	VDE falling edge to VVSYNC rising edge	0	—	0	—	Tv
t4	Vertical blank period	4	—	4	—	Tv
t5	Input clock period	2	—	2	—	Ts (Note 2)
t6	Input clock pulse width high	1	—	1	—	Ts
t7	Input clock pulse width low	1	—	1	—	Ts
t8	Data setup time	5	—	5	—	ns
t9	Data hold time	5	—	5	—	ns
t10	VVSYNC, VDE setup time	5	—	5	—	ns
t11	VVSYNC, VDE hold time	5	—	5	—	ns

1. Tv is the video interface input clock period.
2. Ts is the system clock period.
3. t1+t3+t4 > 100Tv
   t1+t3+t4 > 16 Lines

6.6.2 8-bit YUV Video Interface Timing

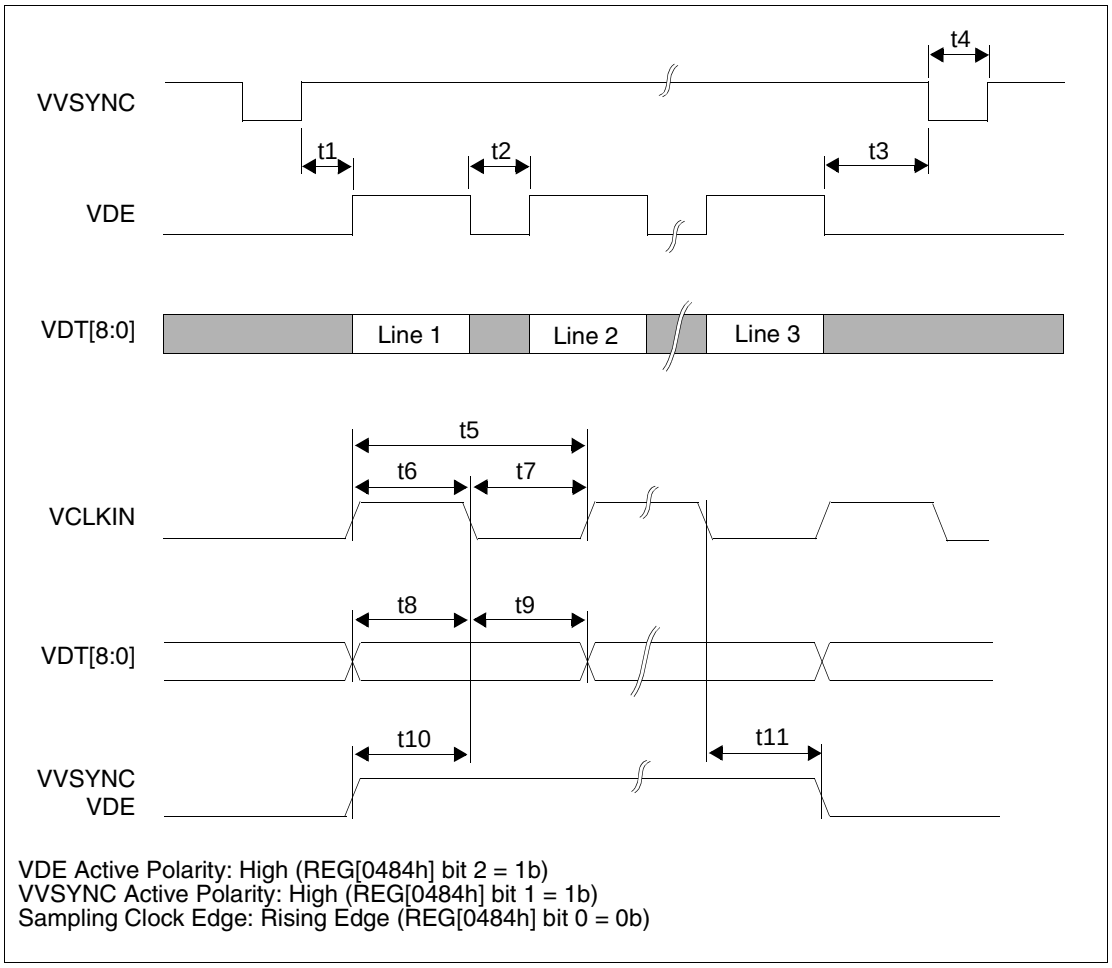


Figure 6-13: 8-bit YUV Video Interface Timing

Table 6-11: 8-bit YUV Video Interface Timing

Symbol	Parameter	HIOVDD = 1.8V		HIOVDD = 2.5V		Units
		Min	Max	Min	Max	
t1	VVSYNC falling edge to VDE rising edge	0	—	0	—	Tv (Note 1)
t2	Horizontal blank period	4	—	4	—	Tv
t3	VDE falling edge to VVSYNC rising edge	0	—	0	—	Tv
t4	Vertical blank period	4	—	4	—	Ts
t5	Input clock period	2	—	2	—	Ts (Note 2)
t6	Input clock pulse width high	1	—	1	—	Ts
t7	Input clock pulse width low	1	—	1	—	Ts
t8	Data setup time	5	—	5	—	ns
t9	Data hold time	5	—	5	—	ns
t10	VDE setup time	5	—	5	—	ns
t11	VDE hold time	5	—	5	—	ns

1. Tv is the video interface input clock period (VCLKIN).
2. Ts is the system clock period.
3. t1+t3+t4 > 100Tv
   t1+t3+t4 > 16 Lines

6.6.3 Video Interface Clock Output Timing

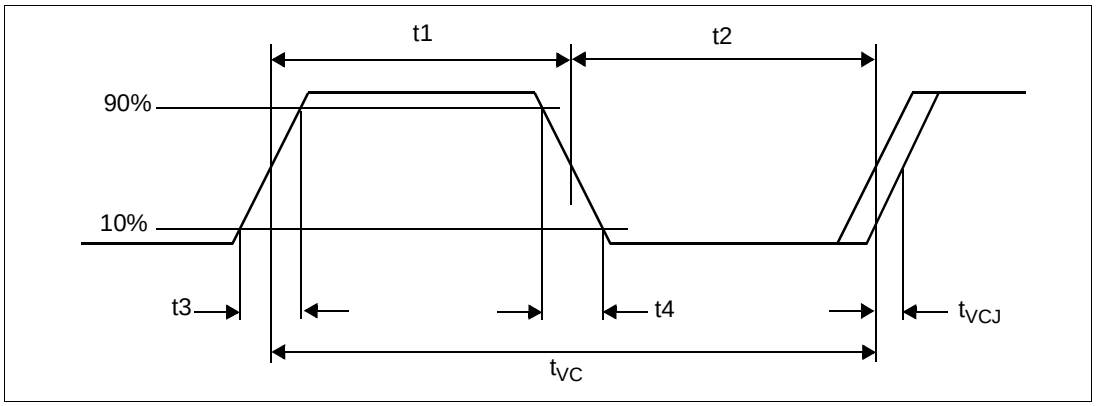


Figure 6-14: Video Clock Output Timing

Table 6-12: Video Clock Output Timing

Symbol	Parameter	HIOVDD = 1.8V			HIOVDD = 2.5V			units
		Min	Typ	Max	Min	Typ	Max	
Fvc	Video Clock Output Frequency	—	—	40 (Note 1)	—	—	40 (Note 1)	MHz
Tvc	Video Clock Output Period	—	1/Fvc	—	—	1/Fvc	—	ns
Tvcj	Video Clock Output Jitter	Note 2	—	Note 2	Note 2	—	Note 2	ps
t1	Output Clock Pulse Width high: REG[0018h] bits 9-8 = 11b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 9-8 = 10b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 9-8 = 01b	Note 5	—	Note 6	Note 5	—	Note 6	ns
	REG[0018h] bits 9-8 = 00b	Note 5	—	Note 6	Note 5	—	Note 6	ns
t2	Output Clock Pulse Width Low: REG[0018h] bits 9-8 = 11b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 9-8 = 10b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 9-8 = 01b	Note 5	—	Note 6	Note 5	—	Note 6	ns
	REG[0018h] bits 9-8 = 00b	Note 5	—	Note 6	Note 5	—	Note 6	ns
t3	Output Clock rise time (10%-90%)	Note 7			Note 7			ns
t4	Output Clock fall time (10%-90%)	Note 7			Note 7			ns

1. Fvcmax depends on tr and tf (see Section 6.1, “Output Signal Rise/Fall Timing” on page 45).
2. Tvcj = System Clock Jitter (±400ps) x Divide Rate (REG[0480h] bits 3-0)
   For example, when the divide rate = 4:1, Tvcj = 400ps x 4 = ±1600ps
3. When the Video Clock Output Divide is 1:1 (REG[0480h] bits 3-0 = 0h), the minimum pulse width = Tvc x 0.40. When the Video Clock Output Divide is not 1:1 (REG[0480h] bits 3-0 ≠ 0h), the minimum pulse width = Tvc x 0.45.
4. When the Video Clock Output Divide is 1:1 (REG[0480h] bits 3-0 = 0h), the maximum pulse width = Tvc x 0.60. When the Video Clock Output Divide is not 1:1 (REG[0480h] bits 3-0 ≠ 0h), the maximum pulse width = Tvc x 0.55.
5. t1min = Tvc x 0.40
   t2min = Tvc x 0.40
6. t1max = Tvc x 0.60
   t2max = Tvc x 0.60
7. Refer to Section 6.1, “Output Signal Rise/Fall Timing” on page 45.

6.7 Panel Interface Timing

6.7.1 LCD1 RGB Interface Panel Timing

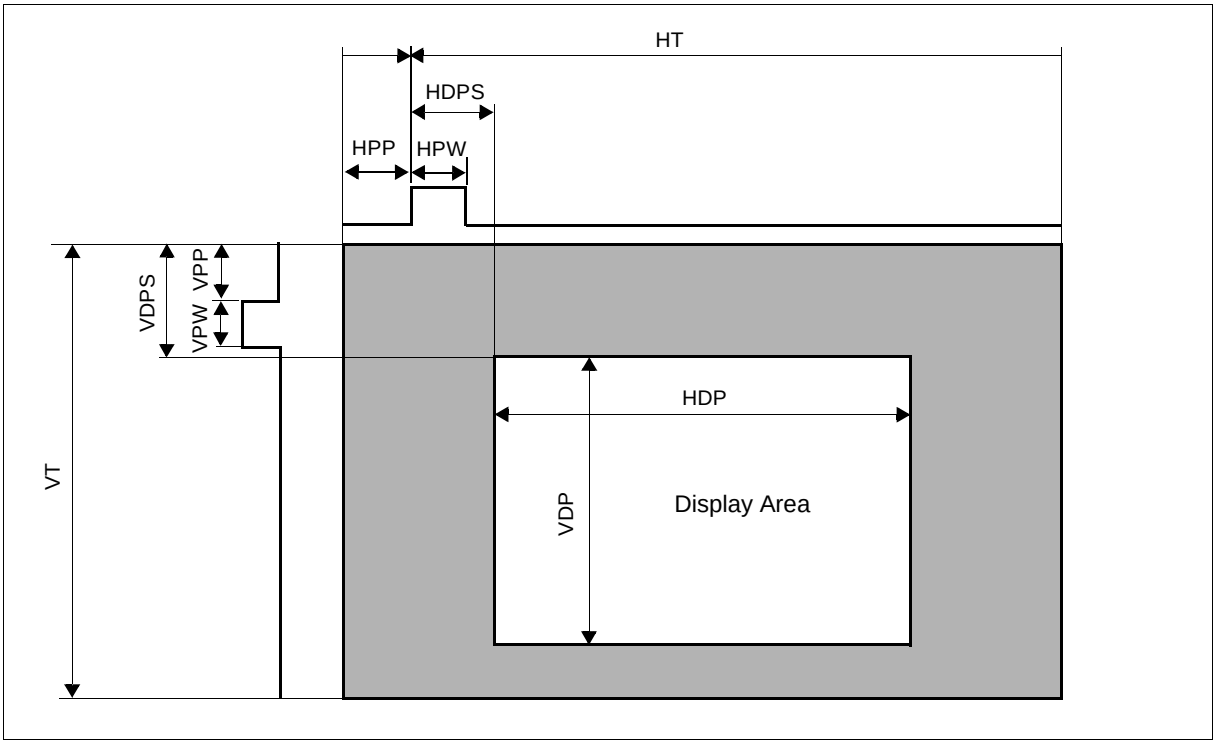


Figure 6-15: LCD1 RGB Interface Panel Timing

Table 6-13: LCD1 RGB Interface Panel Timing

Symbol	Description	Derived From	Units
HT	Horizontal Total	((REG[0140h] bits 6-0) + 1) x 8	Tp (Note 1)
HDP	Horizontal Display Period	((REG[0144h] bits 8-0) + 1) x 2	Tp
HDPS	Horizontal Display Period Start Position	(REG[0148h] bits 9-0) + 9	Tp
HPW	HSYNC Pulse Width	(REG[014Ch] bits 9-0) + 1	Tp
HPP	HSYNC Pulse Position	(REG[0150h] bits 9-0) + 1	Tp
VT	Vertical Total	(REG[0154h] bits 9-0) + 1	Lines
VDP	Vertical Display Period	(REG[0158h] bits 9-0) + 1	Lines
VDPS	Vertical Display Period Start Position	(REG[015Ch] bits 9-0)	Lines
VPW	VSYNC Pulse Width	(REG[0160h] bits 2-0) + 1	Lines
VPP	VSYNC Pulse Position	(REG[0164h] bits 9-0)	Lines

1. Tp = Pixel Clock Period
2. HT ≥ HDP + HDPS
3. VT > VDPS + VDP
4. VT - VDP ≥ 3

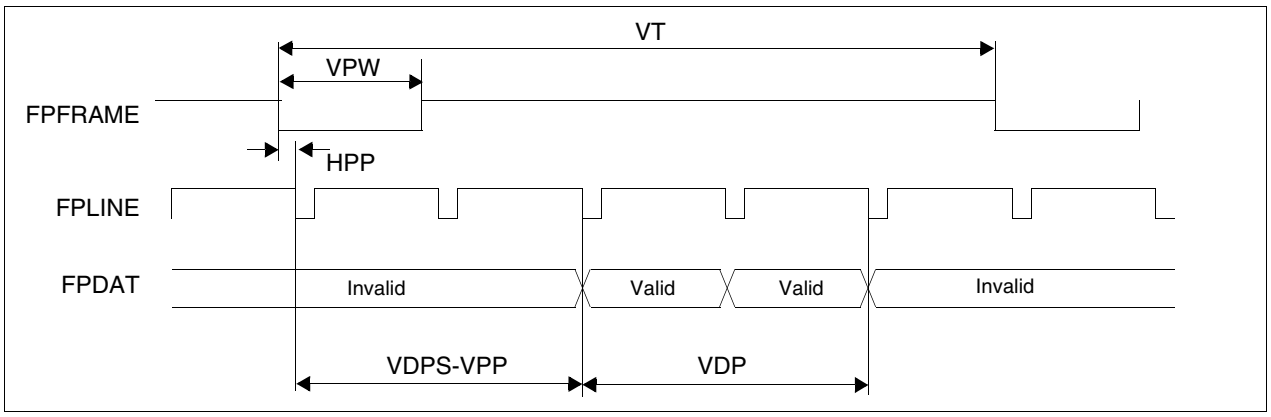


Figure 6-16: LCD1 RGB Interface Vertical Timing

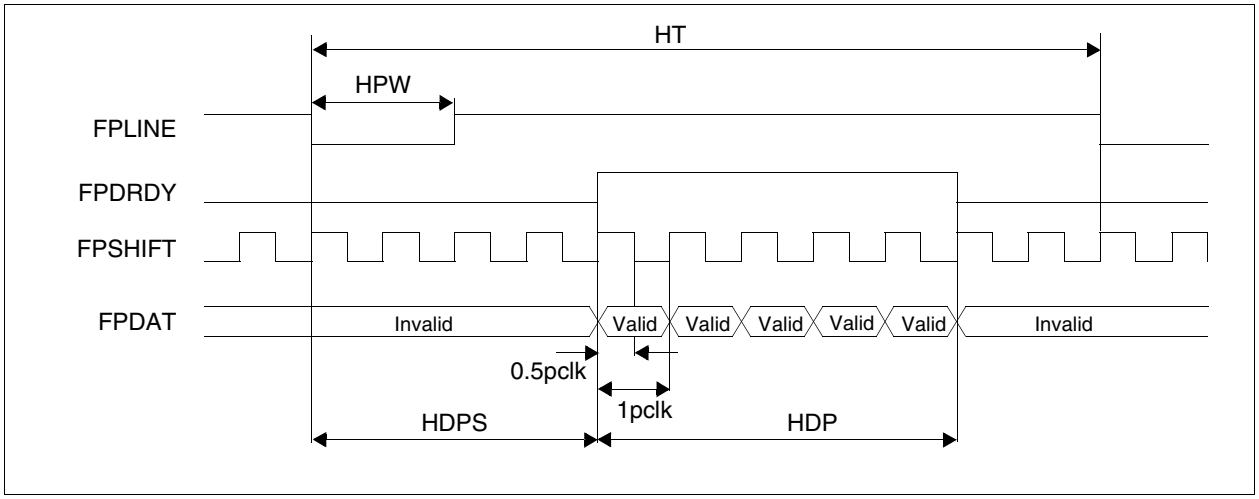


Figure 6-17: LCD1 RGB Interface Horizontal Timing

6.7.2 LCD1, LCD2 4 Wire 8-Bit Serial Interface Timing

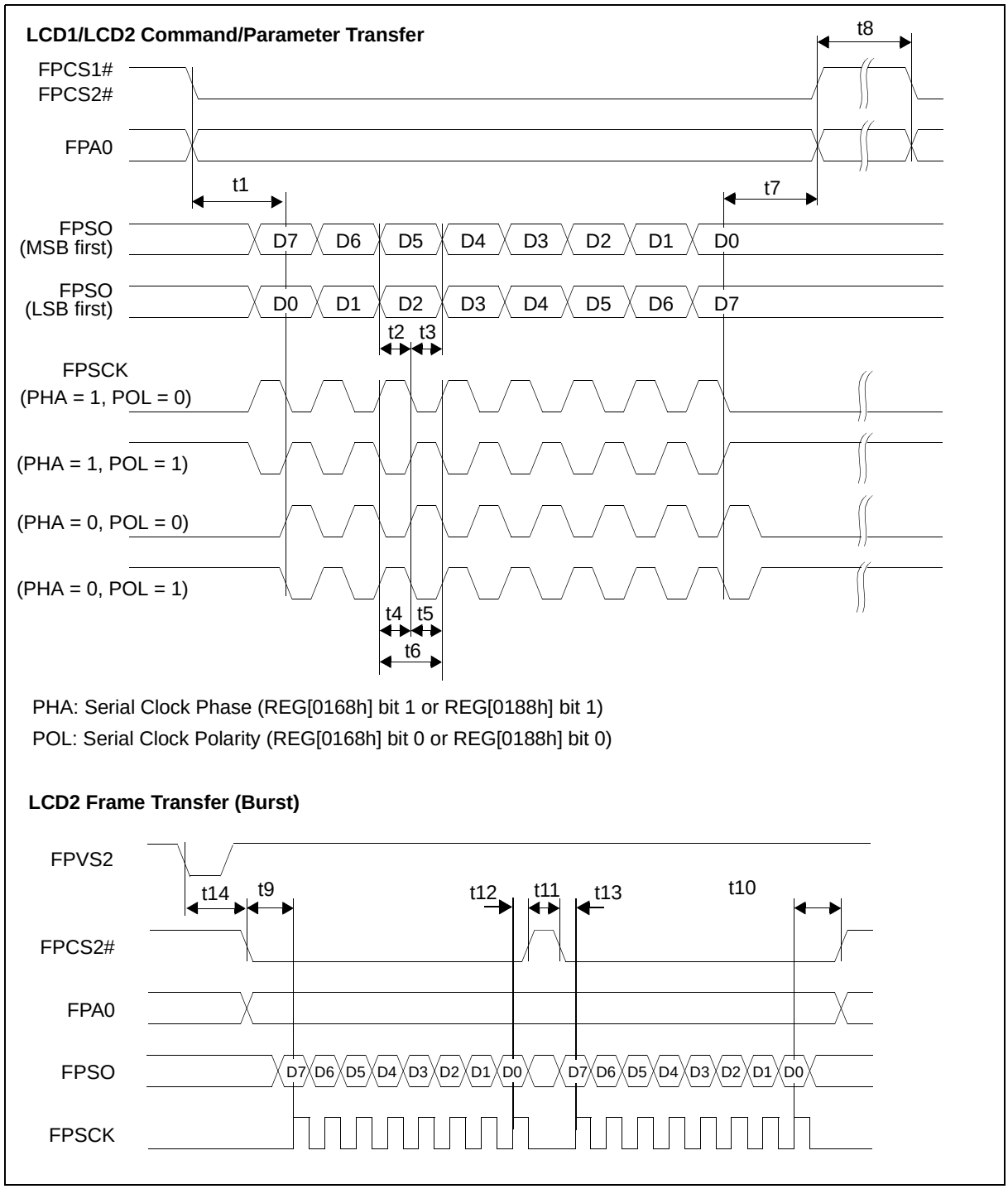


Figure 6-18: LCD1, LCD2 4 Wire 8-Bit Serial Interface Timing

Note

The LCD2 data width is determined by the LCD2 Serial Data Format bits, REG[0188h] bits 3-2.

Table 6-14: LCD1, LCD2 4 Wire 8-bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1.5	—	Ts (Note 1)
t2	Data setup time	—	0.5	—	Ts
t3	Data hold time	—	0.5	—	Ts
t4	Serial clock pulse width low (high)	—	0.5	—	Ts
t5	Serial clock pulse width high (low)	—	0.5	—	Ts
t6	Serial clock period	—	1.0	—	Ts
t7	Chip select hold time	—	1.5	—	Ts
t8	Chip select de-assert to reassert	—	1.0	—	Ts
t9	Chip select setup time at beginning of burst mode	—	1.5	—	Ts
t10	Chip select hold time at end of burst mode	—	2.5	—	Ts
t11	Chip select interval in burst mode	—	1.0	—	Ts
t12	Chip select hold time during burst mode	—	0.5	—	Ts
t13	Chip select setup time during burst mode	—	0.5	—	Ts
t14	FPVS2 falling edge to FPCS2# falling edge	—	—	Note 2	Ts

1. Ts = Serial clock period
2. t14max = (2 x HIS + 200) x Tsysclk + (27 x Tsclk)
   Where:
   - HIS is the largest Horizontal Image Size from the Main1, Main2, PIP1, an PIP2 windows (see REG[0690h], REG[06B4h], REG[072Ch], REG[082Ch]
   - Tsysclk is the system clock period
   - Tsclk is the serial clock period as specified by REG[0100h] bits 10-8

6.7.3 LCD1, LCD2 3 Wire 9-Bit Serial Interface Timing

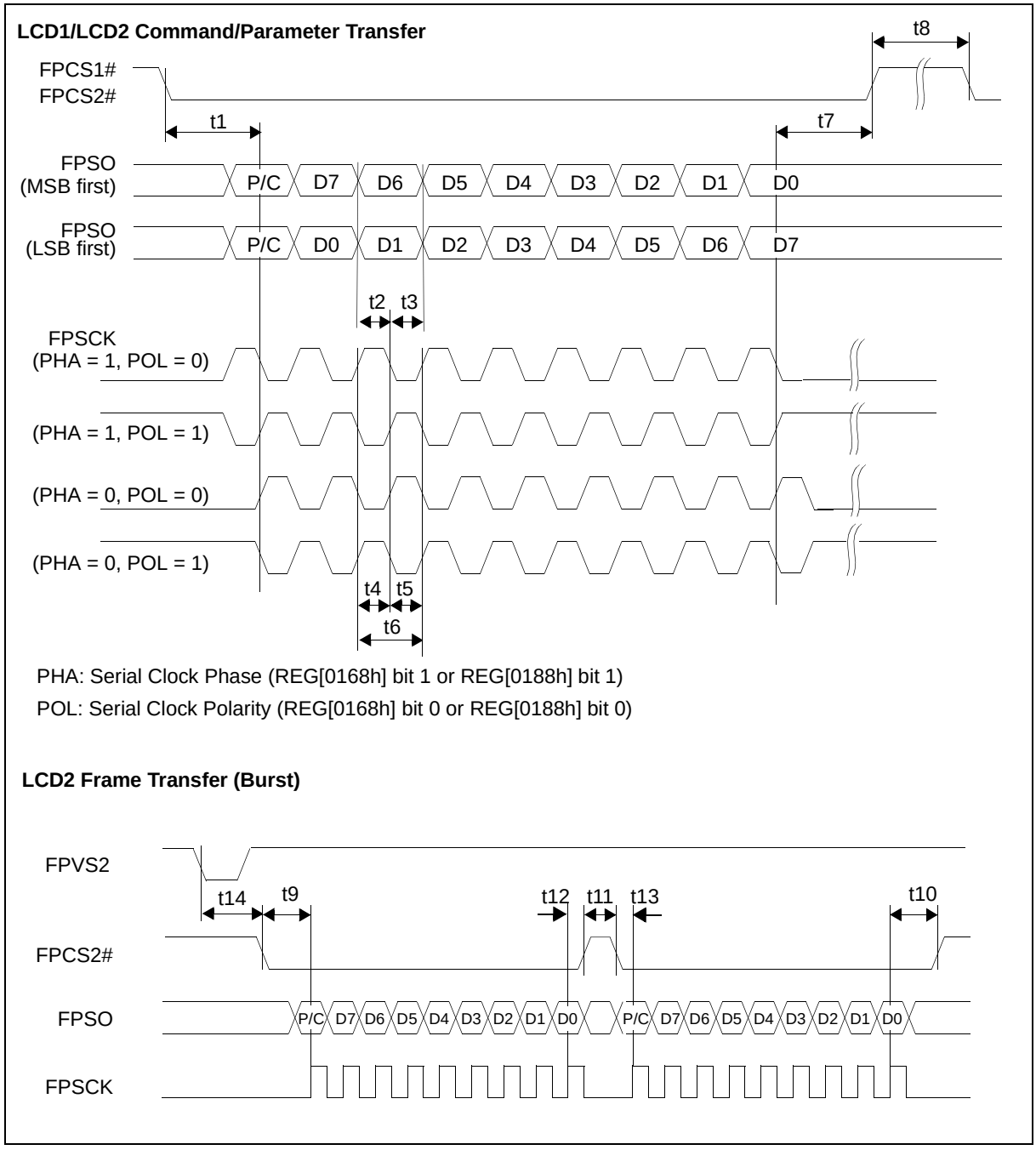


Figure 6-19: LCD1, LCD2 3 Wire 9-Bit Serial Interface Timing

Note

The LCD2 data width is determined by the LCD2 Serial Data Format bits, REG[0188h] bits 3-2.

Table 6-15: LCD1, LCD2 3 Wire 9-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1.5	—	Ts (Note 1)
t2	Data setup time	—	0.5	—	Ts
t3	Data hold time	—	0.5	—	Ts
t4	Serial clock pulse width low (high)	—	0.5	—	Ts
t5	Serial clock pulse width high (low)	—	0.5	—	Ts
t6	Serial clock period	—	1.0	—	Ts
t7	Chip select hold time	—	1.5	—	Ts
t8	Chip select de-assert to reassert	—	1.0	—	Ts
t9	Chip select setup time at beginning of burst mode	—	1.5	—	Ts
t10	Chip select hold time at end of burst mode	—	2.5	—	Ts
t11	Chip select interval in burst mode	—	1.0	—	Ts
t12	Chip select hold time during burst mode	—	0.5	—	Ts
t13	Chip select setup time during burst mode	—	0.5	—	Ts
t14	FPVS2 falling edge to FPCS2# falling edge	—	—	Note 2	Ts

1. Ts = Serial clock period
2. t14max = (2 x HIS + 200) x Tsysclk + (27 x Tsclk)
   Where:
   - HIS is the largest Horizontal Image Size from the Main1, Main2, PIP1, an PIP2 windows (see REG[0690h], REG[06B4h], REG[072Ch], REG[082Ch]
   - Tsysclk is the system clock period
   - Tsclk is the serial clock period as specified by REG[0100h] bits 10-8

6.7.4 LCD1 uWire Serial Interface Timing

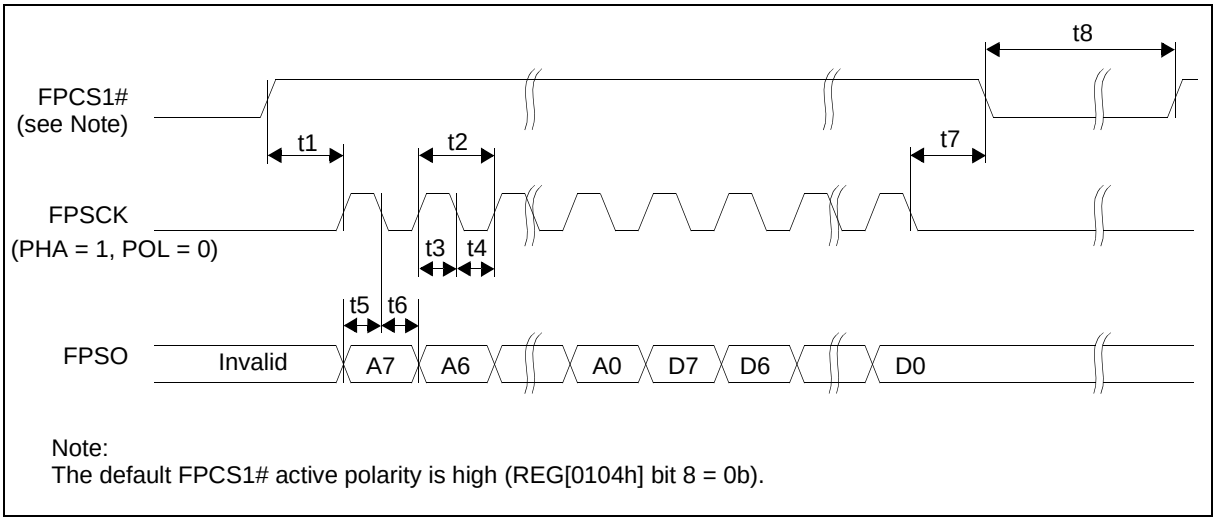


Figure 6-20: LCD1 uWIRE Serial Interface Timing

Table 6-16: LCD1 uWIRE Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1	—	Ts (Note 1)
t2	Serial clock period	—	1	—	Ts
t3	Serial clock pulse width low	—	0.5	—	Ts
t4	Serial clock pulse width high	—	0.5	—	Ts
t5	Data setup time	—	0.5	—	Ts
t6	Data hold time	—	0.5	—	Ts
t7	Chip select hold time	—	1.5	—	Ts
t8	Chip select de-assert to re-assert	—	Note 2	—	Ts

1. Ts = Serial clock period
2. This setting depends on software

Note

When a uWire panel is selected (REG[0168h] bits 7-5 = 10x), FPCS1# idles high until the first uWire transfer is started. After the first transfer, FPCS1# idles low.

6.7.5 LCD1, LCD2 24-bit Serial Interface Timing

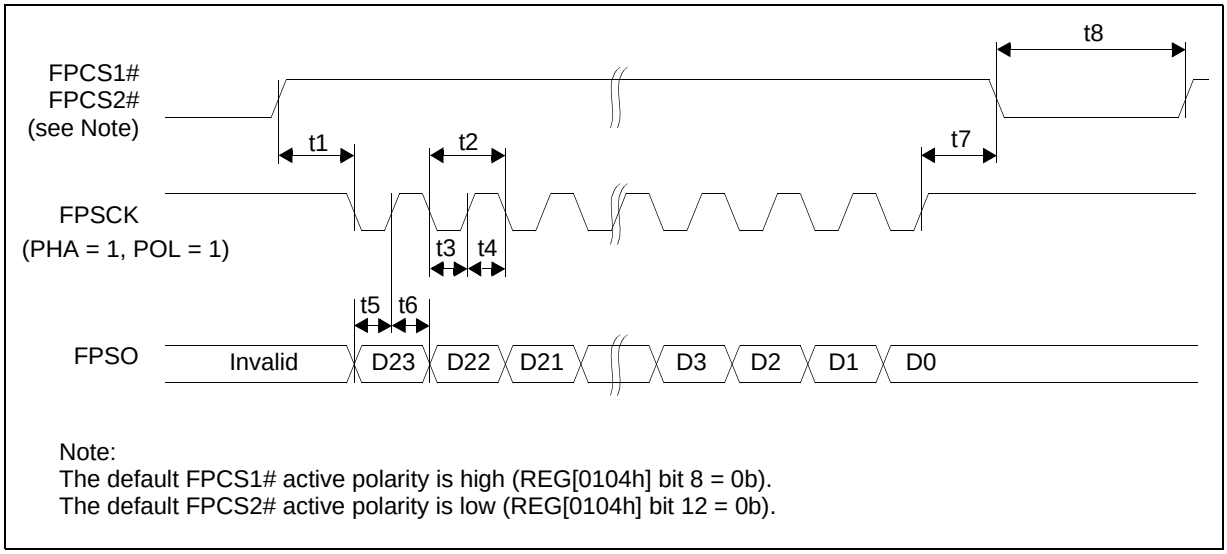


Figure 6-21: LCD1, LCD2 24-bit Serial Interface Timing

Table 6-17: LCD1, LCD2 24-bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	—	1	—	Ts (Note 1)
t2	Serial clock period	—	1	—	Ts
t3	Serial clock pulse width low	—	0.5	—	Ts
t4	Serial clock pulse width high	—	0.5	—	Ts
t5	Data setup time	—	0.5	—	Ts
t6	Data hold time	—	0.5	—	Ts
t7	Chip select hold time	—	1.5	—	Ts
t8	Chip select de-assert to re-assert	—	Note 2	—	Ts

1. Ts = Serial clock period
2. This setting depends on software

6.7.6 LCD2 Parallel Interface (80)

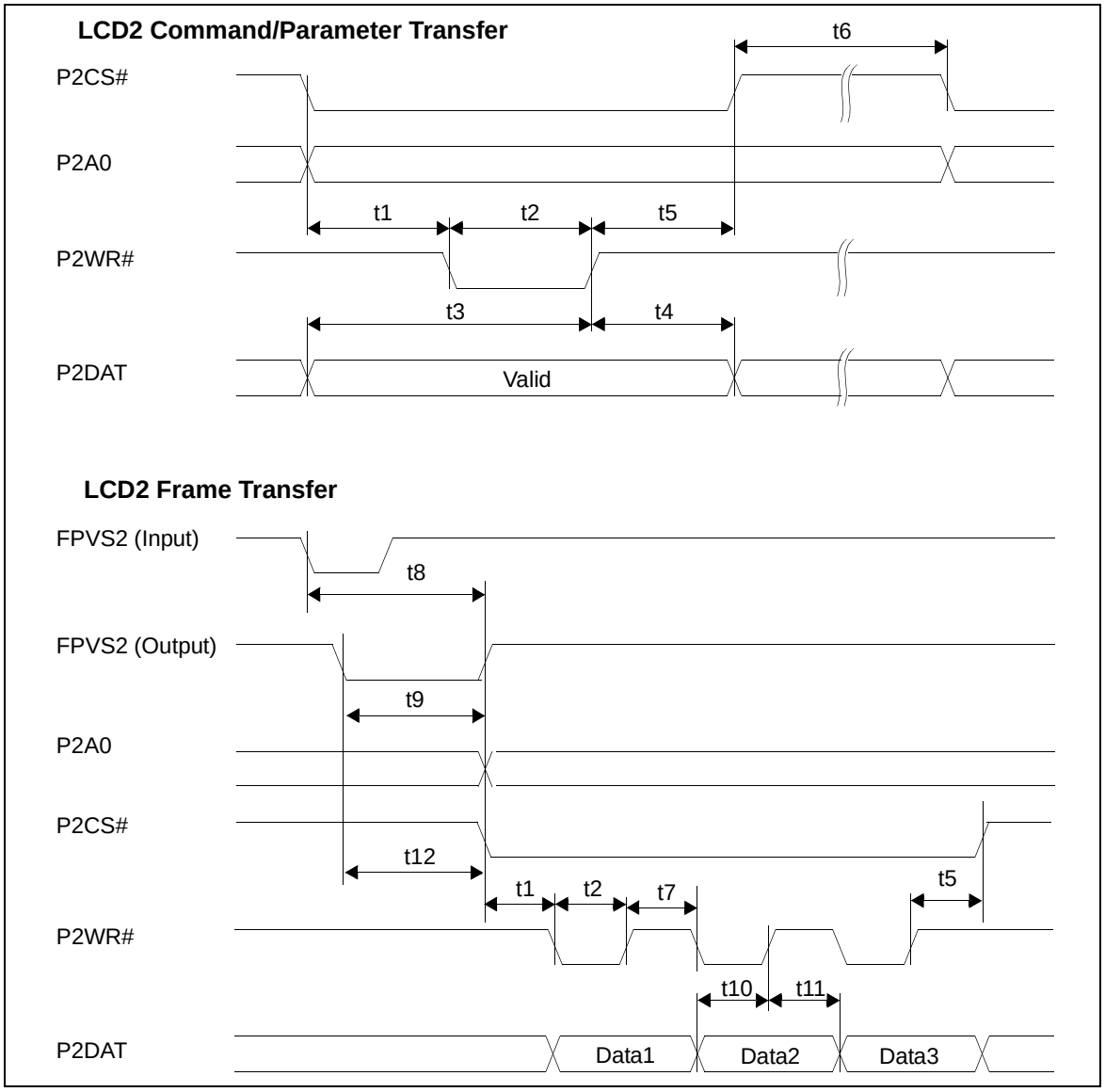


Figure 6-22: LCD2 Parallel Interface Timing (80)

Table 6-18: LCD2 Parallel Interface Timing (80)

Symbol	Parameter	Min	Typ	Max	Units
t1	P2CS# falling edge to P2WR# falling edge	—	1	—	Tp (Note 1)
t2	P2WR# low period	—	1	—	Tp
t3	P2DAT setup time	—	3	—	Tp
t4	P2DAT hold time	—	2	—	Tp
t5	P2WR# rising edge to P2CS# rising edge	—	1	—	Tp
t6	P2CS# de-assert to reassert	—	0	—	Tp
t7	P2WR# high period in burst cycle	—	1	—	Tp
t8	FPVS2 (input) falling edge to P2CS# falling edge	—	—	Note 2	Tp
t9	FPVS2 (output) low period	—	Note 3	—	Tp
t10	P2DAT setup time in burst cycle	—	1	—	Tp
t11	P2DAT hold time in burst cycle	—	1	—	Tp
t12	FPVS2 (output) falling edge to P2CS# falling edge	—	Note 4	—	Tp

1. Tp = Pixel clock period
   = For command/parameter transfers, Tp is defined by REG[0100h] bits 15-12
   = For frame transfers, Tp is defined by REG[0100h] bits 4-0
2. t8max = (2 x HIS + 200) x Tsysclk + (21 x Tp)
   Where:
   - HIS is the largest Horizontal Image Size from the Main1, Main2, PIP1, and PIP2 windows (see REG[0690h], REG[06B4h], REG[072Ch], REG[082Ch]
   - Tsysclk is the system clock period
   - Tp is the pixel clock period as specified by REG[0100h] bits 4-0
3. t9typ = REG[0190h] bits 15-8 x 2
4. t12typ = REG[0190h] bits 7-0 x 2 + 10

6.7.7 LCD2 Parallel Interface (68)

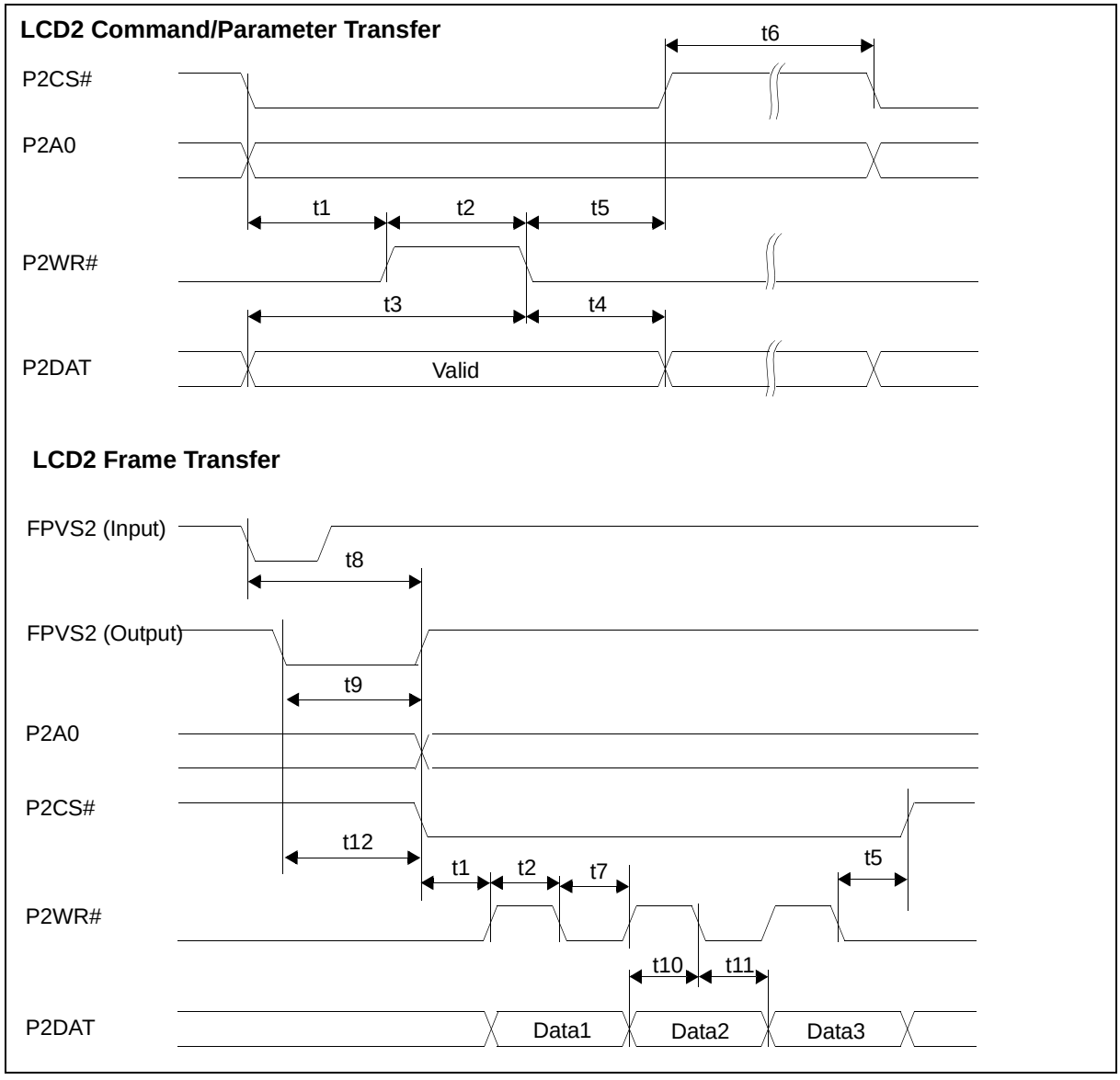


Figure 6-23: LCD2 Parallel Interface Timing (68)

Table 6-19: LCD2 Parallel Interface Timing (68)

Symbol	Parameter	Min	Typ	Max	Units
t1	P2CS# falling edge to P2WR# rising edge	—	1	—	Tp (Note 1)
t2	P2WR# high period	—	1	—	Tp
t3	P2DAT setup time	—	3	—	Tp
t4	P2DAT hold time	—	2	—	Tp
t5	P2WR# falling edge to P2CS# rising edge	—	1	—	Tp
t6	P2CS# deassert to reassert	—	0	—	Tp
t7	P2WR# signal low period in burst cycle	—	1	—	Tp
t8	FPVS2 (input) falling edge to P2CS# falling edge	—	—	Note 2	Tp
t9	FPVS2 (output) low period	—	Note 3	—	Tp
t10	P2DAT setup time in burst cycle	—	1	—	Tp
t11	P2DAT hold time in burst cycle	—	1	—	Tp
t12	FPVS2 (output) falling edge to P2CS# falling edge	—	Note 4	—	Tp

1. Tp = Pixel clock period
   = For command/parameter transfers, Tp is defined by REG[0100h] bits 15-12
   = For frame transfers, Tp is defined by REG[0100h] bits 4-0
2. t8max = (2 x HIS + 200) x Tsysclk + (21 x Tp)
   Where:
   - HIS is the largest Horizontal Image Size from the Main1, Main2, PIP1, and PIP2 windows (see REG[0690h], REG[06B4h], REG[072Ch], REG[082Ch]
   - Tsysclk is the system clock period
   - Tp is the pixel clock period as specified by REG[0100h] bits 4-0
3. t9typ = REG[0190h] bits 15-8 x 2
4. t12typ = REG[0190h] bits 7-0 x 2 + 10

6.7.8 LCD Interface Output Timing

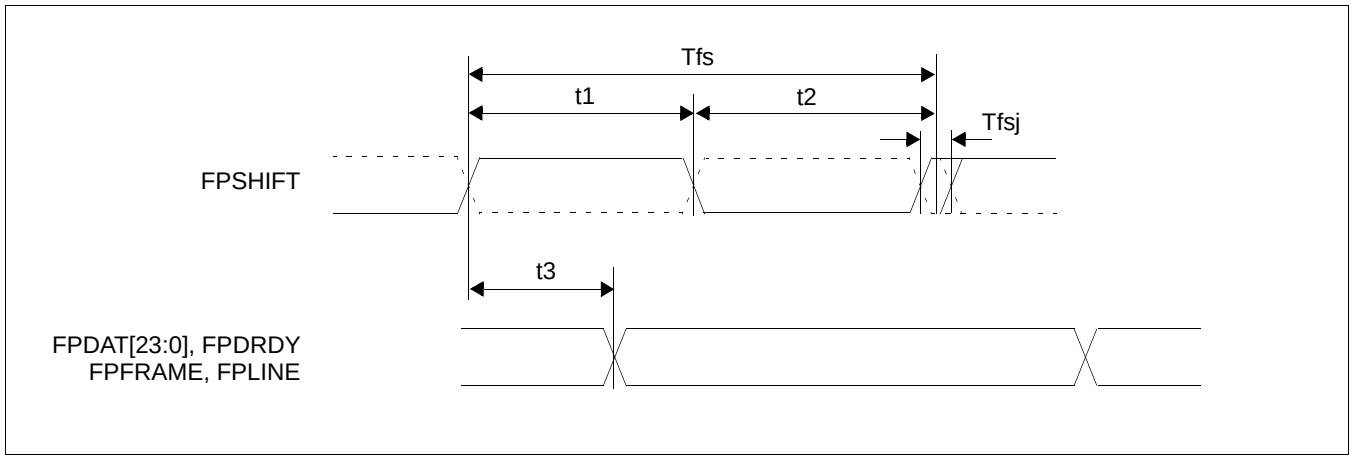


Figure 6-24: LCD Interface Output Timing

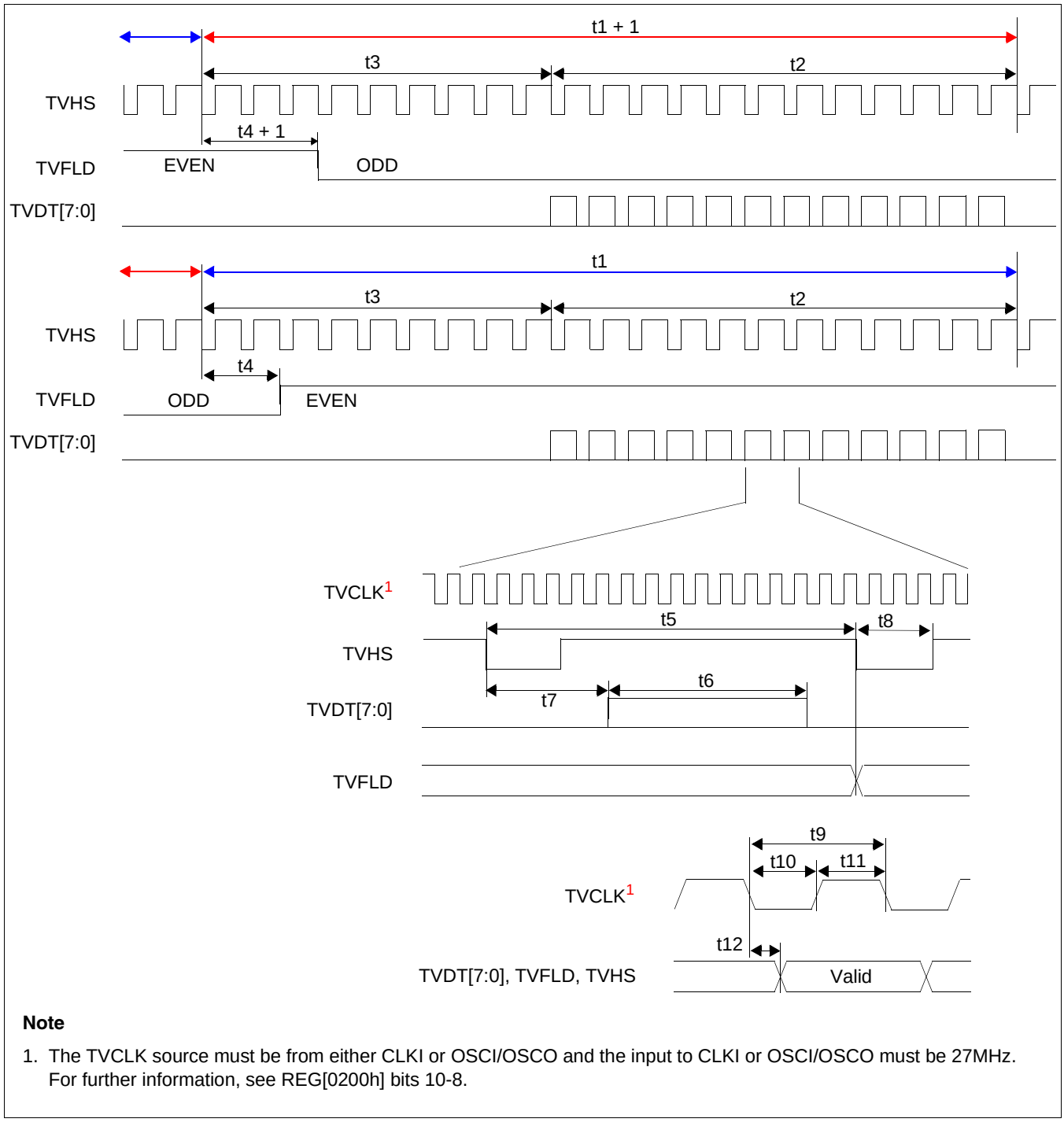
Table 6-20: LCD Interface Output Timing

Symbol	Parameter	PIOVDD = 1.8V			PIOVDD = 2.5V			units
		Min	Typ	Max	Min	Typ	Max	
Ffs	FPSHIFT Output Frequency	—	—	Note 1	—	—	Note 1	MHz
Tfs	FPSHIFT Output Period	—	1/Ffs	—	—	1/Ffs	—	ns
Tfsj	FPSHIFT Output Jitter	Note 2	—	Note 2	Note 2	—	Note 2	ps
t1	FPSHIFT Pulse Width High: REG[0018h] bits 7-6 = 11b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 7-6 = 10b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 7-6 = 01b	Note 5	—	Note 6	Note 5	—	Note 6	ns
	REG[0018h] bits 7-6 = 00b	Note 5	—	Note 6	Note 5	—	Note 6	ns
t2	FPSHIFT Pulse Width Low: REG[0018h] bits 7-6 = 11b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 7-6 = 10b	Note 3	—	Note 4	Note 3	—	Note 4	ns
	REG[0018h] bits 7-6 = 01b	Note 5	—	Note 6	Note 5	—	Note 6	ns
	REG[0018h] bits 7-6 = 00b	Note 5	—	Note 6	Note 5	—	Note 6	ns
t3	FPDAT, FPDRDY, FPRAME, FPLINE Delay Time: REG[0018h] bits 7-6 = 11b	-4	—	4	-4	—	4	ns
	REG[0018h] bits 7-6 = 10b	-4	—	4	-4	—	4	ns
	REG[0018h] bits 7-6 = 01b	-5	—	5	-5	—	5	ns
	REG[0018h] bits 7-6 = 00b	-7.5	—	7.5	-7.5	—	7.5	ns

1. Ffs ≤ System Clock Frequency ÷ 2
   Ffsmax depends on tr and tf (see Section 6.1, “Output Signal Rise/Fall Timing” on page 45).
2. Tfsj = System Clock Jitter (±400ps) x Pixel Clock Divide (REG[0100h] bits 4-0)
   For example, when the pixel clock divide rate is 4:1, Tfsj = 400ps x 4 = ±1600ps.
3. When the Pixel Clock Divide is 1:1 (REG[0100h] bits 4-0 = 00h), the minimum pulse width = Tfs x 0.40.
   When the Pixel Clock Divide is not 1:1 (REG[0100h] bits 4-0 ≠ 00h), the minimum pulse width = Tfs x 0.45.
4. When the Pixel Clock Divide is 1:1 (REG[0100h] bits 4-0 = 00h), the maximum pulse width = Tfs x 0.60.
   When the Pixel Clock Divide is not 1:1 (REG[0100h] bits 4-0 ≠ 00h), the maximum pulse width = Tfs x 0.55.
5. t1min = Tfs x 0.40
   t2min = Tfs x 0.40
6. t1max = Tfs x 0.60
   t2max = Tfs x 0.60

6.8 TV Timing

6.8.1 TV-Out HSYNC and FIELD Type Interface Timing



Note

1. The TVCLK source must be from either CLKI or OSCI/OSCO and the input to CLKI or OSCI/OSCO must be 27MHz. For further information, see REG[0200h] bits 10-8.

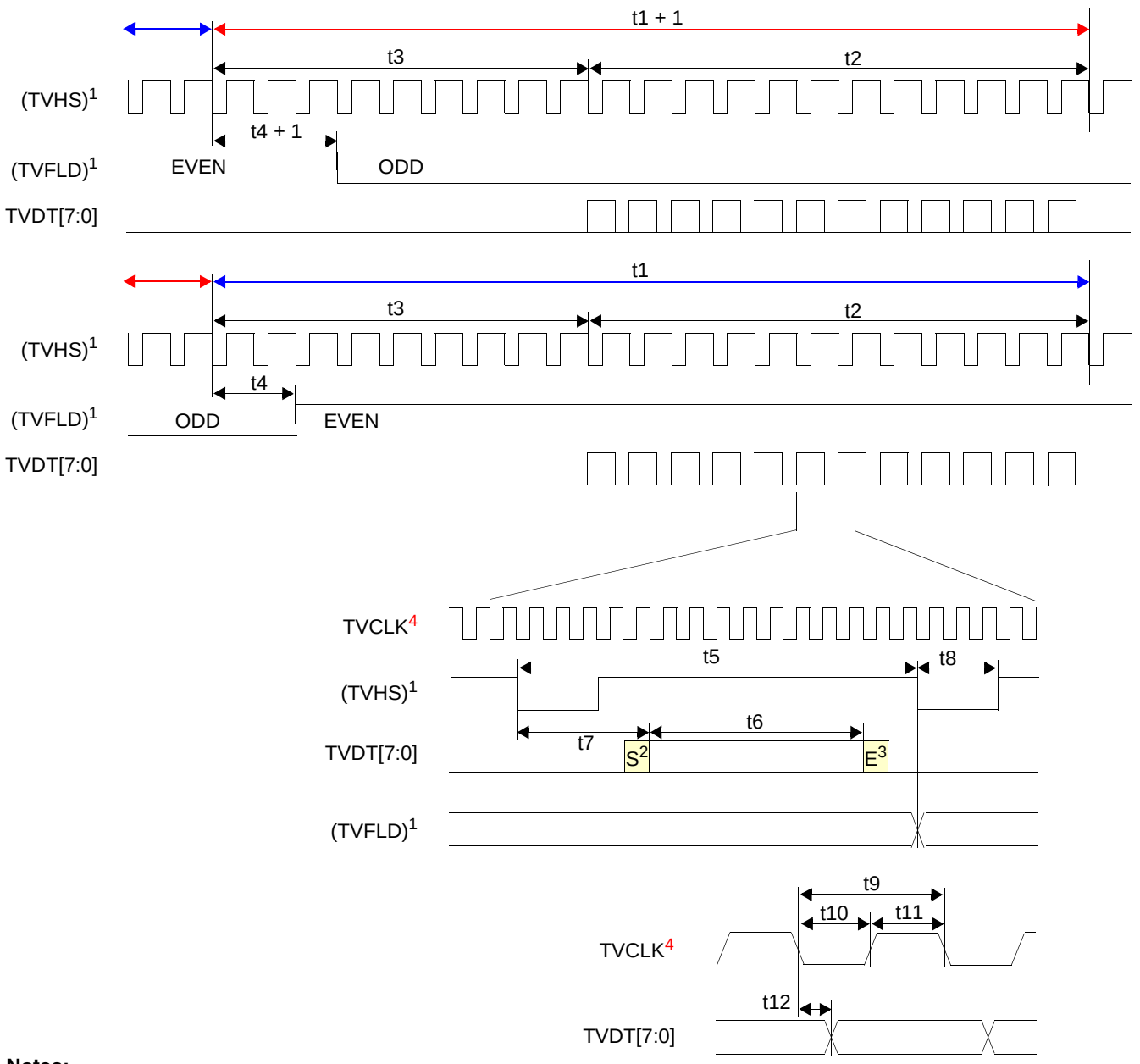
Figure 6-25: TV-Out HSYNC and FIELD Type Interface Timing

Table 6-21: TV-Out HSYNC and FIELD Type Interface Timing

Symbol	Parameter	IOVDD = 1.8V		IOVDD = 2.5V		Units
		Min	Max	Min	Max	
t1	Vertical total (even fields)	REG[0218h] + 1		REG[0218h] + 1		Lines
t2	Vertical display period (odd/even field)	REG[021Ch] + 1		REG[021Ch] + 1		Lines
t3	Vertical display start position (odd/even field)	REG[0220h] + 2		REG[0220h] + 2		Lines
t4	TVFLD signal toggle position	REG[0224h]		REG[0224h]		Lines
t5	Horizontal total	(REG[0204h] + 1) x 2		(REG[0204h] + 1) x 2		Ttv (Note 1)
t6	Horizontal display period	(REG[0208h] + 1) x 4		(REG[0208h] + 1) x 4		Ttv
t7	Horizontal display start position	REG[020Ch] x 2 + 18		REG[020Ch] x 2 + 18		Ttv
t8	TVHS horizontal display sync pulse width low	(REG[0210h] + 1) x 2		(REG[0210h] + 1) x 2		Ttv
t9	TVCLK cycle (Tvcyc)	1		1		Ttv
t10	TVCLK low pulse width (Note 2)	0.4 Tvcyc	0.6 Tvcyc	0.4 Tvcyc	0.6 Tvcyc	ns
t11	TVCLK high pulse width (Note 2)	0.4 Tvcyc	0.6 Tvcyc	0.4 Tvcyc	0.6 Tvcyc	ns
t12	TVDT, TVFLD, TVHS Delay Time (Note 2)	-4	4	-4	4	ns

1. TV-Out Clock Period = CLKI or OSCI/OSCO period
2. The IO drive level is 3.0mA or 3.7mA @1.8V (see REG[0018h]).
   The IO drive level is 6.0mA or 7.4mA @2.5V (see REG[0018h]).
3. Example register settings for NTSC (Output size: Horizontal = 720, Vertical = 480)
   REG[0204h] bits 9-0 = 359h [HT]
   REG[0208h] bits 8-0 = 167h [HDP]
   REG[020Ch] bits 9-0 = 071h [HDPS]
   REG[0210h] bits 6-0 = 00h [HPW]
   REG[0218h] bits 9-0 = 105h [VT]
   REG[021Ch] bits 9-0 = 0EFh [VDP]
   REG[0220h] bits 9-0 = 012h [VDPS]
   REG[0224h] bits 9-0 = 002h [FILD]
   Please adjust horizontal direction of the display with Main1/Main2/PIP1/PIP2 Window X Start Position registers.
   (REG[06A0h], REG[06C4h], REG[073Ch], REG[083Ch] ≥ 30h)
4. Example register settings for PAL BDGHI (Output size: Horizontal = 720, Vertical = 576)
   REG[0204h] bits 9-0 = 35Fh [HT]
   REG[0208h] bits 8-0 = 167h [HDP]
   REG[020Ch] bits 9-0 = 07Fh [HDPS]
   REG[0210h] bits 6-0 = 00h [HPW]
   REG[0218h] bits 9-0 = 137h [VT]
   REG[021Ch] bits 9-0 = 11Fh [VDP]
   REG[0220h] bits 9-0 = 015h [VDPS]
   REG[0224h] bits 9-0 002h [FILD]
   Please adjust horizontal direction of the display with Main1/Main2/PIP1/PIP2 Window X Start Position registers.
   (REG[06A0h], REG[06C4h], REG[073Ch], REG[083Ch] ≥ 30h)

6.8.2 TV-Out ITU-R BT656 Interface Timing



Notes:

1. TVHS, TVFLD are internal signals and are not output.
2. SAV code is added ahead of each line data.
3. EAV code is added behind each line data.
4. The TVCLK source must be from either CLKI or OSCI/OSCO and the input to CLKI or OSCI/OSCO must be 27MHz. For further information, see REG[0200h] bits 10-8.

Figure 6-26: TV-Out ITU-R BT656 Interface Timing

Table 6-22: TV-Out ITU-R BT656 Interface Timing

Symbol	Parameter	IOVDD = 1.8V		IOVDD = 2.5V		Units
		Min	Max	Min	Max	
t1	Vertical total (even fields)	REG[0218h] + 1		REG[0218h] + 1		Lines
t2	Vertical display period (odd/even field)	REG[021Ch] + 1		REG[021Ch] + 1		Lines
t3	Vertical display start position (odd/even field)	REG[0220h] + 2		REG[0220h] + 2		Lines
t4	TVFLD signal toggle position	REG[0224h]		REG[0224h]		Lines
t5	Horizontal total	(REG[0204h] + 1) x2		(REG[0204h] + 1) x2		Ttv (Note1)
t6	Horizontal display period	(REG[0208h] + 1) x4		(REG[0208h] + 1) x4		Ttv
t7	Horizontal display start position	REG[020Ch] x 2 +18		REG[020Ch] x 2 +18		Ttv
t8	TVHS horizontal display sync pulse width low	(REG[0210h] + 1) x2		(REG[0210h] + 1) x2		Ttv
t9	TVCLK cycle (Tvcyc)	1		1		Ttv
t10	TVCLK low pulse width (Note 2)	0.4 Tvcyc	0.6 Tvcyc	0.4 Tvcyc	0.6 Tvcyc	ns
t11	TVCLK high pulse width (Note 2)	0.4 Tvcyc	0.6 Tvcyc	0.4 Tvcyc	0.6 Tvcyc	ns
t12	TVDT Delay Time (Note 2)	-4	4	-4	4	ns

1. TV-Out Clock Period = CLKI or OSCI/OSCO period
2. The IO drive level is 3.0mA or 3.7mA @1.8V (see REG[0018h]).
   The IO drive level is 6.0mA or 7.4mA @2.5V (see REG[0018h]).
3. Example of register setting for NTSC (Output size : Horizontal = 720, Vertical = 480)
   REG[0204h] bits 9-0 = 359h [HT]
   REG[0208h] bits 8-0 = 167h [HDP]
   REG[020Ch] bits 9-0 = 071h [HDPS]
   REG[0210h] bits 6-0 = 00h [HPW]
   REG[0218h] bits 9-0 = 105h [VT]
   REG[021Ch] bits 9-0 = 0EFh [VDP]
   REG[0220h] bits 9-0 = 012h [VDPS]
   REG[0224h] bits 9-0 = 002h [FILD]
   Please adjust horizontal direction of the display with Main1/Main2/PIP1/PIP2 Window X Start Position registers.
   (REG[06A0h], REG[06C4h], REG[073Ch], REG[083Ch] ≥ 30h)
4. Example register settings for PAL BDGHI (Output size: Horizontal = 720, Vertical = 576)
   REG[0204h] bits 9-0 = 35Fh [HT]
   REG[0208h] bits 8-0 = 167h [HDP]
   REG[020Ch] bits 9-0 = 07Fh [HDPS]
   REG[0210h] bits 6-0 = 00h [HPW]
   REG[0218h] bits 9-0 = 137h [VT]
   REG[021Ch] bits 9-0 = 11Fh [VDP]
   REG[0220h] bits 9-0 = 015h [VDPS]
   REG[0224h] bits 9-0 002h [FILD]
   Please adjust horizontal direction of the display with Main1/Main2/PIP1/PIP2 Window X Start Position registers.
   (REG[06A0h], REG[06C4h], REG[073Ch], REG[083Ch] ≥ 30h)

6.8.3 TV-Out Parallel Interface Timing

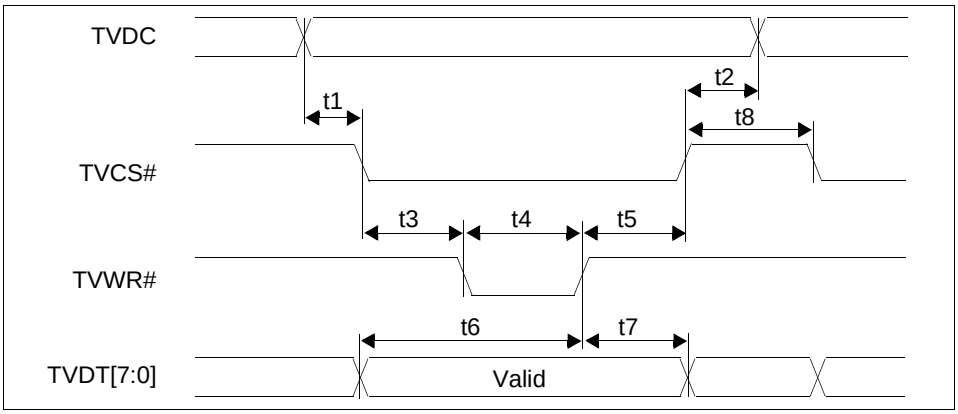


Figure 6-27: TV-Out Parallel Interface Command Write Timing

Table 6-23: TV-Out Parallel Interface Command Write Timing

Symbol	Parameter	IOVDD = 1.8V			IOVDD = 2.5V			Units
		Min	Typ	Max	Min	Typ	Max	
t1	TVDC setup time	0	—	—	0	—	—	ns
t2	TVDC hold time	0	—	—	0	—	—	ns
t3	TVCS# falling edge to TVWR# falling edge	—	1	—	—	1	—	Ttv (Note1)
t4	TVWR# low period	—	1	—	—	1	—	Ttv
t5	TVWR# rising edge to TVCS# rising edge	—	1	—	—	1	—	Ttv
t6	TVDT setup time	—	2	—	—	2	—	Ttv
t7	TVDT hold time	—	1	—	—	1	—	Ttv
t8	TVCS# de-assert to reassert	—	1	—	—	1	—	Ttv

1. Ttv = TV-Out Clock Period

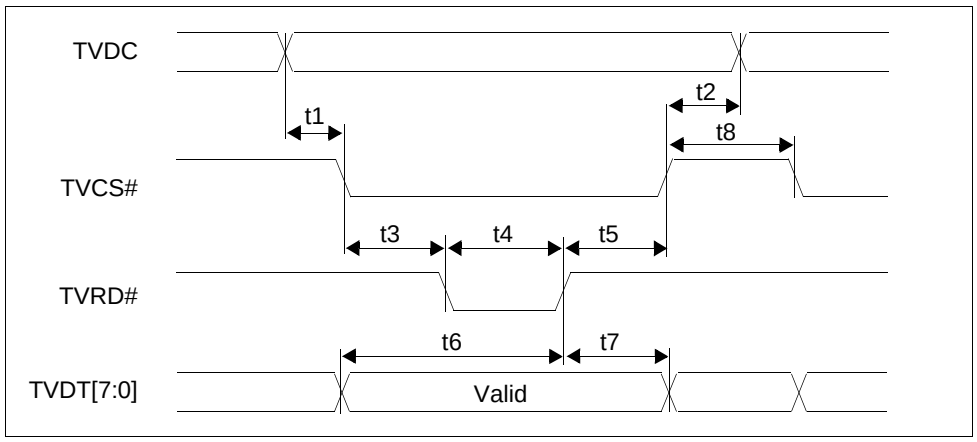


Figure 6-28: TV-Out Parallel Interface Command Read Timing

Table 6-24: TV-Out Parallel Interface Command Read Timing

Symbol	Parameter	IOVDD = 1.8V			IOVDD = 2.5V			Units
		Min	Typ	Max	Min	Typ	Max	
t1	TVDC setup time	0	—	—	0	—	—	ns
t2	TVDC hold time	0	—	—	0	—	—	ns
t3	TVCS# falling edge to TVRD# falling edge	—	0	—	—	0	—	Ttv (Note1)
t4	TVRD# low period	—	0	—	—	0	—	Ttv
t5	TVRD# rising edge to TVCS# rising edge	—	0	—	—	0	—	Ttv
t6	TVDT setup time	Note 2	—	—	Note 2	—	—	ns
t7	TVDT hold time	0	—	—	0	—	—	ns
t8	TVCS# de-assert to reassert	1	—	—	1	—	—	Ttv

1. Ttv = TV-Out Clock Period
2. t6min = Tsysclk + 36ns for IOVDD = 1.8V
   = Tsysclk + 26ns for IOVDD = 2.5V
   Where Tsysclk is the system clock period

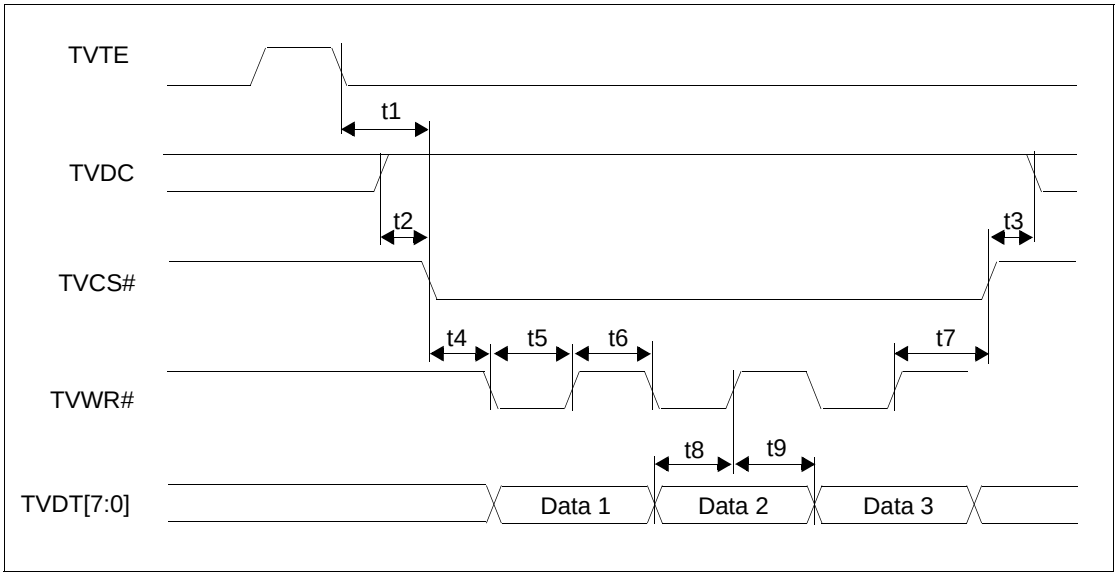


Figure 6-29: TV-Out Parallel Interface Frame Transfer Timing

Table 6-25: TV-Out Parallel Interface Frame Transfer Timing

Symbol	Parameter	IOVDD = 1.8V			IOVDD = 2.5V			Units
		Min	Typ	Max	Min	Typ	Max	
t1	TVTE falling edge to TVCS# falling edge	—	—	Note 2	—	—	Note 2	Ttv (Note1)
t2	TVDC setup time	0	—	—	0	—	—	ns
t3	TVDC hold time	0	—	—	0	—	—	ns
t4	TVCS# falling edge to TVWR# falling edge	—	1	—	—	1	—	Ttv
t5	TVWR# low period	—	1	—	—	1	—	Ttv
t6	TVWR# high period	—	1	—	—	1	—	Ttv
t7	TVWR# rising edge to TVCS# rising edge	—	2	—	—	2	—	Ttv
t8	TVDT setup time	—	1	—	—	1	—	Ttv
t9	TVDT hold time	—	1	—	—	1	—	Ttv

1. Ttv = TV-Out Clock Period
2. t1max = (2 x HIS + 200) x Tsysclk + (21 x Ttvclk)
   Where:
   - HIS is the largest Horizontal Image Size from the Main1, Main2, PIP1, an PIP2 windows (see REG[0690h], REG[06B4h], REG[072Ch], REG[082Ch]
   - Tsysclk is the system clock period
   - Ttvclk is the TV-Out clock period as specified by REG[0200h] bits 10-8

7 Memory

7.1 Physical Memory

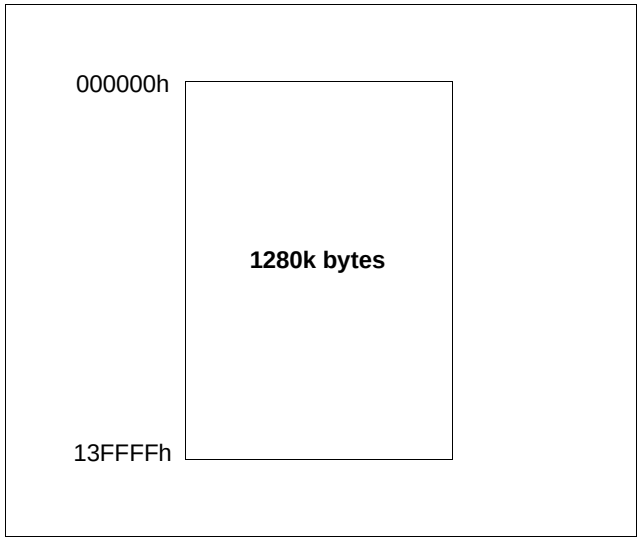


Figure 7-1: Physical Memory

7.2 Example Memory Map

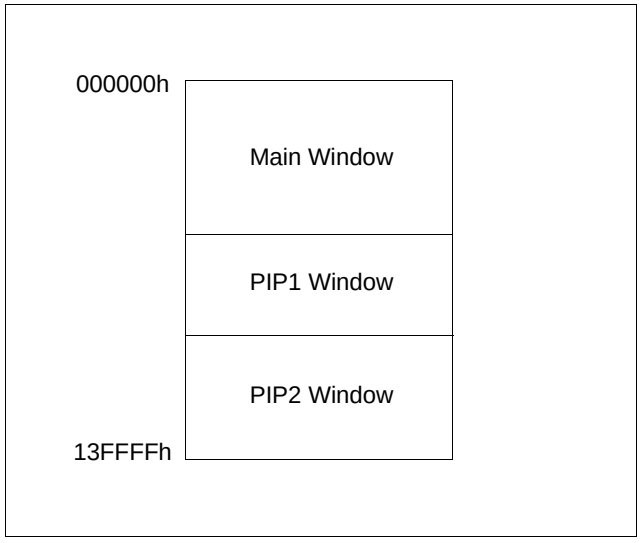


Figure 7-2: Example Memory Map

7.3 Memory Formats

The S1D13774 stores image data in the display memory using the following formats. The pixel data is stored in memory using complex addressing.

Note

RGB 6:6:6 image data is expanded to RGB 8:8:8 before being stored in the display memory.

Table 7-1: RGB 8:8:8 in Memory

RGB 8:8:8 Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Start Address 1st Pixel	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
2nd Pixel	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_0^1	R_1^0	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0
3rd Pixel	G_2^7	G_2^6	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^7	B_2^6	B_2^5	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0
									R_2^7	R_2^6	R_2^5	R_2^4	R_2^3	R_2^2	R_2^1	R_2^0

Table 7-2: RGB 5:6:5 in Memory

RGB 5:6:5 Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Start Address 1st Pixel	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
2nd Pixel	R_1^4	R_1^3	R_1^2	R_0^1	R_1^0	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
3rd Pixel	R_2^4	R_2^3	R_2^2	R_2^1	R_2^0	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0
4th Pixel	R_3^4	R_3^3	R_3^2	R_3^1	R_3^0	G_3^5	G_3^4	G_3^3	G_3^2	G_3^1	G_3^0	B_3^4	B_3^3	B_3^2	B_3^1	B_3^0

Table 7-3: YUV 4:2:2 in Memory

YUV 4:2:2 Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Start Address 1st Pixel	Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^7	Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0
Start Address 2nd Pixel	Y_3^7	Y_3^6	Y_3^5	Y_3^4	Y_3^3	Y_3^2	Y_3^1	Y_3^7	Y_2^7	Y_2^6	Y_2^5	Y_2^4	Y_2^3	Y_2^2	Y_2^1	Y_2^0
Start Address 1st Pixel	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
Start Address 2nd Pixel	V_2^7	V_2^6	V_2^5	V_2^4	V_2^3	V_2^2	V_2^1	V_2^0	U_2^7	U_2^6	U_2^5	U_2^4	U_2^3	U_2^2	U_2^1	U_2^0

Table 7-4: YUV 4:2:0 in Memory

YUV 4:2:2 Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Start Address 1st Pixel	Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^7	Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0
Start Address 2nd Pixel	Y_3^7	Y_3^6	Y_3^5	Y_3^4	Y_3^3	Y_3^2	Y_3^1	Y_3^7	Y_2^7	Y_2^6	Y_2^5	Y_2^4	Y_2^3	Y_2^2	Y_2^1	Y_2^0
Start Address 1st Pixel	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
Start Address 2nd Pixel	V_2^7	V_2^6	V_2^5	V_2^4	V_2^3	V_2^2	V_2^1	V_2^0	U_2^7	U_2^6	U_2^5	U_2^4	U_2^3	U_2^2	U_2^1	U_2^0

Note

The number of UV bytes is 1/2 the number of Y bytes for the frame.

8 Clocks

8.1 Clock Diagram

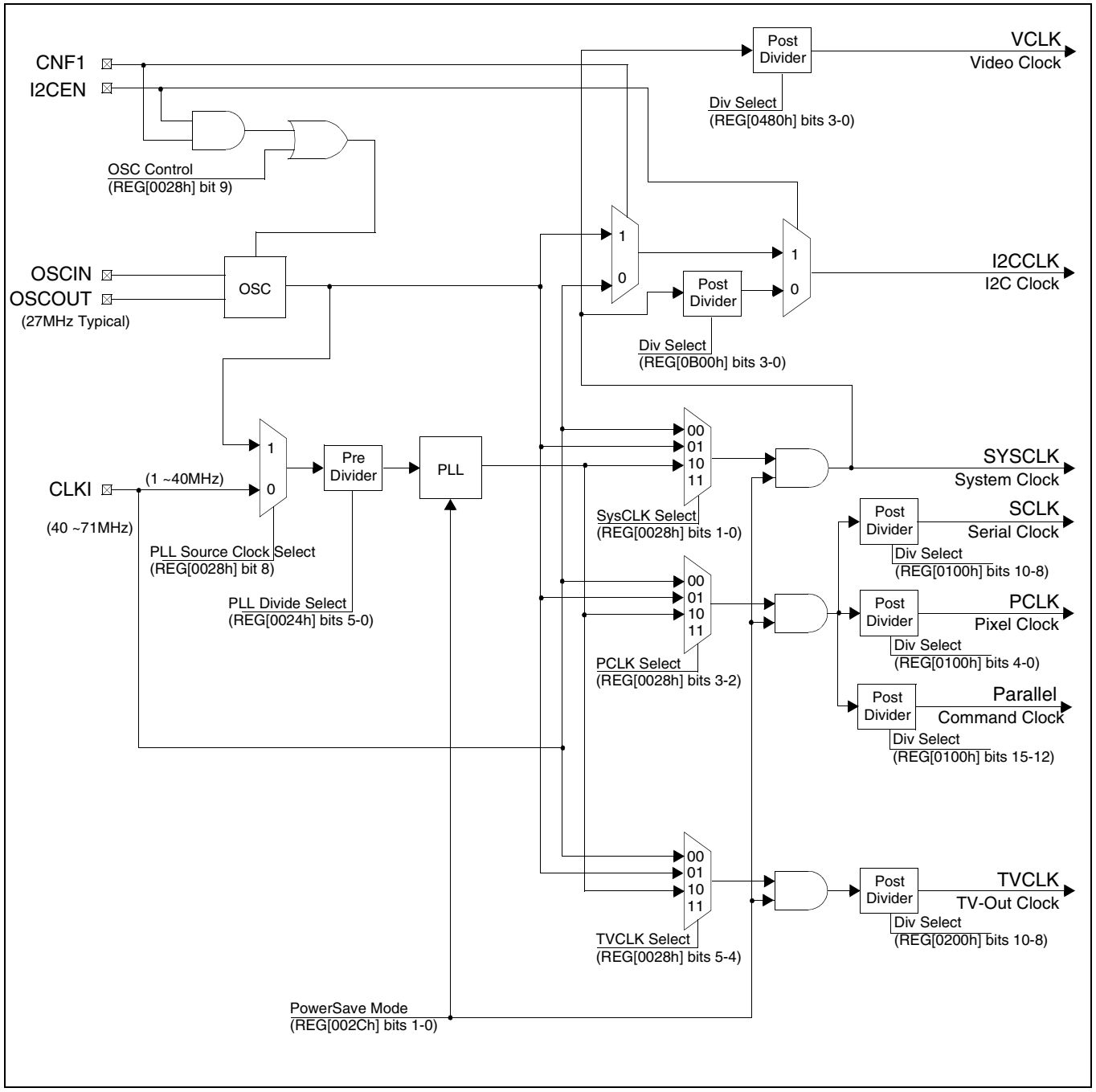


Figure 8-1: Clock Diagram

8.2 Clock Descriptions

8.2.1 System Clock

System clock (SYSCLK) is used for the S1D13774 internal main clock. The system clock source can be selected (REG[0028h] bits 1-0) from either the internal PLL, or an external clock input (CLKI) or X'tal input (OSCI,OSCO).

8.2.2 Pixel Clock

Pixel clock (PCLK) is used for the LCD shift clock of a RGB type panel and for the LCD2 parallel interface timing. The pixels clock source can be selected (REG[0028h] bits 3-2) from either the internal PLL, or an external clock input (CLKI) or X'tal input (OSCI,OSCO). The pixel clock can be divided using the Pixel Clock Divide Select bits (REG[0100h] bits 4-0).

8.2.3 TV-Out Clock

TV-Out clock (TVCLK) is used for TV-Out interface timing. The TV-Out clock source can be selected (REG[0028h] bits 5-4) from either the internal PLL, or an external clock input (CLKI) or X'tal input (OSCI,OSCO). For details on dividing the TV-Out clock, see the TV-Out Clock Divide Select bits description, REG[0200h] bits 10-8.

Note

When the TV-Out interface is configured for Parallel (REG[0200h] bits 1-0 = 10b), the TVCLK source must be the same as the PCLK source (REG[0028h] bits 5-4 = REG[0028h] bits 3-2).

8.2.4 Serial Clock

Serial clock (SCLK) is used for the LCD1 and LCD2 serial interfaces. The serial clock source is always the pixel clock and can be divided using the Serial Clock Divide Select bits (REG[0100h] bits 10-8).

8.2.5 Video Clock

Video clock (VCLK) is used for the video interface. The video clock source is always the system clock. The video output clock can be divided using the Video Clock Divide Select bits (REG[0480h] bits 3-0).

8.2.6 I2C Clock

I2C clock (I2CCLK) is used for the I2C interface. The system clock source can be selected (I2CEN and CNF1) from either the internal PLL, or an external clock input (CLKI) or X'tal input (OSCI,OSCO).

8.3 PLL Diagram

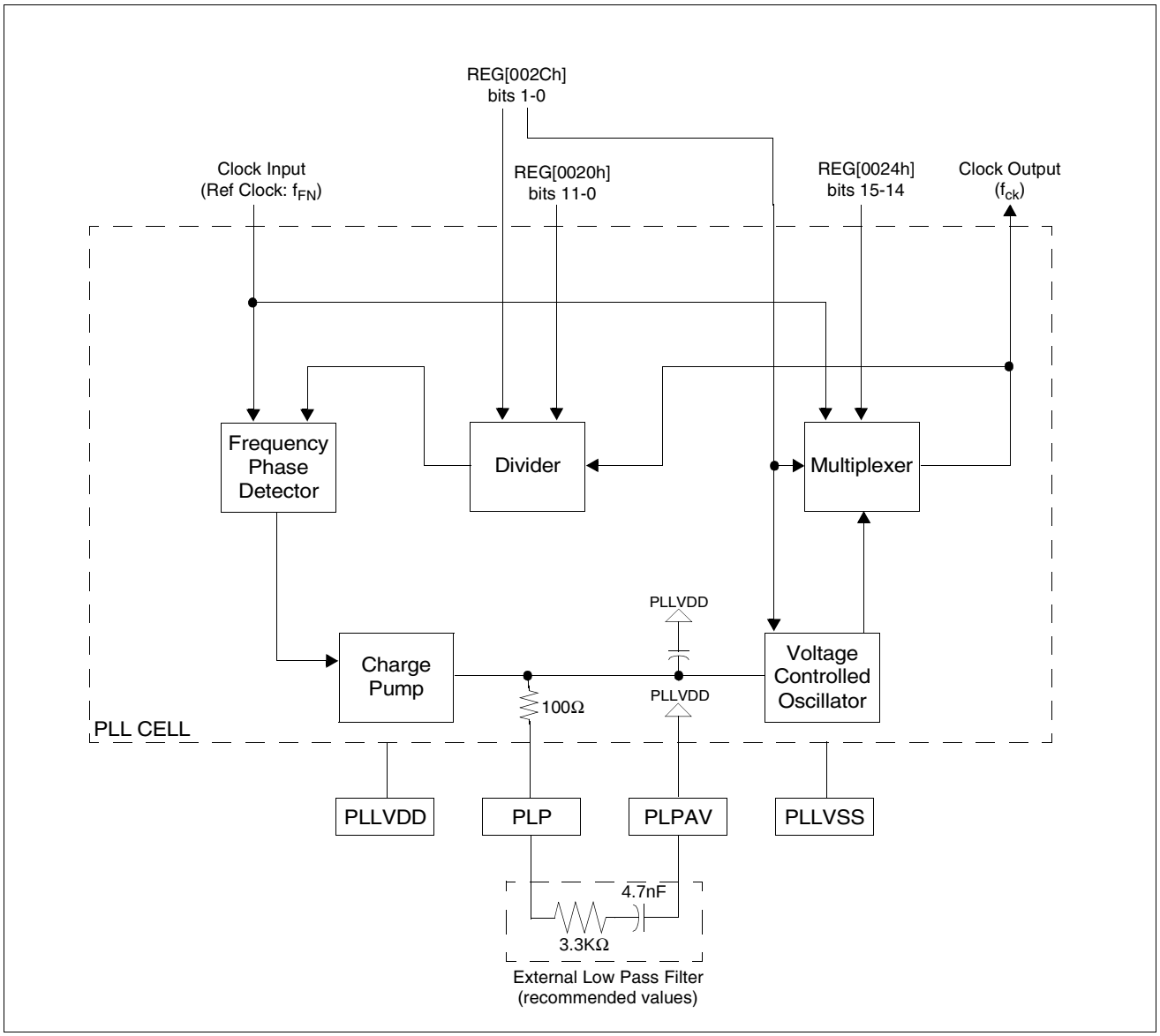


Figure 8-2: PLL Diagram

9 Registers

This section discusses how and where to access the S1D13774 registers. It also provides detailed information about the layout and usage of each register.

9.1 Register Mapping

The S1D13774 registers are memory mapped. Asynchronous registers are accessible at all times. Synchronous registers are available in Standby A, Standby B, and normal operation modes (REG[002Ch] bits 1-0 = 01b or 10b or 11b).

Table 9-1: S1D13774 Register Mapping

Address	Type	Function
0000h to 000Ch	Asynchronous	System Configuration Registers
0020h to 002Ch	Asynchronous	Clock Configuration Registers
0040h	Asynchronous	Software Reset Register
0080h to 0094h	Synchronous	SDRAM Control Registers
0100h to 0114h	Synchronous	LCD Interface Configuration Registers
0140h to 0170h	Synchronous	LCD1 Configuration Registers
0180h to 0190h	Synchronous	LCD2 Configuration Registers
0200h to 022Ch	Synchronous	TV-Out Interface Configuration Registers
0300h to 0350h	Asynchronous	GPIO Registers
0400h to 0420h	Synchronous	Host Interface Registers
0480h to 048Ch	Synchronous	Video Input Interface Registers
0500h to 052Ch	Synchronous	Main Memory Write Path Registers
0580h to 05A8h	Synchronous	Sub Memory Write Path Registers
0600h to 0650h	Synchronous	Display Configuration Registers
0680h to 06C8h	Synchronous	Main Window Configuration Registers
0700h to 0750h	Synchronous	PIP1 Window Configuration Registers
0800h to 086Ch	Synchronous	PIP2 Window Configuration Register
0900h to 0984h	Synchronous	AME (Auto Movie Enhancement) Registers
0A00h to 0A04h	Synchronous	Interrupt Control Registers
0B00h to 0B04h	Synchronous	I2C Slave Configuration Registers
1040h to 1060h	Synchronous	Reserved

9.2 Register Set

The S1D13774 registers are listed in the following table.

Table 9-2: S1D13774 Register Set

System Configuration Registers			
REG[0000h] Product Information Register 0	96	REG[0004h] Product Information Register 1	96
REG[0008h] Configuration Pin Status Register	97	REG[000Ch] is Reserved	97
REG[0010h] is Reserved	97	REG[0014h] is Reserved	97
REG[0018h] Pin Drive Control Register	98		
Clock Configuration Registers			
REG[0020h] PLL Setting Register 0	100	REG[0024h] PLL Setting Register 1	101
REG[0028h] Clock Source Select Register	103	REG[002Ch] Power Save Mode Register (AID)	105
REG[0030h] I2C Quick Enable Register	107		
Software Reset Register			
REG[0040h] Software Reset Register (AID)	108		
SDRAM Control Registers			
REG[0080h] Memory Controller Software Reset Register	109	REG[0084h] Auto Refresh Interval Setting Register	109
REG[0088h] Power-On Sequence Timing Control Register	110	REG[008Ch] Timing Control Register	111
REG[0090h] is Reserved	112	REG[0094h] Memory Control Status Flag Register (AID)	113
LCD Interface Configuration Registers			
REG[0100h] LCD Interface Clock Setting Register	114	REG[0104h] LCD Interface Configuration Register	116
REG[0108h] LCD Interface Command Register	119	REG[010Ch] LCD Interface Parameter Register	120
REG[0110h] LCD Interface ID Register	120	REG[0114h] LCD2 Interface Frame Transfer Register (AID)	121
LCD1 Configuration Registers			
REG[0140h] LCD1 Horizontal Total (FPLINE Period) Register	123	REG[0144h] LCD1 Horizontal Display Period Register	123
REG[0148h] LCD1 Horizontal Display Period Start Position Register	124	REG[014Ch] LCD1 Horizontal Pulse (FPLINE) Register	124
REG[0150h] LCD1 Horizontal Pulse (FPLINE) Start Position Register	125	REG[0154h] LCD1 Vertical Total (FPFRAME Period) Register	125
REG[0158h] LCD1 Vertical Display Period Register	126	REG[015Ch] LCD1 Vertical Display Period Start Position Register	126
REG[0160h] LCD1 Vertical Pulse (FPFRAME) Register	127	REG[0164h] LCD1 Vertical Pulse (FPFRAME) Start Position Register	127
REG[0168h] LCD1 Serial Interface Setting Register	128	REG[016Ch] is Reserved (AID)	129
REG[0170h] is Reserved	129	REG[0174h] is Reserved	129
LCD2 Configuration Registers			
REG[0180h] LCD2 Horizontal Display Period Register	130	REG[0184h] LCD2 Vertical Display Period Register	130
REG[0188h] LCD2 Serial Interface Setting Register	131	REG[018Ch] LCD2 Parallel Interface Setting Register	134
REG[0190h] LCD2 VSYNC Output Register	137		
TV-Out Interface Configuration Registers			
REG[0200h] TV-Out Interface Clock Setting Register	138	REG[0204h] TV-Out Horizontal Total Register	142
REG[0208h] TV-Out Horizontal Display Period Register	143	REG[020Ch] TV-Out Horizontal Display Period Start Position Register	144
REG[0210h] TV-Out Horizontal Pulse (HSYNC) Width Register	144	REG[0214h] is Reserved	144
REG[0218h] TV-Out Vertical Total Register	145	REG[021Ch] TV-Out Vertical Display Period Register	145
REG[0220h] TV-Out Vertical Display Period Start Position Register	146	REG[0224h] TV-Out FIELD Toggle Position Register	146
REG[0228h] TV-Out Data Port Register (AID)	147	REG[022Ch] TV-Out Interface Frame Transfer Register (AID)	148
REG[0230h] TV-Out Blank Data Register	149		
GPIO Registers			
REG[0300h] GPIOP Configuration Register	150	REG[0304h] GPIOH Configuration Register 0	150

Table 9-2: S1D13774 Register Set

REG[0308h] GPIOH Configuration Register 1	150	REG[030Ch] GPIOP Input Enable Register	151
REG[0310h] GPIOH Input Enable Register 0	152	REG[0314h] GPIOH Input Enable Register 1	152
REG[0318h] GPIOP Pull-Up/Down Control Register	153	REG[031Ch] GPIOH Pull-Up/Down Control Register 0	153
REG[0320h] GPIOH Pull-Up/Down Control Register 1	153	REG[0324h] GPIOP Status Register	154
REG[0328h] GPIOH Status Register 0	154	REG[032Ch] GPIOH Status Register 1	154
REG[0330h] GPIOP Positive Edge Interrupt Trigger Register	155	REG[0334h] GPIOH Positive Edge Interrupt Trigger Register 0	156
REG[0338h] GPIOH Positive Edge Interrupt Trigger Register 1	156	REG[033Ch] GPIOP Negative Edge Interrupt Trigger Register	157
REG[0340h] GPIOH Negative Edge Interrupt Trigger Register 0	158	REG[0344h] GPIOH Negative Edge Interrupt Trigger Register 1	158
REG[0348h] GPIOP Interrupt Status Register	159	REG[034Ch] GPIOH Interrupt Status Register 0	159
REG[0350h] GPIOH Interrupt Status Register 1	159		
Host Interface Registers			
REG[0400h] Host Interface Configuration Register	160	REG[0404h] TE Configuration Register	162
REG[0408h] through REG[0414h] are Reserved	165	REG[0418h] Host Memory Write Access Port Register (AID)	165
REG[0420h] is Reserved	165		
Video Input Interface Registers			
REG[0480h] Video Input Interface Output CLK Register	166	REG[0484h] Video Input Interface Configuration Register	167
REG[0488h] Video Input Interface Control Register (AID)	170	REG[048Ch] Video Input Interface Status Register (AID)	170
REG[0490h] is Reserved			
Main Memory Write Path Registers			
REG[0500h] Memory Write Path Configuration Register	171	REG[0504h] Main Memory Write Path Configuration Register	173
REG[0508h] Main Memory Buffer A RGB,Y Start Address Register	177	REG[050Ch] Main Memory Buffer A UV Start Address Register	177
REG[0510h] Main Memory Buffer B RGB,Y Start Address Register	178	REG[0514h] Main Memory Buffer B UV Start Address Register	178
REG[0518h] Main Memory Line Address Offset Register	179	REG[051Ch] Main Memory Vertical Size Register	179
REG[0520h] Main Image Horizontal Size Register	180	REG[0524h] Main Image Vertical Size Register	180
REG[0528h] Main Image X Start Position Register	181	REG[052Ch] Main Image Y Start Position Register	181
Sub Memory Write Path Registers			
REG[0580h] Sub Memory Write Path Enable Register	182	REG[0584h] Sub Memory Buffer A RGB, Y Start Address Register	183
REG[0588h] Sub Memory Buffer A UV Start Address Register	183	REG[058Ch] Sub Memory Buffer B RGB,Y Start Address Register	184
REG[0590h] Sub Memory Buffer B UV Start Address Register	184	REG[0594h] Sub Memory Line Address Offset Register	185
REG[0598h] Sub Memory Vertical Size Register	185	REG[059Ch] Sub Image Horizontal Size Register	186
REG[05A0h] Sub Image Vertical Size Register	186	REG[05A4h] Sub Image X Start Position Register	187
REG[05A8h] Sub Image Y Start Position Register	187		
Display Configuration Registers			
REG[0600h] Display Mode Setting Register 0	188	REG[0604h] Display Mode Setting Register 1	190
REG[0608h] Transparency and Alpha Blend Control Register	193	REG[060Ch] Background Color Setting Register 0	195
REG[0610h] Background Color Setting Register 1	195	REG[0614h] Alpha Blend Ratio Setting Register	196
REG[0618h] PIP1 Window Transparency Key Color Register 0	199	REG[061Ch] PIP1 Window Transparency Key Color Register 1	199
REG[0620h] PIP2 Window Transparency Key Color Register 0	200	REG[0624h] PIP2 Window Transparency Key Color Register 1	200
REG[0628h] Alpha Blend 1 Key Color Register 0	201	REG[062Ch] Alpha Blend 1 Key Color Register 1	201
REG[0630h] Alpha Blend 2 Key Color Register 0	202	REG[0634h] Alpha Blend 2 Key Color Register 1	202
REG[0638h] Alpha Blend 3 Key Color Register 0	203	REG[063Ch] Alpha Blend 3 Key Color Register 1	203
REG[0640h] Alpha Blend 4 Key Color Register 0	204	REG[0644h] Alpha Blend 4 Key Color Register 1	204
REG[0648h] Pseudo Color Setting Register	205	REG[064Ch] LUT Address Counter Register (AID)	206
REG[0650h] LUT Data Port Register (AID)	207		

Table 9-2: S1D13774 Register Set

Main Window Configuration Registers			
REG[0680h] Main Window Control Register	208	REG[0684h] Main1 Memory Start Address Register	210
REG[0688h] Main1 Memory Line Address Offset Register	210	REG[068Ch] Main1 Memory Vertical Size Register	211
REG[0690h] Main1 Image Horizontal Size Register	211	REG[0694h] Main1 Image Vertical Size Register	212
REG[0698h] Main1 Image X Start Position Register	212	REG[069Ch] Main1 Image Y Start Position Register	213
REG[06A0h] Main1 Window X Start Position Register	213	REG[06A4h] Main1 Window Y Start Position Register	214
REG[06A8h] Main2 Memory Start Address Register	214	REG[06ACh] Main2 Memory Line Address Offset Register	215
REG[06B0h] Main2 Memory Vertical Size Register	215	REG[06B4h] Main2 Image Horizontal Size Register	216
REG[06B8h] Main2 Image Vertical Size Register	216	REG[06BCh] Main2 Image X Start Position Register	217
REG[06C0h] Main2 Image Y Start Position Register	217	REG[06C4h] Main2 Window X Start Position Register	218
REG[06C8h] Main2 Window Y Start Position Register	218		
PIP1 Window Configuration Registers			
REG[0700h] PIP1 Control Register	219	REG[0704h] PIP1 Window Scaling Mode Register	221
REG[0708h] PIP1 Window Horizontal Scale Register	223	REG[070Ch] PIP1 Window Vertical Scale Register	224
REG[0710h] is Reserved	224	REG[0714h] PIP1 Memory Buffer A RGB,Y Start Address Register	225
REG[0718h] PIP1 Memory Buffer A UV Start Address Register	225	REG[071Ch] PIP1 Memory Buffer B RGB,Y Start Address Register	226
REG[0720h] PIP1 Memory Buffer B UV Start Address Register	226	REG[0724h] PIP1 Memory Line Address Offset Register	227
REG[0728h] PIP1 Memory Vertical Size Register	227	REG[072Ch] PIP1 Image Horizontal Size Register	228
REG[0730h] PIP1 Image Vertical Size Register	228	REG[0734h] PIP1 Image X Start Position Register	229
REG[0738h] PIP1 Image Y Start Position Register	229	REG[073Ch] PIP1 Window X Start Position Register	230
REG[0740h] PIP1 Window Y Start Position Register	230	REG[0744h] PIP1 Window X End Position Register	231
REG[0748h] PIP1 Window Y End Position Register	231	REG[074Ch] PIP1 Window Scaler Port Address Counter Control Register	232
REG[0750h] PIP1 Scaler Coefficient Table Access Port Register (AID)	233		
PIP2 Window Configuration Register			
REG[0800h] PIP2 Window Control Register	235	REG[0804h] PIP2 Window Scaling Mode Register	238
REG[0808h] PIP2 Window Horizontal Scale Register	239	REG[080Ch] PIP2 Window Vertical Scale Register	240
REG[0810h] is Reserved	240	REG[0814h] PIP2 Memory Buffer A RGB,Y Start Address Register	241
REG[0818h] PIP2 Memory Buffer A UV Start Address Register	241	REG[081Ch] PIP2 Memory Buffer B RGB,Y Start Address Register	242
REG[0820h] PIP2 Memory Buffer B UV Start Address Register	242	REG[0824h] PIP2 Memory Line Address Offset Register	243
REG[0828h] PIP2 Memory Vertical Size Register	243	REG[082Ch] PIP2 Image Horizontal Size Register	244
REG[0830h] PIP2 Image Vertical Size Register	244	REG[0834h] PIP2 Image X Start Position Register	245
REG[0838h] PIP2 Image Y Start Position Register	245	REG[083Ch] PIP2 Window X Start Position Register	246
REG[0840h] PIP2 Window Y Start Position Register	246	REG[0844h] PIP2 Window X End Position Register	247
REG[0848h] PIP2 Window Y End Position Register	247	REG[084Ch] PIP2 Panorama Area A Scale Register	248
REG[0850h] PIP2 Panorama Area B Scale Register	248	REG[0854h] PIP2 Panorama Area 1 Start Position Register	249
REG[0858h] PIP2 Panorama Area 2 Start Position Register	249	REG[085Ch] PIP2 Panorama Area 3 Start Position Register	250
REG[0860h] PIP2 Panorama Area 4 Start Position Register	250	REG[0864h] PIP2 Linear Panorama Area Delta Register	251
REG[0868h] PIP2 Window Scaler Port Address Counter Control Register	252	REG[086Ch] PIP2 Window Scaler Coefficient Table Access Port Register (AID)	253
AME (Auto Movie Enhancement) Registers			
REG[0900h] AME Control Register	255	REG[0904h] AME Parameter Adjust Register	257
REG[0908h] AME Input Image Width Register	258	REG[090Ch] AME Input Image Height Register	259
REG[0910h] AME Processing Horizontal Start Position Register	260	REG[0914h] AME Processing Horizontal End Position Register	260
REG[0918h] AME Processing Vertical Start Position Register	261	REG[091Ch] AME Processing Vertical End Position Register	261
REG[0920h] AME Sampling Area Vertical Start Position Register	262	REG[0924h] AME Sampling Area Horizontal Start Position Register	262

Table 9-2: S1D13774 Register Set

REG[0928h] AME Sampling Area Size Register	263	REG[092Ch] AME Sampling Area Parameter 1 Register	264
REG[0930h] AME Sampling Area Parameter 2 Register	265	REG[0934h] through REG[0984h] are Reserved	265
Interrupt Control Registers			
REG[0A00h] Interrupt Status Register (AID)	266	REG[0A04h] Interrupt Enable Register	266
REG[0A08h] is Reserved	266		
I2C Slave Configuration Registers			
REG[0B00h] I2C Clock Divide Register	267	REG[0B04h] I2C Enable Register	268
REG[0B08h] is Reserved	268	REG[0B0Ch] is Reserved	268
REG[0B10h] is Reserved	268	REG[0B14h] is Reserved	268
REG[1040h] through REG[1060h] are Reserved	268		

Note

AID = Address auto Increment Disable

The Host can perform continuous register read or write accesses using the Auto Increment function. This function allows reads or writes from/to consecutive addresses without requiring the Index register to be reset. However, some registers do not support the Auto Increment function. These registers are identified as Address auto Increment Disable (AID). For further information on the Register Auto Increment function, refer to Section 14.3, “Register Auto Increment” on page 360.

9.3 Register Restrictions

All reserved bits must be set to the default value unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect.

9.4 Register Descriptions

9.4.1 System Configuration Registers

REG[0000h] Product Information Register 0
Default = 0000_0000h — Read Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Revision Code bits 7-0							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

bits 15-8 Revision Code bits [7:0] (Read Only)
These bits indicate the revision code. The revision code for S1D13774 is 00h.

REG[0004h] Product Information Register 1
Default = 0000_0046h — Read Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Product Code bits 15-8							
15	14	13	12	11	10	9	8
Product Code bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Product Code bits [15:0] (Read Only)
These bits indicate the product code. The product code for the S1D13774 is 0046h.

REG[0008h] Configuration Pin Status Register
Default = 0000_001Xh — Read Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a	Reserved		Reserved	CNF[3:0] Status			
7	6	5	4	3	2	1	0

bits 6-5 Reserved
The default value for these bits is 00b.

bit 4 Reserved
The default value for this bit is 1b.

bits 3-0 CNF[3:0] Status (Read Only)
These bits return the status of the configuration pins CNF[3:0] which are latched at the rising edge of RESET#. For details on the configuration options, refer to Section 4.3, “Summary of Configuration Options” on page 31.

REG[000Ch] is Reserved

This register is Reserved and must not be written. The default value for this register is 0000_0000h.

REG[0010h] is Reserved

This register is Reserved and must not be written. The default value for this register is 0000_0010h.

REG[0014h] is Reserved

This register is Reserved and must not be written. The default value for this register is 0000_0000h.

REG[0018h] Pin Drive Control Register							
Default = 0000_03FFh							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						Video Input Interface Drive Control bits 1-0	
15	14	13	12	11	10	9	8
LCD Interface Drive Control bits 1-0		I2C Drive Control bits 1-0		GPIOP Drive Control bits 1-0		GPIOH Drive Control bits 1-0	
7	6	5	4	3	2	1	0

bits 9-8 Video Input Interface Drive Control bits [1:0]

These bits determine the drive level, in mA, for the Video Input interface output pins.

Table 9-3: Video Input Interface Drive Control Selection

REG[0018h] bits 9-8	Drive Current (mA)	Drive Current (mA)
	HIOVDD = 1.8V	HIOVDD = 2.5V
00b	0.7	1.4
01b	1.4	2.8
10b	3.0	6.0
11b (default)	3.7	7.4

bits 7-6 LCD Interface Drive Control bits [1:0]

These bits determine the drive level, in mA, for the LCD interface output pins.

Table 9-4: LCD Interface Drive Control Selection

REG[0018h] bits 7-6	Drive Current (mA)	Drive Current (mA)
	PIOVDD = 1.8V	PIOVDD = 2.5V
00b	0.7	1.4
01b	1.4	2.8
10b	3.0	6.0
11b (default)	3.7	7.4

bits 5-4 I2C Drive Control bits [1:0]

These bits determine the drive level, in mA, for the I2C output pins.

Table 9-5: I2C Drive Control Selection

REG[0018h] bits 5-4	Drive Current (mA)	Drive Current (mA)
	HIOVDD = 1.8V	HIOVDD = 2.5V
00b	0.7	1.4
01b	1.4	2.8
10b	3.0	6.0
11b (default)	3.7	7.4

bits 3-2 GPIOP Drive Control bits [1:0]

These bits determine the drive level, in mA, for the GPIOP output pins.

Table 9-6: GPIOP Drive Control Selection

REG[0018h] bits 3-2	Drive Current (mA)	Drive Current (mA)
	PIOVDD = 1.8V	PIOVDD = 2.5V
00b	0.7	1.4
01b	1.4	2.8
10b	3.0	6.0
11b (default)	3.7	7.4

bits 1-0 GPIOH Drive Control bits [1:0]

These bits determine the drive level, in mA, for the GPIOH pins and Host interface output pins (INT, TE).

Table 9-7: GPIOH Drive Control Selection

REG[0018h] bits 1-0	Drive Current (mA)	Drive Current (mA)
	HIOVDD = 1.8V	HIOVDD = 2.5V
00b	0.7	1.4
01b	1.4	2.8
10b	3.0	6.0
11b (default)	3.7	7.4

9.4.2 Clock Configuration Registers

REG[0020h] PLL Setting Register 0
Default = 0000_3014h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	Reserved			ND bits 11-8			
15	14	13	12	11	10	9	8
ND bits 7-0							
7	6	5	4	3	2	1	0

bits 14-12 Reserved
The default value for these bits is 011b.

bits 11-0ND bits [11:0]
These bits specify the ND value used for configuring the PLL. For more information on the PLL, see Section 8.3, “PLL Diagram” on page 90.

Table 9-8: ND Selection

REG[0020h] bits 11-0	N = f_{CK} / f_{FN}
000h ~ 008h	Reserved
009h	9
•••	•••
00Fh	15
010h	16
•••	•••
014h (default)	20
•••	•••
FFFh	4095

Where:
ND bits 11-0 = f_{CK} / f_{FN}
f_{CK} = CK frequency (output clock)
f_{CK} = f_{FN} x N
f_{CK} = f_{VCO} / F
f_{FN} = FN frequency (reference clock)

Note
The VCO operation range must be between 60MHz and 165 MHz

REG[0024h] PLL Setting Register 1
Default = 0000_4000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Lock Range Control bits 1-0		n/a					
15	14	13	12	11	10	9	8
n/a		PLL Source Clock Divide Select bits 5-0					
7	6	5	4	3	2	1	0

bits 15-14 Lock Range Control bits [1:0]

These bits control the Lock Range used for configuring the PLL. For more information on the PLL, see Section 8.3, “PLL Diagram” on page 90.

Table 9-9: Lock Range Control Selection

REG[0024h] bits 15-14	F = fvco/fck
00b	1
01b (default)	2
10b	4
11b	8

Where:

f_{VCO} = VCO frequency
$f_{VCO} = f_{FN} \times N \times F$
f_{CK} = CK frequency (output clock)
$f_{CK} = f_{FN} \times N$
$f_{CK} = f_{VCO} / F$

Note

1. The VCO operation range must be between 60MHz and 165 MHz.
2. Total PLL operating current may be lowered by setting these bits to 00b.

bits 5-0 PLL Source Clock Divide Select bits [5:0]

These bits determine the divide ratio between the input clock and the actual internal clock to the PLL. For more information on the clock structure, see Section 8, “Clocks” on page 88.

Table 9-10: PLL Source Clock Divide Ratio Selection

REG[0024h] bits 5-0	Divide Ratio
00h	1:1
01h	2:1
02h	3:1
03h	4:1
...	...
1Fh	32:1
20h	33:1
21h ~ 3Fh	Reserved

Note

1. The internal input clock to the PLL (PLLCLK) must be between 1 MHz and 2 MHz. Depending on the frequency of CLKI or OSCI, these bits must be set accordingly.
2. Values higher than 20h are not allowed.

REG[0028h] Clock Source Select Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved		n/a				OSC Enable	PLL Clock Source Select
15	14	13	12	11	10	9	8
n/a		TV-Out Clock Source Select bits 1-0		Pixel Clock Source Select bits 1-0		System Clock Source Select bits 1-0	
7	6	5	4	3	2	1	0

bits 15-14 Reserved
The default value for these bits is 00b.

bit 9 OSC Enable
This bit is one of the ways to control the internal OSC. The internal OSC can also be controlled using the I2CEN pin when CNF1=1. For details on the clock structure, see Section 8.1, “Clock Diagram” on page 88.
When this bit = 0b, the OSC is disabled. (default)
When this bit = 1b, the OSC is enabled.

Note
1. When this bit =1b, the OSC is enabled regardless of I2CEN/CNF1. When I2CEN is High and CNF1=1, the OSC is enabled regardless of the setting of this bit.
2. The OSC should be enabled when the PLL Clock Source is selected as OSCI/OSCO (REG[0028h] bit 8 = 1b).

bit 8 PLL Clock Source Select
This bit selects the PLL clock source. For details on the clock structure, see Section 8.1, “Clock Diagram” on page 88.
When this bit = 0b, CLKI is the PLL clock source.
When this bit = 1b, OSCI/OSCO is the PLL clock source.

bits 5-4 TV-Out Clock Source Select bits [1:0]

These bits select the TV-Out clock source. When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b), the TV-Out clock source must be either CLKI or OSCI/OSCO and the input frequency must be 27MHz. For details on the clock structure, see Section 8.1, "Clock Diagram" on page 88.

Table 9-11: TV-Out Clock Source Selection

REG[0028h] bits 5-4	TV-Out Clock Source
00b	CLKI
01b	OSCI/OSCO (Note 1)
10b	PLL (Note 2)
11b	Reserved

Note

1. When OSCI/OSCO is selected as the TV-Out clock source, the OSC must be enabled (REG[0028h] bit 9 = 1b), otherwise the TV-Out clock source is CLKI.
2. When the PLL is not selected as the system clock source (REG[0028h] bits 1-0 ≠ 10b), the PLL should not be selected as the TV-Out clock source.

bits 3-2 Pixel Clock Source Select bits [1:0]

These bits select the pixel clock source as follows. For details on the clock structure, see Section 8.1, "Clock Diagram" on page 88.

Table 9-12: Pixel Clock Source Selection

REG[0028h] bits 3-2	Pixel Clock Source
00b	CLKI
01b	OSCI/OSCO (Note 1)
10b	PLL (Note 2)
11b	Reserved

Note

1. When OSCI/OSCO is selected as the Pixel clock source, the OSC must be enabled (REG[0028h] bit 9 = 1b), otherwise the Pixel clock source is CLKI.
2. When the PLL is not selected as the system clock source (REG[0028h] bits 1-0 ≠ 10b), the PLL should not be selected as the Pixel clock source.

bits 1-0 System Clock Source Select bits [1:0]

These bits select the system clock source as follows. For details on the clock structure, see Section 8.1, “Clock Diagram” on page 88.

Table 9-13: System Clock Source Selection

REG[0028h] bits 1-0	System Clock Source
00b	CLKI
01b	OSCI/OSCO (see Note)
10b	PLL
11b	Reserved

Note
When OSCI/OSCO is selected as the System clock source, the OSC must be enabled (REG[0028h] bit 9 = 1b), otherwise the System clock source is CLKI.

REG[002Ch] Power Save Mode Register (AID)
Default = 0000_0000h : Address auto increment disable — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						Force PLL Lock	PLL Lock (RO)
15	14	13	12	11	10	9	8
HIF Memory Access Status (RO)	TV-Out Memory Access Status (RO)	LCD Memory Access Status (RO)	Sub Memory Write Path Memory Access Status (RO)	Main Memory Write Path Memory Access Status (RO)	n/a	Power Save Mode Select bits 1-0	
7	6	5	4	3	2	1	0

bit 9 Force PLL Lock

This bit overrides the PLL Lock bit, REG[002Ch] bit 8.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, the PLL Lock bit is forced high.

bit 8 PLL Lock (Read Only)

This bit indicates the status of the PLL output.
When this bit = 0b, the PLL output is not stable. In this state the display buffer must not be accessed.
When this bit = 1b, the PLL output is stable.

Note
When the PLL is disabled (REG[002Ch] bits 1-0 = 00b), the status of this bit should be ignored.

bit 7 HIF Memory Access Status (Read Only)

This bit indicates the status of the memory access by the Host interface.
When this bit = 0b, the status is ready.
When this bit = 1b, the status is busy.

bit 6 TV-Out Memory Access Status (Read Only)
This bit indicates the status of the memory access by the TV-Out interface.
When this bit = 0b, the status is ready.
When this bit = 1b, the status is busy.

bit 5 LCD Memory Access Status (Read Only)
This bit indicates the status of the memory access by LCD interface.
When this bit = 0b, the status is ready.
When this bit = 1b, the status is busy.

bit 4 Sub Memory Write Path Memory Access Status (Read Only)
This bit indicates the status of the memory access by the Sub Memory Write Path.
When this bit = 0b, the status is ready.
When this bit = 1b, the status is busy.

bit 3 Main Memory Write Path Memory Access Status (Read Only)
This bit indicates the status of the memory access by the Main Memory Write Path.
When this bit = 0b, the status is ready.
When this bit = 1b, the status is busy.

bits 1-0 Power Save Mode Select bits [1:0]
These bits control power save mode as follows. For details, see Section 10, “Power Save Modes” on page 269.

Table 9-14: Power Save Mode Selection

REG[002Ch] bits 1-0	Power Save Mode	PLL	DRAM	System Clock
00b	Sleep Mode (Note 3)	OFF	OFF	OFF
01b	Standby Mode A (Note 3)	ON (Note 1)	OFF	OFF
10b	Standby Mode B (Note 3)	ON (Notes 1,2)	ON	OFF
11b	Normal Operation Mode	ON (Notes 1,2)	ON	ON

Note

1. When the PLL is not used as the system clock source (REG[0028h] bits 1-0 ≠ 10b), the PLL is disabled in these modes.
2. Confirm all memory accesses have stopped (REG[002Ch] bits 7-3 = 0_0000b) before changing from Normal Operation Mode to Standby Mode B.
3. The Video Input Interface must be disabled (REG[0480h] bit 7 = 0b) and the Display Output Port must be set to “All Off” (REG[0604h] bits 11-8 = 0000b) before entering Standby or Sleep power save mode.

REG[0030h] I2C Quick Enable Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							I2C Quick Enable
7	6	5	4	3	2	1	0

Note
The I2C interface cannot access this register.

bit 0 I2C Quick Enable
When this bit = 0b, I2C is disabled and the clock supply to the I2C module is stopped.
When this bit = 1b, I2C is enabled and the clock, as selected by CNF1 (CLKI or OSCI,OSCO), is supplied to the I2C module.

Note
This bit has the same function as the I2CEN pin.

9.4.3 Software Reset Register

REG[0040h] Software Reset Register (AID)
Default = not applicable : Address auto increment disable — Write Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Software Reset bits 15-8							
15	14	13	12	11	10	9	8
Software Reset bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Software Reset bits [15:0] (Write Only)
When any value is written to these bits, all registers except REG[0000h]~REG[003Fh], REG[0300h]~REG[0350h], REG[0B00h]~REG[0B14h], and REG[1040h]~REG[1060h] are reset to their default values. A software reset using these bits does not clear the display buffer.

Note
The Host cannot write to this register using the I2C interface.

9.4.4 SDRAM Control Registers

REG[0080h] Memory Controller Software Reset Register
Default = not applicable — Write Only

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
							Memory Controller Software Reset

bit 0 Memory Controller Software Reset (Write Only)
This bit performs a software reset of the memory controller. It has no effect on the configuration registers, REG[0084h] ~ REG[0090h].
Writing a 0b to this bit has no effect on the memory controller.
Writing a 1b to this bit resets the memory controller. If the S1D13774 is in a mode where the memory controller should be active, the power-on sequence is started after the reset completes.

This bit is automatically cleared after the module reset is done.

REG[0084h] Auto Refresh Interval Setting Register
Default = 0000_025Ch — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Auto Refresh Interval Setting bits 9-8	
7	6	5	4	3	2	1	0
Auto Refresh Interval Setting bits 7-0							

bits 9-0 Auto Refresh Interval Setting bits [9:0]
These bits determine the auto refresh interval for the memory and should be set according to the following formula:

REG[0084h] bits 9-0= int(8,000,000 ÷ (1024 x (SYSCLK_PERIOD in ns))) - D

Where:

D = 21 when SYSCLK > 55.5MHz
= 19 when SYSCLK ≤ 55.5MHz

Table 9-15: Auto Refresh Interval Setting Examples

Frequency (MHz)	REG[0084h] bits 9-0
50	173h
66.67	1F3h
71	215h

REG[0088h] Power-On Sequence Timing Control Register
Default = 0000_003Fh Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a	Power-On Sequence Timing Control bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 Power-On Sequence Timing Control bits [6:0]

These bits control the power on sequence timing (tRST and tPS) and should be set according to the following formula:

REG[0088h] bits 6-0 = 200,000 ÷ (SYSCLK_PERIOD in ns) ÷ 256 + 1

Table 9-16: Power-On Sequence Timing Examples

Frequency (MHz)	REG[0088h] bits 6-0
50	28h
66.67	35h
71	38h

REG[008Ch] Timing Control Register
Default = 0000_2513h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a		Read Latency Setting bits 1-0		n/a	Timing Control for Write to Precharge Command Period	n/a	Timing Control for Precharge to Active/Refresh Command Period
7	6	5	4	3	2	1	0
n/a			Timing Control for Active to Read/Write Command Period	n/a	Timing Control for Refresh to Refresh/Active Command bits 2-0		

bits 13-12 Read Latency Setting bits [1:0]

These bits specify the read latency for the memory and should be set according to the system clock frequency.

Table 9-17: Read Latency Selection

REG[008Ch] bits 13-12	System Clock Frequency
00b	Reserved
01b	SYSCLK < 55.5MHz
10b (default)	SYSCLK ≥ 55.5MHz
11b	Reserved

bit 10 Timing Control for Write to Precharge Command Period

This bit controls the timing for the Write to Precharge Command Period (tWR) and should be set according to the system clock frequency.

Table 9-18: Timing Control for Write to Precharge Command Period Selection

REG[008Ch] bit 10	System Clock Frequency
0b	40MHz ≤ SYSCLK ≤ 71MHz
1b (default)	Reserved

bit 8 Timing Control for Precharge to Active/Refresh Command Period
This bit controls the timing for the Precharge to Active/Refresh Command Period (tRP) and should be set according to the system clock frequency.

Table 9-19: Timing Control for Precharge to Active/Refresh Command Period Selection

REG[008Ch] bit 8	System Clock Frequency
0b	SYSCLK < 55.5MHz
1b (default)	SYSCLK ≥ 55.5MHz

bit 4 Timing Control for Active to Read/Write Command Period
This bit controls the timing for the Active to Read/Write Command Period (tRCD) and should be set according to the system clock frequency.

Table 9-20: Timing Control for Active to Read/Write Command Period Selection

REG[008Ch] bit 4	System Clock Frequency
0b	SYSCLK < 55.5MHz
1b (default)	SYSCLK ≥ 55.5MHz

bits 2-0 Timing Control for Refresh to Refresh/Active Command Period bits [2:0]
These bits control the timing for the Refresh to Refresh/Active Command Period (tRC(REF)) and should be set according to the system clock frequency.

Table 9-21: Timing Control for Refresh to Refresh/Active Command Period Selection

REG[008Ch] bits 2-0	System Clock Frequency
000b	Reserved
001b	SYSCLK < 50MHz
010b	50MHz ≤ SYSCLK < 66.67MHz
011b (default)	SYSCLK ≥ 66.67MHz
100b - 111b	Reserved

REG[0090h] is Reserved

This register is Reserved and should not be written.

REG[0094h] Memory Control Status Flag Register (AID)
Default = 0000_0000h : Address auto increment disable — Read Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							Memory Controller Active Status
15	14	13	12	11	10	9	8
Reserved				n/a		Memory Controller Auto Refresh Failure Status Flag	Memory Controller Ready Status Flag
7	6	5	4	3	2	1	0

bit 8 Memory Controller Active Status (Read Only)
This bit indicates the status of the memory controller.
When this bit = 0b, the memory controller is not active (disabled).
When this bit = 1b, the memory controller is active (enabled).

bits 7-4 Reserved
The default value for these bits is 0000b.

bit 1 Memory Controller Auto Refresh Failure Raw Status (Read Only)
This bit indicates when the auto refresh cycle fails.
When this bit = 0b, the auto refresh cycle has not failed.
When this bit = 1b, the auto refresh cycle has failed.

bit 0 Memory Controller Ready Status Flag (Read Only)
This bit indicates when the memory controller power-on sequence is complete.
When this bit = 0b, the power-on sequence is not complete.
When this bit = 1b, the power-on sequence is complete.

Note

The power-on sequence time is approximately 410us. This time is required when changing to Standby Mode B from either Standby Mode A or Sleep Mode. The power-on sequence time is defined from when Standby Mode B is selected (REG[002Ch] bits 1-0 = 10b) until the Memory Controller Ready Status Flag returns 1b (REG[0094h] bit 0 = 1b).

9.4.5 LCD Interface Configuration Registers

REG[0100h] LCD Interface Clock Setting Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Parallel Command Clock Divide Select bits 3-0				n/a	Serial Clock Divide Select bits 2-0		
7	6	5	4	3	2	1	0
n/a			Pixel Clock Divide Select bits 4-0				

bits 15-12 Parallel Command Clock Divide Select bits [3:0]
These bits specify the divide ratio for the Parallel Command Clock which is used for LCD2 parallel command/parameter accesses. The clock source for the Parallel Command Clock is the non-divided Pixel Clock. For LCD2 parallel frame transfers, the Pixel Clock is used (see REG[0100h] bits 4-0). For further information on clock structure, see Section 8, “Clocks” on page 88.

Table 9-22: Parallel Command Clock Divide Ratio Selection

REG[0100h] bits 15-12	Parallel Command Clock Divide Ratio	REG[0100h] bits 15-12	Parallel Command Clock Divide Ratio
0000b	1:1	1000b	9:1
0001b	2:1	1001b	10:1
0010b	3:1	1010b	11:1
0011b	4:1	1011b	12:1
0100b	5:1	1100b	13:1
0101b	6:1	1101b	14:1
0110b	7:1	1110b	15:1
0111b	8:1	1111b	16:1

bits 10-8 Serial Clock Divide Select bits [2:0]
These bits specify the divide ratio for the Serial Clock. The clock source for the Serial Clock is the non divided Pixel Clock. If LCD2 is not a serial interface type LCD panel (REG[0104h] bits 1-0), these bits are ignored. For further information on clock structure, see Section 8, “Clocks” on page 88.

Table 9-23: Serial Clock Divide Ratio Selection

REG[0100h] bits 10-8	Serial Clock Divide Ratio	REG[0100h] bits 10-8	Serial Clock Divide Ratio
000b	2:1	100b	10:1
001b	4:1	101b	12:1
010b	6:1	110b	14:1
011b	8:1	111b	16:1

Note
The Serial Clock frequency cannot be lower than the SYSCLK frequency ÷ 32.

bits 4-0 Pixel Clock Divide Select bits [4:0]

These bits specify the divide ratio for the Pixel Clock. The clock source for the Pixel Clock is selected by the Pixel Clock Source Select bits, REG[0028h] bits 3-2. For LCD1 RGB type panels, the Pixel Clock is the same as the shift clock. When LCD2 is a parallel interface type panel (REG[0104h] bits 1-0 = 01b or 10b), the Pixel Clock is used for the parallel data output timing clock. For further information on clock structure, see Section 8, "Clocks" on page 88.

Table 9-24: Pixel Clock Divide Ratio Selection

REG[0100h] bits 4-0	Pixel Clock Divide Ratio	REG[0100h] bits 4-0	Pixel Clock Divide Ratio
00000b	1:1 (Note 1)	10000b	17:1
00001b	2:1	10001b	18:1
00010b	3:1	10010b	19:1
00011b	4:1	10011b	20:1
00100b	5:1	10100b	21:1
00101b	6:1	10101b	22:1
00110b	7:1	10110b	23:1
00111b	8:1	10111b	24:1
01000b	9:1	11000b	25:1
01001b	10:1	11001b	26:1
01010b	11:1	11010b	27:1
01011b	12:1	11011b	28:1
01100b	13:1	11100b	29:1
01101b	14:1	11101b	30:1
01110b	15:1	11110b	31:1
01111b	16:1	11111b	32:1

Note

1. Pixel Clock Frequency ≤ System Clock Frequency ÷ 2
2. For the LCD2 parallel panel interface, the Pixel Clock frequency cannot be lower than the SYSCLK frequency ÷ 32.

REG[0104h] LCD Interface Configuration Register
Default = 0000_4000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved	VNDP Status (RO)	n/a	FPCS2# Polarity Select	Reserved	A0 Polarity Select	FPDRDY Polarity Select	FPCS1# Polarity Select
15	14	13	12	11	10	9	8
FPSHIFT Polarity Select	Command/ Parameter Port Select	RGB Interface Panel Data Bus Width	n/a		LCD2 Parallel Interface Pins Select	LCD Panel Interface bits 1-0	
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0b.

bit 14 Vertical Non-Display Period Status (Read Only)
This bit indicates whether the LCD1 panel is in a Vertical Non-Display Period (VNDP).
When this bit = 0b, the LCD1 panel output is in a Vertical Display Period.
When this bit = 1b, the LCD1 panel output is in a Vertical Non-Display Period.

bit 12 FPCS2# Polarity Select
This bit sets the polarity of the LCD2 interface chip select (FPCS2#) for parallel/serial type panels.
When this bit = 0b, the FPCS2# signal is not reversed. (Active Low)
When this bit = 1b, the FPCS2# signal is reversed. (Active High)

Note
For Mode 3-2 or Mode 3-3 (see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34), the FPCS2# pin (which is unused) will toggle during LCD2 activity.

bit 11 Reserved
The default value for this bit is 0b.

bit 10 A0 Polarity Select
This bit is only for parallel/serial interface panels on LCD1 or LCD2 and has no effect for RGB type panels. During an LCD Interface Command (see REG[0108h]) or LCD Interface Parameter (see REG[010Ch]) transfer, FPSA0/P2A0 is driven high or low based on the setting of this bit. When LCD1 is a 9-bit serial panel (REG[0168h] bits 7-5 = 001b) or LCD2 is a 9-bit serial panel (REG[0188h] bit 5 = 1b), this bit determines the MSB of the 9-bit data on FPSO.

For LCD2 frame transfers (REG[0114h] bits 1-0), this bits selects the active level.

Table 9-25: A0 Polarity Setting

REG[0104h] bit 10	FPSA0/P2A0 Signal Output		
	Command	Parameter	Frame Transfer
0b	Low	High	Active High
1b	High	Low	Active Low

bit 9 FPDRDY Polarity Select

This bit sets the polarity of the data ready signal (FPDRDY) for RGB type panels.
When this bit = 0b, the FPDRDY signal is not reversed.
When this bit = 1b, the FPDRDY signal is reversed.

bit 8 FPCS1# Polarity Select

This bit sets the polarity of the LCD1 interface chip select (FPCS1#) for serial type panels.

For 4 wire 8-bit or 3 wire 9-bit serial panels:
When this bit = 0b, the FPCS1# signal is not reversed. (Active Low)
When this bit = 1b, the FPCS1# signal is reversed. (Active High)

For uWire or 24-bit serial panels:
When this bit = 0b, the FPCS1# signal is not reversed. (Active High)
When this bit = 1b, the FPCS1# signal is reversed. (Active Low)

bit 7 FPSHIFT Polarity Select

This bit sets the polarity of the shift clock for RGB type panels (inverts FPSHIFT).

If the Pixel Clock Divide Ratio is 1:1 (REG[0100h] bits 4-0 = 00000b):
When this bit = 0b, all panel interface signals change at the falling edge of FPSHIFT.
When this bit = 1b, all panel interface signals change at the rising edge of FPSHIFT.

If the Pixel Clock Divide Ratio is **not** 1:1 (REG[0100h] bits 4-0 ≠ 00000b):
When this bit = 0b, all panel interface signals change at the rising edge of FPSHIFT.
When this bit = 1b, all panel interface signals change at the falling edge of FPSHIFT.

bit 6 Command/Parameter Port Select

This bit determines which output port is selected for command/parameter transfers forwarded from REG[0108h] ~ REG[0110h].
When this bit = 0b, the LCD1 port is selected for serial command/parameter transfers.
When this bit = 1b, the LCD2 port is selected for serial or parallel command/parameter transfers.

Note

For serial interfaces, either REG[0168h] bits 1-0 or REG[0188h] bits 1-0 are used to specify the serial clock phase and serial clock polarity according to the setting of the Command/Parameter Port Select bit (REG[0104h] bit 6) and the Display Output Port Status bits (REG[0604h] bits 15-12). The following table summarizes which register bits are used for each case.

Table 9-26: Serial Interface Clock Phase and Polarity Configuration

Phase/Polarity	Serial Interface	Display Port Status (REG[0604h] bits 15-12)			
		Off (0000b)	LCD1 (0001b	LCD2 (0010b)	Other
LCD1 Serial Clock Phase	LCD1 (REG[0104h] bit 6 = 0b)	REG[0168h] bit 1	REG[0168h] bit 1	REG[0188h] bit 1	REG[0168h] bit 1
LCD1 Serial Clock Polarity		REG[0168h] bit 0	REG[0168h] bit 0	REG[0188h] bit 0	REG[0168h] bit 0
LCD2 Serial Clock Phase	LCD2 (REG[0104h] bit 6 = 1b)	REG[0168h] bit 1	REG[0168h] bit 1	REG[0188h] bit 1	REG[0168h] bit 1
LCD2 Serial Clock Polarity		REG[0168h] bit 0	REG[0168h] bit 0	REG[0188h] bit 0	REG[0168h] bit 0

bit 5 RGB Interface Panel Data Bus Width

This bit determines the LCD1 RGB interface panel data bus width (or size).
When this bit = 0b, the LCD1 RGB interface panel data bus is 18-bit.
When this bit = 1b, the LCD1 RGB interface panel data bus is 24-bit.

bit 2 LCD2 Parallel Interface Pins Select

When the LCD2 parallel interface is configured to use different pins than the LCD1 interface (REG[0104h] bits 1-0 = 10b), these bits select which pins are used. For detailed LCD interface pin mapping, refer to Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.
When this bit = 0b, the LCD2 parallel panel uses GPIOP0 to GPIOP9.
When this bit = 1b, the LCD2 parallel panel uses GPIOH13 to GPIOH23.

Note

This bit should be configured such that the LCD2 parallel interface does not use the same pins as the TV-Out interface (see REG[0200h] bit 2). For a summary of the possible LCD and TV-Out interface modes, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.

bits 1-0 LCD Panel Interface bits [1:0]

These bits determine the LCD panel types for each LCD interface (LCD1 and LCD2). For detailed LCD interface pin mapping, refer to Section 4.6, "LCD and TV-out Interface Pin Mapping" on page 34.

Table 9-27: LCD Panel Interface Selection

REG[0104h] bits 1-0	Mode	LCD1 Panel Interface	LCD2 Panel Interface
00b	1	RGB Interface with Serial Interface	Serial Interface (RAM integrated)
01b	2		Parallel Interface (RAM integrated) (LCD1 and LCD2 data bus use common pins)
10b	3		Parallel Interface (RAM integrated) (LCD1 data pins differ from LCD2 data bus pins)
11b	Reserved		

REG[0108h] LCD Interface Command Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
LCD Interface Command bits 15-8							
15	14	13	12	11	10	9	8
LCD Interface Command bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 LCD Interface Command bits [15:0]

These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels. These bits form the command register for the LCD1 serial and LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used.

When the LCD interface is busy (REG[0114h] bit 4 = 1b), these bits must not be written.

When the LCD interface is not busy (REG[0114h] bit 4 = 0b), the command transfer starts when these bits are written. When the command transfer starts, the FPA0 pin is driven low or high depending on the state of the A0 Polarity Select bit (REG[0104h] bit 10).

Note

1. If the LCD1 serial data type is set to uWIRE (REG[0168h] bits 7-5 = 10xb), the upper byte of REG[0108h] is used for A[7:0] and the lower byte is used for D[7:0].
2. Before the command transfer starts, the output port must be selected (see REG[0104h] bit 6).

REG[010Ch] LCD Interface Parameter Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
LCD Interface Parameter bits 15-8							
15	14	13	12	11	10	9	8
LCD Interface Parameter bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 LCD Interface Parameter Register bits [15:0]

These bits are only for parallel/serial interface panels on LCD1 or LCD2 and have no effect for RGB type panels. These bits form the parameter register for the LCD1 serial and LCD2 parallel/serial interfaces. For 8-bit parallel or serial interfaces, only the lower byte is used.

When the LCD interface is busy (REG[0114h] bit 4 = 1b), these bits must not be written. When the LCD interface is not busy (REG[0114h] bit 4 = 0b), data transfer starts when these bits are written. When the data transfer starts, the FPA0 pin is driven high or low depending on the state of the A0 Polarity Select bit (REG[0104h] bit 10).

Note

1. If the LCD1 serial data type is set to uWIRE (REG[0168h] bits 7-5 = 10xb), the upper byte of REG[010Ch] is used for A[7:0] and the lower byte is used for D[7:0].
2. Before the command transfer starts, the output port must be selected (see REG[0104h] bit 6).

REG[0110h] LCD Interface ID Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
LCD Interface ID bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 LCD Interface ID bits [7:0]

These bits are used for D[23:16] when a 24-bit Serial Interface is selected, REG[0168h] bits 7-5 = 111b or REG[0188h] bits 7-5 = 111b.

REG[0114h] LCD2 Interface Frame Transfer Register (AID)							
Default = 0000_0000h: Address auto increment disable							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			LCD Serial/Parallel Interface Status (RO)	n/a	LCD2 Auto Frame Transfer Trigger Select	LCD2 Interface Auto Frame Transfer Enable	LCD2 Interface Frame Transfer Trigger
7	6	5	4	3	2	1	0

bit 4 LCD Serial/Parallel Interface Status (Read Only)

This bit indicates the status of the LCD1 serial or LCD2 serial/parallel interface. This bit should be read to confirm that the LCD1 serial or LCD2 serial/parallel interface is not busy before transmitting data to the panel.

When this bit = 0b, the LCD1 serial or LCD2 serial/parallel interface is not busy (or ready).

When this bit = 1b, the LCD1 serial or LCD2 serial/parallel interface is busy.

bit 2 LCD2 Interface Auto Frame Transfer Trigger Select

This bit selects the trigger method used when auto frame transfers are enabled, REG[0114h] bit 1 = 1b.

When this bit = 0b, auto frame transfers are synchronized with the Main Memory Write Path write end.

When this bit = 1b, auto frame transfers are synchronized with the Sub Memory Write Path write end.

bit 1 LCD2 Interface Auto Frame Transfer Enable

This bit is only for parallel/serial interfaces on LCD2. This bit controls automatic frame transfers of one frame of display memory to the LCD2 interface. Frame transfers are triggered and synchronized with the DRAM write end (see REG[0114h] bit 2).

When this bit = 0b, auto frame transfer is disabled.

When this bit = 1b, auto frame transfer is enabled.

When this bit = 1b, the LCD2 Interface Status bit (REG[0114h] bit 4) is always busy. When busy, command/parameter and frame transfers cannot be sent manually. This bit should be disabled before Host/Video input is disabled.

bit 0 LCD2 Interface Frame Transfer Trigger

This bit is only for parallel/serial interface panels on LCD2 and has no effect for RGB type panels. This bit is the trigger to transfer 1 frame of data to the LCD interface.

When this bit is set to 1 and the LCD interface is busy (REG[0114h] bit 4 = 1b), the frame transfer request is ignored. Once the LCD interface is no longer busy, this bit is cleared without transferring any data.

When this bit is set to 1 and the LCD interface status is not busy (REG[0114h] bit 4 = 0b), 1 frame of data is transferred to the LCD interface. When the data transfer is finished, this bit is cleared automatically.

Note

When auto frame Transfer is enabled (REG[0114h] bit 1 = 1b), this bit indicates the status of the auto frame transfer.

When this bit = 0b, the auto frame transfer is inactive.

When this bit = 1b, the auto frame transfer is active.

9.4.6 LCD1 Configuration Registers

REG[0140h] LCD1 Horizontal Total (FPLINE Period) Register
Default = 0000_0001h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LCD1 Horizontal Total (FPLINE Period) bits 6-0							

bits 6-0 LCD1 Horizontal Total (FPLINE Period) bits [6:0]
These bits are for RGB Interface panels only and have no effect for a serial interface panel. These bits specify the Horizontal Total (HT), or FPLINE period, for LCD1, in 8 pixel resolution. The Horizontal Total is the sum of the Horizontal Display Period and the Horizontal Non-Display Period. The maximum Horizontal Total is 1024 pixels.

REG[0140h] bits 6-0 = (Horizontal Total in pixels ÷ 8) - 1

Note
These bits must be programmed such that the following are valid.

REG[0140h] bits 6-0 > 0

HT ≥ HDP + HDPS

REG[0144h] LCD1 Horizontal Display Period Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							LCD1 HDP bit 8
15	14	13	12	11	10	9	8
LCD1 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 LCD1 Horizontal Display Period bits [8:0]
These bits specify the Horizontal Display Period (HDP) for LCD1, in 2 pixel resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display Period.

REG[0144h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

REG[0148h] LCD1 Horizontal Display Period Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						LCD1 Horizontal Display Period Start Position bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Horizontal Display Period Start Position bits 7-0							

bits 9-0 LCD1 Horizontal Display Period Start Position bits [9:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel. These bits specify the Horizontal Display Period Start Position (HDPS) for LCD1 in 1 pixel resolution.

REG[0148h] bits 9-0 = Horizontal Display Period Start Position in pixels - 9

REG[014Ch] LCD1 Horizontal Pulse (FPLINE) Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LCD1 Horizontal Pulse (FPLINE) Polarity	LCD1 Horizontal Pulse (FPLINE) Width bits 6-0						

bit 7 LCD1 Horizontal Pulse (FPLINE) Polarity

These bits are for RGB Interface panels only and have no effect for a serial interface panel. This bit selects the polarity of the horizontal pulse signal, or FPLINE, for LCD1.
When this bit = 0b, the horizontal pulse signal, or FPLINE, is active low. (default)
When this bit = 1b, the horizontal pulse signal, or FPLINE, is active high.

bits 6-0 LCD1 Horizontal Pulse (FPLINE) Width bits [6:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel. These bits specify the width of the horizontal pulse signal, or FPLINE, for LCD1, in 1 pixel resolution.

REG[014Ch] bits 6-0 = HSYNC Pulse Width in pixels - 1

REG[0150h] LCD1 Horizontal Pulse (FPLINE) Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						LCD1 Horizontal Pulse (FPLINE) Start Position bits 9-8	
7	6	5	4	3	2	1	0
LCD1 HSYNC Pulse (FPLINE) Start Position bits 7-0							

bits 9-0 LCD1 Horizontal Pulse (FPLINE) Start Position bits [9:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel.

These bits specify the start position of the horizontal pulse (HPP) for LCD1, in pixels.

REG[0150h] bits 9-0 = VSYNC edge to HSYNC edge in pixels - 1

REG[0154h] LCD1 Vertical Total (FPFRAME Period) Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Total (FPFRAME Period) bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Total (FPFRAME Period) bits 7-0							

bits 9-0 LCD1 Vertical Total (FPFRAME Period) bits [9:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel.

These bits specify the Vertical Total (VT), or FPFRAME period, for LCD1, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period. The maximum Vertical Total is 1024 lines.

REG[0154h] bits 9-0 = Vertical Total in lines - 1

Note

This register must be programmed such that the following formula is valid.

$VT > VDPS + VDP$

$VT - VDP \geq 3$

REG[0158h] LCD1 Vertical Display Period Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Display Period bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Display Period bits 7-0							

bits 9-0 Vertical Display Period bits [9:0]

These bits specify the Vertical Display Period (VDP) for LCD1, in 1 line resolution. The Vertical Display Period must be less than the Vertical Total to allow for a sufficient Vertical Non-Display period.

REG[00158h] bits 9-0 = Vertical Display Period in lines - 1

REG[015Ch] LCD1 Vertical Display Period Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Display Period Start Position bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Display Period Start Position bits 7-0							

bits 9-0 LCD1 Vertical Display Period Start Position bits [9:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel. These bits specify the Vertical Display Period Start Position (VDPS) for LCD1, in 1 line resolution.

REG[015Ch] bits 9-0 = Vertical Display Period Start Position in lines

REG[0160h] LCD1 Vertical Pulse (FPFRAME) Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
LCD1 Vertical Pulse (FPFRAME) Polarity	n/a				LCD1 Vertical Pulse (FPFRAME) Width bits 2-0		

bit 7 LCD1 Vertical Pulse (FPFRAME) Polarity

These bits are for RGB Interface panels only and have no effect for a serial interface panel.
This bit selects the polarity of the vertical pulse signal (FPFRAME) for LCD1.
When this bit = 0b, the vertical pulse signal (FPFRAME) is active low. (default)
When this bit = 1b, the vertical pulse signal (FPFRAME) is active high.

bits 2-0 LCD1 Vertical Pulse (FPFRAME) Width bits [2:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel.
These bits specify the width of the vertical pulse signal for LCD1, in lines.

REG[0160h] bits 2-0 = VSYNC Pulse Width in lines - 1

REG[0164h] LCD1 Vertical Pulse (FPFRAME) Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						LCD1 Vertical Pulse (FPFRAME) Start Position bits 9-8	
7	6	5	4	3	2	1	0
LCD1 Vertical Pulse (FPFRAME) Start Position bits 7-0							

bits 9-0 LCD1 Vertical Pulse (FPFRAME) Start Position bits [9:0]

These bits are for RGB Interface panels only and have no effect for a serial interface panel.
These bits specify the start position of the vertical pulse signal (FPFRAME) for LCD1, in lines.

REG[0164h] bits 9-0 = Vertical Pulse Start Position in lines

REG[0168h] LCD1 Serial Interface Setting Register
Default = 0000_0001h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
LCD1 Serial Data Type bits 2-0			LCD1 Serial Data Direction	n/a		LCD1 Serial Clock Phase	LCD1 Serial Clock Polarity
7	6	5	4	3	2	1	0

bits 7-5 LCD1 Serial Data Type bits [2:0]

These bits determine the serial data type for LCD1. For AC timing information, see Section 6.7.2, “LCD1, LCD2 4 Wire 8-Bit Serial Interface Timing” on page 66, Section 6.7.3, “LCD1, LCD2 3 Wire 9-Bit Serial Interface Timing” on page 68, Section 6.7.4, “LCD1 uWire Serial Interface Timing” on page 70, and Section 6.7.5, “LCD1, LCD2 24-bit Serial Interface Timing” on page 71.

Table 9-28: LCD1 Serial Data Type Selection

REG[0168h] bits 7-5	LCD1 Serial Data Type
000b	4 pins (8-bit Serial)
001b	3 pins (9-bit Serial)
010b ~ 011b	Reserved
10xb	uWire (16-bit Serial)
110b	Reserved
111b	24-bit Serial

bit 4 LCD1 Serial Data Direction

This bit determines the serial data direction for LCD1. For details on timing, see Section 6.7, “Panel Interface Timing” on page 64 and refer to the appropriate serial interface.
When this bit = 0b, the msb (most significant bit) is first.
When this bit = 1b, the lsb (least significant bit) is first.

Note
When a 24-bit serial data type is selected (REG[0168h] bits 7-5 = 111b), this bit is not supported and must be set to 0b.

bit 1 LCD1 Serial Clock Phase

This bit specifies the serial clock (FPSCK) phase for LCD1. For a summary of the serial clock phase and polarity settings, see Section Table 9-29:, “LCD1 Serial Clock Polarity and Phase Selection” on page 129. For details on timing, see Section 6.7, “Panel Interface Timing” on page 64 and refer to the appropriate serial interface.

bit 0 LCD1 Serial Clock Polarity

This bit determines the serial clock (FPSCK) polarity for LCD1. For a summary of the serial clock phase and polarity settings, see Section Table 9-29:, “LCD1 Serial Clock Polarity and Phase Selection” on page 129. For details on timing, see Section 6.7, “Panel Interface Timing” on page 64 and refer to the appropriate serial interface.

Table 9-29: LCD1 Serial Clock Polarity and Phase Selection

REG[0168h] bit 1	REG[0168h] bit 0	Serial Data Output Changes	Idling Status of Clock
0b	0b	Falling edge of Serial Clock	Low
0b	1b	Rising edge of Serial Clock	High
1b	0b	Rising edge of Serial Clock	Low
1b	1b	Falling edge of Serial Clock	High

Note

For serial interfaces, either REG[0168h] bits 1-0 or REG[0188h] bits 1-0 are used to specify the serial clock phase and serial clock polarity according to the setting of the Command/Parameter Port Select bit (REG[0104h] bit 6) and the Display Output Port Status bits (REG[0604h] bits 15-12). The following table summarizes which register bits are used for each case.

Table 9-30: Serial Interface Clock Phase and Polarity Configuration

Phase/Polarity	Serial Interface	Display Port Status (REG[0604h] bits 15-12)			
		Off (0000b)	LCD1 (0001b	LCD2 (0010b)	Other
LCD1 Serial Clock Phase	LCD1 (REG[0104h] bit 6 = 0b)	REG[0168h] bit 1	REG[0168h] bit 1	REG[0188h] bit 1	REG[0168h] bit 1
LCD1 Serial Clock Polarity		REG[0168h] bit 0	REG[0168h] bit 0	REG[0188h] bit 0	REG[0168h] bit 0
LCD2 Serial Clock Phase	LCD2 (REG[0104h] bit 6 = 1b)	REG[0168h] bit 1	REG[0168h] bit 1	REG[0188h] bit 1	REG[0168h] bit 1
LCD2 Serial Clock Polarity		REG[0168h] bit 0	REG[0168h] bit 0	REG[0188h] bit 0	REG[0168h] bit 0

REG[016Ch] is Reserved (AID)

This register is Reserved and should not be written.

REG[0170h] is Reserved

This register is Reserved and should not be written.

REG[0174h] is Reserved

This register is Reserved and should not be written.

9.4.7 LCD2 Configuration Registers

REG[0180h] LCD2 Horizontal Display Period Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							LCD2 HDP bit 8
15	14	13	12	11	10	9	8
LCD2 Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 LCD2 Horizontal Display Period bits [8:0]

These bits specify the Horizontal Display Period for LCD2, in 2 pixel resolution.

REG[0180h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note

For Parallel and Serial interface panels (see REG[0104h] bits 1-0), the following formula must be valid.

HDP x VDP ≥ 40 pixels

REG[0184h] LCD2 Vertical Display Period Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						LCD2 VDP bits 9-8	
15	14	13	12	11	10	9	8
LCD2 Vertical Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 LCD2 Vertical Display Period bits [9:0]

These bits specify the Vertical Display Period for LCD2, in 1 line resolution.

REG[0184h] bits 9-0 = Vertical Display Period in lines - 1

Note

For Parallel and Serial interface panels (see REG[0104h] bits 1-0), the following formula must be valid.

HDP x VDP ≥ 40 pixels.

REG[0188h] LCD2 Serial Interface Setting Register							
Default = 0000_0001h							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
LCD2 Serial Mode Select bits 2-0			LCD2 Serial Data Direction	LCD2 Serial Data Format bits 1-0		LCD2 Serial Clock Phase	LCD2 Serial Clock Polarity
7	6	5	4	3	2	1	0

bits 7-5 LCD2 Serial Mode Select bits [2:0]

These bits select the data width and data type for the serial panel on LCD2 depending on whether a command/parameter access or frame transfer access is being done. The following table summarizes the available modes.

Table 9-31: LCD2 Serial Interface Mode Selection

REG[0188h] bits 7-5	LCD2 Serial Command/Parameter Access Mode	LCD2 Serial Frame Transfer Access Mode
000b	4-pin (8-bit serial)	4-pin (8-bit serial)
001b	3-pin (9-bit serial)	3-pin (9-bit serial)
010b ~ 101b	Reserved	Reserved
100b	Reserved	4-pin (16/18-bit serial) (see Note)
101b	Reserved	3-pin (17/19-bit serial) (see Note)
110b	Reserved	Reserved
111b	3-pin (24-bit serial)	Reserved

Note

1. The data width, 16/17-bit or 18/19-bit, is determined by the LCD2 Serial Data Format bits, REG[0188h] bits 3-2.
2. For LCD2 24-bit serial mode, FPCS2# is active Low by default (which differs from LCD1 24-bit serial mode) and is controlled by the FPCS2# Polarity Select bit, REG[0104h] bit 12.
3. For normal operations of LCD2 frame transfer, the LCD1 serial type must not be 24-bit serial interface (REG[0168h] bits 7-5 ≠ 111b).

bit 4 LCD2 Serial Data Direction

This bit determines the LCD2 serial data direction for command accesses, except for 24-bit serial accesses and accesses using frame transfer mode.
When this bit = 0b, the msb (most significant bit) is sent first.
When this bit = 1b, the lsb (least significant bit) is sent first.

Note

When a 24-bit serial data type is selected (REG[0188h] bits 7-5 = 111b), this bit is not supported and must be set to 0b.

bits 3-2 LCD2 Serial Data Format bits [1:0]

These bits determine the LCD2 serial data format for frame transfers.

Table 9-32: LCD2 Serial Data Format Selection

REG[0188h] bits 3-2	REG[0188h] bit 7	REG[0188h] bit 5	LCD2 Serial Data Format		
			Data Length	Serial Data Type	Data Format
00b	0b	0b	8-bit	4-pin 8-bit	RGB 3:3:2 (1 cycle / pixel)
		1b		3-pin 9-bit	
	1b	0b	16-bit	4-pin 16-bit	RGB 4:4:4 (LSB unused)
		1b		3-pin 17-bit	
01b	0b	0b	8-bit	4-pin 8-bit	RGB 4:4:4 (3 cycles / 2 pixels)
		1b		3-pin 9-bit	
	1b	0b	16-bit	4-pin 16-bit	RGB 4:4:4 (MSB unused)
		1b		3-pin 17-bit	
10b	0b	0b	Reserved		
		1b			
	1b	0b	16-bit	4-pin 16-bit	RGB 5:6:5
		1b		3-pin 17-bit	
11b	0b	0b	Reserved		
		1b			
	1b	0b	18-bit	4-pin 18-bit	RGB 6:6:6
		1b		3-pin 19-bit	

bit 1 LCD2 Serial Clock Phase

This bit specifies the serial clock phase and is used in conjunction with the LCD2 Serial Clock Polarity bit (REG[0188h] bit 0) to configure the serial clock (FPSCK) which is used for the LCD2 serial panel interface. For a summary of the FPSCK phase and polarity settings, see Section Table 9-33:, “LCD2 Serial Clock Polarity and Phase Selection” on page 133.

bit 0 LCD2 Serial Clock Polarity

This bit specifies the serial clock polarity and is used in conjunction with the LCD2 Serial Clock Phase bit (REG[0188h] bit 1) to configure the serial clock (FPSCK) which is used for the LCD2 serial panel interface. For a summary of the FPSCK phase and polarity settings, see Section Table 9-33:, "LCD2 Serial Clock Polarity and Phase Selection" on page 133.

Table 9-33: LCD2 Serial Clock Polarity and Phase Selection

REG[0188h] bit 1	REG[0188h] bit 0	Serial Data Output Changes	Idling Status of Clock
0b	0b	Falling edge of Serial Clock	Low
0b	1b	Rising edge of Serial Clock	High
1b	0b	Rising edge of Serial Clock	Low
1b	1b	Falling edge of Serial Clock	High

Note

For serial interfaces, either REG[0168h] bits 1-0 or REG[0188h] bits 1-0 are used to specify the serial clock phase and serial clock polarity according to the setting of the Command/Parameter Port Select bit (REG[0104h] bit 6) and the Display Output Port Status bits (REG[0604h] bits 15-12). The following table summarizes which register bits are used for each case.

Table 9-34: Serial Interface Clock Phase and Polarity Configuration

Phase/Polarity	Serial Interface	Display Port Status (REG[0604h] bits 15-12)			
		Off (0000b)	LCD1 (0001b	LCD2 (0010b)	Other
LCD1 Serial Clock Phase	LCD1 (REG[0104h] bit 6 = 0b)	REG[0168h] bit 1	REG[0168h] bit 1	REG[0188h] bit 1	REG[0168h] bit 1
LCD1 Serial Clock Polarity		REG[0168h] bit 0	REG[0168h] bit 0	REG[0188h] bit 0	REG[0168h] bit 0
LCD2 Serial Clock Phase	LCD2 (REG[0104h] bit 6 = 1b)	REG[0168h] bit 1	REG[0168h] bit 1	REG[0188h] bit 1	REG[0168h] bit 1
LCD2 Serial Clock Polarity		REG[0168h] bit 0	REG[0168h] bit 0	REG[0188h] bit 0	REG[0168h] bit 0

REG[018Ch] LCD2 Parallel Interface Setting Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
LCD2 FPVS2 Pin Type Select	LCD2 FPVS2 Polarity Select	LCD2 FPVS2 Pin Enable	n/a				LCD2 Parallel Command/Parameter Mode Select
15	14	13	12	11	10	9	8
LCD2 VSYNC Input Enable	LCD2 Parallel Type Select	LCD2 Parallel Command/Parameter Pin bits 1-0		LCD2 Parallel Data Format bits 3-0			
7	6	5	4	3	2	1	0

bit 15 LCD2 FPVS2 Pin Type Select

This bit selects the FPVS2 pin type for parallel panels on LCD2. When a serial interface is selected, this bit must be set to 0b. When an output is selected, the vertical synchronizing signal is output from FPVS2.
When this bit = 0b, FPVS2 is configured as an input. (default)
When this bit = 1b, FPVS2 is configured as an output.

bit 14 LCD2 FPVS2 Polarity Select

This bit is for the LCD2 parallel/serial interface. This bit controls the polarity of FPVS2 both when it is an input vertical sync and an output vertical sync (see REG[018Ch] bit 15).
When this bit = 0b, FPVS2 is active low. (default)
When this bit = 1b, FPVS2 is active high.

bit 13 LCD2 FPVS2 Pin Enable

This bit is for the LCD2 parallel/serial interface. This bit controls the FPVS2 pin.
When this bit = 0b, the FPVS2 pin is disabled (used as GPIOP14).
When this bit = 1b, the FPVS2 pin is enabled.

bit 8 LCD2 Parallel Command/Parameter Mode Select

When the LCD1 and LCD2 panels use separate pins (REG[0104h] bits 1-0 = 10b), this bit selects the method of Command/Parameter forwarding for LCD2.
When this bit = 0b, 8-bit transfer mode is selected. The data written to REG[0108h] bits 7-0 / REG[010Ch] bits 7-0 is output from P2DAT[7:0] in 1 cycle.
When this bit = 1b, 16-bit transfer mode is selected. The data written to REG[0108h] bits 15-0 / REG[010Ch] bits 15-0 is output from P2DAT[7:0] in 2 cycles.

Note

If display mode 2 is selected (REG[0104h] bits 1-0 = 01b), this bit must be set to 0b.

bit 7 LCD2 VSYNC Input Enable

This bit is for the LCD2 parallel/serial interface. This bit allows the transfer of a frame of data synced to an external VSYNC input (FPVS2).
When this bit = 0b, the LCD2 data output is independent of an external VSYNC input.
When this bit = 1b, the LCD2 data output is synchronous with an external VSYNC input.

Note

The FPVS2 signal period must be longer than the time it takes to transfer a frame of data. If the FPVS2 period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next FPVS2 falling edge.

bit 6 LCD2 Parallel Type Select

This bit determines the LCD2 parallel interface type.
When this bit = 0b, the parallel interface is type 80.
When this bit = 1b, the parallel interface is type 68.

bits 5-4 LCD2 Parallel Command/Parameter Pin bits [1:0]

These bits determine which FPDAT[17:0] pins are used for the parallel panel command/parameter. When the LCD2 data pins differ from the LCD1 data pins (REG[0104h] bits 1-0 = 10b), these bits are ignored.

Table 9-35: LCD2 Parallel Command/Parameter Pin Mapping

REG[018Ch] bits 5-4	Command/Parameter Pin Mapping
00b (default)	FPDAT[15:0]
01b	FPDAT[17:10],[8:1]
10b	FPDAT[17:13],[11:1]
11b	Reserved

bits 3-0 LCD2 Parallel Data Format bits [3:0]

These bits determine the LCD2 parallel data format. When the LCD2 data pins differ from the LCD1 data pins (REG[0104h] bits 1-0 = 10b), these bits should be set for an 8-bit bus width.

Table 9-36: LCD2 Parallel Data Format Selection

REG[018Ch] bits 3-0	LCD2 Parallel Data Format	
	Data Bus Width	**Frame Transfer Data Format**
0000b	8-bit	RGB = 3:3:2 (1 cycle / pixel)
0001b		RGB = 4:4:4 (3 cycles / 2 pixels)
0010b	16-bit	RGB = 8:8:8 (3 cycles / 2 pixels)
0011b	8-bit	RGB = 8:8:8 (3 cycles / pixel)
0100b	24-bit	RGB = 8:8:8 (1 cycle / pixel)
0101b	16-bit	RGB = 4:4:4 (1 cycle / pixel)
0110b		RGB = 5:6:5 (1 cycle / pixel)
0111b	18-bit	RGB = 6:6:6 (1 cycle / pixel)
1xxxb	8-bit	RGB = 5:6:5 (2 cycles / pixel)

REG[0190h] LCD2 VSYNC Output Register
Default = 0000_0101h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
LCD2 VSYNC Width bits 7-0							
15	14	13	12	11	10	9	8
LCD2 VSYNC Position bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 LCD2 VSYNC Width bits [7:0]

These bits are only used when FPVS2 (LCD2 VSYNC) is configured as an output, REG[018Ch] bit 15 = 1b. These bits determine the width of VSYNC for LCD2, in PCLKs.

REG[0190h] bits 15-8 = LCD2 VSYNC Width ÷ 2

Note

These bits must not be set to 00h.

bits 7-0 LCD2 VSYNC Position bits [7:0]

These bits are used only when FPVS2 (LCD2 VSYNC) is configured as an output, REG[018Ch] bit 15 = 1b. These bits determine the position of VSYNC for LCD2, in PCLKs.

REG[0190h] bits 7-0 = (LCD2 VSYNC Position - 10) ÷ 2

Note

These bits must not be set to 00h.

9.4.8 TV-Out Interface Configuration Registers

REG[0200h] TV-Out Interface Clock Setting Register
Default = 0000_0020h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a		Reserved			TV-Out Clock Divide Select bits 2-0		
7	6	5	4	3	2	1	0
RGB Output Data Type Select	YUV Output Data Type Select bits 1-0		TV-Out TE Input Enable	Reserved	TV-Out Interface Pins Select	TV-Out Interface Type Select bits 1-0	

bits 13-11 Reserved
The default value for these bits is 000b.

bits 10-8 TV-Out Clock Divide Select bits [2:0]
These bits select the divide ratio for the TV-Out clock. The clock source for the TV-Out clock is selected by the TV-Out Clock Source Select bits, REG[0028h] bits 5-4. For more information on the clock structure, see Section 8, “Clocks” on page 88.

Table 9-37: TV-Out Clock Divide Ratio Selection

REG[0200h] bits 10-8	TV-Out Clock Divide Ratio	REG[0200h] bits 10-8	TV-Out Clock Divide Ratio
000b	1:1	100b	8:1
001b	2:1	101b	10:1
010b	4:1	110b	12:1
011b	6:1	111b	14:1

Note

1. When the TV-Out interface type is configured for parallel interface (REG[0200h] bits 1-0 = 10b), the following formula must be valid.
   TV-Out Clock Frequency < System Clock Frequency ÷ 2.
2. When the TV-Out interface type is configured for parallel interface (REG[0200h] bits 1-0 = 10b), the TV-Out Clock frequency cannot be lower than the SYSCLK frequency ÷ 32.
3. When the TV-Out interface type is configured for HSYNC & FIELD or ITU-R BT656 (REG[0200h] bits 1-0 = 01b or 11b) , the TV-Out clock source must be set to either CLKI or OSCI/OSCO (REG[0028h] bits 5-4 = 00b or 01b). Additionally, 27MHz must be input to CLKI or OSCI/OSCO, and the TV-Out Clock Divide must be set to 2:1 (REG[0200h] bits 10-8 = 001b).

Table 9-38: TV-Out Clock Selection

REG[0200h] bits 1-0	TV-Clock Source	REG[0200h] bits 10-8	TV-Clock Frequency (Internal)	TVCLK pin Frequency	Required System Clock Frequency
01b (HSYNC & FIELD)	CLKI or OSCI (27MHz)	001b	13.5 MHz	27 MHz	≥ 40MHz
10b (Parallel)	CLKI or OSCI or PLL	000b - 111b	Source Clock ÷ TV-Clock Divide Ratio (Note 4)	Note 4	≥ 40MHz
11b (ITU-R BT656)	CLKI or OSCI (27MHz)	001b	13.5 MHz	27 MHz	≥ 40MHz

Note

4. The cycle time for writing 1 byte is 2 x (internal TV-Clock period).

bit 7 RGB Output Data Type Select

These bits are for the parallel TV-Out interface type only (REG[0200h] bits 1-0 = 10b).These bits determine the RGB format of the TV-Out data output.
When this bit = 0b, the TV-Out data output is RGB 5:6:5. (1 pixel / 2 cycles)
When this bit = 1b, the TV-Out data output is RGB 8:8:8. (1 pixel / 3 cycles)

bits 6-5 YUV Output Data Type Select bits [1:0]

These bits specify whether an UV offset is applied to the output data.

Table 9-39: YUV Output Data Type Selection

REG[0200h] bits 6-5	Data Mode	Output Data Range
00b	YUV Offset	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255
01b (default)	YCbCr Offset	16 ≤ Y ≤ 235 16 ≤ U ≤ 240 16 ≤ V ≤ 240
10b	YUV	0 ≤ Y ≤ 255 -128 ≤ U ≤ 127 -128 ≤ V ≤ 127
11b	YCbCr	16 ≤ Y ≤ 235 -112 ≤ U ≤ 112 -112 ≤ V ≤ 112

Note

When the TV-Out interface type is configured for ITU-R BT656 interface (REG[0200h] bits 1-0 = 11b), these bits must be set to 01b. (YCbCr Offset)

bit 4 TV-Out TE Input Enable

These bits are for the parallel TV-Out interface type only (REG[0200h] bits 1-0 = 10b). This bit allows the transfer of a frame of data synced to an external TE input (TVTE). When this bit = 0b, the TV-Out data output is independent of an external TE input. When this bit = 1b, the TV-Out data output is synchronous with an external TE input.

Note

1. The TE signal period must be longer than the time it takes to transfer a frame of data. If the TE period is shorter than the time it takes to transfer a complete frame to the panel, the current frame transfer is interrupted at the next TE falling edge.
2. TV-Out command read/write cycles are not supported in TE input mode. Therefore, this bit must be set to 0b before initiating TV-Out command read/write cycles using REG[0228h].

bit 3 Reserved

The default value for this bit is 0b.

bit 2 TV-Out Interface Pins Select

This bit selects which pins are used for the TV-Out interface. Note that the pins used varies according to the TV-Out Interface Type that is selected (see REG[0200h] bits 1-0).

Table 9-40: TV-Output Interface Pin Usage Summary

REG[0200h] bits 1-0	REG[0200h] bit 2	TV-Out Interface Pins
01b	0b	use GPIOP0 to GPIOP10
	1b	use GPIOH2 to GPIOH12
10b	0b	use GPIOP0 to GPIOP12
	1b	use GPIOH0 to GPIOH12
11b	0b	use GPIOP0 to GPIOP7, GPIOP10
	1b	use GPIOH2 to GPIOH9, GPIOH12

Note

This bit should be configured such that the TV-Out interface does not use the same pins as the LCD2 parallel interface (see REG[0104h] bit 2). For a summary of the possible LCD and TV-Out interface modes, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.

bits 1-0 TV-Out Interface Type Select bits [1:0]

These bits determine the TV-Out interface type. When these bits are set to 00b, TV-Out Interface is not used and the pins can be used as GPIO pins.

Table 9-41: TV-Out Interface Selection

REG[0200h] bits 1-0	TV-Out Interface Type	Output Format
00b	TV-Out Interface is not used	—
01b	HSYNC & FIELD Interface	YcbCr 4:2:2 / YUV 4:2:2
10b	Parallel Interface (MPU Interface)	RGB 5:6:5 / RGB 8:8:8
11b	ITU-R BT656 Interface	YCbCr 4:2:2

Note

When the TV-out interface type is set for HSYNC & FIELD (bits = 01b) or ITU-R BT656 (bits = 11b), the interface must be set to “TV-Out interface is not used” (bits = 00b) before switching to another TV-Out interface type.

REG[0204h] TV-Out Horizontal Total Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						TV-Out Horizontal Total bits 9-8	
7	6	5	4	3	2	1	0
TV-Out Horizontal Total bits 7-0							

bits 9-0 TV-Out Horizontal Total bits [9:0]

These bits are for the HSYNC & FIELD and ITU-R BT656 TV-Out interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the Horizontal Total Period for TV-Out, in 2 TV-CLOCK resolution.

REG[0204h] bits 9-0 = (Horizontal Total in TV-CLOCKS ÷ 2) - 1

Note

The following formulae must be valid.

HT ≥ HDP + HNDP

10 < (REG[0204h] bits 9-0) <1023

REG[0208h] TV-Out Horizontal Display Period Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							TV-Out HDP bit 8
15	14	13	12	11	10	9	8
TV-Out Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 TV-Out Horizontal Display Period bits [8:0]

For the HSYNC & FIELD and ITU-R BT656 TV-Out interfaces (REG[0200h] bits 1-0 = 01b or 11b), these bits specify the Horizontal Display Period for TV-Out, in 4 TV-CLOCK resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for a sufficient Horizontal Non-Display Period.

REG[0208h] bits 8-0 = (Horizontal Display Period in TV-CLOCKs ÷ 4) - 1

For the Parallel TV-Out interface (REG[0200h] bits 1-0 = 10b), these bits specify the Horizontal Display Period for TV-Out, in 2 pixel resolution.

REG[0208h] bits 8-0 = (Horizontal Display Period in pixels ÷ 2) - 1

Note

1. These bits must be programmed such that the following formula is valid.
   REG[0208h] bits 8-0 > 0
2. For the Parallel TV-Out interface (REG[0200h] bits 1-0 = 10b), the following formula must be valid.
   HDP x VDP ≥ 128 pixels

REG[020Ch] TV-Out Horizontal Display Period Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						TV-Out Horizontal Display Period Start Position bits 9-8	
7	6	5	4	3	2	1	0
TV-Out Horizontal Display Period Start Position bits 7-0							

bits 9-0 TV-Out Horizontal Display Period Start Position bits [9:0]
These bits are for the HSYNC & FIELD and ITU-R BT656 TV-Out interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the Horizontal Display Period Start Position for TV-Out , in 2 TV-CLOCK resolution.

REG[020Ch] bits 9-0 = (Horizontal Display Period Start Position in CLOCKs - 18) ÷ 2

Note
These bits must be programmed such that the following formula is valid.

REG[020Ch] bits 9-0 < 3F2h

REG[0210h] TV-Out Horizontal Pulse (HSYNC) Width Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a	TV-Out Horizontal Pulse (HSYNC) Width bits 6-0						

bits 6-0 TV-Out Horizontal Pulse (HSYNC) Width bits [6:0]
These bits are for the HSYNC & FIELD TV-Out interface only (REG[0200h] bits 1-0 = 01b). These bits specify the width of the horizontal sync signal for TV-Out, in 2 TV-CLOCK resolution.

REG[0210h] bits 6-0 = (HSYNC width in CLOCKs ÷ 2) - 1

REG[0214h] is Reserved

This register is Reserved and should not be written.

REG[0218h] TV-Out Vertical Total Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						TV-Out Vertical Total bits 9-8	
7	6	5	4	3	2	1	0
TV-Out Vertical Total bits 7-0							

bits 9-0 TV-Out Vertical Total bits [9:0]

These bits are for the HSYNC & FIELD and ITU-R BT656 TV-Out interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the Vertical Total period for TV-Out, in 1 line resolution. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period.

REG[00218h] bits 9-0 = Vertical Total in lines - 1

Note

These bits must be programmed such that the following formula is valid.

REG[0218h] bits 9-0 < 3FFh

REG[021Ch] TV-Out Vertical Display Period Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						TV-Out Vertical Display Period bits 9-8	
7	6	5	4	3	2	1	0
TV-Out Vertical Display Period bits 7-0							

bits 9-0 Vertical Display Period bits [9:0]

These bits specify the Vertical Display period for TV-Out , in 1 line resolution. The Vertical Display Period must be less than the Vertical Total to allow for a sufficient Vertical Non-Display Period.

REG[021Ch] bits 9-0 = Vertical Display Period in lines - 1

Note

For the Parallel TV-Out interface (REG[0200h] bits 1-0 = 10b), the following formula must be valid.

HDP x VDP ≥ 128 pixels

REG[0220h] TV-Out Vertical Display Period Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						TV-Out Vertical Display Period Start Position bits 9-8	
7	6	5	4	3	2	1	0
TV-Out Vertical Display Period Start Position bits 7-0							

bits 9-0 TV-Out Vertical Display Period Start Position bits [9:0]

These bits are for the HSYNC & FIELD and ITU-R BT656 interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the Vertical Display Period Start Position for TV-Out , in 1 line resolution.

REG[0220h] bits 9-0 = Vertical Display Start Position - 2

Note

These bits must be programmed such that the following formula is valid.

REG[0220h] bits 9-0 < 3FFh

REG[0224h] TV-Out FIELD Toggle Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						TV-Out FIELD Toggle Position bits 9-8	
7	6	5	4	3	2	1	0
TV-Out FIELD Toggle Position bits 7-0							

bits 9-0 TV-Out FIELD Toggle Position bits [9:0]

These bits are for the HSYNC & FIELD and ITU-R BT656 TV-Out interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the position of the TVFIELD signal toggle position for TV-Out, in 1 line resolution.

REG[0228h] TV-Out Data Port Register (AID)
Default = 0000_0000h: Address auto increment disable — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a					TV-Out TVDC Level Select	TV-Out Command R/W Cycle	TV-Out Command Access Start
15	14	13	12	11	10	9	8
TV-Out Command Port bits 7-0							
7	6	5	4	3	2	1	0

bit 10 TV-Out TVDC Level Select

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit selects the state of the TVDC pin when a write is done with the TV-Out interface.
When this bit = 0b, the TVDC pin is Low.
When this bit = 1b, the TVDC pin is High.

bit 9 TV-Out Command Read/Write Cycle

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit determines whether a command read or write operation takes place.
When this bit = 0b, a write operation takes place. (default)
When this bit = 1b, a read operation takes place.

bit 8 TV-Out Command Access Start

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit is available when TV-Out is selected as a Display Output Port (REG[0604h] bits 15-12 = 0100b or 1011b). This bit starts an 8-bit data access to/from the parallel TV-Out interface device according to the setting of the TV-Out Command Read/Write Cycle bit (see REG[0228h] bit 9).

For write operations (REG[0228h] bit 9 = 0b), the data can be written to the TV-Out Command Port (see REG[0228h] bits 7-0) simultaneous to the writing of this bit. This bit is automatically reset to 0b when the write access completes. Once this bit returns a 0b, the next write operation can be started.

For read operations (REG[0228h] bit 9 = 1b), write a 1b to this bit. The data can be read from the TV-Out Command Port (see REG[0228h] bits 7-0) once this bit returns a 0b.

Note
TV-Out TE input must be disabled (REG[0200h] bit 4 = 0b) before a TV-Out command access is started.

bits 7-0 TV-Out Command Port bits [7:0]

These bits are for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). These bits are the Data Port for the parallel TV-Out interface.

For write operations (REG[0228h] bit 9 = 0b), the TV-Out Command Access Start bit can be set to 1b (see REG[0228h] bit 8) simultaneous to the writing of these bits.

For read operations (REG[0228h] bit 9 = 1b), the valid data can be read once the TV-Out Command Access Start bit reads a 0b (REG[0228h] bit 8 = 0b).

REG[022Ch] TV-Out Interface Frame Transfer Register (AID)

Default = 0000_0000h: Address auto increment disable — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			TV-Out Interface Status (RO)	n/a	TV-Out Auto Frame Transfer Trigger Select	TV-Out Interface Auto Frame Transfer Enable	TV-Out Interface Frame Transfer Trigger
7	6	5	4	3	2	1	0

bit 4 TV-Out Interface Status (Read Only)

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit indicates the status of the parallel TV-Out interface. This bit should be read to confirm that the parallel TV-Out interface is not busy before transmitting data.
When this bit = 0b, the parallel TV-Out interface is not busy (or ready).
When this bit = 1b, the parallel TV-Out interface is busy.

bit 2 TV-Out Interface Auto Frame Transfer Trigger Select

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit selects the trigger method used when Auto Frame Transfers are enabled, REG[022Ch] bit 1 = 1b.
When this bit = 0b, auto frame transfers are synchronized with the Main Memory Write Path write end.
When this bit = 1b, auto frame transfers are synchronized with the Sub Memory Write Path write end.

bit 1 TV-Out Interface Auto Frame Transfer Enable

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit controls automatic frame transfers of one frame of display memory to the TV-Out interface. Frame transfers are triggered and synchronized with the DRAM write end (see REG[022Ch] bit 2).
When this bit = 0b, auto frame transfer is disabled.
When this bit = 1b, auto frame transfer is enabled.

When this bit = 1b, the TV-Out Interface Status bit (REG[022Ch] bit 4) is always busy. When busy, command/parameter and frame transfers cannot be sent manually. This bit should be disabled before Host/Video input is disabled.

bit 0 TV-Out Interface Frame Transfer Trigger

This bit is for the Parallel TV-Out interface only (REG[0200h] bits 1-0 = 10b). This bit is the trigger to transfer 1 frame of data to the TV-Out interface.

When this bit is set to 1b and the TV-Out interface is busy (REG[022Ch] bit 4 = 0b), the frame transfer request is ignored. Once the TV-Out interface is no longer busy, this bit is cleared without transferring any data.

When this bit is set to 1b and the TV-Out interface status is not busy (REG[022Ch] bit 4 = 0b), 1 frame of data is transferred to the TV-Out interface. When the data transfer is finished, this bit is cleared automatically.

Note

When auto frame transfer is enabled (REG[022Ch] bit 1 = 1b), this bit indicates the status of the auto frame transfer.

When this bit = 0b, the auto frame transfer is inactive.

When this bit = 1b, the auto frame transfer is active.

REG[0230h] TV-Out Blank Data Register

Default = 0000_8010h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
TV-Out Blank CbCr Data bits 7-0							
15	14	13	12	11	10	9	8
TV-Out Blank Y Data bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 TV-Out Blank CbCr Data bits [7:0]

These bits are for the HSYNC & FIELD and ITU-R BT656 interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the CbCr data during blank period.

bits 7-0 TV-Out Blank Y Data bits [7:0]

These bits are for the HSYNC & FIELD and ITU-R BT656 interfaces only (REG[0200h] bits 1-0 = 01b or 11b). These bits specify the Y data during blank period.

9.4.9 GPIO Registers

Note
The GPIO registers are asynchronous.

REG[0300h] GPIOP Configuration Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Config	GPIOP13 Config	GPIOP12 Config	GPIOP11 Config	GPIOP10 Config	GPIOP9 Config	GPIOP8 Config
15	14	13	12	11	10	9	8
GPIOP7 Config	GPIOP6 Config	GPIOP5 Config	GPIOP4 Config	GPIOP3 Config	GPIOP2 Config	GPIOP1 Config	GPIOP0 Config
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Configuration
These bits configure each individual GPIOP pin between an input or an output.
When this bit = 0b, the corresponding GPIOP pin is configured as an input pin. (default)
When this bit = 1b, the corresponding GPIOP pin is configured as an output pin.

REG[0304h] GPIOH Configuration Register 0
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Config	GPIOH14 Config	GPIOH13 Config	GPIOH12 Config	GPIOH11 Config	GPIOH10 Config	GPIOH9 Config	GPIOH8 Config
15	14	13	12	11	10	9	8
GPIOH7 Config	GPIOH6 Config	GPIOH5 Config	GPIOH4 Config	GPIOH3 Config	GPIOH2 Config	GPIOH1 Config	GPIOH0 Config
7	6	5	4	3	2	1	0

REG[0308h] GPIOH Configuration Register 1
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Config	GPIOH22 Config	GPIOH21 Config	GPIOH20 Config	GPIOH19 Config	GPIOH18 Config	GPIOH17 Config	GPIOH16 Config
7	6	5	4	3	2	1	0

REG[0308h] bits 7-0
REG[0304h] bits 15-0 GPIOH [23:0] Configuration
These bits configure each individual GPIOH pin between an input or an output.
When this bit = 0b, the corresponding GPIOH pin is configured as an input pin. (default)
When this bit = 1b, the corresponding GPIOH pin is configured as an output pin.

REG[030Ch] GPIOP Input Enable Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Input Enable	GPIOP13 Input Enable	GPIOP12 Input Enable	GPIOP11 Input Enable	GPIOP10 Input Enable	GPIOP9 Input Enable	GPIOP8 Input Enable
15	14	13	12	11	10	9	8
GPIOP7 Input Enable	GPIOP6 Input Enable	GPIOP5 Input Enable	GPIOP4 Input Enable	GPIOP3 Input Enable	GPIOP2 Input Enable	GPIOP1 Input Enable	GPIOP0 Input Enable
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Input Enable

Theses bits enable the input function of each individual GPIOP pin. They must be changed to 1b after power-on/reset to enable the input function of the corresponding GPIOP pin.

When this bit = 0b, the input function for the corresponding GPIOP pin is disabled. (default)

When this bit = 1b, the input function for the corresponding GPIOP pin is enabled.

REG[0310h] GPIOH Input Enable Register 0
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Input Enable	GPIOH14 Input Enable	GPIOH13 Input Enable	GPIOH12 Input Enable	GPIOH11 Input Enable	GPIOH10 Input Enable	GPIOH9 Input Enable	GPIOH8 Input Enable
15	14	13	12	11	10	9	8
GPIOH7 Input Enable	GPIOH6 Input Enable	GPIOH5 Input Enable	GPIOH4 Input Enable	GPIOH3 Input Enable	GPIOH2 Input Enable	GPIOH1 Input Enable	GPIOH0 Input Enable
7	6	5	4	3	2	1	0

REG[0314h] GPIOH Input Enable Register 1
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Input Enable	GPIOH22 Input Enable	GPIOH21 Input Enable	GPIOH20 Input Enable	GPIOH19 Input Enable	GPIOH18 Input Enable	GPIOH17 Input Enable	GPIOH16 Input Enable
7	6	5	4	3	2	1	0

REG[0314h] bits 7-0
REG[0310h] bits 15-0 GPIOH[23:0] Input Enable

Theses bits enable the input function of each individual GPIOH pin. They must be changed to 1b after power-on/reset to enable the input function of the corresponding GPIOH pin.

When this bit = 0b, the input function for the corresponding GPIOH pin is disabled. (default)

When this bit = 1b, the input function for the corresponding GPIOH pin is enabled.

REG[0318h] GPIOP Pull-Up/Down Control Register
Default = 0000_7FFFh — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Pull-down Control	GPIOP13 Pull-down Control	GPIOP12 Pull-down Control	GPIOP11 Pull-up Control	GPIOP10 Pull-down Control	GPIOP9 Pull-down Control	GPIOP8 Pull-down Control
15	14	13	12	11	10	9	8
GPIOP7 Pull-down Control	GPIOP6 Pull-down Control	GPIOP5 Pull-down Control	GPIOP4 Pull-down Control	GPIOP3 Pull-down Control	GPIOP2 Pull-down Control	GPIOP1 Pull-down Control	GPIOP0 Pull-down Control
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Pull-up/down Control

All GPIOP pins have internal pull-up/down resistors. These bits control the state of the pull-up/down resistor for each GPIOP pin.

When this bit = 0b, the pull-up/down resistor for the associated GPIOP pin is inactive.

When this bit = 1b, the pull-up/down resistor for the associated GPIOP pin is active regardless of the pin direction (input/output).

REG[031Ch] GPIOH Pull-Up/Down Control Register 0
Default = 0000_FFFFh — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Pull-down Control	GPIOH14 Pull-down Control	GPIOH13 Pull-down Control	GPIOH12 Pull-down Control	GPIOH11 Pull-down Control	GPIOH10 Pull-down Control	GPIOH9 Pull-down Control	GPIOH8 Pull-down Control
15	14	13	12	11	10	9	8
GPIOH7 Pull-down Control	GPIOH6 Pull-down Control	GPIOH5 Pull-down Control	GPIOH4 Pull-down Control	GPIOH3 Pull-down Control	GPIOH2 Pull-down Control	GPIOH1 Pull-up Control	GPIOH0 Pull-down Control
7	6	5	4	3	2	1	0

REG[0320h] GPIOH Pull-Up/Down Control Register 1
Default = 0000_00FFh — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Pull-up Control	GPIOH22 Pull-down Control	GPIOH21 Pull-down Control	GPIOH20 Pull-down Control	GPIOH19 Pull-down Control	GPIOH18 Pull-down Control	GPIOH17 Pull-down Control	GPIOH16 Pull-down Control
7	6	5	4	3	2	1	0

REG[0320h] bits 7-0
REG[031Ch] bits 15-0 GPIOH[23:0] Pull-Up/down Control

All GPIOH pins have internal pull-up/down resistors. These bits control the state of the pull-up/down resistor for each GPIOH pin.

When this bit = 0b, the pull-up/down resistor for the associated GPIOH pin is inactive.

When this bit = 1b, the pull-up/down resistor for the associated GPIOH pin is active regardless of the pin direction (input/output).

REG[0324h] GPIOP Status Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Status	GPIOP13 Status	GPIOP12 Status	GPIOP11 Status	GPIOP10 Status	GPIOP9 Status	GPIOP8 Status
15	14	13	12	11	10	9	8
GPIOP7 Status	GPIOP6 Status	GPIOP5 Status	GPIOP4 Status	GPIOP3 Status	GPIOP2 Status	GPIOP1 Status	GPIOP0 Status
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Status

When GPIOPx is configured as an output (see REG[0300h]), writing a 1b to these bits drives GPIOPx high and writing a 0b to these bits drives GPIOPx low.

When GPIOPx is configured as an input (see REG[0300h]), a read from these bits returns the status of GPIOPx.

REG[0328h] GPIOH Status Register 0
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Status	GPIOH14 Status	GPIOH13 Status	GPIOH12 Status	GPIOH11 Status	GPIOH10 Status	GPIOH9 Status	GPIOH8 Status
15	14	13	12	11	10	9	8
GPIOH7 Status	GPIOH6 Status	GPIOH5 Status	GPIOH4 Status	GPIOH3 Status	GPIOH2 Status	GPIOH1 Status	GPIOH0 Status
7	6	5	4	3	2	1	0

REG[032Ch] GPIOH Status Register 1
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Status	GPIOH22 Status	GPIOH21 Status	GPIOH20 Status	GPIOH19 Status	GPIOH18 Status	GPIOH17 Status	GPIOH16 Status
7	6	5	4	3	2	1	0

REG[032Ch] bits 7-0
REG[0328h] bits 15-0 GPIOH[23:0] Status

When GPIOHx is configured as an output (see REG[0304h] ~ REG[0308h]), writing a 1b to these bits drives GPIOHx high and writing a 0b to these bits drives GPIOHx low.

When GPIOHx is configured as an input (see REG[0304h] ~ REG[0308h]), a read from these bits returns the status of GPIOHx.

REG[0330h] GPIOP Positive Edge Interrupt Trigger Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Positive Edge Trigger	GPIOP13 Positive Edge Trigger	GPIOP12 Positive Edge Trigger	GPIOP11 Positive Edge Trigger	GPIOP10 Positive Edge Trigger	GPIOP9 Positive Edge Trigger	GPIOP8 Positive Edge Trigger
15	14	13	12	11	10	9	8
GPIOP7 Positive Edge Trigger	GPIOP6 Positive Edge Trigger	GPIOP5 Positive Edge Trigger	GPIOP4 Positive Edge Trigger	GPIOP3 Positive Edge Trigger	GPIOP2 Positive Edge Trigger	GPIOP1 Positive Edge Trigger	GPIOP0 Positive Edge Trigger
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Positive Edge Trigger

These bits determine whether the corresponding GPIOP interrupt (see REG[0348h]) is triggered on the positive edge (when the GPIOPx pin changes from 0 to 1).

When this bit = 0b, the corresponding GPIOP interrupt is not triggered on the positive edge.

When this bit = 1b, the corresponding GPIOP interrupt is triggered on the positive edge.

REG[0334h] GPIOH Positive Edge Interrupt Trigger Register 0
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Positive Edge Trigger	GPIOH14 Positive Edge Trigger	GPIOH13 Positive Edge Trigger	GPIOH12 Positive Edge Trigger	GPIOH11 Positive Edge Trigger	GPIOH10 Positive Edge Trigger	GPIOH9 Positive Edge Trigger	GPIOH8 Positive Edge Trigger
15	14	13	12	11	10	9	8
GPIOH7 Positive Edge Trigger	GPIOH6 Positive Edge Trigger	GPIOH5 Positive Edge Trigger	GPIOH4 Positive Edge Trigger	GPIOH3 Positive Edge Trigger	GPIOH2 Positive Edge Trigger	GPIOH1 Positive Edge Trigger	GPIOH0 Positive Edge Trigger
7	6	5	4	3	2	1	0

REG[0338h] GPIOH Positive Edge Interrupt Trigger Register 1
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Positive Edge Trigger	GPIOH22 Positive Edge Trigger	GPIOH21 Positive Edge Trigger	GPIOH20 Positive Edge Trigger	GPIOH19 Positive Edge Trigger	GPIOH18 Positive Edge Trigger	GPIOH17 Positive Edge Trigger	GPIOH16 Positive Edge Trigger
7	6	5	4	3	2	1	0

REG[0338h] bits 7-0
REG[0334h] bits 15-0 GPIOH[23:0] Positive Edge Trigger

These bits determine whether the corresponding GPIOH interrupt (see REG[034Ch] ~ REG[0350h]) is triggered on the positive edge (when the GPIOHx pin changes from 0 to 1).

When this bit = 0b, the corresponding GPIOH interrupt is not triggered on the positive edge.

When this bit = 1b, the corresponding GPIOH interrupt is triggered on the positive edge.

REG[033Ch] GPIOP Negative Edge Interrupt Trigger Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Negative Edge Trigger	GPIOP13 Negative Edge Trigger	GPIOP12 Negative Edge Trigger	GPIOP11 Negative Edge Trigger	GPIOP10 Negative Edge Trigger	GPIOP9 Negative Edge Trigger	GPIOP8 Negative Edge Trigger
15	14	13	12	11	10	9	8
GPIOP7 Negative Edge Trigger	GPIOP6 Negative Edge Trigger	GPIOP5 Negative Edge Trigger	GPIOP4 Negative Edge Trigger	GPIOP3 Negative Edge Trigger	GPIOP2 Negative Edge Trigger	GPIOP1 Negative Edge Trigger	GPIOP0 Negative Edge Trigger
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Negative Edge Trigger

These bits determine whether the corresponding GPIOP interrupt (see REG[0348h]) is triggered on the negative edge (when the GPIOPx pin changes from 1 to 0).

When this bit = 0b, the corresponding GPIOP interrupt is not triggered on the negative edge.

When this bit = 1b, the corresponding GPIOP interrupt is triggered on the negative edge.

REG[0340h] GPIOH Negative Edge Interrupt Trigger Register 0
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Negative Edge Trigger	GPIOH14 Negative Edge Trigger	GPIOH13 Negative Edge Trigger	GPIOH12 Negative Edge Trigger	GPIOH11 Negative Edge Trigger	GPIOH10 Negative Edge Trigger	GPIOH9 Negative Edge Trigger	GPIOH8 Negative Edge Trigger
15	14	13	12	11	10	9	8
GPIOH7 Negative Edge Trigger	GPIOH6 Negative Edge Trigger	GPIOH5 Negative Edge Trigger	GPIOH4 Negative Edge Trigger	GPIOH3 Negative Edge Trigger	GPIOH2 Negative Edge Trigger	GPIOH1 Negative Edge Trigger	GPIOH0 Negative Edge Trigger
7	6	5	4	3	2	1	0

REG[0344h] GPIOH Negative Edge Interrupt Trigger Register 1
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Negative Edge Trigger	GPIOH22 Negative Edge Trigger	GPIOH21 Negative Edge Trigger	GPIOH20 Negative Edge Trigger	GPIOH19 Negative Edge Trigger	GPIOH18 Negative Edge Trigger	GPIOH17 Negative Edge Trigger	GPIOH16 Negative Edge Trigger
7	6	5	4	3	2	1	0

REG[0344h] bits 7-0

REG[0340h] bits 15-0 GPIOH[23:0] Negative Edge Trigger

These bits determine whether the corresponding GPIOH interrupt (see REG[034Ch] ~ REG[0350h]) is triggered on the negative edge (when the GPIOHx pin changes from 1 to 0).

When this bit = 0b, the corresponding GPIOH interrupt is not triggered on the negative edge.

When this bit = 1b, the corresponding GPIOH interrupt is triggered on the negative edge.

REG[0348h] GPIOP Interrupt Status Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	GPIOP14 Interrupt Status	GPIOP13 Interrupt Status	GPIOP12 Interrupt Status	GPIOP11 Interrupt Status	GPIOP10 Interrupt Status	GPIOP9 Interrupt Status	GPIOP8 Interrupt Status
15	14	13	12	11	10	9	8
GPIOP7 Interrupt Status	GPIOP6 Interrupt Status	GPIOP5 Interrupt Status	GPIOP4 Interrupt Status	GPIOP3 Interrupt Status	GPIOP2 Interrupt Status	GPIOP1 Interrupt Status	GPIOP0 Interrupt Status
7	6	5	4	3	2	1	0

bits 14-0 GPIOP[14:0] Interrupt Status
These bits indicate the status of the corresponding GPIOPx interrupt.
When this bit = 0b, a GPIOPx interrupt has not occurred.
When this bit = 1b, a GPIOPx interrupt has occurred.

To clear a GPIOPx Interrupt Status bit, write a 1b then a 0b to the bit.

REG[034Ch] GPIOH Interrupt Status Register 0
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIOH15 Interrupt Status	GPIOH14 Interrupt Status	GPIOH13 Interrupt Status	GPIOH12 Interrupt Status	GPIOH11 Interrupt Status	GPIOH10 Interrupt Status	GPIOH9 Interrupt Status	GPIOH8 Interrupt Status
15	14	13	12	11	10	9	8
GPIOH7 Interrupt Status	GPIOH6 Interrupt Status	GPIOH5 Interrupt Status	GPIOH4 Interrupt Status	GPIOH3 Interrupt Status	GPIOH2 Interrupt Status	GPIOH1 Interrupt Status	GPIOH0 Interrupt Status
7	6	5	4	3	2	1	0

REG[0350h] GPIOH Interrupt Status Register 1
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
GPIOH23 Interrupt Status	GPIOH22 Interrupt Status	GPIOH21 Interrupt Status	GPIOH20 Interrupt Status	GPIOH19 Interrupt Status	GPIOH18 Interrupt Status	GPIOH17 Interrupt Status	GPIOH16 Interrupt Status
7	6	5	4	3	2	1	0

REG[0350h] bits 7-0
REG[034Ch] bits 15-0 GPIOH[23:0] Interrupt Status
These bits indicate the status of the corresponding GPIOHx interrupt.
When this bit = 0b, a GPIOHx interrupt has not occurred.
When this bit = 1b, a GPIOHx interrupt has occurred.

To clear a GPIOHx Interrupt Status bit, write a 1b then a 0b to the bit.

9.4.10 Host Interface Registers

REG[0400h] Host Interface Configuration Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
TE Output Pin Enable	Reserved	n/a					YUV Data Type Select
15	14	13	12	11	10	9	8
n/a	Indirect Interface Data Format Select bits 2-0			n/a	Host Interface Data Type Select bits 2-0		
7	6	5	4	3	2	1	0

bit 15 TE Output Pin Enable
This bit determines whether the state of TE is output on the TE pin.
When this bit = 0b, the TE output pin is disabled.
When this bit = 1b, the TE output pin is enabled.

bit 14 Reserved
The default value for this bit is 0b.

bit 8 YUV Data Type Select
This bit is for the Indirect interface and has no effect on the I2C interface. This bit is used for YUV data only (REG[0400h] bits 2-0) and specifies whether an UV offset is applied to the incoming data.

Table 9-42: YUV Data Type Selection

REG[0400h] bits 8	Data Type	Input Data Range	Output Data Range
0b (default)	YUV Offset	$0 \le Y \le 255$ $0 \le U \le 255$ $0 \le V \le 255$	$0 \le Y \le 255$ $0 \le U \le 255$ $0 \le V \le 255$
	YcbCr Offset	$16 \le Y \le 235$ $16 \le U \le 240$ $16 \le V \le 240$	$16 \le Y \le 235$ $16 \le U \le 240$ $16 \le V \le 240$
1b	YUV	$0 \le Y \le 255$ $-128 \le U \le 127$ $-128 \le V \le 127$	$0 \le Y \le 255$ $0 \le U \le 255$ $0 \le V \le 255$
	YCbCr	$16 \le Y \le 235$ $-112 \le U \le 112$ $-112 \le V \le 112$	$16 \le Y \le 235$ $16 \le U \le 240$ $16 \le V \le 240$

bits 6-4 Indirect Interface Data Format Select bits [2:0]

These bits are for the Indirect interface and have no effect for the I2C interface. Some Host input data formats support different arrangements of the color components. These bits determine which format (1-5) is selected for the Host input data format as configured by REG[0400h] bits 2-0.

The following table summarizes which variations are available for each data format. For details on the data formats, see Section 14.5, "Host Interface Input Format" on page 362.

Table 9-43: Indirect Interface Data Format Selection

REG[0400h] bits 6-4	Format	Data Format				
		RGB 8:8:8	RGB 6:6:6	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
000b	Format 1	Yes	Yes	Yes	Yes	Yes
001b	Format 2	Yes	Yes	No	Yes	Yes
010b	Format 3	Yes	Yes	No	No	No
011b	Format 4	Yes	Yes	No	No	No
100b	Format 5	No	Yes	No	No	No
101b-111b	Reserved					

bits 2-0 Host Interface Data Type Select bits [2:0]

These bits are for the Indirect interface and have no effect for the I2C interface. These bits select the data format for Host interface input. Each format support from 1 to 5 variations in how the color components are arranged (see REG[0400h] bits 6-4).

The following table summarizes which data formats can be selected for each interface type or function. For details on the data formats, see Section 14.5, "Host Interface Input Format" on page 362.

Table 9-44: Host Interface Data Type Selection

REG[0400h] bits 2-0	Data Type	Indirect Interface
000b	RGB 5:6:5	Yes
001b	RGB 6:6:6	Yes
010b	RGB 8:8:8	Yes
011b	Reserved	
100b	YUV 4:2:2	Yes
101b	Reserved	
110b	YUV 4:2:0	Yes
111b	Reserved	

Note

When the Main Memory Write Path is used as the host interface write path (REG[0500h] bit 0 = 0b), the Main Memory Write Path must be reset (REG[0504h] bit 15 = 1b) after changing this bit.

When the Sub Memory Write Path is used as the host interface write path (REG[0500h] bit 0 = 1b), the Sub Memory Write Path must be reset (REG[0580h] bit 15 = 1b) after changing this bit.

REG[0404h] TE Configuration Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
TE Output Rate bits 3-0				TE Source Select bits 1-0		TE Delay Control bits 9-8	
15	14	13	12	11	10	9	8
TE Delay Control bits 7-0							
7	6	5	4	3	2	1	0

bits 15-12 TE Output Rate bits [3:0]

These bits are used when REG[0404h] bits 11-10 = 00b or 10b to control the TE output rate. For the LCD Interface, the TE signal wave is the same as VSYNC for the LCD Interface. For the TV-Out Interface, the TE signal wave is a 1 line wide pulse.

Table 9-45: TE Output Rate Selection

REG[0404h] bits 15-12	TE Frame Rate	
	LCD Interface REG[0404h] bits 11-10 = 00b	TV-Out Interface REG[0404h] bits 11-10 = 10b (HSYNC & FIELD or ITU-R BT656)
0000b	Stop	Stop
0001b	1 TE is output for every 1 frame	Reserved
0010b	1 TE is output for every 2 frame	1 TE is output for every odd field
0011b	1 TE is output for every 3 frame	Reserved
0100b	1 TE is output for every 4 frame	1 TE is output for every 2 odd field
0101b	1 TE is output for every 5 frame	Reserved
0110b	1 TE is output for every 6 frame	1 TE is output for every 3 odd field
0111b	1 TE is output for every 7 frame	Reserved
1000b	1 TE is output for every 8 frame	1 TE is output for every 4 odd field
1001b	1 TE is output for every 9 frame	Reserved
1010b	1 TE is output for every 10 frame	1 TE is output for every 5 odd field
1011b	1 TE is output for every 11 frame	Reserved
1100b	1 TE is output for every 12 frame	1 TE is output for every 6 odd field
1101b	1 TE is output for every 13 frame	Reserved
1110b	1 TE is output for every 14 frame	1 TE is output for every 7 odd field
1111b	1 TE is output for every 15 frame	Reserved

Note

When the TE output pin is enabled (REG[0400h] bit 15 = 1b), the TE signal is output from the TE pin.

bits 11-10 TE Source Select bits [1:0]
These bits select the source of the TE signal.

Table 9-46: TE Source Signal Selection

REG[0404h] bits 11-10	TE Source Signal
00b	VSYNC (LCD1 RGB Interface)
01b	FPVS2 Input
10b	VSYNC (TV-Out HSYNC & FIELD or ITU-R BT656 Type Interfaces) (see Note 1)
11b	TVTE Input (see Note 2)

Note

1. When the TE source is TV-Out HSYNC & FIELD or ITU-R BT656, the TE pin output is active Low when enabled.
2. TVTE input has an effect regardless of the setting of the TV-Out TE Input Enable bit, REG[0200h] bit 4.

bits 9-0 TE Delay Control bits [9:0]
These bits are used when REG[0404h] bits 11-10 = 00b or 10b to specify the delay, in number of lines, from VSYNC for the LCD Interface or TV-Out Interface.

Table 9-47: TE Delay Selection

REG[0404h] bits 9-0	TE Delay
000h	No Delay
001h	1 Line
002h	2 Lines
003h	3 Lines
...	...

Note

When the LCD1 RGB interface is selected (REG[0404h] bits 11-10 = 00b), the following formula must be valid.

TED < VT - VPW

Where:

TED = TE Delay = REG[0404h] bits 9-0
VPW = Vertical Pulse Width = REG[0160h] bits 2-0 + 1
VT = Vertical Total = REG[0154h] bits 9-0 + 1

When the TV-Out HSYNC & FIELD type interface is selected (REG[0404h] bits 11-10 = 10b), the following formula must be valid.

TED < VT - 1

Where:

TED = TE Delay = REG[0404h] bits 9-0 + 1
VT = Vertical Total = REG[0218h] bits 9-0 + 1

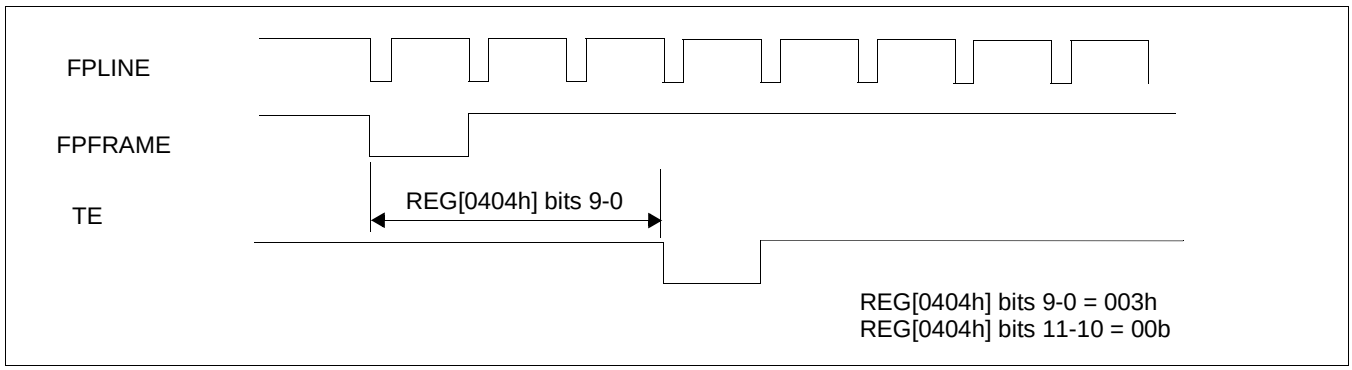


Figure 9-1: TE Output Timing for LCD1 RGB Interface

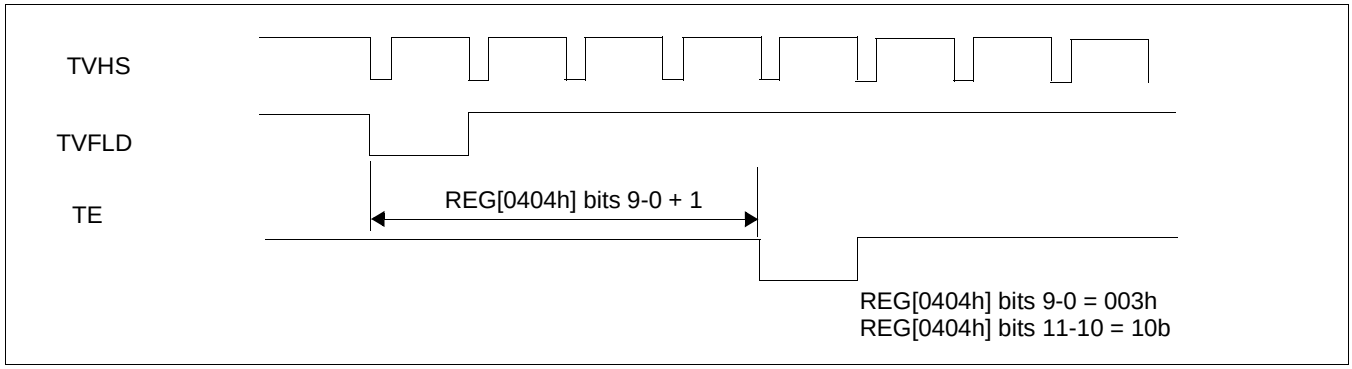


Figure 9-2: TE Output Timing for HSYNC & FIELD TV-Out Interface

REG[0408h] through REG[0414h] are Reserved

These registers are Reserved and should not be written.

REG[0418h] Host Memory Write Access Port Register (AID)
Default = not applicable: Address auto increment disable — Write Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Host Memory Write Access Port bits 15-8							
15	14	13	12	11	10	9	8
Host Memory Write Access Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Host Memory Write Access Port bits [15:0] (Write Only)
These bits are used by the Indirect interface. These bits are the 16-bit data port for memory writes that use the Main or Sub Memory Write Paths. For further information on using the Main or Sub Memory Write Paths, see Section 14.1.3, “Memory Write Access using Main/Sub Memory Write Path” on page 354.

REG[0420h] is Reserved

This register is Reserved and should not be written.

9.4.11 Video Input Interface Registers

REG[0480h] Video Input Interface Output CLK Register
Default = 0000_4000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
n/a							
Video Input Module Software Reset (WO)	Reserved	n/a					Reserved
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Video Input Module Enable	n/a		Video Clock Output Enable	Video Clock Output Divide Select bits 3-0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

bit 15 Video Input Interface Software Reset (Write Only)
This bit performs a software reset of the Video Input Interface module.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit resets the Video Input Interface module.

bit 14 Reserved
The default value of this bit is 1b.

bit 8 Reserved
The default value of this bit is 0b.

bit 7 Video Input Interface Enable
This bit controls the Video Input Interface.
When this bit = 0b, the Video Input Interface is disabled.
When this bit = 1b, the Video Input Interface is enabled.

bit 4 Video Clock Output Enable
This bit controls the Video Clock which is output on the VCLKOUT pin. If enabled, VCLKOUT is output while video frame captures are performed (REG[0488h] bit 0 = 1b).
When this bit = 0b, Video Clock output is disabled.
When this bit = 1b, Video Clock output is enabled.

Note
The Video Input Interface Type Select bits must be set to a valid video input interface type (REG[0484h] bits 5-4 = 01b, 10b, or 11b) in order to output VCLKOUT.

bits 3-0 Video Clock Output Divide Select bits [3:0]

These bits select the divide ratio used to generate the Video Clock output from the System Clock. The output clock frequency must be 40MHz or less.

Table 9-48: Video Clock Output Divide Ratio

REG[0480h] bits 3-0	Output Clock Divide Ratio	REG[0480h] bits 3-0	Output Clock Divide Ratio
0000b	1:1	1000b	9:1
0001b	2:1	1001b	10:1
0010b	3:1	1010b	11:1
0011b	4:1	1011b	12:1
0100b	5:1	1100b	13:1
0101b	6:1	1101b	14:1
0110b	7:1	1110b	15:1
0111b	8:1	1111b	16:1

REG[0484h] Video Input Interface Configuration Register

Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Active Pull-up/down Disable	RGB Data Format Select bits 2-0			YUV 4:2:2 Data Format Select bits 1-0		n/a	
15	14	13	12	11	10	9	8
n/a	YUV Data Type Select	Video Input Interface Type Select bits 1-0		n/a	VDE Active Select	VVSYNC Active Select	Valid Input Clock Edge
7	6	5	4	3	2	1	0

bit 15 Active Pull-up/down Disable

This bit controls the pull-up/down resistors on the video input interface pins.

When this bit = 0b, the pull-up/down resistors are active regardless of the pin direction (input/output).

When this bit = 1b, the pull-up/down resistors are inactive.

Table 9-49: Video Input Interface Active Pull-up/down Resistor Summary

Video Input Interface Pin	Resistor Type
VDT[11:0]	Pull-down
VVSYNC	Pull-up
VDE	Pull-down
VCLKIN	Pull-down

bits 14-12 RGB Data Format Select bits [2:0]

These bits are used for RGB data only (REG[0484h] bits 5-4 = 00b or 01b). These bits select the RGB data format for the Video Input Interface.

Table 9-50: RGB Data Format Selection

REG[0484h] bits 14-12	Data Format
	12-bit RGB Interface (REG[0484h] bits 5-4 = 01b)
000b	RGB 8:8:8
001b	RGB 6:6:6 Format 1
010b	RGB 6:6:6 Format 2
011b	RGB 5:6:5 Format 1
100b	RGB 5:6:5 Format 2
101b	Reserved
110b ~ 111b	Reserved

Note

When the Main Memory Write Path is used as the video input interface write path (REG[0500h] bit 0 = 1b), the Main Memory Write Path must be reset after changing these bits (REG[0504h] bit 15 = 1b).

When the Sub Memory Write Path is used as the video input interface write path (REG[0500h] bit 0 = 0b), the Sub Memory Write Path must be reset after changing these bits (REG[0580h] bit 15 = 1b).

bits 11-10 YUV 4:2:2 Data Format Select bits [1:0]

These bits are used for YUV data only (REG[0484h] bits 5-4 = 10b or 11b). These bits select the YUV data sequence order for the Video Input Interface.

Table 9-51: YUV 4:2:2 Data Format Selection

REG[0484h] bits 11-10	YUV 4:2:2 Format
00b	1st UYVY •••
01b	1st VYUY •••
10b	1st YUYV •••
11b	1st YVYU •••

bit 6 YUV Data Type Select

This bit is used for YUV data only (REG[0484h] bits 5-4 = 10b or 11b). This bit selects whether an UV offset is applied to the incoming data.

Table 9-52: YUV Data Type Selection

REG[0484h] bit 6	Data Type	Input Data Range	Output Data Range
0b (default)	YUV Offset	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255
	YcbCr Offset	16 ≤ Y ≤ 235 16 ≤ U ≤ 240 16 ≤ V ≤ 240	16 ≤ Y ≤ 235 16 ≤ U ≤ 240 16 ≤ V ≤ 240
1b	YUV	0 ≤ Y ≤ 255 -128 ≤ U ≤ 127 -128 ≤ V ≤ 127	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255
	YCbCr	16 ≤ Y ≤ 235 -112 ≤ U ≤ 112 -112 ≤ V ≤ 112	16 ≤ Y ≤ 235 16 ≤ U ≤ 240 16 ≤ V ≤ 240

bits 5-4 Video Input Interface Type Select bits [1:0]

These bits select the type of Video Input Interface.

Table 9-53: Video Input Interface Type Selection

REG[0484h] bits 5-4	Video Input Interface Type
00b	Reserved
01b	12-bit RGB Interface
10b	8-bit YUV 4:2:2 Interface
11b	8-bit YUV 4:2:2 ITU-R BT656 Interface (Note 1)

Note

1. When these bits = 11b, the ITU-R BT656 camera interface is active. In this mode the hsync and vsync signals are mixed with the data signals.
2. When the Main Memory Write Path is used as the video input interface write path (REG[0500h] bit 0 = 1b), the Main Memory Write Path must be reset (REG[0504h] bit 15 = 1b) after changing this bit.
   When the Sub Memory Write Path is used as the video input interface write path (REG[0500h] bit 0 = 0b), the Sub Memory Write Path must be reset (REG[0580h] bit 15 = 1b) after changing this bit.

bit 2 VDE Active Select

This bit selects the polarity of the VDE signal used for the Video Input Interface.
When this bit = 0b, VDE is active High.
When this bit = 1b, VDE is active Low.

bit 1 VVSYNC Active Select

This bit selects the polarity of the VVSYNC signal used for the Video Input Interface.
When this bit = 0b, VVSYNC is active High.
When this bit = 1b, VVSYNC is active Low.

bit 0 Valid Input Clock Edge

This bit determines which edge of the video input clock (VCLKIN) is used to sample input data.
When this bit = 0b, the input data is sampled on the rising edge of VCLKIN.
When this bit = 1b, the input data is sampled on the falling edge of VCLKIN.

REG[0488h] Video Input Interface Control Register (AID)
Default = 0000_0000h: Address auto increment disable — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
							Video Frame Capture Start/Stop

bit 0 Video Frame Capture Start/Stop

This bit controls image frame captures from the video interface. After a video frame capture is stopped by writing a 0b to this bit, it should be read until it returns a value of 0b. Once it returns 0b, the video interface module can be disabled using the Video Input Interface Enable bit, REG[0480h] bit 7 = 0b.
For Writes:
Writing a 0b to this bit stops the video frame capture at the end of the next video frame.
Writing a 1b to this bit starts the video frame capture at the start of the next video frame.
For Reads:
When this bit = 0b, a video frame is not being captured.
When this bit = 1b, a video frame is being captured.

REG[048Ch] Video Input Interface Status Register (AID)
Default = 0000_000Xh: Address auto increment disable — Read Only

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
							VVSYNC Pin Status (RO)

bit 0 VVSYNC Pin Status (Read Only)

This bit indicates the current status of the VVSYNC input pin from the video interface.
When this bit = 0b, VVSYNC input is low.
When this bit = 1b, VVSYNC input is high.

REG[0490h] is Reserved

This register is Reserved and should not be written.

9.4.12 Main Memory Write Path Registers

REG[0500h] Memory Write Path Configuration Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved	n/a					Sub Memory Write Path Overflow Flag	Main Memory Write Path Overflow Flag
15	14	13	12	11	10	9	8
Reserved	Reserved	Sub Memory Write Path Register Update	Main Memory Write Path Register Update	n/a			Memory Write Path Select
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 0b.

bit 9 Sub Memory Write Path Overflow Flag
This bit indicates the raw status of the Sub Memory Write Path Overflow flag.
When this bit = 0b, an overflow has not occurred.
When this bit = 1b, an overflow has occurred.

To clear this flag, write a 1b to this bit.

bit 8 Main Memory Write Path Overflow Flag
This bit indicates the raw status of the Main Memory Write Path Overflow flag.
When this bit = 0b, an overflow has not occurred.
When this bit = 1b, an overflow has occurred.

To clear this flag, write a 1b to this bit.

bit 7 Reserved
The default value for this bit is 0b.

bit 6 Reserved
The default value for this bit is 0b.

bit 5 Sub Memory Write Path Register Update
When the Video Input Interface is changed to use the Sub Memory Write Path (REG[0500h] bit 0 = 0b) or any of the Sub Memory Write Path registers (REG[0580h] ~ REG[05A8h]) are changed while the Video Input Interface is using the Sub Memory Write Path, this bit must be set to 1b to update the internal register values.

When the Host Interface uses the Sub Memory Write Path (REG[0500h] bit 0 = 1b), the internal registers are updated regardless of the setting of this bit.

Note
When this bit returns 1b, the Host can write a 0b to this bit to stop the register update from being done.

bit 4

Main Memory Write Path Register Update
When the Video Input Interface is changed to use the Main Memory Write path (REG[0500h] bit 0 = 1b) or any of the Main Memory Write Path registers (REG[0504h] ~ REG[052Ch]) are changed while the Video Input Interface is using the Main Memory Write Path, this bit must be set to 1b to update the internal register values.

When the Host Interface uses the Main Memory Write Path (REG[0500h] bit 0 = 0b), the internal registers are updated regardless of the setting of this bit.

Note
When this bit returns 1b, the Host can write a 0b to this bit to stop the register update from being done.

bit 0

Memory Write Path Select
This bit selects which memory write path is used by each of the Host and Video interfaces.
When this bit = 0b, the Host Interface uses the Main Memory Write Path and the Video Interface uses the Sub Memory Write Path.
When this bit = 1b, the Host Interface uses the Sub Memory Write Path and the Video Interface uses the Main Memory Write Path.

Note
After changing this bit, both the Main Memory Write Path and Sub Memory Write Path must be reset (REG[0504h] bit 15 = 1b, REG[0580] bit 15 = 1b).

REG[0504h] Main Memory Write Path Configuration Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Main Memory Write Path Software Reset (WO)	n/a	eIC Mode Select	eIC Unit Select	Alpha Blend Key Color Preserve	PIP2 Transparency Key Color Preserve	PIP1 Transparency Key Color Preserve	eIC Enable
15	14	13	12	11	10	9	8
Double Buffer Status	Double Buffer Mode Enable	YUV 4:2:0 Conversion Enable	RYC0 Enable	Mirror Enable	Rotation Mode Select bits 1-0		Main Memory Write Path Enable
7	6	5	4	3	2	1	0

bit 15 Main Memory Write Path Software Reset (Write Only)
This bit performs a software reset of the Main Memory Write Path module.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit performs a software reset of the Main Memory Write Path module.

bit 13 eIC Mode Select
When the eIC is enabled (REG[0504h] bit 8 = 1b), this bit selects the eIC mode used for RGB format input data. For YUV format input data, this bit must be set to 1b (YUV can only use Normal mode).
When this bit = 0b, adaptive mode is selected.
When this bit = 1b, normal mode is selected.

Note
When partial eIC mode is selected (REG[0504h] bit 12 = 1b), this setting is ignored and normal mode is used.

bit 12 eIC Unit Select
When the eIC is enabled (REG[0504h] bit 8 = 1b), this bit selects the eIC unit used for RGB format input data.
When this bit = 0b, line eIC mode is selected.
When this bit = 1b, partial eIC mode is selected.

bit 11 Alpha Blend Key Color Preserve

When the eIC is enabled (REG[0504h] bit 8 = 1b), this bit ensures that the Alpha Blend key colors are reproduced accurately.
When this bit = 0b, key color preserve is disabled.
When this bit = 1b, key color preserve is enabled.

When Alpha Blend Key Color Preserve is used, the following sequence must be followed.

1. Set the Alpha Blend Key colors in REG[0628h] ~ REG[0644h]
2. Enable Alpha Blend Key Color Preserve (REG[0504h] bit 11 = 1b)
3. Write frame data to the main memory write path.

Note
The Alpha Blend Key colors (REG[0628h] ~ REG[0644h]) must not be changed after the eIC has been used.

bit 10 PIP2 Transparency Key Color Preserve

When the eIC is enabled, this bit ensures that the PIP2 Transparency key color is reproduced accurately.
When this bit = 0b, key color preserve is disabled.
When this bit = 1b, key color preserve is enabled.

When PIP2 Transparency Key Color Preserve is used, the following sequence must be followed.

1. Set the PIP2 Transparency Key colors in REG[0620h] ~ REG[0624h]
2. Enable PIP2 Transparency Key Color Preserve (REG[0504h] bit 10 = 1b)
3. Write frame data to the main memory write path.

Note
The PIP2 Transparency Key colors (REG[0620h] ~ REG[0624h]) must not be changed after the eIC has been used.

bit 9 PIP1 Transparency Key Color Preserve

When the eIC is enabled, this bit ensures that the PIP1 Transparency key color is reproduced accurately.
When this bit = 0b, key color preserve is disabled.
When this bit = 1b, key color preserve is enabled.

When PIP1 Transparency Key Color Preserve is used, the following sequence must be followed.

1. Set the PIP1 Transparency Key colors in REG[0618h] ~ REG[061Ch]
2. Enable PIP1 Transparency Key Color Preserve (REG[0504h] bit 9 = 1b)
3. Write frame data to the main memory write path.

Note
The PIP1 Transparency Key colors (REG[0618h] ~ REG[061Ch]) must not be changed after the eIC has been used.

bit 8 eIC Enable

This bit controls whether the eIC is used for the Main Memory Write Path. The eIC is configured using the eIC Mode Select bit (bit 13) and the eIC Unit Select bit (bit 12).
When this bit = 0b, the eIC is disabled (bypassed).
When this bit = 1b, the eIC is enabled.

bit 7 Double Buffer Status

For Reads:
When double buffer mode is enabled (REG[0504h] bit 6 = 1b), this bit indicates which buffer is being written.
When this bit = 0b, Buffer A is being written (when the write to Buffer A completes, this bit changes to 1b).
When this bit = 1b, Buffer B is being written (when the write to Buffer B completes, this bit changes to 0b).
For Writes:
This bit selects which buffer is written first. Set this bit while writes to eDRAM have stopped (REG[002Ch] bit 3 = 0b).
When this bit = 0b, Buffer A is written first.
When this bit = 1b, Buffer B is written first.

bit 6 Double Buffer Mode Enable

This bit controls double buffer mode for the Main Memory Write Path. When double buffering is enabled, writes are done alternately to Buffer A and Buffer B. When Double buffering is disabled, writes are done to Buffer A only. For information on setting the start addresses for Buffer A and Buffer B, see the bit descriptions for REG[0508h] ~ REG[0514h].
When this bit = 0b, double buffer mode is disabled (Buffer A is used).
When this bit = 1b, double buffer mode is enabled (Buffer A and Buffer B are used).

bit 5 YUV 4:2:0 Conversion Enable
This bit is only available when the RYC0 is enabled, REG[0504h] bit 4 = 1b.
This bit controls whether YUV 4:2:2 image data, that has been previously converted from RGB by the RYC0, is converted to YUV 4:2:0 image data during writes using the Main a Memory Write Path.
When this bit = 0b, YUV 4:2:2 to YUV 4:2:0 conversion is disabled.
When this bit = 1b, YUV 4:2:2 to YUV 4:2:0 conversion is enabled.

bit 4 RYC0 Enable
This bit controls whether RGB 8:8:8 and RGB 5:6:5 image data is converted to YUV 4:2:2 image data during writes using the Main Memory Write Path.
When this bit = 0b, RGB to YUV 4:2:2 conversion is disabled.
When this bit = 1b, RGB to YUV 4:2:2 conversion is enabled.

bit 3 Mirror Enable
This bit controls whether the mirror function is enabled for writes using the Main Memory Write Path.
When this bit = 0b, the mirror function is disabled.
When this bit = 1b, the mirror function is enabled.

bits 2-1 Rotation Mode Select bits [1:0]
These bits select the rotation applied for writes using the Main Memory Write Path.

Table 9-54: Rotation Mode Selection

REG[0504h] bits 2-1	Rotation Mode
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

bit 0 Main Memory Write Path Enable
This bit controls the Main Memory Write Path.
When this bit = 0b, the Main Memory Write Path is disabled.
When this bit = 1b, the Main Memory Write Path is enabled.

REG[0508h] Main Memory Buffer A RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Main Memory Buffer A RGB,Y Start Address bits 12-8				
7	6	5	4	3	2	1	0
Main Memory Buffer A RGB,Y Start Address bits 7-0							

bits 12-0 Main Memory Buffer A RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the Main Memory Write Path where RGB or Y data is written, in 256 byte resolution. When double buffer mode is enabled (REG[0504h] bit 6 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0504h] bit 6 = 0b), this address is always used.

REG[0508h] bits 12-0 = start address in bytes ÷ 256

REG[050Ch] Main Memory Buffer A UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Main Memory Buffer A UV Start Address bits 12-8				
7	6	5	4	3	2	1	0
Main Memory Buffer A UV Start Address bits 7-0							

bits 12-0 Main Memory Buffer A UV Start Address bits [12:0]

These bits determine the memory start address for the Main Memory Write Path where UV data is written, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0504h] bit 6 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0504h] bit 6 = 0b), this address is always used.

REG[050Ch] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[0510h] Main Memory Buffer B RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Main Memory Buffer B RGB,Y Start Address bits 12-8				
7	6	5	4	3	2	1	0
Main Memory Buffer B RGB,Y Start Address bits 7-0							

bits 12-0 Main Memory Buffer B RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the Main Memory Write Path where RGB or Y data is written, in 256 byte resolution. When double buffer mode is enabled (REG[0504h] bit 6 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0504h] bit 6 = 0b), this address is not used.

REG[0510h] bits 12-0 = start address in bytes ÷ 256

REG[0514h] Main Memory Buffer B UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Main Memory Buffer B UV Start Address bits 12-8				
7	6	5	4	3	2	1	0
Main Memory Buffer B UV Start Address bits 7-0							

bits 12-0 Main Memory Buffer B UV Start Address bits [12:0]

These bits determine the memory start address for the Main Memory Write Path where UV data is written, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0504h] bit 6 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0504h] bit 6 = 0b), this address is not used.

REG[0514h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[0518h] Main Memory Line Address Offset Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Main Memory Line Address Offset bits 6-0							

bits 6-0 Main Memory Line Address Offset bits [6:0]

These bits determine the line address offset for the Main Memory Write Path, in bytes. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[0518h] bits 6-0 = line address offset in bytes ÷ 32

Note

These bits must be set so that the line address offset is 64 byte aligned (bit 0 = 0b).

REG[051Ch] Main Memory Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Main Memory Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Main Memory Vertical Size bits [7:0]

These bits determine the memory area vertical size for the Main Memory Write Path, in 4 line resolution. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[051Ch] bits 7-0 = vertical size in lines ÷ 4 - 1

Note

The memory area vertical size can range from a minimum of 4 lines (REG[051Ch] = 0000h) to a maximum of 864 lines (REG[051Ch] = 00D7h).

REG[0520h] Main Image Horizontal Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main Image Horizontal Size bits 9-8	
7	6	5	4	3	2	1	0
Main Image Horizontal Size bits 7-0							

bits 9-0 Main Image Horizontal Size bits [9:0]

These bits determine the write window horizontal size before rotation is applied (see REG[0504h] bits 2-1), in pixels. The write window is the area where the actual image data is written within the Main Memory Write Path memory area. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[0520h] bits 9-0 = horizontal size in pixels - 1

Note

1. The write window horizontal size can range from a minimum of 1 pixel (REG[0520h] = 0000h) to a maximum of 864 pixels (REG[0520h] = 035Fh).
2. For YUV 4:2:2 or YUV 4:2:0, the write window horizontal size must be an even number.

REG[0524h] Main Image Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main Image Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
Main Image Vertical Size bits 7-0							

bits 9-0 Main Image Vertical Size bits [9:0]

These bits determine the write window vertical size before rotation is applied (see REG[0504h] bits 2-1), in lines. The write window is the area where the actual image data is written within the Main Memory Write Path memory area. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[0524h] bits 9-0 = vertical size in lines - 1

Note

1. The write window vertical size can range from a minimum of 1 line (REG[0524h] = 0000h) to a maximum of 864 lines (REG[0524h] = 035Fh).
2. For YUV 4:2:0, the write window vertical size must be an even number.

REG[0528h] Main Image X Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main Image X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main Image X Start Position bits 7-0							

bits 9-0 Main Image X Start Position bits [9:0]

These bits determine the write window X start position for the Main Memory Write Path, in pixels. The write window X start position defines the position, in the X direction, where the write window starts relative to the left side of the defined memory area (position 0). For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[0528h] bits 9-0 = X start position in pixels

Note

1. The write window X start position can range from a minimum of 0 pixels (REG[0528h] = 0000h) to a maximum of 863 pixels (REG[0528h] = 035Fh).
2. For YUV 4:2:2 or YUV 4:2:0, the write window X start position must be an even number.

REG[052Ch] Main Image Y Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main Image Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main Image Y Start Position bits 7-0							

bits 9-0 Main Image Y Start Position bits [9:0]

These bits determine the write window Y start position for the Main Memory Write Path, in lines. The write window Y start position defines the position, in the Y direction, where the write window starts relative to the top of the defined memory area (position 0). For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[052Ch] bits 9-0 = Y start position in lines.

Note

1. The write window Y start position can range from a minimum of 0 lines (REG[052Ch] = 0000h) to a maximum of 863 lines (REG[052Ch] = 035Fh).
2. For YUV 4:2:0, the write window Y start position must be an even number.

9.4.13 Sub Memory Write Path Registers

REG[0580h] Sub Memory Write Path Enable Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Sub Memory Write Path Software Reset (WO)	n/a						
15	14	13	12	11	10	9	8
Double Buffer Status	Double Buffer Mode Enable	n/a					Sub Memory Write Path Enable
7	6	5	4	3	2	1	0

bit 15 Sub Memory Write Path Software Reset (Write Only)
This bit performs a software reset of the Sub Memory Write Path module.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit performs a software reset of the Sub Memory Write Path module.

bit 7 Double Buffer Status
For Reads:
When double buffer mode is enabled (REG[0580h] bit 6 = 1b), this bit indicates which buffer is being written.
When this bit = 0b, Buffer A is being written (when the write to BufferA completes, this bit changes to 1b).
When this bit = 1b, Buffer B is being written (when the write to BufferB completes, this bit changes to 0b).
For Writes:
This bit selects which buffer is written first. Set to this bit while writes to eDRAM have stopped (REG[002Ch] bit 4 = 0b).
When this bit = 0b, Buffer A is written first.
When this bit = 1b, Buffer B is written first.

bit 6 Double Buffer Mode Enable
This bit controls double buffer mode for the Sub Memory Write Path. When double buffering is enabled, writes are done alternately to Buffer A and Buffer B. When double buffering is disabled, writes are done to Buffer A only. For information on setting the start addresses for Buffer A and Buffer B, see the bit descriptions for REG[0584h] ~ REG[0590h].
When this bit = 0b, double buffer mode is disabled (Buffer A is used).
When this bit = 1b, double buffer mode is enabled (Buffer A and Buffer B are used).

bit 0 Sub Memory Write Path Enable
This bit controls the Sub Memory Write Path.
When this bit = 0b, the Sub Memory Write Path is disabled.
When this bit = 1b, the Sub Memory Write Path is enabled.

REG[0584h] Sub Memory Buffer A RGB, Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Sub Memory Buffer A RGB,Y Start Address bits 12-8				
7	6	5	4	3	2	1	0
Sub Memory Buffer A RGB,Y Start Address bits 7-0							

bits 12-0 Sub Memory BufferA RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the Sub Memory Write Path where RGB or Y data is written, in 256 byte resolution. When double buffer mode is enabled (REG[0580h] bit 6 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0580h] bit 6 = 0b), this address is always used.

REG[0584h] bits 12-0 = start address in bytes ÷ 256

REG[0588h] Sub Memory Buffer A UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Sub Memory Buffer A UV Start Address bits 12-8				
7	6	5	4	3	2	1	0
Sub Memory Buffer A UV Start Address bits 7-0							

bits 12-0 Sub Memory Buffer A UV Start Address bits [12:0]

These bits determine the memory start address for the Sub Memory Write Path where UV data is written, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0580h] bit 6 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0580h] bit 6 = 0b), this address is always used.

REG[0588h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[058Ch] Sub Memory Buffer B RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			Sub Memory Buffer B RGB,Y Start Address bits 12-8				
15	14	13	12	11	10	9	8
Sub Memory Buffer B RGB,Y Start Address bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Sub Memory Buffer B RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the Sub Memory Write Path where RGB or Y data is written, in 256 byte resolution. When double buffer mode is enabled (REG[0580h] bit 6 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0580h] bit 6 = 0b), this address is not used.

REG[058Ch] bits 12-0 = start address in bytes ÷ 256

REG[0590h] Sub Memory Buffer B UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			Sub Memory Buffer B UV Start Address bits 12-8				
15	14	13	12	11	10	9	8
Sub Memory Buffer B UV Start Address bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 Sub Memory Buffer B UV Start Address bits[12:0]

These bits determine the memory start address for the Sub Memory Write Path where UV data is written, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0580h] bit 6 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0580h] bit 6 = 0b), this address is not used.

REG[0590h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[0594h] Sub Memory Line Address Offset Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Sub Memory Line Address Offset bits 6-0							

bits 6-0 Sub Memory Line Address Offset bits [6:0]

These bits determine the line address offset for the Sub Memory Write Path, in bytes. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[0594h] bits 6-0 = line address offset in bytes ÷ 32

Note

These bits must be set so that the line address offset is 64 by aligned (bit 0 = 0b)

REG[0598h] Sub Memory Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Sub Memory Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Sub Memory Vertical Size bits [7:0]

These bits determine the memory area vertical size for the Sub Memory Write Path, in 4 line resolution. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[0598h] bits 7-0 = vertical size in lines ÷ 4 - 1

Note

The memory area vertical size can range from a minimum of 4 lines (REG[0598h] = 0000h) to a maximum of 1024 lines (REG[0598h] = 00FFh).

REG[059Ch] Sub Image Horizontal Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Sub Image Horizontal Size bits 9-8	
7	6	5	4	3	2	1	0
Sub Image Horizontal Size bits 7-0							

bits 9-0 Sub Image Horizontal Size bits [9:0]

These bits determine the write window horizontal size for the Sub Memory Write Path, in pixels. The write window is the area where the actual image data is written within the Sub Memory Write Path memory area. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[059Ch] bits 9-0 = horizontal size in pixels - 1

Note

1. The write window horizontal size can range from a minimum of 1 pixel (REG[059Ch] = 0000h) to a maximum of 1022 pixels (REG[059Ch] = 03FDh). (REG[059Ch] = 0000h) to a maximum of 1024 pixels (REG[059Ch] = 03FFh).
2. For YUV 4:2:2 or YUV 4:2:0, the write window horizontal size must be an even number.

REG[05A0h] Sub Image Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Sub Image Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
Sub Image Vertical Size bits 7-0							

bits 9-0 Sub Image Vertical Size bits [9:0]

These bits determine the write window vertical size for the Sub Memory Write Path, in lines. The write window is the area where the actual image data is written within the Sub Memory Write Path memory area. For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[05A0h] bits 9-0 = vertical size in lines - 1

Note

1. The write window vertical size can range from a minimum of 1 line (REG[05A0h] = 0000h) to a maximum of 1024 lines (REG[05A0h] = 03FFh).
2. For YUV 4:2:0, the write window vertical size must be an even number.

REG[05A4h] Sub Image X Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Sub Image X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Sub Image X Start Position bits 7-0							

bits 9-0 Sub Image X Start Position bits [9:0]

These bits determine the write window X start position for the Sub Memory Write Path, in pixels. The write window X start position defines the position, in the X direction, where the write window starts relative to the left side of the defined memory area (position 0). For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[05A4h] bits 9-0 = X start position in pixels

Note

1. The write window X start position can range from a minimum of 0 pixels (REG[05A4h] = 0000h) to a maximum of 1023 pixels (REG[05A4h] = 03FFh).
2. For YUV 4:2:2 or YUV 4:2:0, the write window X start position must be an even number.

REG[05A8h] Sub Image Y Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Sub Image Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Sub Image Y Start Position bits 7-0							

bits 9-0 Sub Image Y Start Position bits [9:0]

These bits determine the write window Y start position for the Sub Memory Write Path, in pixels. The write window Y start position defines the position, in the Y direction, where the write window starts relative to the top of the defined memory area (position 0). For further information on writing image data to memory, see Section 11.1, “Configuring the Write Paths” on page 277.

REG[05A8h] bits 9-0 = Y start position in lines

Note

1. The write window Y start position can range from a minimum of 0 lines (REG[05A8h] = 0000h) to a maximum of 1023 lines (REG[05A8h] = 03FFh).
2. For YUV 4:2:0, the write window Y start position must be an even number.

9.4.14 Display Configuration Registers

REG[0600h] Display Mode Setting Register 0
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
TV-Out Interface Register Update	LCD Interface Register Update	n/a		Reserved	LCD SW Video Invert	TV-Out Display Blank	LCD Display Blank
15	14	13	12	11	10	9	8
LCD and TV-Out Software Reset (WO)	n/a	LUT Enable	n/a			LUT Address Clear (WO)	n/a
7	6	5	4	3	2	1	0

bit 15 TV-Out Interface Register Update

When a register related to the TV-Out interface is changed while the TV is being displayed, a 1b must be written to this bit. Once the new register values are updated in the internal circuits, this bit is automatically reset to 0b.

When REG[0604h] bits 15-12 = 0100b, the Main/PIP1/PIP2 window registers are all updated at the same time. When REG[0604h] bits 15-12 = 1011b, the PIP1/PIP2 window registers are updated at the same time.

Note
When the Display Output Port is configured for simultaneous LCD + TV-Out (REG[0604h] bits 15-12 = 1011b), set bits 15 and 14 to 1b at the same time.

bit 14 LCD Interface Register Update

When a register related to the LCD interface is changed while the LCD is being displayed, a 1b must be written to this bit. Once the new register values are updated in the internal circuits, this bit is automatically reset to 0b.

When REG[0604h] bits 15-12 = 0001b or 0010b, the Main/PIP1/PIP2 window registers are all updated at the same time. When REG[0604h] bits 15-12 = 1011b, the Main window register is updated.

Note
When the Display Output Port is configured for simultaneous LCD + TV-Out (REG[0604h] bits 15-12 = 1011b), set bits 15 and 14 to 1b at the same time.

bit 11 Reserved

The default value for this bit is 0b.

bit 10 LCD Software Video Invert

This bit determines whether the RGB type panel data output is inverted or left unchanged (normal). This bit has an effect when the display is active and when the display is blanked (see REG[0600h] bit 8).
When this bit = 0b, the panel data output is left unchanged (normal).
When this bit = 1b, the panel data output is inverted.

bit 9 TV-Out Display Blank

This bit blanks the display of Hsync & FIELD Type / ITU-R BT656 TV-Out interfaces by disabling the display pipe and forcing all data outputs low.
When this bit = 0b, the display is active.
When this bit = 1b, display is blanked and all data outputs are forced low.

bit 8 LCD Display Blank

This bit blanks the display of RGB type panels by disabling the display pipe and forcing all data outputs low (or high).
When this bit = 0b, the display is active.
When this bit = 1b, the display is blanked and all data outputs are forced low or high based on the setting of the LCD Software Video Invert bit (REG[0600h] bit 10).

Table 9-55: LCD Interface Data Output Selection

REG[0600h] bit 8	REG[0600h] bit 10	Data Output
0b	0b	Normal
	1b	Inverted
1b	0b	Force low
	1b	Force high

bit 7 LCD and TV-Out Software Reset (Write Only)

This bit performs a software reset of the LCD and TV-Out interface.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit performs a software reset of the LCD and TV-Out interface. (AME, YRC1, YRC2, RYC3, Transparency , LUT, LCD Interface, TV-Out Interface)

bit 5 LUT Enable

This bit controls the LUT (Look-up Table).
When this bit = 0b, the LUT is bypassed.
When this bit = 1b, the LUT is used.

Note

When the Display Output Port is set for LCD1 (Main) + TV-Out (PIP1/PIP2) (REG[0604h] bits 11-8 = 1011b), the LUT function is applied only to the TV-Out display and has no effect on LCD1.

bit 1 LUT Address Clear (Write Only)

This bit clears the LUT Address Counter (REG[064Ch] bits 7-0).
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit clears the LUT Address Counter bits (REG[064Ch] bits 7-0).

REG[0604h] Display Mode Setting Register 1
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Display Output Port Status bits 3-0 (RO)				Display Output Port Select bits 3-0			
15	14	13	12	11	10	9	8
n/a	Layer Mode Select bits 1-0		n/a	PIP2 Window Display Enable	PIP1 Window Display Enable	Main2 Window Display Enable	Main1 Window Display Enable
7	6	5	4	3	2	1	0

bits 15-12 Display Output Port Status bits [3:0] (Read Only)

These bits indicate the selected display output port is active. Before sending image data to the port, confirm that the desired port is active. When the LCD2 port or TV-Out parallel port is selected, confirm that the desired port is active before performing the transfer. These bits are read only and are changed using the Display Output Port Select bits (REG[0604h] bits 11-8).

Table 9-56: Display Output Port Status

REG[0604h] bits 15-12	Display Output Port
0000b	All Off
0001b	LCD1 (Main/PIP1/PIP2)
0010b	LCD2 (Main/PIP1/PIP2)
0011b	Reserved
0100b	TV-Out (Main/PIP1/PIP2)
0101b - 1010b	Reserved
1011b	LCD1 (Main) + TV-Out (PIP1/PIP2)
1100b - 1111b	Reserved

bits 11-8 Display Output Port Select bits [3:0]

These bits specify the valid display output port. Changes to these bits take effect after the end of the current frame. The auto transfer bits (REG[0114h] bit 1, REG[022Ch] bit 1) must be cleared before changing these bits.

Table 9-57: Display Output Port Selection

REG[0604h] bits 11-8	Display Output Port	Frame Transfer Requirements
0000b	All Off	Not applicable.
0001b	LCD1 (Main/PIP1/PIP2)	Not applicable.
0010b	LCD2 (Main/PIP1/PIP2)	At least one window (Main1, Main2, PIP1, PIP2) must be enabled before a frame transfer can be done.
0011b	Reserved	—
0100b	TV-Out (Main/PIP1/PIP2)	When the TV-Out interface is configured for Parallel (REG[0200h] bits 1-0 = 10b), at least one window (Main1, Main2, PIP1, PIP2) must be enabled before a frame transfer can be done.
0101b - 1010b	Reserved	—
1011b	LCD1 (Main) + TV-Out (PIP1/PIP2)	When the TV-Out interface is configured for Parallel (REG[0200h] bits 1-0 = 10b), at least one window (PIP1 or PIP2) must be enabled before a frame transfer can be done.
1100b - 1111b	Reserved	—

Note

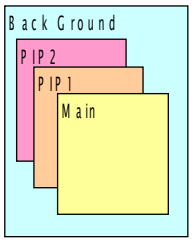
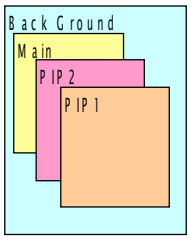
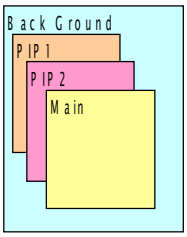
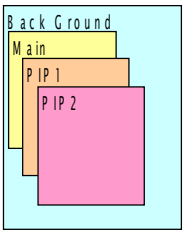
The display output port should not be changed directly between “active” modes. To change the active display output port use the following sequence.

1. Set the display output port to “All Off” (REG[0604h] bits 11-8 = 0000b).
2. Wait until the Display Output Port Status bits return 0000b (REG[0604h] bits 15-12).
3. Perform LCD and TV-Out Software Reset (REG[0600h] bit 7 = 1b).
4. If necessary, set the LCD and TV-Out interface registers.
5. Set the register update bits (For the LCD interface: REG[0600h] bit 14 = 1b, For the TV-Out interface: REG[0600h] bit 14 = 1b).
6. Select the desired display output port using REG[0604h] bits 11-8.

bits 6-5 Layer Mode Select bits [1:0]

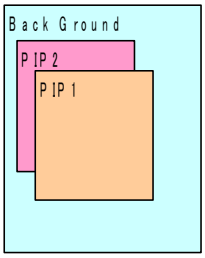
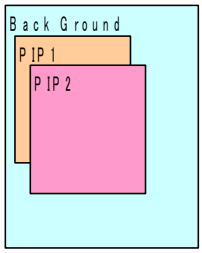
These bits select the window display order for the display output port modes for LCD1, LCD2, and TV-Out that use the Main/PIP1/PIP2 windows (REG[0604h] bits 15-12 = 0001b, 0010b, and 0100b). For these modes use the following table to determine the layer order.

Table 9-58: Layer Mode Selection 1

REG[0604h] bits 6-5	00b	01b	10b	11b
Layer Order				

For the display output port mode for LCD1 + TV-Out where TV-Out uses only the PIP1 and PIP2 windows (REG[0604h] bits 15-12 = 1011b), use the following table to determine the layer order.

Table 9-59: Layer Mode Selection 2

REG[0604h] bits 6-5	00b	01b	10b	11b
Layer Order	Reserved	Reserved		

bit 3 PIP2 Window Display Enable

This bit controls whether the PIP2 window is displayed.
When this bit = 0b, PIP2 window is disabled.
When this bit = 1b, PIP2 window is enabled.

Note

For some configurations at least one window (Main1, Main2, PIP1, PIP2) must be enabled before a frame transfer can take place. For a summary of this requirement, see Table 9-57: “Display Output Port Selection,” on page 191.

bit 2 PIP1 Window Display Enable
This bit controls whether the PIP1 window is displayed.
When this bit = 0b, PIP1 window is disabled.
When this bit = 1b, PIP1 window is enabled.

Note
For some configurations at least one window (Main1, Main2, PIP1, PIP2) must be enabled before a frame transfer can take place. For a summary of this requirement, see Table 9-57: "Display Output Port Selection," on page 191.

bit 1 Main2 Window Display Enable
This bit controls whether the Main2 window is displayed.
When this bit = 0b, Main2 window is disabled.
When this bit = 1b, Main2 window is enabled.

Note
For some configurations at least one window (Main1, Main2, PIP1, PIP2) must be enabled before a frame transfer can take place. For a summary of this requirement, see Table 9-57: "Display Output Port Selection," on page 191.

bit 0 Main1 Window Display Enable
This bit controls whether the Main1 window is displayed.
When this bit = 0b, Main1 window is disabled.
When this bit = 1b, Main1 window is enabled.

Note
For some configurations at least one window (Main1, Main2, PIP1, PIP2) must be enabled before a frame transfer can take place. For a summary of this requirement, see Table 9-57: "Display Output Port Selection," on page 191.

REG[0608h] Transparency and Alpha Blend Control Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a				Alpha Blend 4 Key Color Enable	Alpha Blend 3 Key Color Enable	Alpha Blend 2 Key Color Enable	Alpha Blend 1 Key Color Enable
15	14	13	12	11	10	9	8
Alpha Blend Mode Select	n/a				PIP2 Transparency Enable	PIP1 Transparency Enable	n/a
7	6	5	4	3	2	1	0

bit 11 Alpha Blend 4 Key Color Enable
This bit controls the Alpha Blend 4 Key Color.
When this bit = 0b, the Alpha Blend Key Color4 is disabled.
When this bit = 1b, the Alpha Blend Key Color4 is enabled.

bit 10 Alpha Blend 3 Key Color Enable
This bit controls the Alpha Blend 3Key Color.
When this bit = 0b, the Alpha Blend 3 Key Color is disabled.
When this bit = 1b, the Alpha Blend 3 Key Color is enabled.

bit 9 Alpha Blend 2 Key Color Enable
This bit controls the Alpha Blend 2 Key Color.
When this bit = 0b, the Alpha Blend 2 Key Color is disabled.
When this bit = 1b, the Alpha Blend 2 Key Color is enabled.

bit 8 Alpha Blend 1 Key Color Enable
This bit controls the Alpha Blend 1 Key Color.
When this bit = 0b, the Alpha Blend 1 Key Color is disabled.
When this bit = 1b, the Alpha Blend 1 Key Color is enabled.

bit 7 Alpha Blend Mode Select
This bit selects which windows are alpha blended.
When this bit = 0b, alpha blending is performed on the Main and PIP windows.
When this bit = 1b, alpha blending is performed on the PIP1 and PIP2 windows.

Note

When the LCD + TV-Out display output port is selected (REG[0604h] bits 15-12 = 1011b):

- REG[0608h] bit 7 must be set to 1b.
- When PIP1 Filter Scaling Mode is enabled (REG[0704h] bit 15 = 1b), the alpha blend has no effect even if the alpha blend is enabled (REG[0608h] bit 11, 10, 9, or 8 = 1b).
- When AME is active in PIP1 (REG[0900h] bits 1-0 = 01b), the alpha blend has no effect even if the alpha blend is enabled (REG[0608h] bit 11, 10, 9, or 8 = 1b).

bit 2 PIP2 Transparency Enable
This bit controls the PIP2 transparency.
When this bit = 0b, the PIP2 transparency is disabled.
When this bit = 1b, the PIP2 transparency is enabled.

Note

1. When PIP2 Filter Scaling Mode is enabled (REG[0804h] bit 15 = 1b), the PIP2 transparency has no effect even if REG[0608h] bit 2 = 1b.
2. When AME is active in PIP2 (REG[0900h] bits 1-0 = 10b), the PIP2 transparency has no effect even if REG[0608h] bit 2 = 1b.

bit 1 PIP1 Transparency Enable
This bit controls the PIP1 transparency.
When this bit = 0b, the PIP1 transparency is disabled.
When this bit = 1b, the PIP1 transparency is enabled.

Note

1. When the LCD + TV-Out display output port is selected (REG[0604h] bits 15-12 = 1011b), this bit must be set to 0b.
2. When PIP1 Filter Scaling Mode is enabled (REG[0704h] bit 15 = 1b), the PIP1 transparency has no effect even if REG[0608h] bit 1 = 1b.
3. When AME is active in PIP1 (REG[0900h] bits 1-0 = 01b), the PIP1 transparency has no effect even if REG[0608h] bit 1 = 1b.

REG[060Ch] Background Color Setting Register 0
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Background Color Green bits 7-0							
15	14	13	12	11	10	9	8
Background Color Blue bits 7-0							
7	6	5	4	3	2	1	0

REG[0610h] Background Color Setting Register 1
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Background Color Red bits 7-0							
7	6	5	4	3	2	1	0

REG[0610h] bits 7-0 Background Color Red bits [7:0]
REG[060Ch] bits 15-8 Background Color Green bits [7:0]
REG[060Ch] bits 7-0 Background Color Blue bits [7:0]
These bits specify the background color in RGB 8:8:8 format.

REG[0614h] Alpha Blend Ratio Setting Register
Default = 0000_8888h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Alpha Blend 4 Ratio Setting bits 3-0				Alpha Blend 3 Ratio Setting bits 3-0			
15	14	13	12	11	10	9	8
Alpha Blend 2 Ratio Setting bits 3-0				Alpha Blend 1 Ratio Setting bits 3-0			
7	6	5	4	3	2	1	0

bits 15-12 Alpha Blend 4 Ratio Setting bits [3:0]
These bits only have an effect when Alpha Blend 4 Key Color is enabled, REG[0608h] bit 11 = 1b.

Table 9-60: Alpha Blend 4 Ratio Selection

REG[0614h] bits 15-12	Alpha Blend 4 Ratio					
	REG[0604h] bits 15-12 = 0001b, 0010b, 0100b				REG[0604h] bits 15-12 = 1011b	
	REG[0608h] bit 7 = 0b		REG[0608h] bit 7 = 1b		REG[0608h] bit 7 = 1b	
	Main	PIP1 or PIP2	PIP1	PIP2	PIP1	PIP2
0000b (0h)	100%	0%	100%	0%	100%	0%
0001b (1h)	87.5%	12.5%	87.5%	12.5%	87.5%	12.5%
0010b (2h)	75%	25%	75%	25%	75%	25%
0011b (3h)	62.5%	37.5%	62.5%	37.5%	62.5%	37.5%
0100b (4h)	50%	50%	50%	50%	50%	50%
0101b (5h)	37.5%	62.5%	37.5%	62.5%	37.5%	62.5%
0110b (6h)	25%	75%	25%	75%	25%	75%
0111b (7h)	12.5%	87.5%	12.5%	87.5%	12.5%	87.5%
1000b (8h)	0%	100%	0%	100%	0%	100%
1001b ~ 1111b	Reserved					

bits 11-8 Alpha Blend 3 Ratio Setting bits [3:0]
These bits only have an effect when Alpha Blend 3 Key Color is enabled, REG[0608h] bit 10 = 1b.

Table 9-61: Alpha Blend 3 Ratio Selection

REG[0614h] bits 11-8	Alpha Blend 3 Ratio
0000b (0h)	0%
0001b (1h)	12.5%
0010b (2h)	25%
0011b (3h)	37.5%
0100b (4h)	50%
0101b (5h)	62.5%
0110b (6h)	75%
0111b (7h)	87.5%
1000b (8h)	100%
1001b ~ 1111b	Reserved

bits 7-4 Alpha Blend 2 Ratio Setting bits [3:0]
These bits only have an effect when Alpha Blend 2 Key Color is enabled, REG[0608h] bit 9 = 1b.

Table 9-62: Alpha Blend 2 Ratio Selection

REG[0614h] bits 7-4	Alpha Blend 2 Ratio
0000b (0h)	0%
0001b (1h)	12.5%
0010b (2h)	25%
0011b (3h)	37.5%
0100b (4h)	50%
0101b (5h)	62.5%
0110b (6h)	75%
0111b (7h)	87.5%
1000b (8h)	100%
1001b ~ 1111b	Reserved

bits 3-0 Alpha Blend 1 Ratio Setting bits [3:0]

These bits only have an effect when Alpha Blend 1 Key Color is enabled, REG[0608h] bit 8 = 1b.

Table 9-63: Alpha Blend 1 Ratio Selection

REG[0614h] bits 3-0	Alpha Blend 1 Ratio
0000b (0h)	0%
0001b (1h)	12.5%
0010b (2h)	25%
0011b (3h)	37.5%
0100b (4h)	50%
0101b (5h)	62.5%
0110b (6h)	75%
0111b (7h)	87.5%
1000b (8h)	100%
1001b ~ 1111b	Reserved

REG[0618h] PIP1 Window Transparency Key Color Register 0
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PIP1 Window Transparency Key Color Green bits 7-0							
7	6	5	4	3	2	1	0
PIP1 Window Transparency Key Color Blue bits 7-0							

REG[061Ch] PIP1 Window Transparency Key Color Register 1
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
PIP1 Window Transparency Key Color Red bits 7-0							

REG[061Ch] bits 7-0 PIP1 Window Transparency Key Color Red bits [7:0]
REG[0618h] bits 15-8 PIP1 Window Transparency Key Color Green bits [7:0]
REG[0618h] bits 7-0 PIP1 Window Transparency Key Color Blue bits [7:0]
These bits specify the PIP1 transparency key color, in RGB 8:8:8 format, that is compared with the PIP1 window pixel data. For RGB 5:6:5 formats, fill the least significant bits as follows.

Table 9-64: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5							RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

REG[0620h] PIP2 Window Transparency Key Color Register 0
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
PIP2 Window Transparency Key Color Green bits 7-0							
15	14	13	12	11	10	9	8
PIP2 Window Transparency Key Color Blue bits 7-0							
7	6	5	4	3	2	1	0

REG[0624h] PIP2 Window Transparency Key Color Register 1
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PIP2 Window Transparency Key Color Red bits 7-0							
7	6	5	4	3	2	1	0

REG[0624h] bits 7-0 PIP2 Window Transparency Key Color Red bits [7:0]
REG[0620h] bits 15-8 PIP2 Window Transparency Key Color Green bits [7:0]
REG[0620h] bits 7-0 PIP2 Window Transparency Key Color Blue bits [7:0]
These bits specify the PIP2 transparency key color, in RGB 8:8:8 format, that is compared with the PIP2 window pixel data. For RGB 5:6:5 formats, fill the least significant bits as follows.

Table 9-65: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5						→	RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

REG[0628h] Alpha Blend 1 Key Color Register 0
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Alpha Blend 1 Key Color Green bits 7-0							
7	6	5	4	3	2	1	0
Alpha Blend 1 Key Color Blue bits 7-0							

REG[062Ch] Alpha Blend 1 Key Color Register 1
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Alpha Blend 1 Key Color Red bits 7-0							

REG[062Ch] bits 7-0 Alpha Blend 1 Key Color Red bits [7:0]
REG[0628h] bits 15-8 Alpha Blend 1 Key Color Green bits [7:0]
REG[0628h] bits 7-0 Alpha Blend 1 Key Color Blue bits [7:0]
These bits only have an effect when the Alpha Blend 1 Key Color is enabled, REG[0608h] bit 8 = 1b.

For display output port modes for LCD1, LCD2, and TV-Out that use the Main/PIP1/PIP2 windows (REG[0604h] bits 15-12 = 0001b, 0010b, and 0100b), the Alpha Blend 1 Key Color is compared with the Main window pixel data.

For the display output port mode for LCD1 + TV-Out where TV-Out uses the PIP1/PIP2 windows (REG[0604h] bits 15-12 = 1011b), the Alpha Blend 1 Key Color is compared with the PIP1 window pixel data.

For RGB 5:6:5 formats, fill the least significant bits as follows.

Table 9-66: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5						→	RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

REG[0630h] Alpha Blend 2 Key Color Register 0
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Alpha Blend 2 Key Color Green bits 7-0							
7	6	5	4	3	2	1	0
Alpha Blend 2 Key Color Blue bits 7-0							

REG[0634h] Alpha Blend 2 Key Color Register 1
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Alpha Blend 2 Key Color Red bits 7-0							

REG[0634h] bits 7-0 Alpha Blend 2 Key Color Red bits [7:0]
REG[0630h] bits 15-8 Alpha Blend 2 Key Color Green bits [7:0]
REG[0630h] bits 7-0 Alpha Blend 2 Key Color Blue bits [7:0]
These bits only have an effect when the Alpha Blend 2 Key Color is enabled, REG[0608h] bit 9 = 1b.

For display output port modes for LCD1, LCD2, and TV-Out that use the Main/PIP1/PIP2 windows (REG[0604h] bits 15-12 = 0001b, 0010b, and 0100b), the Alpha Blend 2 Key Color is compared with the Main window pixel data.

For the display output port mode for LCD1 + TV-Out where TV-Out uses the PIP1/PIP2 windows (REG[0604h] bits 15-12 = 1011b), the Alpha Blend 2 Key Color is compared with the PIP1 window pixel data.

For RGB 5:6:5 formats, fill the least significant bits as follows.

Table 9-67: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5						→	RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

REG[0638h] Alpha Blend 3 Key Color Register 0
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Alpha Blend 3 Key Color Green bits 7-0							
7	6	5	4	3	2	1	0
Alpha Blend 3 Key Color Blue bits 7-0							

REG[063Ch] Alpha Blend 3 Key Color Register 1
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Alpha Blend 3 Key Color Red bits 7-0							

REG[063Ch] bits 7-0 Alpha Blend 3 Key Color Red bits [7:0]
REG[0638h] bits 15-8 Alpha Blend 3 Key Color Green bits [7:0]
REG[0638h] bits 7-0 Alpha Blend 3 Key Color Blue bits [7:0]
These bits only have an effect when the Alpha Blend 3 Key Color is enabled, REG[0608h] bit 10 = 1b.

For display output port modes for LCD1, LCD2, and TV-Out that use the Main/PIP1/PIP2 windows (REG[0604h] bits 15-12 = 0001b, 0010b, and 0100b), the Alpha Blend 3 Key Color is compared with the Main window pixel data.

For the display output port mode for LCD1 + TV-Out where TV-Out uses the PIP1/PIP2 windows (REG[0604h] bits 15-12 = 1011b), the Alpha Blend 3 Key Color is compared with the PIP1 window pixel data.

For RGB 5:6:5 formats, fill the least significant bits as follows.

Table 9-68: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5						→	RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

REG[0640h] Alpha Blend 4 Key Color Register 0
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Alpha Blend 4 Key Color Green bits 7-0							
7	6	5	4	3	2	1	0
Alpha Blend 4 Key Color Blue bits 7-0							

REG[0644h] Alpha Blend 4 Key Color Register 1
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Alpha Blend 4 Key Color Red bits 7-0							

REG[0644h] bits 7-0 Alpha Blend 4 Key Color Red bits [7:0]
REG[0640h] bits 15-8 Alpha Blend 4 Key Color Green bits [7:0]
REG[0640h] bits 7-0 Alpha Blend 4 Key Color Blue bits [7:0]
These bits only have an effect when the Alpha Blend 4 Key Color is enabled, REG[0608h] bit 11 = 1b.

For display output port modes for LCD1, LCD2, and TV-Out that use the Main/PIP1/PIP2 windows (REG[0604h] bits 15-12 = 0001b, 0010b, and 0100b), the Alpha Blend 4 Key Color is compared with the Main window pixel data.

For the display output port mode for LCD1 + TV-Out where TV-Out uses the PIP1/PIP2 windows (REG[0604h] bits 15-12 = 1011b), the Alpha Blend 4 Key Color is compared with the PIP1 window pixel data.

For RGB 5:6:5 formats, fill the least significant bits as follows.

Table 9-69: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5						→	RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

REG[0648h] Pseudo Color Setting Register
Default = 0000_0020h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a		Pseudo RGB Output Color Format bits 1-0		n/a	Pseudo Color Output Mode bits 2-0		
7	6	5	4	3	2	1	0

bits 5-4 Pseudo RGB Output Color Format bits [1:0]

When a valid Pseudo Color Output Mode is selected (see REG[0648h] bits 2-0), these bits select the RGB format that is output to the LCD panel interface. It is recommended that these bits be set according to the data width of the panel (i.e. 18-bit panel uses RGB 6:6:6).

Table 9-70: Pseudo Output Color Format

REG[0648h] bits 5-4	Pseudo Output Color Format
00b	RGB 4:4:4
01b	RGB 5:6:5
10b	RGB 6:6:6
11b	Reserved

bits 2-0 Pseudo Color Output Mode bits [2:0]

These bits select the method used to convert internal RGB 8:8:8 image data to RGB 4:4:4, RGB 5:6:5, or RGB 6:6:6 data for output to the LCD interface. This function is designed for panels with data widths of less than 24-bit. The output color format is selected using the Pseudo RGB output Color Format bits, REG[0648h] bits 5-4.

The following methods are available.

Table 9-71: Pseudo Mode Selection

REG[0648h] bits 2-0	Pseudo Color Output Mode
000b	Disable (Pas-through)
001b	2x2 Matrix Dither Enable
010b (see Note)	FRM Enable
100b (see Note)	Error Diffusion Enable
101b ~ 111b	Reserved

Note
For displays using parallel/serial LCD interfaces or using the parallel TV-Out interface, these settings are not valid.

REG[064Ch] LUT Address Counter Register (AID)
Default = 0000_0000h: Address auto increment disable — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							LUT Address Counter bit 8
15	14	13	12	11	10	9	8
LUT Address Counter bits 7-0							
7	6	5	4	3	2	1	0

bits 8-0 LUT Address Counter bits [8:0]

These bits specify the address (or index) into the LUT (Look-up Table) which consists of 256 RGB entries.

The RGB entries are written into the LUT using the LUT Data Port (REG[0650h] bits 15-0) as shown in Table 9-72: “LUT Data Mapping,” on page 207. After each RGB data write to the LUT Data Port is completed, the counter is automatically incremented up to a value of 1FFh. When the address counter value reaches 1FFh, the address counter is reset to 00h.

Note

The LUT can only be accessed when the display output port is “All Off” (REG[0604h] bits 15-12 = 0000b) and the S1D13774 is in normal operation mode (REG[002Ch] bits 1-0 = 11b).

REG[0650h] LUT Data Port Register (AID)							
Default = 0000_XXXXh: Address auto increment disable							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
LUT Data Port bits 15-8							
15	14	13	12	11	10	9	8
LUT Data Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 LUT Data Port bits [15:0]

These bits are the access port for setting the LUT RGB data. The LUT can only be accessed when the display output port is “All Off” (REG[0604h] bits 15-12 = 0000b) and the S1D13774 is in normal operation mode (REG[002Ch] bits 1-0 = 11b). The LUT data must be set as follows.

Table 9-72: LUT Data Mapping

Cycle	LUT Address (REG[064Ch] bits 8-0)	REG[0650h] bits 15-8	REG[0650h] bits 7-0
1	000h	Green 0	Red 0
2	001h	n/a	Blue 0
3	002h	Green 1	Red 1
4	003h	n/a	Blue 1
...	...	...	...
511	1FEh	Green 255	Red 255
512	1FFh	n/a	Blue 255

Note

1. When the host interface is configured for indirect interface, the LUT Data Port can be continuously read without re-setting the index address. During burst reads, the register index of REG[0650h] must not be set again between each data read. The register index of REG[0650h] should be set only once after setting the LUT address counter (REG[064Ch]).
2. When the host interface is configured forI2C, the LUT Data Port can be continuously read with multiple register accesses. If reading this register with single accesses, set the LUT Address Counter (REG[064Ch]) before reading the data port.

9.4.15 Main Window Configuration Registers

REG[0680h] Main Window Control Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Main Window Software Reset (WO)	n/a				Main Window eIC Mode Unit Select	Reserved	Main Window eIC Enable
15	14	13	12	11	10	9	8
Main Input Format Select	n/a			Main2 Window Vertical Pixel Doubling Enable	Main2 Window Horizontal Pixel Doubling Enable	Main1 Window Vertical Pixel Doubling Enable	Main1 Window Horizontal Pixel Doubling Enable
7	6	5	4	3	2	1	0

bit 15 Main Window Software Reset (Write Only)
This bit initiates a software reset of the Main window module. A Main Window Software Reset has no effect on other LCDC functions.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initiates a software reset of the Main window module.

Note
After initiating a Main window software reset, a TV-Out Interface Register Update (REG[0600h] bit 15) or a LCD Interface Register Update (REG[0600h] bit 14) must be triggered according to the current active display output port (see REG[0604h] bits 15-12).

bit 10 Main Window eIC Mode Unit Select
This bit selects the eIC mode unit used for processing memory data for the Main window.
When this bit = 0b, line eIC mode is selected.
When this bit = 1b, partial eIC mode is selected.

Note
The setting of this bit affects both the Main1 window and the Main2 window. The eIC mode cannot be independently configured for the Main1 and Main2 windows.

bit 9 Reserved
The default value for this bit is 0b..

bit 8 Main Window eIC Enable
This bit controls the eIC function for the Main window.
When this bit = 0b, the eIC is disabled (bypassed).
When this bit = 1b, the eIC is enabled.

Note
The setting of this bit affects both the Main1 window and the Main2 window. The eIC cannot be independently configured for the Main1 and Main2 windows.

bit 7 Main Window Input Format Select
This bit selects the input format for the Main window.
When this bit = 0b, RGB 5:6:5 format is selected.
When this bit = 1b, RGB 8:8:8 format is selected.

Note
The setting of this bit affects both the Main1 window and the Main2 window. The eIC cannot be independently configured for the Main1 and Main2 windows.

bit 3 Main2 Window Vertical Pixel Doubling Enable
This bit controls pixel doubling for the vertical dimension (height), of the Main2 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling for the vertical dimension (height) is enabled.

bit 2 Main2 Window Horizontal Pixel Doubling Enable
This bit controls pixel doubling for the horizontal dimension (width) of the Main2 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling for the horizontal dimension (width) is enabled.

bit 1 Main1 Window Vertical Pixel Doubling Enable
This bit controls pixel doubling for the vertical dimension (height) of the Main1 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling for the vertical dimension (height) is enabled.

bit 0 Main1 Window Horizontal Pixel Doubling Enable
This bit controls pixel doubling for the horizontal dimension (width) of the Main1 window.
When this bit = 0b, there is no hardware effect.
When this bit = 1b, pixel doubling for the horizontal dimension (width) is enabled.

REG[0684h] Main1 Memory Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Main1 Memory Start Address bits 12-8				
7	6	5	4	3	2	1	0
Main1 Memory Start Address bits 7-0							

bits 12-0 Main1 Memory Start Address bits [12:0]

These bits determine the memory start address for the Main1 window, in 256 byte resolution. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0684h] bits 12-0 = Main1 memory start address in bytes ÷ 256

REG[0688h] Main1 Memory Line Address Offset Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a	Main1 Memory Line Address Offset bits 6-0						

bits6-0 Main1 Memory Line Address Offset bits [6:0]

These bits determine the memory line address offset for the Main1 window, in bytes. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0688h] bits 6-0 = Main1 memory line address offset in bytes ÷ 32

Note

These bits must be set so that the line address offset is 64 byte aligned (bit 0 = 0b).

REG[068Ch] Main1 Memory Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Main1 Memory Vertical Size bits 7-0							

bits 7-0 Main1 Memory Vertical Size bits [7:0]

These bits determine the memory area vertical size for the Main1 window, in 4 line resolution. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[068Ch] bits 7-0 = Main1 memory vertical size in lines ÷ 4 - 1

Note

The memory area vertical size can range from a minimum of 4 lines (REG[068Ch] = 0000h) to a maximum of 1024 lines (REG[068Ch] = 00FFh).

REG[0690h] Main1 Image Horizontal Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main1 Image Horizontal Size bits 9-8	
7	6	5	4	3	2	1	0
Main1 Image Horizontal Size bits 7-0							

bits 9-0 Main1 Image Horizontal Size bits [9:0]

These bits determine the horizontal size of the Main1 window image before pixel doubling is applied (see REG[0680h] bit 0), in pixels. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0690h] bits 9-0 = Main1 image horizontal size in pixels - 1

Note

The Main1 image horizontal size can range from a minimum of 16 pixels (REG[0690h] = 000Fh) to a maximum of 1024 pixels (REG[0690h] = 03FFh).

REG[0694h] Main1 Image Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main1 Image Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
Main1 Image Vertical Size bits 7-0							

bits 9-0 Main1 Image Vertical Size bits [9:0]

These bits determine the vertical size of the Main1 window image before pixel doubling is applied (see REG[0680h] bit 1), in lines. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0694h] bits 9-0 = Main1 image vertical size in lines - 1

Note

The Main1 image vertical size can range from a minimum of 1 line (REG[0694h] = 0000h) to a maximum of 1024 lines (REG[0694h] = 03FFh).

REG[0698h] Main1 Image X Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main1 Image X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main1 Image X Start Position bits 7-0							

bits 9-0 Main1 Image X Start Position bits [9:0]

These bits determine the X start position of the Main1 window image, in pixels. The Main1 image X start position defines the position, in the X direction, where the image starts relative to the left side of the defined image area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0698h] bits 9-0 = Main1 image X start position in pixels

Note

The Main1 image X start position can range from a minimum of 0 pixels (REG[0698h] = 0000h) to a maximum of 1023 pixels (REG[0698h] = 03FFh).

REG[069Ch] Main1 Image Y Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main1 Image Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main1 Image Y Start Position bits 7-0							

bits 9-0 Main1 Image Y Start Position bits [9:0]

These bits determine the Y start position of the Main1 window image, in lines. The Main1 image Y start position defines the position, in the Y direction, where the image starts relative to the top of the defined image area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[069Ch] bits 9-0 = Main1 image Y start position in lines

Note

The Main1 image Y start position can range from a minimum of 0 lines (REG[069Ch] = 0000h) to a maximum of 1023 lines (REG[069Ch] = 03FFh).

REG[06A0h] Main1 Window X Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main1 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main1 Window X Start Position bits 7-0							

bits 9-0 Main1 Window X Start Position bits [9:0]

These bits determine the X start position of the Main1 window in relation to the origin of the panel, in pixels. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

Note

When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the Main1 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[06A4h] Main1 Window Y Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main1 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main1 Window Y Start Position bits 7-0							

bits 9-0 Main1 Window Y Start Position bits [9:0]

These bits determine the Y start position of the Main1 window in relation to the origin of the panel, in lines. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

Note

When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the Main1 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[06A8h] Main2 Memory Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			Main2 Memory Start Address bits 12-8				
7	6	5	4	3	2	1	0
Main2 Memory Start Address bits 7-0							

bits 12-0 Main2 Memory Start Address bits [12:0]

These bits determine the memory start address for the Main2 window, in 256 byte resolution. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06A8h] bits 12-0 = Main2 memory start address in bytes ÷ 256

REG[06ACh] Main2 Memory Line Address Offset Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Main2 Memory Line Address Offset bits 6-0							

bits6-0 Main2 Memory Line Address Offset bits [6:0]
These bits determine the memory line address offset for the Main2 window, in bytes. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06ACh] bits 6-0 = Main2 memory line address offset in bytes ÷ 32

Note
These bits must be set so that the line address offset is 64 byte aligned (bit 0 = 0b).

REG[06B0h] Main2 Memory Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Main2 Memory Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Main2 Memory Vertical Size bits [7:0]
These bits determine the memory area vertical size for the Main2 window, in 4 line resolution. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06B0h] bits 7-0 = Main2 memory vertical size in lines ÷ 4 - 1

Note
The memory area vertical size can range from a minimum of 4 lines (REG[06B0h] = 0000h) to a maximum of 1024 lines (REG[06B0h] = 00FFh).

REG[06B4h] Main2 Image Horizontal Size Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main2 Image Horizontal Size bits 9-8	
7	6	5	4	3	2	1	0
Main2 Image Horizontal Size bits 7-0							

bits 9-0 Main2 Image Horizontal Size bits [9:0]

These bits determine the horizontal size of the Main2 window image before pixel doubling is applied (see REG[0680h] bit 2), in pixels. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06B4h] bits 9-0 = Main2 image horizontal size in pixels - 1

Note

The Main2 image horizontal size can range from a minimum of 16 pixels (REG[06B4h] = 000Fh) to a maximum of 1024 pixels (REG[06B4h] = 03FFh).

REG[06B8h] Main2 Image Vertical Size Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main2 Image Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
Main2 Image Vertical Size bits 7-0							

bits 9-0 Main2 Image Vertical Size bits [9:0]

These bits determine the vertical size of the Main2 window image before pixel doubling is applied (see REG[0680h] bit 3), in lines. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06B8h] bits 9-0 = Main2 image vertical size in lines - 1

Note

The Main2 image vertical size can range from a minimum of 1 line (REG[06B8h] = 0000h) to a maximum of 1024 lines (REG[06B8h] = 03FFh).

REG[06BCh] Main2 Image X Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main2 Image X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main2 Image X Start Position bits 7-0							

bits 9-0 Main2 Image X Start Position bits [9:0]

These bits determine the X start position of the Main2 window image, in pixels. The Main2 image X start position defines the position, in the X direction, where the image starts relative to the left side of the defined image area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06BCh] bits 9-0 = Main2 image X start position in pixels

Note

The Main2 image X start position can range from a minimum of 0 pixels (REG[06BCh] = 0000h) to a maximum of 1023 pixels (REG[06BCh] = 03FFh).

REG[06C0h] Main2 Image Y Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main2 Image Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main2 Image Y Start Position bits 7-0							

bits 9-0 Main2 Image Y Start Position bits [9:0]

These bits determine Y start position of the Main2 window image, in lines. The Main2 image Y start position defines the position, in the Y direction, where the image starts relative to the top of the defined image area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[06C0h] bits 9-0 = Main2 image Y start position in lines

Note

The Main2 image Y start position can range from a minimum of 0 lines (REG[06C0h] = 0000h) to a maximum of 1023 lines (REG[06C0h] = 03FFh).

REG[06C4h] Main2 Window X Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main2 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main2 Window X Start Position bits 7-0							

bits 9-0 Main2 Window X Start Position bits [9:0]

These bits determine the X start position of the Main2 window in relation to the origin of the panel, in pixels. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

Note

When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the Main2 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[06C8h] Main2 Window Y Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						Main2 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
Main2 Window Y Start Position bits 7-0							

bits 9-0 Main2 Window Y Start Position bits [9:0]

These bits determine the Y start position of the Main2 window in relation to the origin of the panel, in lines. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

Note

1. The Main1 and Main2 windows must satisfy the following expression so they do not overlap.
   Main1 Window Y End Position < Main2 Window Y Start Position
2. When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the Main2 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

9.4.16 PIP1 Window Configuration Registers

REG[0700h] PIP1 Control Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
n/a							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PIP1 Software Reset (WO)	PIP1 YUV Data Type Select	n/a		PIP1 eIC Mode Unit Select	n/a	Reserved	PIP1 eIC Enable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PIP1 Input Format Select bits 1-0		PIP1 Double Buffer Status (RO)	PIP1 Buffer Change Trigger Select	PIP1 Double Buffer Mode Enable	n/a		

bit 15 PIP1 Software Reset (Write Only)

This bit initiates a software reset of the PIP1 window module. A PIP1 Software Reset has no effect on other LCDC functions.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initiates a software reset of the PIP1 window module.

Note

After initiating a PIP1 software reset, a TV-Out Interface Register Update (REG[0600h] bit 15) or a LCD Interface Register Update (REG[0600h] bit 14) must be triggered according to the current active display output port (see REG[0604h] bits 15-12).

bit 14 PIP1 YUV Data Type Select

These bits are used for YUV data only (REG[0700h] bits 7-6 = 10b or 11b). This bit selects the YUV data type in memory.

Table 9-73: PIP1 Window YUV Data Type Select

REG[0700h] bit 14	Data Mode	Input Data Range
0b (default)	YUV Offset	$0 \le Y \le 255$ $0 \le U \le 255$ $0 \le V \le 255$
1b	YcbCr Offset	$16 \le Y \le 235$ $16 \le U \le 240$ $16 \le V \le 240$

bit 11 PIP1 eIC Mode Unit Select

This bit selects the eIC Mode unit used for processing memory data for the PIP1 window.
When this bit = 0b, line eIC mode is selected.
When this bit = 1b, partial eIC mode is selected.

bit 9 Reserved

The default value for this bit is 0b..

bit 8

PIP1 eIC Enable
This bit controls the eIC function for the PIP1 window.
When this bit = 0b, the eIC is disabled (bypassed).
When this bit = 1b, the eIC is enabled.

bits 7-6

PIP1 Input Format Select bits [1:0]
These bits select the input format for the PIP1 window.

Table 9-74: PIP1 Input Format Selection

REG[0700h] bits 7-6	PIP1 Input Format
00b	RGB 5:6:5
01b	RGB 8:8:8
10b	YUV 4:2:2
11b	YUV 4:2:0

bit 5

PIP1 Double Buffer Status (Read Only)
When PIP1 double buffer mode is enabled (REG[0700h] bit 3 = 1b), this bit indicates which buffer is being displayed.
When this bit = 0b, Buffer A is being displayed.
When this bit = 1b, Buffer B is being displayed.

bit 4

PIP1 Buffer Change Trigger Select
When PIP1 double buffer mode is enabled (REG[0700h] bit 3 = 1b), this bit selects which write path is used as the trigger for changing the read buffer.
When this bit = 0b, the read buffer changes when 1 frame write to the Main Memory Write Path ends.
When this bit = 1b, the read buffer changes when 1 frame write to the Sub Memory Write Path ends.

bit 3

PIP1 Double Buffer Mode Enable
This bit controls double buffer mode for the PIP1 window which alternately reads from Buffer A and Buffer B. The trigger used for changing the read buffer is when a write of one frame to the selected write path (see REG[0700h] bit 4) ends.
When this bit = 0b, PIP1 double buffer mode is disabled.
When this bit = 1b, PIP1 double buffer mode is enabled.

REG[0704h] PIP1 Window Scaling Mode Register
Default = 0000_020Ah — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
PIP1 Filter Scaling Mode Enable	n/a		Reserved	Reserved	Reserved	Reserved	Reserved
15	14	13	12	11	10	9	8
PIP1 Edge Enhance Enable	PIP1 Edge Enhance Effect bits 2-0			Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0

bit 15 PIP1 Filter Scaling Mode Enable

This bit controls filter scaling for the PIP1 window. For more information on scaling, see Section 12.3.3, “Scaling” on page 304.

When this bit = 0b, filter scaling is disabled (over/down sampling scaling). When this mode is selected, image data can be expanded up to 8x or reduced down to 1/8x.

When this bit = 1b, filter scaling is enabled (Bi-Cubic scaling). When this mode is selected, image data can be expanded up to 8x or reduced down to 1/2x.

Note

When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b and REG[0604h] bits 15-12 = 0100b or 1011b), this bit must be set to 0b.

bit 12 Reserved

The default value for this bit is 0b.

bit 11 Reserved

The default value for this bit is 0b.

bit 10 Reserved

The default value for this bit is 0b.

bit 9 Reserved

The default value for this bit is 1b.

bit 8 Reserved

The default value for this bit is 0b.

bit 7 PIP1 Edge Enhance Enable

This bit controls the edge enhance effect for the PIP1 window. The strength of the edge enhance effect is configured by the PIP1 Edge Enhance Effect bits, REG[0704h] bits 6-4. Note that edge enhance only has an effect on the horizontal direction.

When this bit = 0b, the edge enhance effect is disabled.

When this bit = 1b, the edge enhance effect is enabled.

Note

This bit only has an effect when PIP1 Filter Scaling Mode is enabled, REG[0704h] bit 15 = 1b.

bits 6-4	PIP1 Edge Enhance Effect bits [2:0] When PIP1 Edge Enhance is enabled (REG[0704h] bit 7 = 1b), these bits specify the strength of the edge enhance effect. A value of 001b specifies the weakest edge enhance and a value of 111b specifies the strongest edge enhance. A value of 000b disables the edge enhance effect.
bit 3	Reserved The default value for this bit is 1b.
bit 2	Reserved The default value for this bit is 0b.
bit 1	Reserved The default value for this bit is 1b.
bit 0	Reserved The default value for this bit is 0b.

REG[0708h] PIP1 Window Horizontal Scale Register
Default = 0000_0400h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved			PIP1 Window Horizontal Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP1 Window Horizontal Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP1 Window Horizontal Scale bits [12:0]
These bits determine the horizontal scaling factor for the scalar and must be programmed based on the following formula.

REG[0708h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[0708h] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[0708h] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[0708h] bits 12-0 should be programmed as follows.

REG[0708h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

1. When the PIP1 horizontal scale is set to ZOOM (or scale-up), the PIP1 vertical scale should also be set to ZOOM (or scale-up). When the PIP1 horizontal scale is set to SHRINK (or scale-down), the PIP1 vertical scale should also be set to SHRINK (or scale-down).
2. When Filter Scaling is not enabled (REG[0704h] bit 15 = 0b), the PIP1 image can be scaled-down to 1/8x the original size.
   When Filter Scaling is enabled (REG[0704h] bit 15 = 1b), the PIP1 image can be scaled-down to 1/2x the original size.

REG[070Ch] PIP1 Window Vertical Scale Register
Default = 0000_0400h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved			PIP1 Window Vertical Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP1 Window Vertical Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP1 Window Vertical Scale bits [12:0]
These bits determine the vertical scaling factor for the scalar and must be programmed based on the following formula.

REG[070Ch] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[070Ch] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[070Ch] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[070Ch] bits 12-0 should be programmed as follows.

REG[070Ch] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

1. When the PIP1 horizontal scale is set to ZOOM (or scale-up), the PIP1 vertical scale should also be set to ZOOM (or scale-up). When the PIP1 horizontal scale is set to SHRINK (or scale-down), the PIP1 vertical scale should also be set to SHRINK (or scale-down).
2. When Filter Scaling is not enabled (REG[0704h] bit 15 = 0b), the PIP1 image can be scaled-down to 1/8x the original size.
   When Filter Scaling is enabled (REG[0704h] bit 15 = 1b), the PIP1 image can be scaled-down to 1/2x the original size.

REG[0710h] is Reserved

This register is Reserved and should not be written.

REG[0714h] PIP1 Memory Buffer A RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			PIP1 Memory Buffer A RGB,Y Start Address bits 12-8				
7	6	5	4	3	2	1	0
PIP1 Memory Buffer A RGB,Y Start Address bits 7-0							

bits 12-0 PIP1 Memory Buffer A RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the PIP1 window where RGB or Y data is stored, in 256 byte resolution. When double buffer mode is enabled (REG[0700h] bit 3 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0700h] bit 3 = 0b), this address is always used.

REG[0714h] bits 12-0 = start address in bytes ÷ 256

REG[0718h] PIP1 Memory Buffer A UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			PIP1 Memory Buffer A UV Start Address bits 12-8				
7	6	5	4	3	2	1	0
PIP1 Memory Buffer A UV Start Address bits 7-0							

bits 12-0 PIP1 Memory Buffer A UV Start Address bits [12:0]

These bits determine the memory start address for the PIP1 window where UV data is stored, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0700h] bit 3 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0700h] bit 3 = 0b), this address is always used.

REG[0718h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[071Ch] PIP1 Memory Buffer B RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			PIP1 Memory Buffer B RGB,Y Start Address bits 12-8				
15	14	13	12	11	10	9	8
PIP1 Memory Buffer B RGB,Y Start Address bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 PIP1 Memory Buffer B RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the PIP1 window where RGB or Y data is stored, in 256 byte resolution. When double buffer mode is enabled (REG[0700h] bit 3 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0700h] bit 3 = 0b), this address is not used.

REG[071Ch] bits 12-0 = start address in bytes ÷ 256

REG[0720h] PIP1 Memory Buffer B UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			PIP1 Memory Buffer B UV Start Address bits 12-8				
15	14	13	12	11	10	9	8
PIP1 Memory Buffer B UV Start Address bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 PIP1 Memory Buffer B UV Start Address bits [12:0]

These bits determine the memory start address for PIP1 window where UV data is stored, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0700h] bit 3 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0700h] bit 3 = 0b), this address is not used.

REG[0720h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[0724h] PIP1 Memory Line Address Offset Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved							n/a
15	14	13	12	11	10	9	8
n/a	PIP1 Memory Line Address Offset bits 6-0						
7	6	5	4	3	2	1	0

bits 15-9 Reserved
The default value for these bits is 000_0000b.

bits 6-0 PIP1 Memory Line Address Offset bits [6:0]
These bits determine the memory address offset for the PIP1 window, in bytes. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0724h] bits 6-0 = line address offset in bytes ÷ 32

Note
These bits must be set so that the line address offset is 64 byte aligned (bit 0 = 0b).

REG[0728h] PIP1 Memory Vertical Size Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PIP1 Memory Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PIP1 Memory Vertical Size bits [7:0]
These bits determine the memory area vertical size for the PIP1 window, in 4 line resolution. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0728h] bits 7-0 = memory vertical size in lines ÷ 4 - 1

Note
The memory area vertical size can range from a minimum of 4 lines (REG[0728h] = 0000h) to a maximum of 1024 lines (REG[0728h] = 00FFh).

REG[072Ch] PIP1 Image Horizontal Size Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Image Horizontal Size bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Image Horizontal Size bits 7-0							

bits 9-0 PIP1 Image Horizontal Size bits [9:0]

These bits determine the horizontal size of the PIP1 image before scaling is applied (see REG[0708h]), in pixels. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[072Ch] bits 9-0 = image horizontal size in pixels - 1

Note

1. The image horizontal size can range from a minimum of 16 pixels (REG[072Ch] = 000Fh) to a maximum of 864 pixels (REG[072Ch] = 037Fh).
2. For YUV 4:2:2, the image horizontal size must be an even number.

REG[0730h] PIP1 Image Vertical Size Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Image Vertical Size bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Image Vertical Size bits 7-0							

bits 9-0 PIP1 Image Vertical Size bits [9:0]

These bits determine the vertical size of the PIP1 image before scaling is applied (see REG[070Ch]), in lines. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0730h] bits 9-0 = image vertical size in lines - 1

Note

The image vertical size can range from a minimum of 1 line (REG[0730h] = 0000h) to a maximum of 1024 lines (REG[0730h] = 03FFh).

REG[0734h] PIP1 Image X Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Image X Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Image X Start Position bits 7-0							

bits 9-0 PIP1 Image X Start Position bits [9:0]

These bits determine the X start position of the PIP1 window image, in pixels. The image X start position defines the position, in the X direction, where the image starts relative to the left side of the defined memory area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0734h] bits 9-0 = image X start position in pixels

Note

1. The image X start position can range from a minimum of 0 pixels (REG[0734h] = 0000h) to a maximum of 895 pixels (REG[0734h] = 037Fh).
2. For YUV 4:2:2, the image X start position must be set to an even number.

REG[0738h] PIP1 Image Y Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Image Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Image Y Start Position bits 7-0							

bits 9-0 PIP1 Image Y Start Position bits [9:0]

These bits determine the Y start position of the PIP1 window image, in lines. The image Y start position defines the position, in the Y direction, where the image starts relative to the top of the defined memory area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0738h] bits 9-0 = image Y start position in lines

Note

The image Y start position can range from a minimum of 0 lines (REG[0738h] = 0000h) to a maximum of 1023 lines (REG[0738h] = 03FFh).

REG[073Ch] PIP1 Window X Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Window X Start Position bits 7-0							

bits 9-0 PIP1 Window X Start Position bits [9:0]
These bits determine the X start position of the PIP1 window in relation to the origin of the panel, in pixels.

Note

1. The PIP1 window X size (REG[0744h] - REG[073Ch] + 1) must be the same as the horizontal size after scaling.
2. These bits must be programmed such that the following formula is valid.
   REG[0744h] bits 9-0 - REG[073Ch] bits 9-0 ≥ 15
3. When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the PIP1 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[0740h] PIP1 Window Y Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Window Y Start Position bits 7-0							

bits 9-0 PIP1 Window Y Start Position bits [9:0]
These bits determine the Y start position of the PIP1 window in relation to the origin of the panel, in pixels.

Note

1. The PIP1 window Y size (REG[0748h] - REG[0740h] + 1) must be the same as the vertical size after scaling.
2. This register must be programmed such that the following formula is valid.
   REG[0748h] bits 9-0 - REG[0740h] bits 9-0 ≥ 4
3. When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the PIP1 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[0744h] PIP1 Window X End Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Window X End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Window X End Position bits 7-0							

bits 9-0 PIP1 Window X End Position bits [9:0]
These bits determine the X end position of the PIP1 window in relation to the origin of the panel, in pixels.

Note

1. The PIP1 window X size (REG[0744h] - REG[073Ch] + 1) must be the same as the horizontal size after scaling.
2. These bits must be programmed such that the following formula is valid.
   REG[0744h] bits 9-0 - REG[073Ch] bits 9-0 ≥ 15

REG[0748h] PIP1 Window Y End Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP1 Window Y End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP1 Window Y End Position bits 7-0							

bits 9-0 PIP1 Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP1 window in relation to the origin of the panel, in pixels.

Note

1. The PIP1 window Y size (REG[0748h] - REG[0740h] + 1) must be the same as the vertical size after scaling.
2. This register must be programmed such that the following formula is valid.
   REG[0748h] bits 9-0 - REG[0740h] bits 9-0 ≥ 4

REG[074Ch] PIP1 Window Scaler Port Address Counter Control Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	PIP1 Port Address Counter bits 6-0 (RO)						
15	14	13	12	11	10	9	8
n/a			PIP1 Filter Coefficient Select	n/a		Reserved	PIP1 Port Address Counter Reset (WO)
7	6	5	4	3	2	1	0

bits 14-8 PIP1 Port Address Counter bits [6:0] (Read Only)
These bits indicate the address of the scaler filter coefficient. After each write to the PIP1 Coefficient Table Access Port (REG[0750h] bits 7-0) is completed, this counter is automatically incremented up to a maximum value of 3Fh. When the port address counter value reaches 3Fh, it must be manually reset to 00h. This counter is not incremented when the PIP1 Coefficient Table Access Port is read.

bit 4 PIP1 Filter Coefficient Select
This bit selects which scaler filter coefficients (Horizontal Filter or Vertical Filter) are accessed through the PIP1 Coefficient Table Access Port, REG[0750h] bits 7-0.
When this bit = 0b, the PIP1 scaler horizontal filter coefficient is selected.
When this bit = 1b, the PIP1 scaler vertical filter coefficient is selected.

bit 1 Reserved
The default value for this bit is 0b.

bit 0 PIP1 Port Address Counter Reset (Write Only)
This bit resets the PIP1 Port Address Counter, REG[074Ch] bits 14-8.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit resets the PIP1 Port Address Counter.

REG[0750h] PIP1 Scaler Coefficient Table Access Port Register (AID)							
Default = 0000_0000h: Address auto increment disable							Write Only
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PIP1 Coefficient Table Access Port bits 7-0 (WO)							
7	6	5	4	3	2	1	0

bits 7-0 PIP1 Coefficient Table Access Port bits [7:0] (Write Only)

These bits are the access port for the PIP1 scaler horizontal/vertical filter coefficient tables. The PIP1 Filter Coefficient Select bit is used to select whether the horizontal or vertical filter coefficient table is accessed (see REG[074Ch] bit 4). The filter coefficients must be set before the scaler filter operation starts.

The Scaler horizontal filter and vertical filter coefficients should be set according to the values shown in the following tables. The column used varies based on the scaling rates which are set individually for the horizontal filter and the vertical filter.

Table 9-75: PIP1 Filter Horizontal Coefficient Examples (REG[074Ch] bit 4 = 0b)

Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient
00h	00h	10h	00h	20h	00h	30h	00h
01h	FDh	11h	FDh	21h	FDh	31h	FFh
02h	FBh	12h	FBh	22h	FBh	32h	FEh
03h	F8h	13h	F8h	23h	F8h	33h	FCh
04h	F7h	14h	F7h	24h	F7h	34h	FCh
05h	F7h	15h	F7h	25h	F7h	35h	FCh
06h	FAh	16h	FAh	26h	FAh	36h	FDh
07h	00h	17h	00h	27h	00h	37h	00h
08h	08h	18h	08h	28h	08h	38h	05h
09h	13h	19h	13h	29h	13h	39h	0Eh
0Ah	1Dh	1Ah	1Dh	2Ah	1Dh	3Ah	18h
0Bh	28h	1Bh	28h	2Bh	28h	3Bh	24h
0Ch	31h	1Ch	31h	2Ch	31h	3Ch	2Eh
0Dh	39h	1Dh	39h	2Dh	39h	3Dh	37h
0Eh	3Eh	1Eh	3Eh	2Eh	3Eh	3Eh	3Dh
0Fh	40h	1Fh	40h	2Fh	40h	3Fh	40h

Table 9-76: PIP1 Filter Vertical Coefficient Examples (REG[074Ch] bit 4 = 1b)

Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient
00h	08h	10h	08h	20h	Do not set	30h	Do not set
01h	10h	11h	10h	21h		31h	
02h	18h	12h	18h	22h		32h	
03h	20h	13h	20h	23h		33h	
04h	28h	14h	28h	24h		34h	
05h	30h	15h	30h	25h		35h	
06h	38h	16h	38h	26h		36h	
07h	40h	17h	40h	27h		37h	
08h	08h	18h	08h	28h		38h	
09h	10h	19h	10h	29h		39h	
0Ah	18h	1Ah	18h	2Ah		3Ah	
0Bh	20h	1Bh	20h	2Bh		3Bh	
0Ch	28h	1Ch	28h	2Ch		3Ch	
0Dh	30h	1Dh	30h	2Dh		3Dh	
0Eh	38h	1Eh	38h	2Eh		3Eh	
0Fh	40h	1Fh	40h	2Fh		3Fh	

9.4.17 PIP2 Window Configuration Register

REG[0800h] PIP2 Window Control Register Default = 0000_0000h							Read/Write
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
PIP2 Software Reset (WO)	PIP2 YUV Data Type Select	n/a		PIP2 eIC Unit Select	n/a	Reserved	PIP2 eIC Enable
15	14	13	12	11	10	9	8
PIP2 Input Format Select bits 1-0		PIP2 Double Buffer Status (RO)	PIP2 Buffer Change Trigger Select	PIP2 Double Buffer Mode Enable	PIP2 Wide Scaling Mode Select bits 2-0		
7	6	5	4	3	2	1	0

bit 15 PIP2 Software Reset (Write Only)
This bit initiates a software reset of the PIP2 window module. A PIP2 Software Reset has no effect on other LCDC functions.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initiates a software reset of the PIP2 window module.

Note
After initiating a PIP2 software reset, a TV-Out Interface Register Update (REG[0600h] bit 15) or a LCD Interface Register Update (REG[0600h] bit 14) must be triggered according to the current active display output port (see REG[0604h] bits 15-12).

bit 14 PIP2 YUV Data Type Select
These bits are used for YUV data only (REG[0800h] bits 7-6 = 10b or 11b). This bit selects the YUV data type in memory.

Table 9-77: PIP2 YUV Data Type Select

REG[0800h] bit 14	Data Mode	Input Data Range
0b (default)	YUV Offset	$0 \le Y \le 255$ $0 \le U \le 255$ $0 \le V \le 255$
1b	YcbCr Offset	$16 \le Y \le 235$ $16 \le U \le 240$ $16 \le V \le 240$

bit 11 PIP2 eIC Unit Select
This bit selects the eIC unit used for processing memory data for the PIP2 window.
When this bit = 0b, line eIC mode is selected.
When this bit = 1b, partial eIC mode is selected.

bit 9 Reserved
The default value for this bit is 0b.

bit 8 PIP2 eIC Enable
This bit controls the eIC function for the PIP2 window.
When this bit = 0b, the eIC is disabled (bypassed).
When this bit = 1b, the eIC is enabled.

bits 7-6 PIP2 Input Format Select bits [1:0]
These bits select the input format for the PIP2 window.

Table 9-78: PIP2 Input Format Selection

REG[0800h] bits 7-6	Format
00b	RGB 5:6:5
01b	RGB 8:8:8
10b	YUV 4:2:2
11b	YUV 4:2:0

bit 5 PIP2 Double Buffer Status (Read Only)
When PIP2 double buffer mode is enabled (REG[0800h] bit 3 = 1b), this bit indicates which buffer is being displayed.
When this bit = 0b, Buffer A is being displayed.
When this bit = 1b, Buffer B is being displayed.

bit 4 PIP2 Buffer Change Trigger Select
When PIP2 double buffer mode is enabled (REG[0800h] bit 3 = 1b), this bit selects which write path is used as the trigger for changing the read buffer.
When this bit = 0b, the read buffer changes when 1 frame write to the Main Memory Write Path ends.
When this bit = 1b, the read buffer changes when 1 frame write to the Sub Memory Write Path ends.

bit 3 PIP2 Double Buffer Mode Enable
This bit controls double buffer mode for the PIP2 window which alternately reads from Buffer A and Buffer B. The trigger used for changing the read buffer is when a write of one frame to the selected write path (see REG[0800h] bit 4) ends.
When this bit = 0b, PIP2 double buffer mode is disabled.
When this bit = 1b, PIP2 double buffer mode is enabled.

bits 2-0 PIP2 Wide Scaling Mode Select bits [2:0]

These bits select the wide scaling mode (or Panorama) for the PIP2 window. The following table summarizes the possible settings. For further information on wide scaling mode, see Section 12.6, “PIP2 Panorama Scaling” on page 327.

Table 9-79: PIP2 Wide Scaling Mode Selection

REG[0804h] bit 15	REG[0800h] bits 2-0	Scaling Mode		Non Interlace	Interlace (Note 1)
0b	000b	Non Filter Mode	Normal Scaling	Yes	Yes
	001b		Vertical Partial Panorama	No	No
	010b		Vertical Linear Panorama	No	No
	011b		Horizontal Partial Panorama	Yes (Note 2)	Yes (Note 2)
	100b		Horizontal Linear Panorama	Yes (Note 2)	Yes (Note 2)
	101b ~ 111b		Reserved	—	—
1b	000b	Filter Mode	Normal Scaling	Yes	No
	001b		Vertical Partial Panorama	Yes	No
	010b		Vertical Linear Panorama	Yes	No
	011b		Horizontal Partial Panorama	Yes	No
	100b		Horizontal Linear Panorama	Yes	No
	101b - 111b		Reserved	—	—

Note

1. When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b and REG[0604h] bits 15-12 = 0100b or 1011b), the image data is output in interlace mode.
2. For horizontal partial and linear panorama, the PIP2 Window Horizontal Scale bits must be set less than 400h.

   REG[0808h] < 400h

REG[0804h] PIP2 Window Scaling Mode Register
Default = 0000_020Ah Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
PIP2 Filter Scaling Mode Enable	n/a		Reserved				Reserved
15	14	13	12	11	10	9	8
PIP2 Edge Enhance Enable	PIP2 Edge Enhance Effect bits 2-0			Reserved			
7	6	5	4	3	2	1	0

bit 15 PIP2 Filter Scaling Mode Enable

This bit controls filter scaling for the PIP1 window. For more information on scaling, see Section 12.3.3, “Scaling” on page 304.

When this bit = 0b, filter scaling is disabled (over/down sampling scaling). When this mode is selected, image data can be expanded up to 8x or reduced down to 1/8x.

When this bit = 1b, filter scaling is enabled (Bi-Cubic scaling). When this mode is selected, image data can be expanded up to 8x or reduced down to 1/2x.

Note

When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b and REG[0604h] bits 15-12 = 0100b or 1011b), this bit must be set to 0b.

bits 12-9 Reserved

The default value for these bits is 0000b.

bit 8 Reserved

The default value for this bit is 0b.

bit 7 PIP2 Edge Enhance Enable

This bit controls the edge enhance effect for the PIP2 window. The strength of the edge enhance effect is configured by the PIP2 Edge Enhance Effect bits, REG[0804h] bits 6-4. Note that edge enhance only has an effect on the horizontal direction.

When this bit = 0b, the edge enhance effect is disabled.

When this bit = 1b, the edge enhance effect is enabled.

Note

This bit only has an effect when PIP2 Filter Scaling Mode is enabled, REG[0804h] bit 15 = 1b.

bits 6-4 PIP2 Edge Enhance Effect bits [2:0]

When the PIP2 Edge Enhance is enabled (REG[0804h] bit 7 = 1b), these bits specify the strength of the edge enhance effect. A value of 001b specifies the weakest edge enhance and a value of 111b specifies the strongest edge enhance. A value of 000b disables the edge enhance effect.

bits 3-0 Reserved

The default value for these bits is 1010b.

REG[0808h] PIP2 Window Horizontal Scale Register
Default = 0000_0400h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Reserved			PIP2 Window Horizontal Scale bits 12-8				
7	6	5	4	3	2	1	0
PIP2 Window Horizontal Scale bits 7-0							

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP2 Window Horizontal Scale bits [12:0]
These bits determine the horizontal scaling factor for the scalar and must be programmed based on the following formula.

REG[0808h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[0808h] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[0808h] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[0808h] bits 12-0 should be programmed as follows.

REG[0808h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

1. When the PIP2 horizontal scale is set to ZOOM (or scale-up), the PIP2 vertical scale should also be set to ZOOM (or scale-up). When the PIP2 horizontal scale is set to SHRINK (or scale-down), the PIP2 vertical scale should also be set to SHRINK (or scale-down).
2. When Filter Scaling is not enabled (REG[0804h] bit 15 = 0b), the PIP2 image can be scaled-down to 1/8x the original size.
   When Filter Scaling is enabled (REG[0804h] bit 15 = 1b), the PIP2 image can be scaled-down to 1/2x the original size.

REG[080Ch] PIP2 Window Vertical Scale Register
Default = 0000_0400h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
Reserved			PIP2 Window Vertical Scale bits 12-8				
15	14	13	12	11	10	9	8
PIP2 Window Vertical Scale bits 7-0							
7	6	5	4	3	2	1	0

bits 15-13 Reserved
The default value for these bits is 000b.

bits 12-0 PIP2 Window Vertical Scale bits [12:0]
These bits determine the vertical scaling factor for the scalar and must be programmed based on the following formula.

REG[080Ch] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

The fractional point is to the right of bit 10. If the scaling mode is ZOOM (Scaled up), REG[080Ch] bits 12-10 should equal zero. If the scaling mode is SHRINK (Scaled down), REG[080Ch] bits 12-10 should be non-zero.

Example: For a scaling ratio of 3.51 (Zoom case), REG[080Ch] bits 12-0 should be programmed as follows.

REG[080Ch] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

Note

1. When the PIP2 horizontal scale is set to ZOOM (or scale-up), the PIP2 vertical scale should also be set to ZOOM (or scale-up). When the PIP2 horizontal scale is set to SHRINK (or scale-down), the PIP2 vertical scale should also be set to SHRINK (or scale-down).
2. When Filter Scaling is not enabled (REG[0804h] bit 15 = 0b), the PIP2 image can be scaled-down to 1/8x the original size.
   When Filter Scaling is enabled (REG[0804h] bit 15 = 1b), the PIP2 image can be scaled-down to 1/2x the original size.

REG[0810h] is Reserved

This register is Reserved and should not be written.

REG[0814h] PIP2 Memory Buffer A RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			PIP2 Memory Buffer A RGB,Y Start Address bits 12-8				
7	6	5	4	3	2	1	0
PIP2 Memory Buffer A RGB,Y Start Address bits 7-0							

bits 12-0 PIP2 Memory Buffer A RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the PIP2 window where RGB or Y data is stored, in 256 byte resolution. When double buffer mode is enabled (REG[0800h] bit 3 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0800h] bit 3 = 0b), this address is always used.

REG[0814h] bits 12-0 = start address in bytes ÷ 256

REG[0818h] PIP2 Memory Buffer A UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			PIP2 Memory Buffer A UV Start Address bits 12-8				
7	6	5	4	3	2	1	0
PIP2 Memory Buffer A UV Start Address bits 7-0							

bits 12-0 PIP2 Memory Buffer A UV Start Address bits [12:0]

These bits determine the memory start address for the PIP2 window where UV data is stored, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0800h] bit 3 = 1b), this address is the memory start address for Buffer A. When double buffer mode is disabled (REG[0800h] bit 3 = 0b), this address is always used.

REG[0818h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[081Ch] PIP2 Memory Buffer B RGB,Y Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			PIP2 Memory Buffer B RGB,Y Start Address bits 12-8				
15	14	13	12	11	10	9	8
PIP2 Memory Buffer B RGB,Y Start Address bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 PIP2 Memory Buffer B RGB,Y Start Address bits [12:0]

These bits determine the memory start address for the PIP2 window where RGB or Y data is stored, in 256 byte resolution. When double buffer mode is enabled (REG[0800h] bit 3 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0800h] bit 3 = 0b), this address is not used.

REG[081Ch] bits 12-0 = start address in bytes ÷ 256

REG[0820h] PIP2 Memory Buffer B UV Start Address Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			PIP2 Memory Buffer B UV Start Address bits 12-8				
15	14	13	12	11	10	9	8
PIP2 Memory Buffer B UV Start Address bits 7-0							
7	6	5	4	3	2	1	0

bits 12-0 PIP2 Memory Buffer B UV Start Address bits [12:0]

These bits determine the memory start address for the PIP2 window where UV data is stored, in 256 byte resolution. When RGB data is selected, these bits are not used. When double buffer mode is enabled (REG[0800h] bit 3 = 1b), this address is the memory start address for Buffer B. When double buffer mode is disabled (REG[0800h] bit 3 = 0b), this address is not used.

REG[0820h] bits 12-0 = (RGB,Y start address + line address offset x memory vertical size) ÷ 256

REG[0824h] PIP2 Memory Line Address Offset Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
Reserved							n/a
7	6	5	4	3	2	1	0
n/a	PIP2 Memory Line Address Offset bits 6-0						

bits 15-9 Reserved
The default value for these bits is 000_0000b.

bits 6-0 PIP2 Memory Line Address Offset bits [6:0]
These bits determine the memory address offset for the PIP2 window, in bytes. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0824h] bits 6-0 = line address offset in bytes ÷ 32

Note
These bits must be set so that the line address offset is 64 byte aligned (bit 0 = 0b).

REG[0828h] PIP2 Memory Vertical Size Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PIP2 Memory Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PIP2 Memory Vertical Size bits [7:0]
These bits determine the memory area vertical size for the PIP2 window, in 4 line resolution. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0828h] bits 7-0 = memory vertical size in lines ÷ 4 - 1

Note
The memory area vertical size can range from a minimum of 4 lines (REG[0828h] = 0000h) to a maximum of 1024 lines (REG[0828h] = 00FFh).

REG[082Ch] PIP2 Image Horizontal Size Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Image Horizontal Size bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Image Horizontal Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Image Horizontal Size bits [9:0]

These bits determine the horizontal size of the PIP2 image before scaling is applied (see REG[0808h]), in pixels. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[082Ch] bits 9-0 = image horizontal size in pixels - 1

Note

1. The image horizontal size can range from a minimum of 16 pixels (REG[082Ch] = 000Fh) to a maximum of 864 (REG[082Ch] = 037Fh).
2. For YUV 4:2:2, the image horizontal size must be an even number.

REG[0830h] PIP2 Image Vertical Size Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Image Vertical Size bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Image Vertical Size bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Image Vertical Size bits [9:0]

These bits determine the vertical size of the PIP2 image before scaling is applied (see REG[080Ch], in lines. For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0830h] bits 9-0 = image vertical size in lines - 1

Note

The image vertical size can range from a minimum of 1 line (REG[0830h] = 0000h) to a maximum of 1024 (REG[0830h] = 03FFh).

REG[0834h] PIP2 Image X Start Position Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Image X Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Image X Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Image X Start Position bits [9:0]

These bits determine the X start position of the PIP2 window image, in pixels. The image X start position defines the position, in the X direction, where the image starts relative to the left side of the defined memory area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294..

REG[0834h] bits 9-0 = image X start position in pixels

Note

1. The image X start position can range from a minimum of 0 pixels (REG[0834h] = 0000h) to a maximum of 895 pixels (REG[0834h] = 037Fh).
2. For YUV 4:2:2, the image X start position must be set to an even number.

REG[0838h] PIP2 Image Y Start Position Register
Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Image Y Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Image Y Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Image Y Start Position bits [9:0]

These bits determine the Y start position of the PIP2 window image, in lines. The image Y start position defines the position, in the Y direction, where the image starts relative to the top of the defined memory area (position 0). For further information on displaying image data from memory, see Section 12.1, “Configuring the Display Paths” on page 294.

REG[0838h] bits 9-0 = image Y start position in lines

Note

The image Y start position can range from a minimum of 0 lines (REG[0838h] = 0000h) to a maximum of 1023 lines (REG[0838h] = 03FFh).

REG[083Ch] PIP2 Window X Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP2 Window X Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window X Start Position bits 7-0							

bits 9-0 PIP2 Window X Start Position bits [9:0]
These bits determine the X start position of the PIP2 window in relation to the origin of the panel, in pixels.

Note

1. The PIP2 window X size (REG[0844h] - REG[083Ch] + 1) must be the same as the horizontal size after scaling.
2. These bits must be programmed such that the following formula is valid.
   REG[0844h] bits 9-0 - REG[083Ch] bits 9-0 ≥ 15
3. When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the PIP1 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[0840h] PIP2 Window Y Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP2 Window Y Start Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window Y Start Position bits 7-0							

bits 9-0 PIP2 Window Y Start Position bits [9:0]
These bits determine the Y start position of the PIP2 window in relation to the origin of the panel, in pixels.

Note

1. The PIP2 window Y size (REG[0848h] - REG[0840h] + 1) must be the same as the vertical size after scaling.
2. This register must be programmed such that the following formula is valid.
   REG[0848h] bits 9-0 - REG[0840h] bits 9-0 ≥ 4
3. When the active display output port is set for LCD2 (REG[0604h] bits 15-12 = 0010b) or parallel TV-Out (REG[0604h] bits 15-12 = 0100b or 1011b **and** REG[0200h] bits 1-0 = 10b), the PIP1 window X,Y start position must not be set to 1~10,0. For example, a position of 5,0 is not allowed.

REG[0844h] PIP2 Window X End Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP2 Window X End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window X End Position bits 7-0							

bits 9-0 PIP2 Window X End Position bits [9:0]
These bits determine the X end position of the PIP2 window in relation to the origin of the panel, in pixels.

Note

1. The PIP2 window X size (REG[0844h] - REG[083Ch] + 1) must be the same as the horizontal size after scaling.
2. This register must be programmed such that the following formula is valid.
   REG[0844h] bits 9-0 - REG[083Ch] bits 9-0 ≥ 15

REG[0848h] PIP2 Window Y End Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a						PIP2 Window Y End Position bits 9-8	
7	6	5	4	3	2	1	0
PIP2 Window Y End Position bits 7-0							

bits 9-0 PIP2 Window Y End Position bits [9:0]
These bits determine the Y end position of the PIP2 window in relation to the origin of the panel, in pixels.

Note

1. The PIP2 window Y size (REG[0848h] - REG[0840h] + 1) must be the same as the vertical size after scaling.
2. This register must be programmed such that the following formula is valid.
   REG[0848h] bits 9-0 - REG[0840h] bits 9-0 ≥ 4

The following Panorama registers are used for both Vertical and Horizontal Panorama (see REG[0800h] bits 2-0).

REG[084Ch] PIP2 Panorama Area A Scale Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			PIP2 Panorama Area A Scale bits 12-8				
7	6	5	4	3	2	1	0
PIP2 Panorama Area A Scale bits 7-0							

bits 12-0 PIP2 Panorama Area A Scale bits [12:0]

These bits determine the scaling factor for the PIP2 scalar and must be programmed based on the following formula.

REG[084Ch] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

Note

When linear panorama scaling mode is selected (see REG[0800h] bits 2-0), the initial scale value should be specified in this register.

REG[0850h] PIP2 Panorama Area B Scale Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a			PIP2 Panorama Area B Scale bits 12-8				
7	6	5	4	3	2	1	0
PIP2 Panorama Area B Scale bits 7-0							

bits 12-0 PIP2 Panorama Area B Scale bits [12:0]

These bits determine the scaling factor for the PIP2 scalar and must be programmed based on the following formula.

REG[0850h] bits 12-0 = 1024 x (1 ÷ Scaling Ratio)

Note

When linear panorama scaling mode is selected (see REG[0800h] bits 2-0), these bits have no effect.

REG[0854h] PIP2 Panorama Area 1 Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Panorama Area 1 Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Panorama Area 1 Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Panorama Area 1 Start Position bits [9:0]

These bits specify the PIP2 Panorama Area 1 start position, in pixels.

REG[0854h] bits 9-0 = PIP2 panorama area 1 start position in pixels

Note

When linear panorama scaling mode is selected (see REG[0800h] bits 2-0), the normal scaling area start position should be specified in this register in pixels.

REG[0858h] PIP2 Panorama Area 2 Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Panorama Area 2 Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Panorama Area 2 Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Panorama Area 2 Start Position bits [9:0]

These bits specify the PIP2 Panorama Area 2 start position, in pixels.

REG[0858h] bits 9-0 = PIP2 panorama area 2 start position in pixels

Note

When linear panorama scaling mode is selected (see REG[0800h] bits 2-0), the panorama area 2 start pixel should be specified in this register in pixels.

REG[085Ch] PIP2 Panorama Area 3 Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Panorama Area 3 Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Panorama Area 3 Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Panorama Area 3 Start Position bits [9:0]

These bits specify the PIP2 Panorama Area 3 start position, in pixels.

REG[085Ch] bits 9-0 = PIP2 panorama area 3 start position in pixels

Note

When linear panorama scaling mode is selected (see REG[0800h] bits 2-0), these bits have no effect.

REG[0860h] PIP2 Panorama Area 4 Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						PIP2 Panorama Area 4 Start Position bits 9-8	
15	14	13	12	11	10	9	8
PIP2 Panorama Area 4 Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 PIP2 Panorama Area 4 Start Position bits [9:0]

These bits specify the PIP2 Panorama Area 4 start position, in pixels.

REG[0860h] bits 9-0 = PIP2 Panorama Area 4 Start position in pixels

Note

When linear panorama scaling mode is selected (see REG[0800h] bits 2-0), these bits have no effect.

REG[0864h] PIP2 Linear Panorama Area Delta Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a		PIP2 Linear Panorama Area Delta bits 13-8					
15	14	13	12	11	10	9	8
PIP2 Linear Panorama Area Delta bits 7-0							
7	6	5	4	3	2	1	0

bits 13- 0 PIP2 Linear Panorama Area Delta bits [13:0]

These bits determine the linear panorama mode Horizontal/vertical scaling factor delta for the scaler and must be programmed based on the following formula.

(REG[0864h] bits 13-0) = 256 x Δscale

Where:

For Horizontal Panorama mode:

Δscale = (REG[0808h] - REG[084Ch]) ÷ (REG[0854h] - 1)

For Vertical Panorama mode:

Δscale = (REG[080Ch] - REG[084Ch]) ÷ (REG[0854h] - 1)

Note

These bits only have an effect when Linear Panorama Scaling Mode is selected, REG[0800h] bits 2-0 = 010b or 100b.

REG[0868h] PIP2 Window Scaler Port Address Counter Control Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a	PIP2 Port Address Counter bits 6-0 (RO)						
15	14	13	12	11	10	9	8
n/a			PIP2 Filter Coefficient Select	n/a		Reserved	PIP2 Port Address Counter Reset (WO)
7	6	5	4	3	2	1	0

bits 14-8 PIP2 Port Address Counter bits [6:0] (Read Only)
These bits indicate the address of the scaler filter coefficient. After each write to the PIP2 Coefficient Table Access Port (REG[086Ch] bits 7-0) is completed, this counter is automatically incremented up to a maximum value of 3Fh. When the port address counter value reaches 3Fh, it must be manually reset to 00h. This counter is not incremented when the PIP2 Coefficient Table Access Port is read.

bit 4 PIP2 Filter Coefficient Select
This bit selects which scaler filter coefficients (Horizontal Filter or Vertical Filter) are accessed through the PIP2 Coefficient Table Access Port, REG[086Ch] bits 7-0.
When this bit = 0b, the PIP2 scalar horizontal filter coefficient is selected.
When this bit = 1b, the PIP2 scalar vertical filter coefficient is selected.

bit 1 Reserved
The default value for this bit is 0b.

bit 0 PIP2 Port Address Counter Reset (Write Only)
This bit resets the PIP2 Port Address Counter, REG[0868h] bits 14-8.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit resets the PIP2 Port Address Counter.

REG[086Ch] PIP2 Window Scaler Coefficient Table Access Port Register (AID)							
Default = 0000_0000h: Address auto increment disable							Write Only
n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
PIP2 Coefficient Table Access Port bits 7-0 (WO))							
7	6	5	4	3	2	1	0

bits 7-0 PIP2 Coefficient Table Access Port bits [7:0] (Write Only)

These bits are the access port for the PIP2 scaler horizontal/vertical filter coefficient tables. The PIP2 Filter Coefficient Select bit is used to select whether the horizontal or vertical filter coefficient table is accessed (see REG[0868h] bit 4). The filter coefficients must be set before the scaler filter operation starts.

The Scaler horizontal filter and vertical filter coefficients should be set according to the values shown in the following tables. The column used varies based on the scaling rates which are set individually for the horizontal filter and the vertical filter.

Table 9-80: PIP2 Filter Horizontal Coefficient Examples (REG[0868h] bit 4 = 0b)

Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient
00h	00h	10h	00h	20h	00h	30h	00h
01h	FDh	11h	FDh	21h	FDh	31h	FFh
02h	FBh	12h	FBh	22h	FBh	32h	FEh
03h	F8h	13h	F8h	23h	F8h	33h	FCh
04h	F7h	14h	F7h	24h	F7h	34h	FCh
05h	F7h	15h	F7h	25h	F7h	35h	FCh
06h	FAh	16h	FAh	26h	FAh	36h	FDh
07h	00h	17h	00h	27h	00h	37h	00h
08h	08h	18h	08h	28h	08h	38h	05h
09h	13h	19h	13h	29h	13h	39h	0Eh
0Ah	1Dh	1Ah	1Dh	2Ah	1Dh	3Ah	18h
0Bh	28h	1Bh	28h	2Bh	28h	3Bh	24h
0Ch	31h	1Ch	31h	2Ch	31h	3Ch	2Eh
0Dh	39h	1Dh	39h	2Dh	39h	3Dh	37h
0Eh	3Eh	1Eh	3Eh	2Eh	3Eh	3Eh	3Dh
0Fh	40h	1Fh	40h	2Fh	40h	3Fh	40h

Table 9-81: PIP2 Filter Vertical Coefficient Examples (REG[0868h] bit 4 = 1b)

Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient	Port Address Counter	Coefficient
00h	08h	10h	08h	20h	Do not set	30h	Do not set
01h	10h	11h	10h	21h		31h	
02h	18h	12h	18h	22h		32h	
03h	20h	13h	20h	23h		33h	
04h	28h	14h	28h	24h		34h	
05h	30h	15h	30h	25h		35h	
06h	38h	16h	38h	26h		36h	
07h	40h	17h	40h	27h		37h	
08h	08h	18h	08h	28h		38h	
09h	10h	19h	10h	29h		39h	
0Ah	18h	1Ah	18h	2Ah		3Ah	
0Bh	20h	1Bh	20h	2Bh		3Bh	
0Ch	28h	1Ch	28h	2Ch		3Ch	
0Dh	30h	1Dh	30h	2Dh		3Dh	
0Eh	38h	1Eh	38h	2Eh		3Eh	
0Fh	40h	1Fh	40h	2Fh		3Fh	

9.4.18 AME (Auto Movie Enhancement) Registers

REG[0900h] AME Control Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a			AME Sampling Area Enable	Reserved			
15	14	13	12	11	10	9	8
AME Initialize (WO)	Contrast Adjust Enable	Gamma Adjust Enable	Chroma Adjust Enable	n/a	Reserved	AME Enable bits 1-0	
7	6	5	4	3	2	1	0

bit 12 AME Sampling Area Enable
When AME is active for the PIP1 or PIP2 window (REG[0900h] bits 1-0 = 01b or 10b), this bit must be set to 1b.

bits 11-8 Reserved
The default value for these bits is 0000b and they should not be written.

bit 7 AME Initialize (Write Only)
This bit initializes the AME (Auto Movie Enhancement) module.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initializes the AME module.

Note
When the LCD2 parallel/serial interface or parallel TV-Out interface is selected, two frame transfers must be triggered (REG[0114h] bit 0 = 1b or REG[022Ch] bit 0 = 1b). The AME Initialize bit must be set before the first frame transfer as shown in the following sequence.

1. Set AME Initialize bit (REG[0900h] bit 7 = 1b)
2. Trigger first frame transfer (REG[0114h] bit 0 = 1b or REG[022Ch] bit 0 = 1b) Note that the first frame transfer may show an image that has not been AME adjusted.
3. Wait for frame transfer to complete (REG[0114h] bit 4 or REG[022Ch] bit 4)
4. Trigger second frame transfer (REG[0114h] bit 0 = 1b or REG[022Ch] bit 0 = 1b)

bit 6 Contrast Adjust Enable
This bit controls the contrast adjust function.
When this bit = 0b, contrast adjust is disabled.
When this bit = 1b, contrast adjust is enabled.

Note
The contrast adjust function requires several frames before settling to the level programmed in the AME Contrast Adjust Level bits, REG[0904h] bits 2-0.

bit 5 Gamma Adjust Enable
This bit controls the gamma adjust function.
When this bit = 0b, gamma adjust is disabled.
When this bit = 1b, gamma adjust is enabled.

Note
The gamma adjust function requires several frames before settling to the level programmed in the AME Gamma Adjust Level bits, REG[0904h] bits 10-8.

bit 4 Chroma Adjust Enable
This bit controls the chroma adjust function.
When this bit = 0b, chroma adjust is disabled.
When this bit = 1b, chroma adjust is enabled.

Note
The chroma adjust function requires several frames before settling to the level programmed in the AME Chroma Adjust Level bits, REG[0904h] bits 6-4.

bit 2 Reserved
The default value for this bit is 0b.

bits 1-0 AME Enable bits [1:0]
These bits determine which window (PIP1 or PIP2) is affected by the enabled AME adjust functions. To enable the desired AME adjust functions, set bits 6-4 appropriately.

Table 9-82: AME Enable Settings

REG[0900h] bits 1-0	AME Active Window
00b	All Off
01b	AME active in PIP1 window
10b	AME active in PIP2 window
11b	Reserved

REG[0904h] AME Parameter Adjust Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a					AME Gamma Adjust Level bits 2-0		
15	14	13	12	11	10	9	8
n/a	AME Chroma Adjust Level bits 2-0			n/a	AME Contrast Adjust Level bits 2-0		
7	6	5	4	3	2	1	0

bits 10-8 AME Gamma Adjust Level bits [2:0]

These bits control the strength of the gamma adjustment performed by the AME. The gamma adjust function must be enabled to have an effect (REG[0900h] bit 5 = 1b).

Table 9-83: AME Gamma Adjust Level Settings

REG[0904h] bits 10-8	Gamma Adjust Level
000b	Reserved
001b	Weakest
010b	
011b	
100b	
101b	Strongest
110b ~ 111b	Reserved

bits 6-4 AME Chroma Adjust Level bits [2:0]

These bits control the strength of the chroma adjustment performed by the AME. The chroma adjust function must be enabled to have an effect (REG[0900h] bit 4 = 1b).

Table 9-84: AME Chroma Adjust Level Settings

REG[0904h] bits 6-4	Chroma Adjust Level
000b	Reserved
001b	Weakest
010b	
011b	
100b	
101b	Strongest
110b ~ 111b	Reserved

bits 2-0 AME Contrast Adjust Level bits [2:0]

These bits control the strength of the contrast adjustment performed by the AME. The contrast adjust function must be enabled to have an effect (REG[0900h] bit 6 = 1b).

Table 9-85: AME Contrast Adjust Level Settings

REG[0904h] bits 2-0	Contrast Adjust Level
000b	Reserved
001b	Weakest
010b	
011b	
100b	
101b	Strongest
110b ~ 111b	Reserved

REG[0908h] AME Input Image Width Register

Default = 0000_0000h Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a					Reserved	AME Input Image Width bits 9-8	
15	14	13	12	11	10	9	8
AME Input Image Width bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved

The default value for this bit is 0b.

bits 9-0 AME Input Image Width bits [9:0]

These bits specify the width of the image input to the AME, in pixels. If the image size is changed using the scaler before being input to the AME, set the input image width to the scaled size. The input image width can range from a minimum of 64 pixels to a maximum of 1024 pixels.

When AME is used for the PIP1 window (REG[0900h] bits 1-0 = 01b), these bits should be set according to the following formula.

REG[0908h] bits 9-0 = PIP1 Window X Size - 1
= (REG[0744h] bits 9-0 - REG[073Ch] bits 9-0)

When AME is used for the PIP2 window (REG[0900h] bits 1-0 = 10b), these bits should be set according to the following formula.

REG[0908h] bits 9-0 = PIP2 Window X Size - 1
= (REG[0844h] bits 9-0 - REG[083Ch] bits 9-0)

For more information on configuring the input image width, see Section 12.5, “AME” on page 325.

REG[090Ch] AME Input Image Height Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a					Reserved	AME Input Image Height bits 9-8	
15	14	13	12	11	10	9	8
AME Input Image Height bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0b.

bits 9-0 AME Input Image Height bits [9:0]
These bits specify the height of the image input to the AME, in lines. If the image size is changed using the scaler before being input to the AME, set the input image height to the scaled size. The input image height can range from a minimum of 64 lines to a maximum of 1024 lines.

When AME is used for the PIP1 window (REG[0900h] bits 1-0 = 01b), these bits should be set according to the following formula.

REG[090Ch] bits 9-0 = PIP1 Window Y Size - 1
= (REG[0748h] bits 9-0 - REG[0740h] bits 9-0)

When AME is used for the PIP2 window (REG[0900h] bits 1-0 = 10b), these bits should be set according to the following formula.

REG[090Ch] bits 9-0 = PIP2 Window Y Size - 1
= (REG[0848h] bits 9-0 - REG[0840h] bits 9-0)

For more information on configuring the input image width, see Section 12.5, “AME” on page 325.

Note
For HSYNC & FIELD or ITU-R BT656 TV-Out interfaces (REG[0200h] bits 1-0 = 01b or 11b), set the input image height to 1/2 of the normal height.
REG[090Ch] bits 9-0 = AME Input Image Height ÷ 2 - 1

REG[0910h] AME Processing Horizontal Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a					Reserved	AME Processing Horizontal Start Position bits 9-8	
15	14	13	12	11	10	9	8
AME Processing Horizontal Start Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value of this bit is 0b.

bits 9-0 AME Processing Horizontal Start Position bits [9:0]
These bits define the horizontal start position, in pixels, of the first pixel in the input image to be processed by the AME. When these bits are set to 0, the AME processes image data from the first pixel of the input line. For more information on configuring the processing area, see Section 12.5, “AME” on page 325.

REG[0914h] AME Processing Horizontal End Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a					Reserved	AME Processing Horizontal End Position bits 9-8	
15	14	13	12	11	10	9	8
AME Processing Horizontal End Position bits 7-0							
7	6	5	4	3	2	1	0

bit 10 Reserved
The default value for this bit is 0b.

bits 9-0 AME Processing Horizontal End Position bits [9:0]
These bits define the horizontal end position, in pixels, of the last pixel in the input image to be processed by the AME. For more information on configuring the processing area, see Section 12.5, “AME” on page 325.

REG[0918h] AME Processing Vertical Start Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	AME Processing Vertical Start Position bits 9-8	
7	6	5	4	3	2	1	0
AME Processing Vertical Start Position bits 7-0							

bit 10 Reserved
The default value for this bit is 0b.

bits 9-0 AME Processing Vertical Start Position bits [9:0]
These bits define the vertical start position, in lines, of the first pixel in the input image to be processed by the AME. When these bits are set to 0, the AME processes image data from the first line of the input image. For more information on configuring the processing area, see Section 12.5, “AME” on page 325.

Note
For HSYNC & FIELD or ITU-R BT656 TV-Out interfaces (REG[0200h] bits 1-0 = 01b or 11b), set the vertical start position to 1/2 of the normal setting

REG[091Ch] AME Processing Vertical End Position Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	AME Processing Vertical End Position bits 9-8	
7	6	5	4	3	2	1	0
AME Processing Vertical End Position bits 7-0							

bit 10 Reserved
The default value for this bit is 0b.

bits 9-0 AME Processing Vertical End Position bits [9:0]
These bits define the vertical end position, in lines, of the last pixel in the input image to be processed by the AME. For more information on configuring the processing area, see Section 12.5, “AME” on page 325.

Note
For HSYNC & FIELD or ITU-R BT656 TV-Out interfaces (REG[0200h] bits 1-0 = 01b or 11b), set the vertical end position to 1/2 of the normal setting

REG[0920h] AME Sampling Area Vertical Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	AME Sampling Area Vertical Start Position bits 9-8	
7	6	5	4	3	2	1	0
AME Sampling Area Vertical Start Position bits 7-0							

bit 10 Reserved
The default value for this bit is 0b.

bits 9-0 AME Sampling Area Vertical Start Position bits [9:0]
These bits define the vertical start position, in lines, of the first pixel in the input image to be sampled by the AME. When these bits are set to 0, the AME samples image data from the first line of the input image. For more information on configuring the sampling area, see Section 12.5, “AME” on page 325.

REG[0924h] AME Sampling Area Horizontal Start Position Register
Default = 0000_0000h Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a					Reserved	AME Sampling Area Horizontal Start Position bits 9-8	
7	6	5	4	3	2	1	0
AME Sampling Area Horizontal Start Position bits 7-0							

bit 10 Reserved
The default value for this bit is 0b.

bits 9-0 AME Sampling Area Horizontal Start Position bits [9:0]
These bits define the horizontal start position, in pixels, of the first pixel in the input image to be sampled by the AME. When these bits are set to 0, the AME samples image data from the first pixel of the input line. For more information on configuring the sampling area, see Section 12.5, “AME” on page 325.

REG[0928h] AME Sampling Area Size Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a					AME Sampling Area Size bits 2-0		
7	6	5	4	3	2	1	0

bits 2-0 AME Sampling Area Size bits [2:0]

These bits specify the width and height of the AME sampling area, in pixels x lines. The AME sampling area must be within the AME processing area. For more information on configuring the sampling area, see Section 12.5, “AME” on page 325.

Table 9-86: AME Sampling Area Size Selection

REG[0928h] bits 2-0	AME Sampling Area Size (pixels x lines)
000b	16 x 16
001b	32 x 32
010b	64 x 64
011b	128 x 128
100b	256 x 256
101b	512 x 512
110b ~ 111b	Reserved

REG[092Ch] AME Sampling Area Parameter 1 Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a						AME Sampling Area Parameter 1 bits 9-8	
15	14	13	12	11	10	9	8
AME Sampling Area Parameter 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 9-0 AME Sampling Area Parameter 1 bits [9:0]
When AME is active for the PIP1 or PIP2 window (REG[0900h] bits 1-0 = 01b or 10b), these bits must be set according to the total pixel count of the AME processing area.

Table 9-87: AME Sampling Area Parameter 1 Settings

AME Processing Area Size	Total Pixel Count of AME Processing Area	REG[092Ch] bits 9-0
less than QVGA	4096 to 76799 pixels	18h
QVGA to WQVGA	76800 to 95999 pixels	20h
WQVGA to VGA	96000 to 307199 pixels	26h
VGA to WVGA	307200 to 383999 pixels	3Ah
WVGA or greater	384000 or greater pixels	3Fh

REG[0930h] AME Sampling Area Parameter 2 Register
Default = 0000_0000h — Read/Write

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a		AME Sampling Area Parameter 2 bits 13-8					
15	14	13	12	11	10	9	8
AME Sampling Area Parameter 2 bits 7-0							
7	6	5	4	3	2	1	0

bits 13-0 AME Sampling Area Parameter 2 bits [13:0]
When AME is active for the PIP1 or PIP2 window (REG[0900h] bits 1-0 = 01b or 10b), these bits must be set according to the total pixel count of the AME processing area.

Table 9-88: AME Sampling Area Parameter 2 Settings

AME Processing Area Size	Total Pixel Count of AME Processing Area	REG[0930h] bits 13-0
less than QVGA	4096 to 76799 pixels	A4h
QVGA to VGA	76800 to 307199 pixels	28Fh
VGA or greater	307200 or greater pixels	3FFh

REG[0934h] through REG[0984h] are Reserved

These registers are Reserved and should not be written.

9.4.19 Interrupt Control Registers

REG[0A00h] Interrupt Status Register (AID)
Default = 0000_0000h: Address auto increment disable — Read Only

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIO Interrupt Status (RO)	n/a						
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

bit 15 GPIO Interrupt Status (Read Only)
This bit indicates the status of the GPIO interrupt. This bit is masked by the GPIO Interrupt Enable bit and is only available when REG[0A04h] bit 15 = 1b.
When this bit = 0b, a GPIO interrupt has not occurred.
When this bit = 1b, a GPIO interrupt has occurred. To determine the exact nature of the interrupt, refer to the status bits in REG[0348h] ~ REG[0350h].

To clear this status bit, write a 1b then a 0b to the GPIO Interrupt Status bit that caused the interrupt (see REG[0348h] ~ REG[0350h].

REG[0A04h] Interrupt Enable Register
Default = 0000_0000h — Write/Read

n/a							
31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
GPIO Interrupt Enable	n/a						
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

bit 15 GPIO Interrupt Enable
This bit controls the GPIO interrupt. The status of the GPIO interrupt is indicated by the GPIO Interrupt Status bit, REG[0A00h] bit 15.
When this bit = 0b, the GPIO interrupt is disabled.
When this bit = 1b, the GPIO interrupt is enabled.

REG[0A08h] is Reserved

This register is Reserved and should not be written.

9.4.20 I2C Slave Configuration Registers

Note
The I2C interface cannot access the following registers.

REG[0B00h] I2C Clock Divide Register
Default = 0000_0000h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	22	21	20	19	18	17	16
n/a							
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				I2C Clock Divide Select bits 3-0			

bits 3-0 I2C Clock Divide Select bits [3:0]
These bits specify the divide ratio for the I2C clock. The I2C clock source is selected by CNF1 (see Section 4.3, “Summary of Configuration Options” on page 31). For further details on the clock structure, see Section 8, “Clocks” on page 88.

Table 9-89: I2C Clock Divide Ratio Selection

REG[0B00h] bits 3-0	I2C Clock Divide Ratio	REG[0B00h] bits 3-0	I2C Clock Divide Ratio
0000b	1:1	1000b	9:1
0001b	2:1	1001b	10:1
0010b	3:1	1010b	11:1
0011b	4:1	1011b	12:1
0100b	5:1	1100b	13:1
0101b	6:1	1101b	14:1
0110b	7:1	1110b	15:1
0111b	8:1	1111b	16:1

Note
For fast mode (400kbps):
I2C Clock = System Clock frequency ÷ Divide Ratio ≥ 24MHz
For standard mode (100kbps):
I2C Clock = System Clock frequency ÷ Divide Ratio ≥ 5.4MHz

REG[0B04h] I2C Enable Register
Default = 0000_55X0h — Read/Write

31	30	29	28	27	26	25	24
n/a							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
n/a							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
n/a	I2C Slave Address bits 6-0						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a			I2C Enable Status (RO)	n/a			I2C Enable

bits 14-8 I2C Slave Address bits [6:0]
These bits determine the 7-bit slave address for the I2C. These bits can be changed only when the I2C module is disabled, REG[0B04h] bit 0 = 0b.

bit 4 I2C Enable Status (Read Only)
This bit indicates the status of the I2C module as set by bit 0.
When this bit = 0b, the I2C module is disabled.
When this bit = 1b, the I2C module is enabled.

bit 0 I2C Enable
This bit controls whether the I2C module is enabled.
Writing a 0b to this bit disables the I2C module.
Writing a 1b to this bit enables the I2C module.

Note
The I2C is enabled when either the I2CEN pin is High or this bit 0 = 1b.

REG[0B08h] is Reserved

This register is Reserved and should not be written. The default value is 0000_0036h.

REG[0B0Ch] is Reserved

This register is Reserved and should not be written. The default value is 0000_0040h.

REG[0B10h] is Reserved

This register is Reserved and should not be written. The default value is 0000_0009h.

REG[0B14h] is Reserved

This register is Reserved and should not be written. The default value is 0000_0012h.

REG[1040h] through REG[1060h] are Reserved

These registers are Reserved and should not be written.

10 Power Save Modes

10.1 Power-On Sequence (PLL Used)

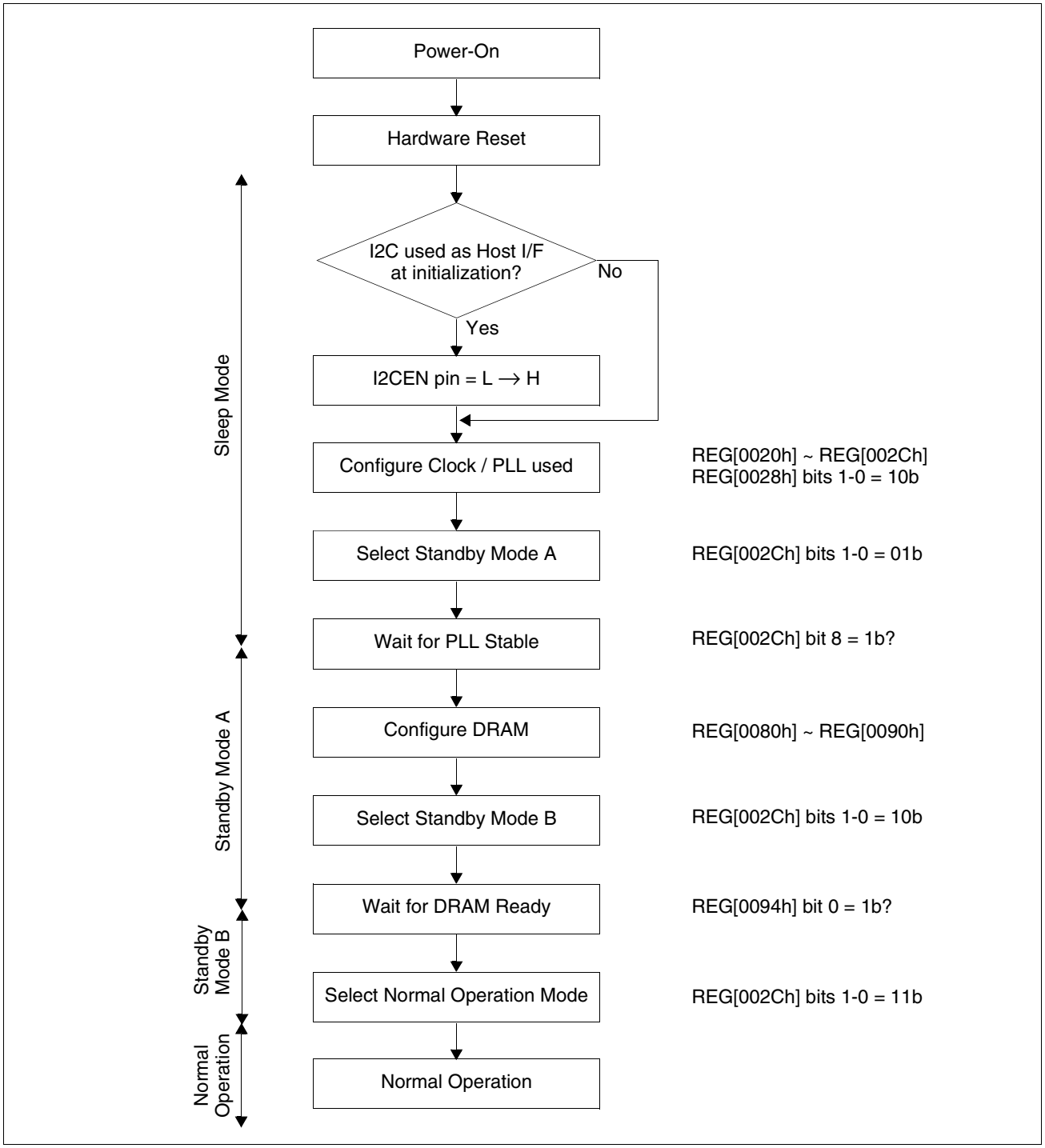


Figure 10-1: Power-On Sequence (PLL Used)

10.2 Power-On Sequence (PLL Bypassed)

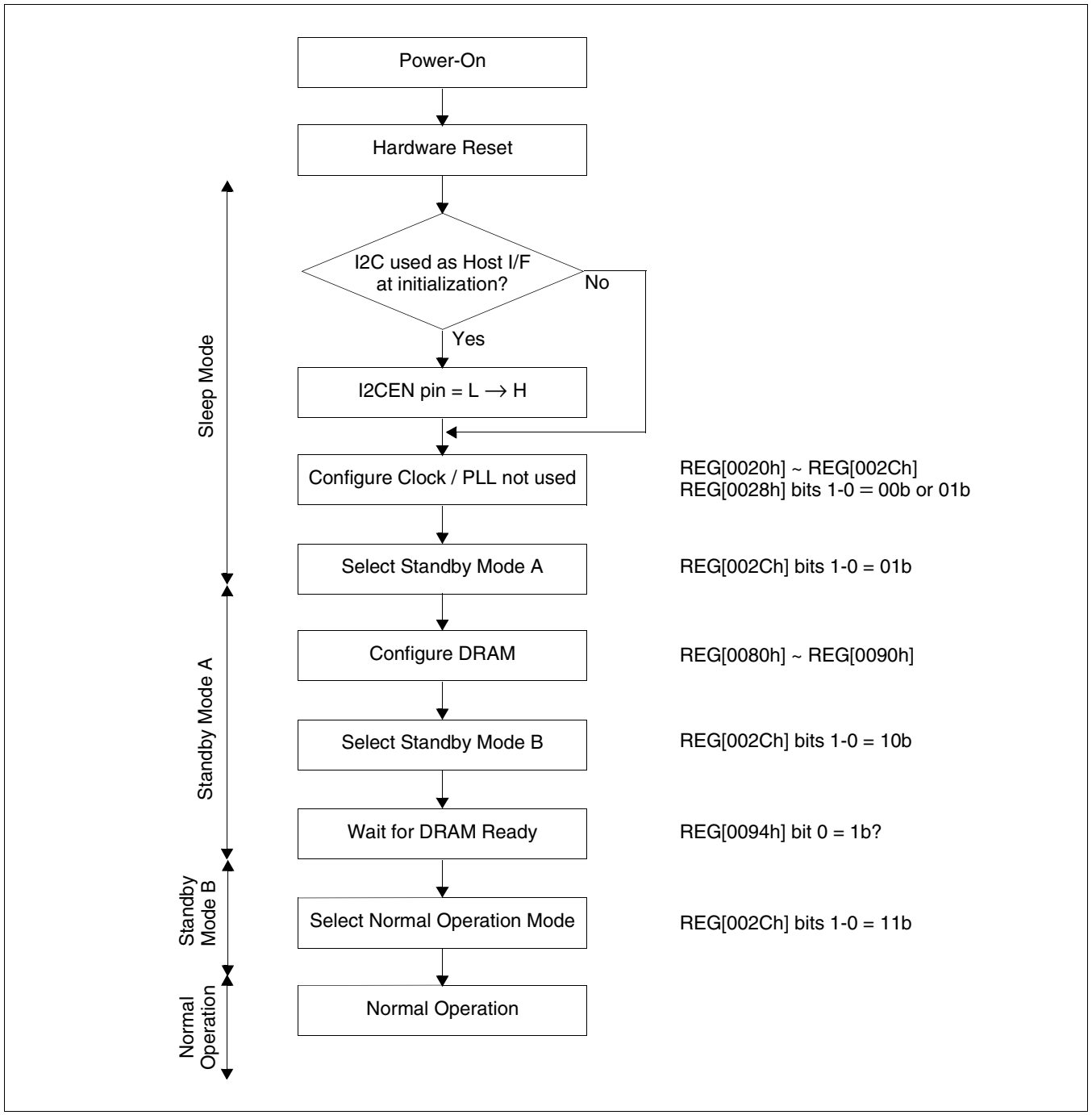


Figure 10-2: Power-On Sequence (PLL Bypassed)

10.3 Power-Off Sequence

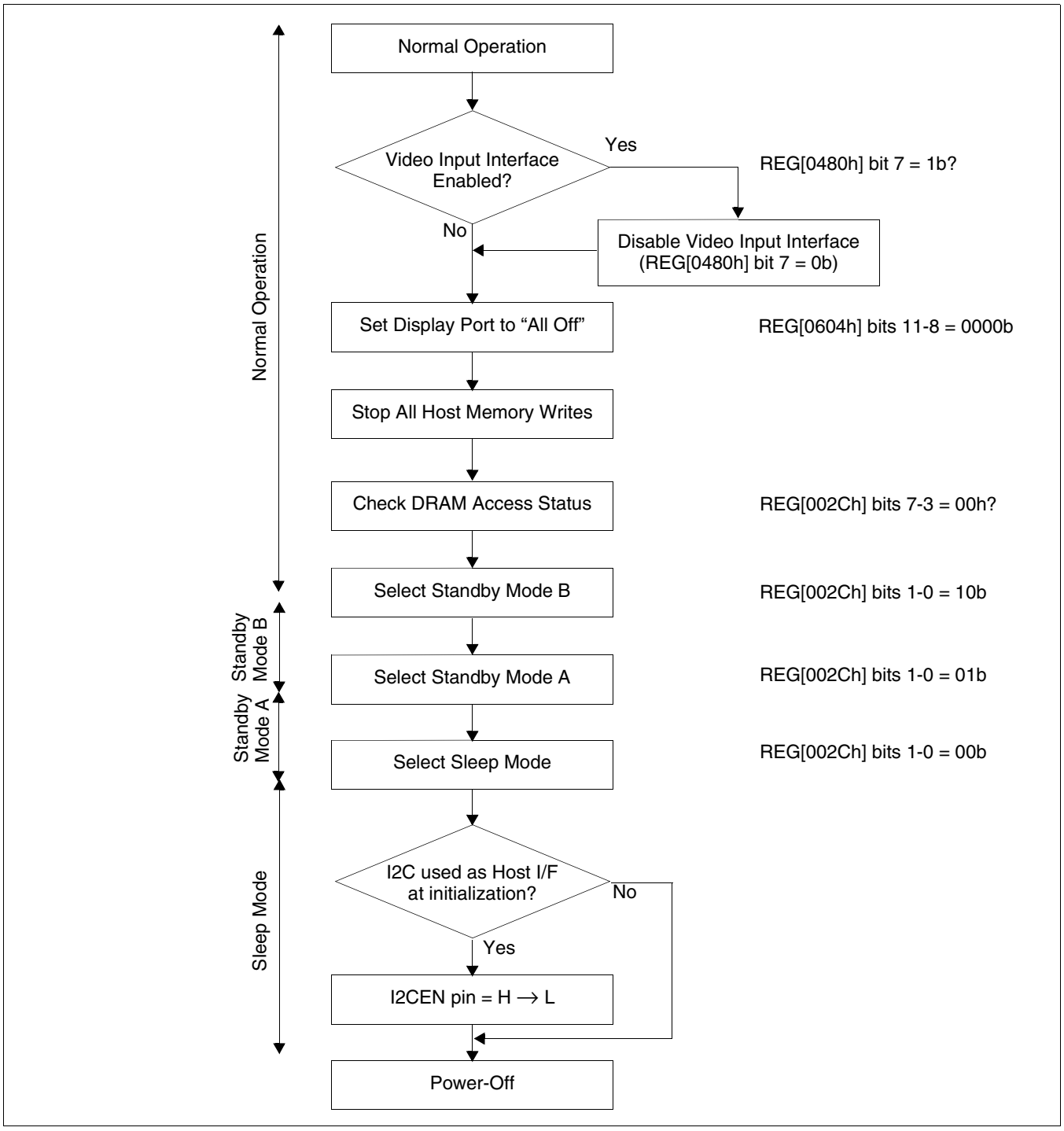


Figure 10-3: Power-Off Sequence

10.4 Operational Modes

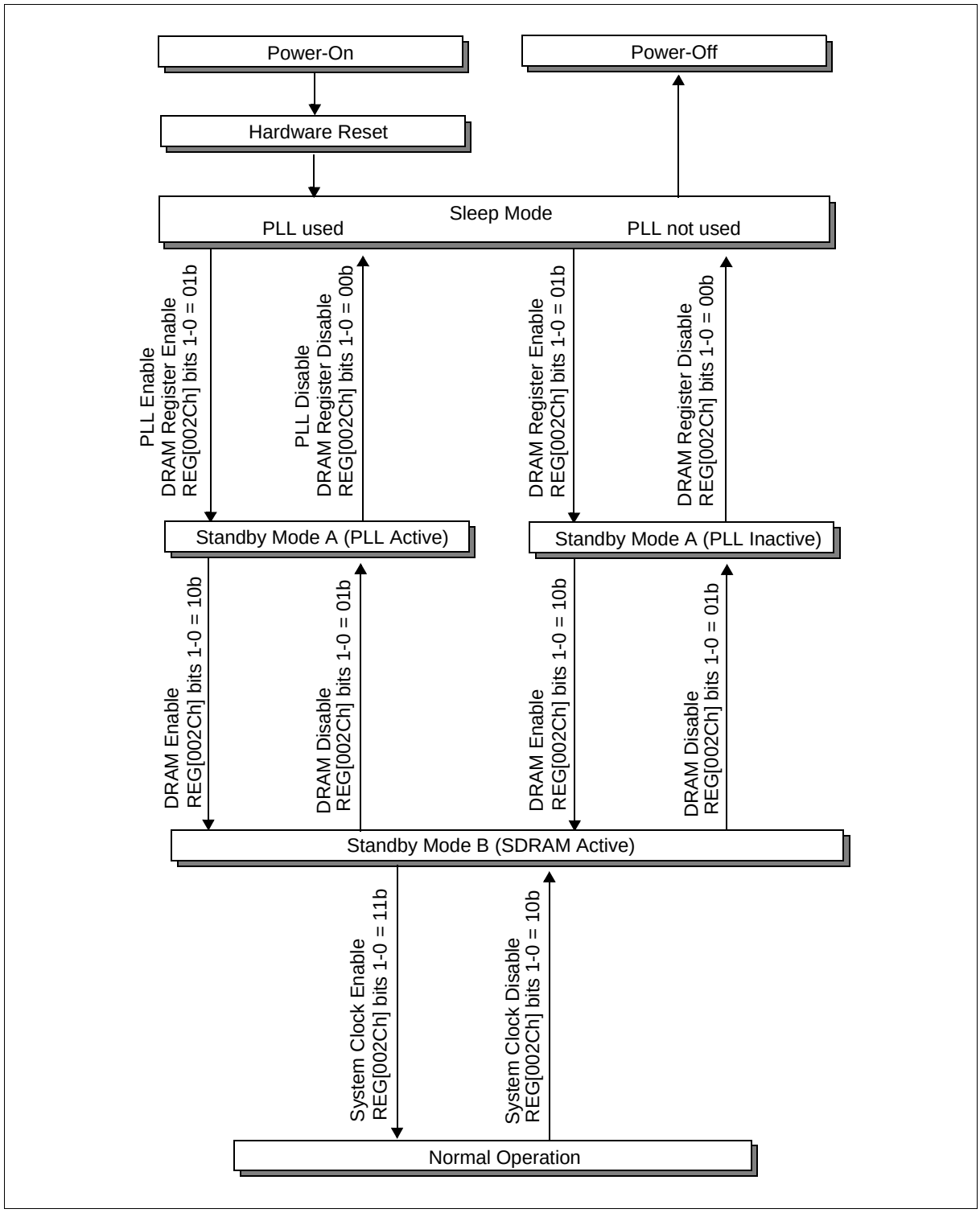


Figure 10-4: Power Modes

Note

The Video Input Interface must be disabled (REG[0480h] bit 7 = 0b), the Display Output Port must be set to "All Off" (REG[0604h] bits 11-8 = 0000b), and all memory accesses must have completed (see REG[002Ch] bits 7-3) **before** entering Standby or Sleep power save mode.

10.5 Power Save Mode Functions

Table 10-1: Power Save Mode Functions

Item		Reset State	Sleep Mode	Standby Mode A	Standby Mode B	Normal Mode
PLL		Inactive	Inactive	Active	Active	Active
DRAM Access		No (No Refresh)	No (No Refresh)	No (No Refresh)	No (Refresh)	Yes
Register Access	REG[0000h] ~ REG[0040h] REG[0300h] ~ REG[0350h]	No	Yes	Yes	Yes	Yes
	Other registers except REG[0650h]	No	No	Yes	Yes	Yes
LUT Access	REG[0650h]	No	No	No	No	Yes
GPIO Pins configured as GPIOs		Input	GPIO state	GPIO state	GPIO state	GPIO state
Host Interface Pins	INT	Forced Low	Active	Active	Active	Active
	TE	Forced Low	Inactive	Inactive	Inactive	Active
LCD1 RGB Interface Pins	FPDAT[17:0]	Forced Low	Note 1	Note 1	Note 1	Active
	FPDAT[23:18]	Input (GPIO)	Note 1	Note 1	Note 1	Active
	FPDRDY	Forced Low	Note 2	Note 2	Note 2	Active
	FPFRAME	Forced Low	Forced Low	Forced Low	Forced Low	Active
	FPLINE	Forced Low	Note 3	Note 3	Note 3	Active
	FPSHIFT	Forced Low	Note 4	Note 4	Note 4	Active
LCD1, LCD2 Serial Interface Pins	FPCS1#	Forced High	Note 5	Note 5	Note 5	Active
	FPCS2#	Forced High	Note 6	Note 6	Note 6	Active
	FPSCLK	Forced High	Note 7	Note 7	Note 7	Active
	FPA0	Forced Low	Note 8	Note 8	Note 8	Active
	FPSO	Forced Low	Forced Low	Forced Low	Forced Low	Active
	FPVS2 (REG[018Ch] bit 15 =0b)	Input (GPIO)	Input	Input	Input	Input
	FPVS2 (REG[018Ch] bit 15 =1b)	Input (GPIO)	Note 9	Note 9	Note 9	Active
LCD2 Parallel Interface Pins (Mode 3)	P2DAT[7:0]	Input (GPIO)	Note 1	Note 1	Note 1	Active
	P2CS#	Input (GPIO)	Note 6	Note 6	Note 6	Active
	P2WR#	Input (GPIO)	Forced High	Forced High	Forced High	Active
	P2A0	Input (GPIO)	Forced Low	Forced Low	Forced Low	Active
TV-Out Interface Pins (HSYNC & FIELD or BT656)	TVDT[7:0]	Input (GPIO)	Note 10	Note 10	Note 10	Active
	TVCLK, TVHS, TVFLD	Input (GPIO)	Forced Low	Forced Low	Forced Low	Active
TV-Out Interface Pins (Parallel)	TVDT[7:0]	Input (GPIO)	Forced Low	Forced Low	Forced Low	Active
	TVCS#, TVWR#, TVRD#, TVDC	Input (GPIO)	Forced High	Forced High	Forced High	Active
	TVTE	Input (GPIO)	Input	Input	Input	Input
Video Interface Pins	VCLKOUT	Forced Low	Forced Low	Forced Low	Forced Low	Active

Table 10-1: Power Save Mode Functions

I2C Pins	I2CEN=H or REG[0030h] bit 0 = 1b	Hi-Z	Active	Active	Active	Active
	I2CEN=L and REG[0030h] bit 0 = 0b	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Active
Host Indirect Interface		Inactive	Active	Active	Active	Active
I2C	I2CEN=H or REG[0030h] bit 0 = 1b	Inactive	Active	Active	Active	Active
	I2CEN=L and REG[0030h] bit 0 = 0b	Inactive	Inactive	Inactive	Inactive	Active
Video Input Interface		Inactive	Inactive	Inactive	Inactive	Active
LCD Interface		Inactive	Inactive	Inactive	Inactive	Active
TV-Out Interface		Inactive	Inactive	Inactive	Inactive	Active

1. When REG[0600h] bit 10 = 0b, these pins are forced low. When REG[0600h] bit 10 = 1b, these pins are forced high.
2. This pin is inactive and depends on REG[0104h] bit 9.
3. This pin is inactive and depends on REG[014Ch] bit 7.
4. When REG[0104h] bit 7 = 0b, this pin is forced low. When REG[0104h] bit 7 = 1b, this pin is forced high.
5. This pin is inactive and depends on REG[0104h] bit 8.
6. This pin is inactive and depends on REG[0104h] bit 12.
7. When REG[0168h] bit 0 = 0b, this pin is forced low. When REG[0168h] bit 0 = 1b, this pin is forced high.
8. When REG[0104h] bit 10 = 0b, this pin is forced low. When REG[0104h] bit 10 = 1b, this pin is forced high.
9. This pin is inactive and depends on REG[018Ch] bit 14.
10. These pins depend on REG[0230h] bits 15-0.

11 Writing Image Data to Memory

There are two paths that can be used for writing image data from the Host and Video interfaces into memory.

- Main Memory Write Path
- Sub Memory Write Path

The Host and Video interfaces can be routed through either write path, as shown in the following figure. It is also possible to use both paths simultaneously if the total bandwidth satisfies the following formula.

(Host Interface bit rate) x 0.8) + (Video Interface bit rate) < 576Mbps

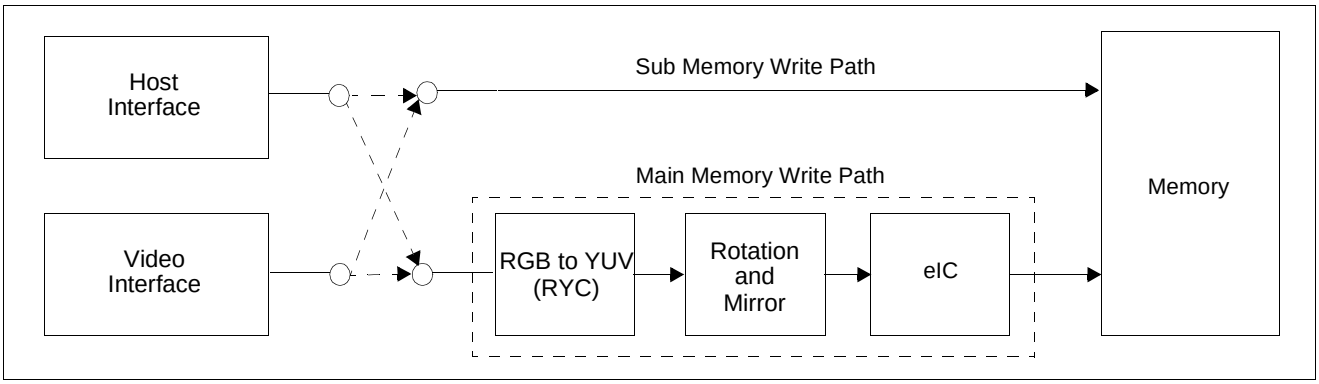


Figure 11-1: Write Path Overview

Both write paths allow image data to be written to memory using either a single or double buffer method. However, the Main Memory Write Path supports some additional features such as rotation, mirror, RGB to YUV conversion, and processing by the eIC (eco Image Codec). The following table summarizes the options available for each write path.

Table 11-1: Write Path Function Summary

Write Path	Image Data Format	Double Buffer	Rotation, Mirror	RGB to YUV	eIC
Main Memory	RGB 8:8:8, RGB 6:6:6 (Note 1), RGB 5:6:5, YUV 4:2:2, YUV 4:2:0	√	√	√	√
Sub Memory	RGB 8:8:8, RGB 6:6:6 (Note 1), RGB 5:6:5, YUV 4:2:2, YUV 4:2:0	√	X	X	X

Note

RGB 6:6:6 image data is converted to RGB 8:8:8 before being written to memory.

11.1 Configuring the Write Paths

The size of the memory area and input image must be configured for each write path. The size of the memory area is configured by specifying a start address (MSA), line address offset (MAO), and vertical size (MVS). The input image is defined using a horizontal size (IHS), vertical size (IVS), and start position (XSP, YSP).

The memory area can be set to a larger area than required for the input image. The following figure shows the write path parameters that must be configured.

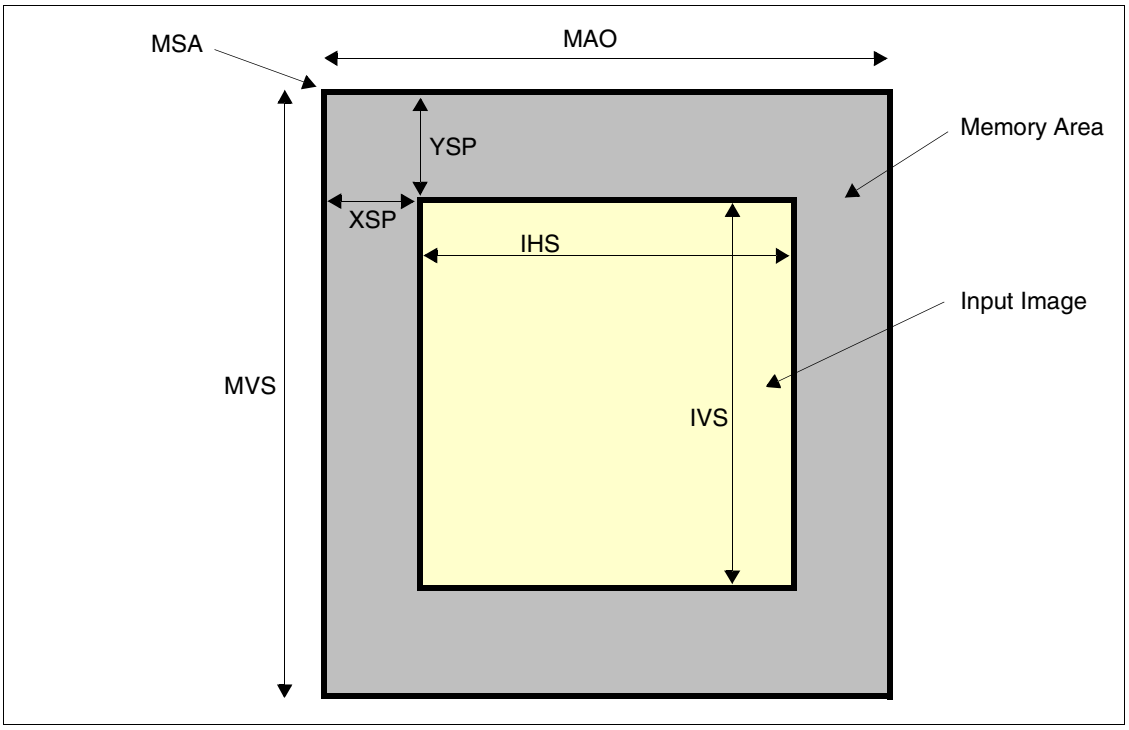


Figure 11-2: Write Path Parameters

When YUV 4:2:2 or 4:2:0 format image data is written to memory, the Y and UV data are stored separately which requires two memory start addresses (MSA). For RGB format image data, only one memory start address is used. The following table provides a summary of the minimum and maximum values and registers used for each write path.

Table 11-2: Write Path Parameter Summary

Symbol	Description	Min	Max	Units	Main Memory Write Path Registers	Sub Memory Write Path Registers
MSA	Memory Start Address	—	—	bytes	REG[0508h] REG[050Ch]	REG[0584h] REG[0588h]
MAO	Memory Line Address Offset	64	4032	bytes	REG[0518h]	REG[0594h]
MVS	Memory Vertical Size	4	864 (main) 1024 (sub)	pixels	REG[051Ch]	REG[0598h]
IHS	Input Image Horizontal Size	1	864 (main) 1024 (sub)	pixels	REG[0520h]	REG[059Ch]
IVS	Input Image Vertical Size	1	864 (main) 1024 (sub)	pixels	REG[0524h]	REG[05A0h]
XSP	Image X Start Position	0	863 (main) 1023 (sub)	pixels	REG[0528h]	REG[05A4h]
YSP	Image Y Start Position	0	863 (main) 1023 (sub)	pixels	REG[052Ch]	REG[05A8h]

Many of the write path parameters have alignment or resolution restrictions that determine which values can be programmed. For all cases, the line address offset (MAO) must be 64 byte aligned and the memory vertical size (MVS) must be set to a multiple of 4 pixels. Restrictions for all other parameters are determined by the combination of data format, eIC mode, and rotation options selected. The following tables show the write path parameter restrictions that must be observed for each possible combination.

Table 11-3: Write Path Parameter Restrictions: eIC Disabled and 0° or 180° Rotation

Symbol	Description	Data Format				
		RGB 8:8:8	RGB 6:6:6	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel
XSP	Image X Start Position	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Table 11-4: Write Path Parameter Restrictions: eIC Disabled and 90° or 270° Rotation

Symbol	Description	Data Format				
		RGB 8:8:8	RGB 6:6:6	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
XSP	Image X Start Position	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Table 11-5: Write Path Parameter Restrictions: Line eIC Mode and 0° Rotation

Symbol	Description	Data Format				
		RGB 8:8:8	RGB 6:6:6	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel
XSP	Image X Start Position	Note	Note	Note	Note	Note
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Note
When line eIC mode is used, XSP must equal 0.

Table 11-6: Write Path Parameter Restrictions: Partial eIC Mode and 0° or 180° Rotation

Symbol	Description	Data Format				
		RGB 8:8:8	RGB 6:6:6	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	4 Pixel	4 Pixel	5 Pixel	8 Pixel	8 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel
XSP	Image X Start Position	4 Pixel	4 Pixel	5 Pixel	8 Pixel	8 Pixel
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Table 11-7: Write Path Parameter Restrictions: Partial eIC Mode and 90° or 270° Rotation

Symbol	Description	Data Format				
		RGB 8:8:8	RGB 6:6:6	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	4 Pixel	4 Pixel	5 Pixel	8 Pixel	8 Pixel
XSP	Image X Start Position	4 Pixel	4 Pixel	5 Pixel	8 Pixel	8 Pixel
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	1 Pixel	2 Pixel

11.1.1 Memory Area and Input Image Restrictions

When configuring the memory area and input image parameters, the input image must remain within the boundary of the specified memory area. The following configurations are not allowed.

- YSP + IVS < MVS
- XSP + IHS ≤ MA0

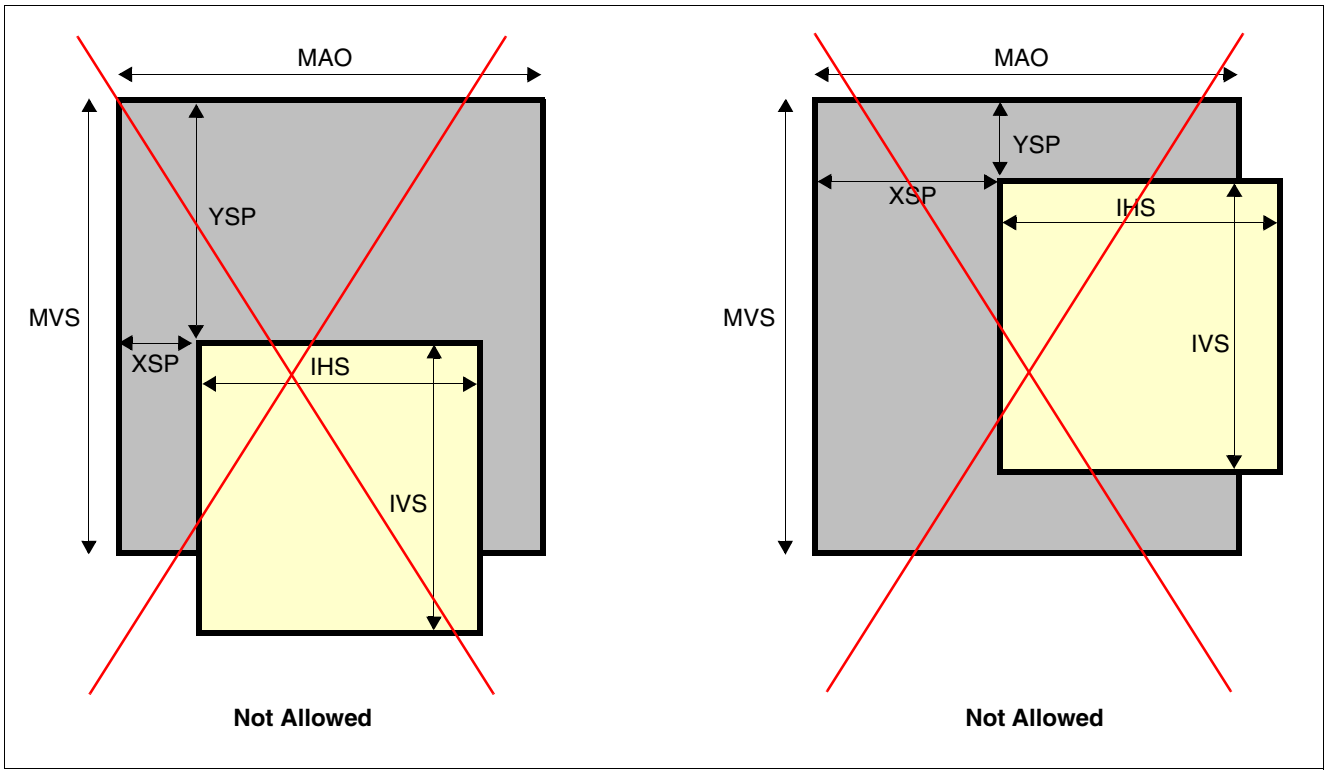


Figure 11-3: Memory Area and Input Image Restrictions

11.1.2 Required Memory Size

When determining the required size for each memory, the Memory Line Address Offset (MAO) is calculated based on three factors: data format, eIC mode, and horizontal size in pixels. The following table provides the required calculations for each combination.

Table 11-8: Memory Line Address Offset Calculations

Data Format	eIC Mode	Memory Line Address Offset (byte) Horizontal Size = n pixel
RGB 8:8:8	eIC disabled	ROUNDUP(3n ÷ 64) x 64
	Line eIC mode	ROUNDUP(1.5 (n + 1) ÷ 64) x 64
	Partial eIC mode	ROUNDUP(2n ÷ 64) x 64
RGB 5:6:5	eIC disabled	ROUNDUP(2n ÷ 64) x 64
	Line eIC mode	ROUNDUP((1.5n + 0.5) ÷ 64) x 64
	Partial eIC mode	ROUNDUP(1.6n ÷ 64) x 64
YUV 4:2:2	eIC disabled	ROUNDUP(n ÷ 64) x 64
	Line eIC mode	ROUNDUP((0.5n + 1) ÷ 64) x 64
	Partial eIC mode	ROUNDUP((ROUNDUP(n ÷ 24) x 16) ÷ 64) x 64
YUV 4:2:0	eIC disabled	ROUNDUP(n ÷ 64) x 64
	Line eIC mode	ROUNDUP((0.5n + 1) ÷ 64) x 64
	Partial eIC mode	ROUNDUP((ROUNDUP(n ÷ 24) x 16) ÷ 64) x 64

Once the Memory Line Address Offset (MAO) has been determined, the required memory size can be calculated by multiplying the MAO by the Memory Vertical Size (MVS). The MVS must be a multiple of 4 pixels. The number of bytes required for each data format is determined using the following equations.

For RGB 5:6:5 and 8:8:8:
MAO x MVS (bytes)

For YUV 4:2:2:
2 x MAO x MVS (bytes)

For YUV 4:2:0:
MAO x (MVS + 2 x ROUNDUP(MVS ÷ 4)) (bytes)

Example 1: Calculate the required memory size for a 500 pixel (horizontal size) by 600 pixel (vertical size) YUV 4:2:2 image using Partial eIC Mode.

MAO = ROUNDUP((ROUNDUP(500 ÷ 24) x 16) ÷ 64) x 64
= ROUNDUP((21 x 16) ÷ 64) x 64
= 6 x 64 = 384 byte

Required Memory Size
= 2 x 384 x 600 = 460,800 byte

Example 2: Calculate the required memory size for a 480 pixel (horizontal size) by 642 pixel (vertical size YUV 4:2:0 image using Line eIC Mode.

MAO = ROUNDUP((0.5 x 480 + 1) ÷ 64) x 64
= ROUNDUP(241 ÷ 64) x 64
= 4 x 64 = 256 byte

Requierd Memory Size
= 256 x (642 + 2 x (ROUNDUP(642 ÷ 4))
= 256 x (642 + 2 x 161) = 246,784 byte

11.2 Main Memory Write Path

The Main Memory Write Path can be used to write image data from either the Host or Video interface to memory. The Main Memory Write Path includes several optional functions that can be enabled during the write process.

- Double Buffering
- RGB to YUV Conversion
- Rotation and Mirror
- eIC (eco Image Codec)

For an overview of the write paths, see Figure 11-1: "Write Path Overview," on page 276. For further information on each function, see to the following sections.

11.2.1 Double Buffering

Input image data written to memory using the Main Memory Write Path can be double buffered. For more information on double buffering, see Section 11.4, "Double Buffering" on page 291.

11.2.2 RYC (RGB to YUV Converter)

The Main Memory Write Path can convert RGB image data input from the Host or Video interface into YUV 4:2:2 image data before it is stored in memory. It is converted into YUV according to the ITU-R BT.470-6 System B and G conversion type recommendation using the following expressions. The YUV 4:2:2 image data can be further converted to YUV 4:2:0 using the YUV 4:2:0 Conversion Enable bit, REG[0504h] bit 5.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.169 & -0.331 & 0.500 \\ 0.500 & -0.419 & -0.081 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Note
The RYC equation results in YUV non-offset data. However, the actual RYC block outputs the data to memory as YUV offset.

11.2.3 Rotation and Mirror

When the Main Memory Write Path is used to write input image data from the Host or Video interface into memory, the image data can be rotated or "mirrored". Rotation performs a 90°, 180°, or 270° clockwise rotation of the image data as it is written to memory. The Mirror function performs a horizontal flip on the image data as it is written to memory. If both functions are enabled, rotation is applied before mirroring.

The input image data is written to memory according to the configuration of the Rotation Mode Select bits (REG[0504h] bits 2-1), the Mirror Enable bit (REG[0504h] bit 3), and the following parameters. The main memory and main image parameters do not have to be changed when the selected rotation and mirror settings are changed. However if 90° or 270° rotations will be used, the Main Memory Line Address Offset (MAO) and Main Memory Vertical Size (MVS) must be configured such that the rotated image will fit within the specified memory size.

Table 11-9: Rotation and Mirror Register Summary

Symbol	Description	Register
MSA	Main Memory Start Address (either buffer A or B)	REG[0508h] ~ REG[0514h]
MAO	Main Memory Line Address Offset	REG[0518h]
MVS	Main Memory Vertical Size	REG[051Ch]
IHS	Main Image Horizontal Size	REG[0520h]
IVS	Main Image Vertical Size	REG[0524h]
XSP	Main Image X Start Position	REG[0528h]
YSP	Main Image Y Start Position	REG[052Ch]

Note
For 90° and 270° rotations, the IHS specifies the "vertical" size and the IVS specifies the "horizontal" size.

The following sections provide examples for each combination of Rotation and Mirror settings.

0° Rotation and Mirror Disabled

For the Main Memory Write Path when 0° rotation is selected (REG[0504h] bits 2-1 = 00b) and Mirror is disabled (REG[0504h] bit 3 = 0b), input image data from the Host or Video interface is written to memory as follows.

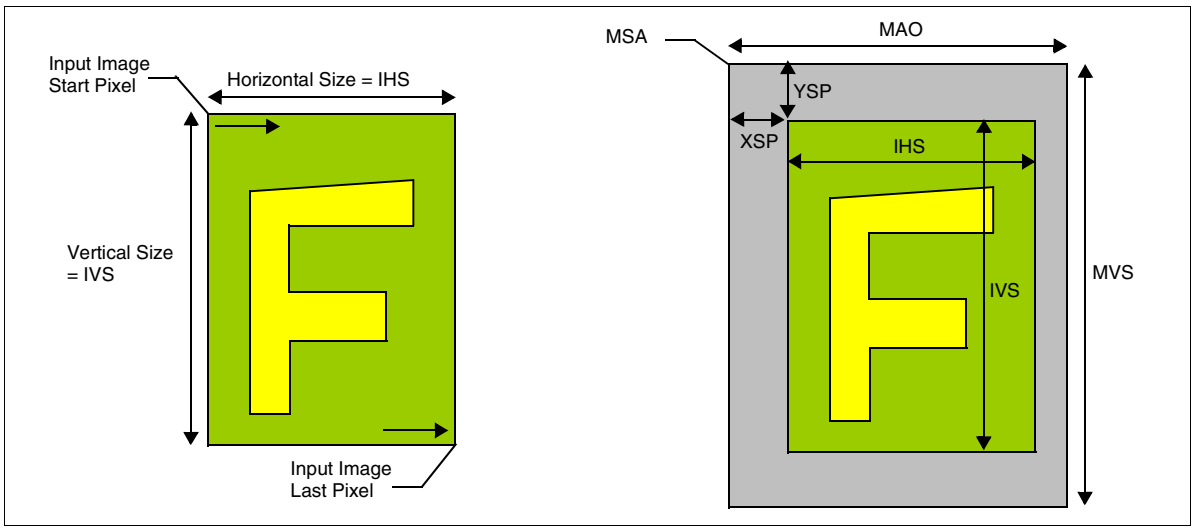


Figure 11-4: 0° Rotation and Mirror Disabled

90° Rotation and Mirror Disabled

For the Main Memory Write Path when 90° rotation is selected (REG[0504h] bits 2-1 = 01b) and Mirror is disabled (REG[0504h] bit 3 = 0b), input image data from the Host or Video interface is written to memory as follows.

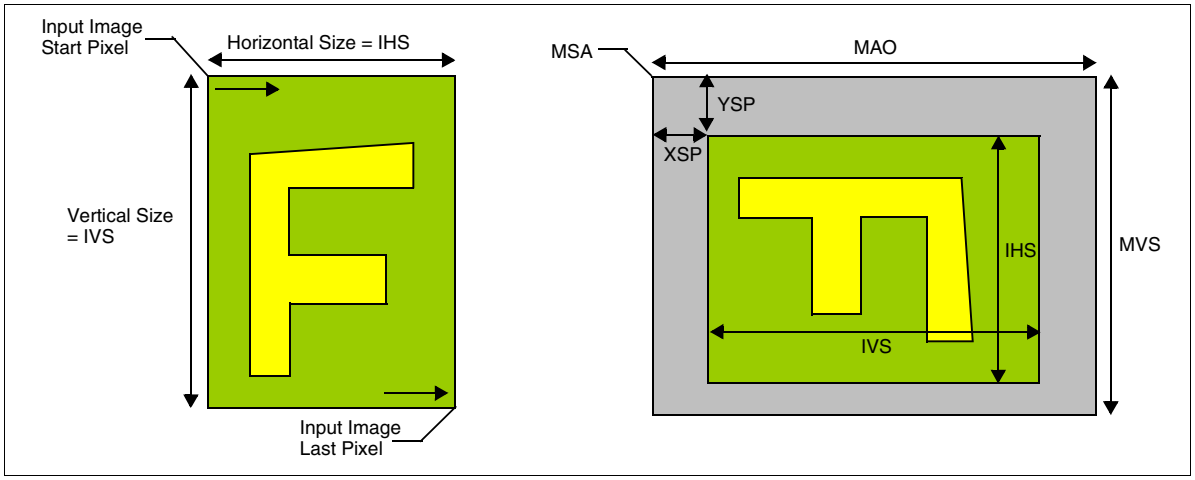


Figure 11-5: 90° Rotation and Mirror Disabled

Note

The IHS specifies the “vertical” size and the IVS specifies the “horizontal” size.

180° Rotation and Mirror Disabled

For the Main Memory Write Path when 180° rotation is selected (REG[0504h] bits 2-1 = 10b) and Mirror is disabled (REG[0504h] bit 3 = 0b), input image data from the Host or Video interface is written to memory as follows.

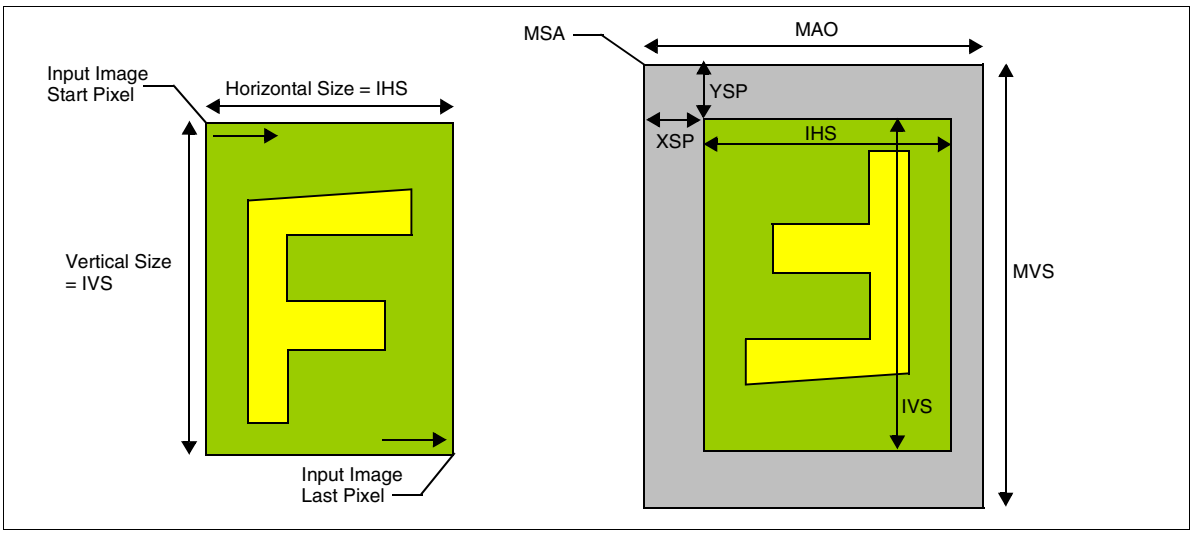


Figure 11-6: 180° Rotation and Mirror Disabled

270° Rotation and Mirror Disabled

For the Main Memory Write Path when 270° rotation is selected (REG[0504h] bits 2-1 = 11b) and Mirror is disabled (REG[0504h] bit 3 = 0b), input image data from the Host or Video interface is written to memory as follows.

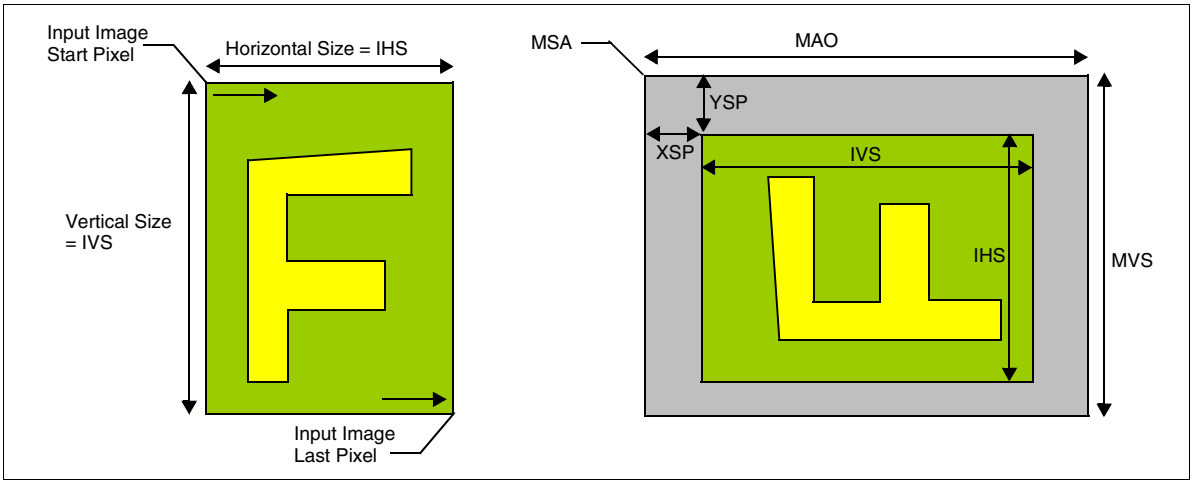


Figure 11-7: 270° Rotation and Mirror Disabled

Note

The IHS specifies the "vertical" size and the IVS specifies the "horizontal" size.

0° Rotation and Mirror Enabled

For the Main Memory Write Path when 0° rotation is selected (REG[0504h] bits 2-1 = 00b) and Mirror is enabled (REG[0504h] bit 3 = 1b), input image data from the Host or Video interface is written to memory as follows.

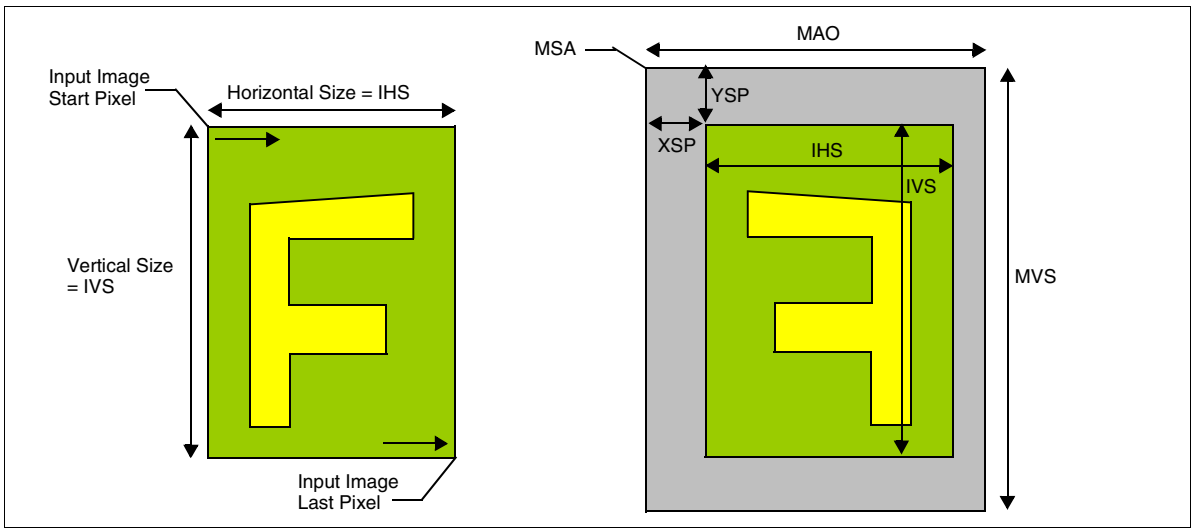


Figure 11-8: 0° Rotation and Mirror Enabled

90° Rotation and Mirror Enabled

For the Main Memory Write Path when 90° rotation is selected (REG[0504h] bits 2-1 = 01b) and Mirror is enabled (REG[0504h] bit 3 = 1b), input image data from the Host or Video interface is written to memory as follows.

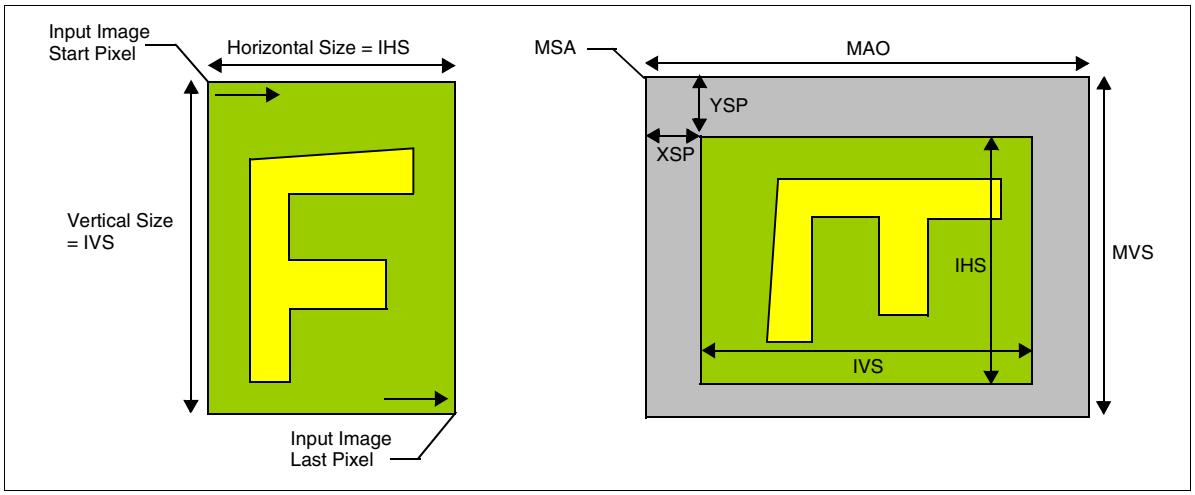


Figure 11-9: 90° Rotation and Mirror Enabled

Note

The IHS specifies the “vertical” size and the IVS specifies the “horizontal” size.

180° Rotation and Mirror Enabled

For the Main Memory Write Path when 180° rotation is selected (REG[0504h] bits 2-1 = 10b) and Mirror is enabled (REG[0504h] bit 3 = 1b), input image data from the Host or Video interface is written to memory as follows.

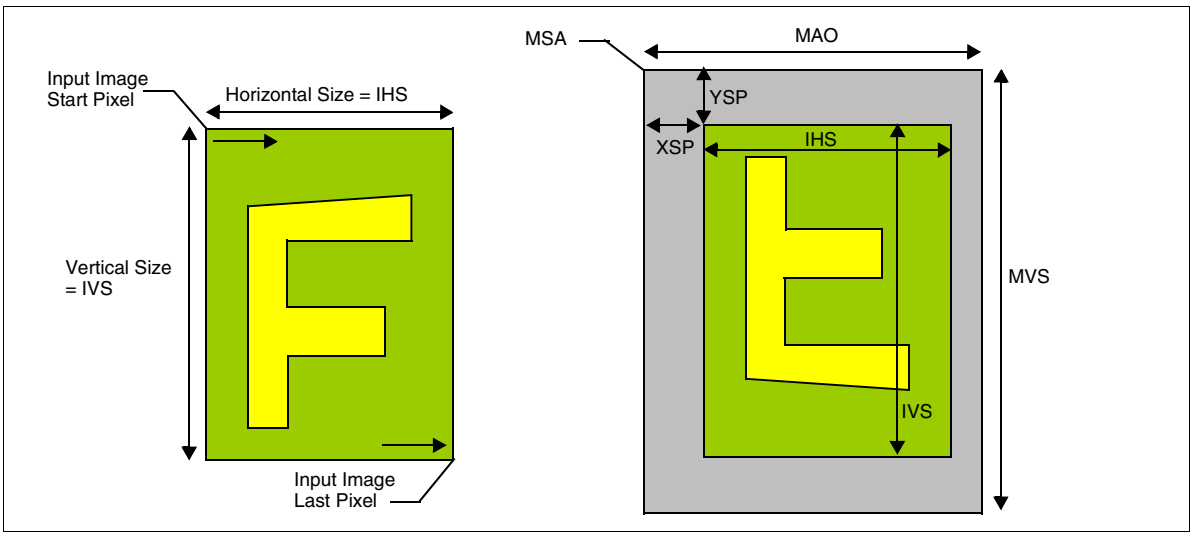


Figure 11-10: 180° Rotation and Mirror Enabled

270° Rotation and Mirror Enabled

For the Main Memory Write Path when 270° rotation is selected (REG[0504h] bits 2-1 = 11b) and Mirror is enabled (REG[0504h] bit 3 = 1b), input image data from the Host or Video interface is written to memory as follows.

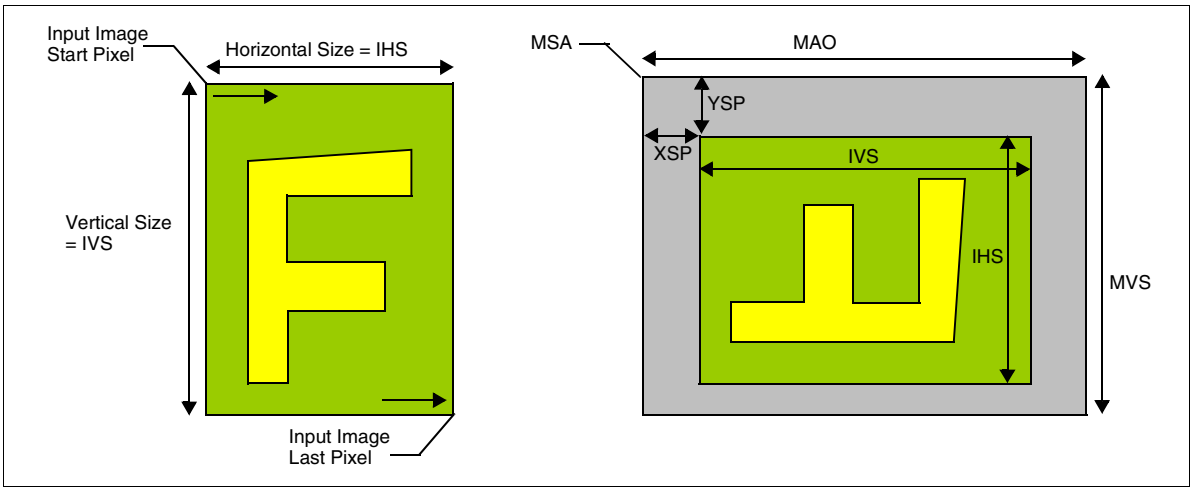


Figure 11-11: 270° Rotation and Mirror Enabled

Note
The IHS specifies the "vertical" size and the IVS specifies the "horizontal" size.

11.2.4 eIC (eco Image Codec)

When the Main Memory Write Path is used to write input image data from the Host or Video interface into memory, the image data can be processed before being written to memory. This function is useful when storing multiple large images for display. Both RGB and YUV data formats can be processed.

The eIC has two settings that must be configured:

- the unit that will be processed
- the method of processed

When the eIC is enabled (REG[0504h] bit 8 = 1b), each line can be processed (eIC line mode) or smaller pixel units can be processed (eIC partial mode). This setting is controlled by the eIC Unit Select bit (REG[0504h] bit 12).

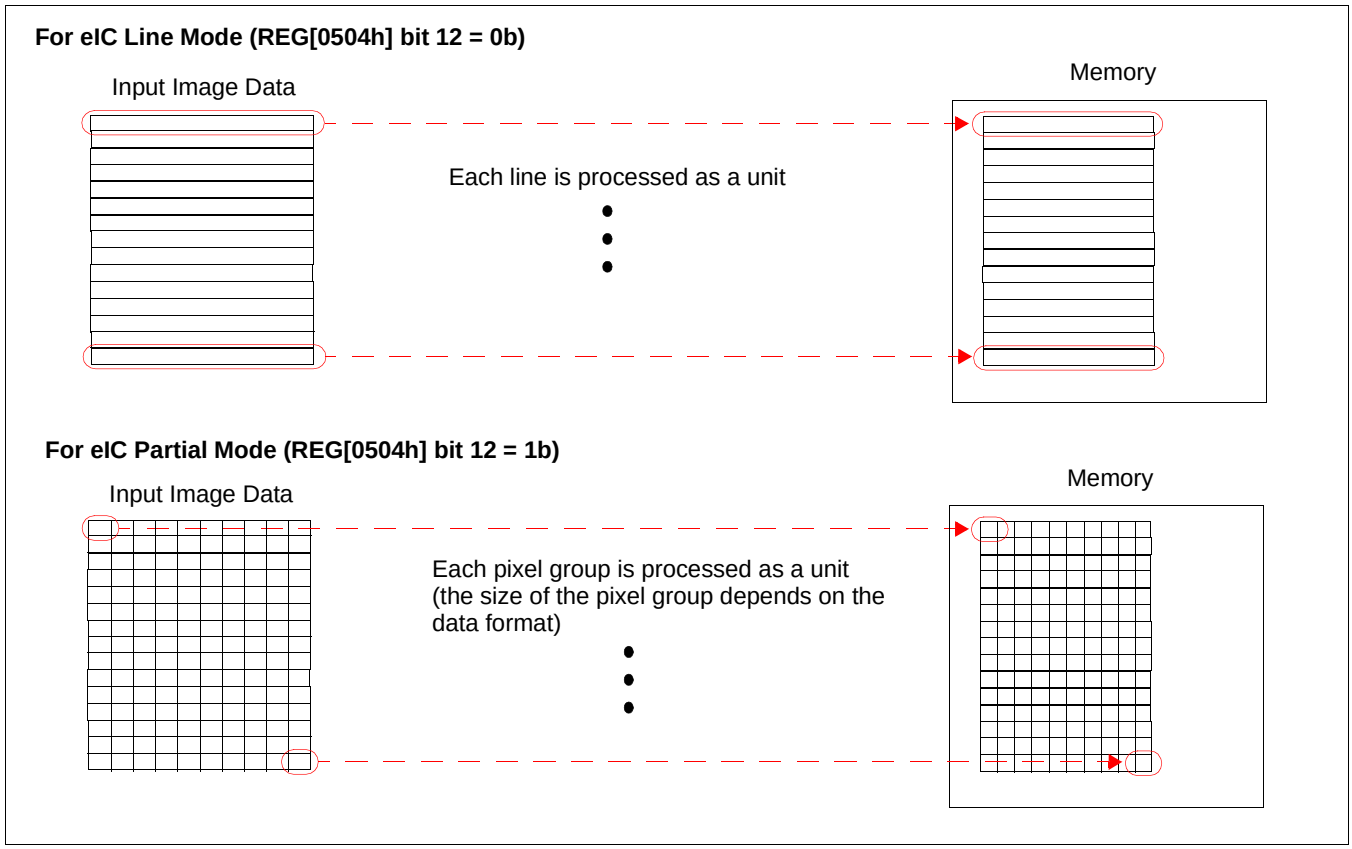


Figure 11-12: eIC Units: Line vs. Partial

When eIC partial mode is selected, processing is done in pixel groups according to the data format as follows.

Table 11-10: eIC Partial Mode: Pixel Groups

Data Format	Pixel Group Size
RGB 8:8:8	4 pixels
RGB 5:6:5	5 pixels
YUV 4:2:2	8 pixels
YUV 4:2:0	8 pixels

eIC line mode offers different processing than eIC partial mode, but eIC partial mode allows greater flexibility when updating image data. For example, if a portion of the image must be updated while eIC line mode is selected, all lines containing the new image data must be updated. When eIC partial mode is used, only the pixel groups that contain the new image must be updated.

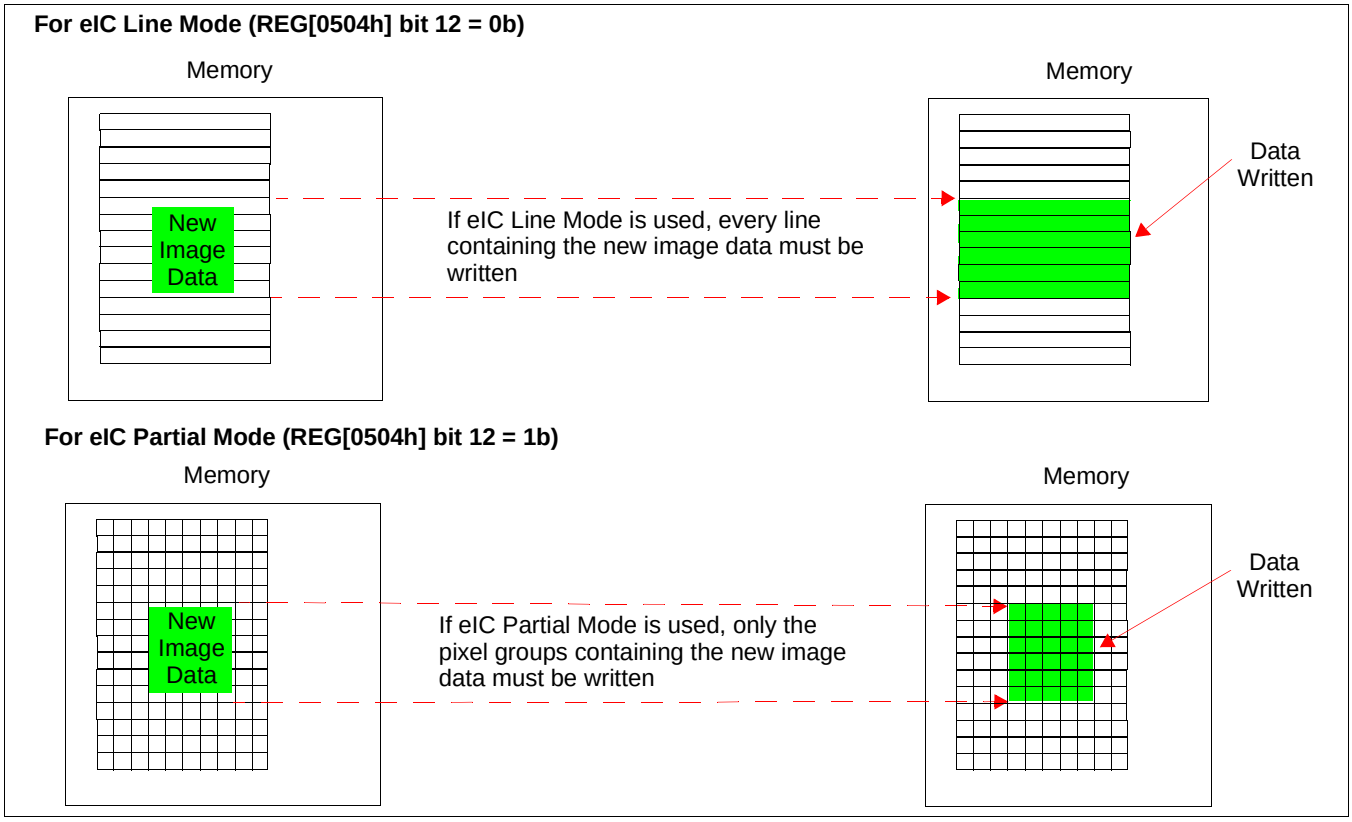


Figure 11-13: Updating Image Data: eIC Line Mode vs. Partial Mode

The second setting that must be configured is the eIC mode. There are two modes that can be selected using the eIC Mode Select bit, REG[0504h] bit 13. Adaptive eIC mode (REG[0504h] bit 13 = 0b) improves the quality of text in the display image. However, adaptive eIC mode is only available for RGB data formats and when eIC line mode is used. Normal eIC mode (REG[0504h] bit 13 = 1b) is available for all configurations.

eIC Rate

The following table summarizes the typical eIC rates for each configuration.

Table 11-11: eIC Rates

Format		eIC Line Mode		eIC Partial Mode	
		Original Size of 1 Line (bits)	**Size of 1 Line (bits)**	**Original Size (bits)**	**Size (bits)**
RGB 8:8:8		24 x n (Note 1)	12 x n + 12	96 per 4 pixels	64
RGB 5:6:5		16 x n	12 x n + 4	80 per 5 pixels	64
YUV 4:2:2 YUV 4:2:0	Y	8 x n	4 x n + 8	64 per 8 pixels	40 (Note 2)
	UV	8 x n	4 x n + 8	64 per 8 pixels	40 (Note 2)

Note

1. n is the number of pixels in one line.
2. The memory of 128bit is occupied with (120bit) in each 24pixel.

eIC Options Summary

The following table summarizes the eIC options that are available.

Table 11-12: eIC Line Mode, Partial Mode

	eIC Disabled	**eIC Line Mode**	**eIC Partial Mode**
Supports Format in Memory	RGB 8:8:8, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0	RGB 8:8:8, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0	RGB 8:8:8, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0
Adaptive Mode	X	√ (only RGB)	X
Rotation	√	X	√
Mirror	√	X	√
Image Scroll	√	√	√
Transparency, Alpha Blending	√ (only RGB)	√ (only RGB)	√ (only RGB)
Unit of Ca of image in memory	For RGB: 1 pixel For YUV: 2 pixels	1 line	For RGB 8:8:8: 4 pixels For RGB 6:6:6: 4 pixels For RGB 5:6:5: 5 pixels For YUV 4:2:2: 8 pixels For YUV 4:2:0: 8 pixels
Start of image in horizontal direction of LCD display position (cutting out display)	For RGB: 1 pixel For YUV: 2 pixels	Only top of Line	For RGB 8:8:8: 4 pixels For RGB 6:6:6: 4 pixels For RGB 5:6:5: 5 pixels For YUV 4:2:2: 8 pixels For YUV 4:2:0: 8 pixels

11.3 Sub Memory Write Path

The Sub Memory Write Path can be used to write image data from either the Host or Video interface to memory. The Sub Memory Write Path can be double buffered (see Section 11.4, “Double Buffering” on page 291), but does not include the other functions that the Main Memory Write Path provides.

For an overview of the write paths, see Figure 11-1: “Write Path Overview,” on page 276.

11.4 Double Buffering

Double buffering is available for both the Main Memory Write Path and Sub Memory Write Path. It is intended for writing streaming image data that will be displayed in either the PIP1 or PIP2 window. Image data for the Main window must not be double buffered.

When double buffering is enabled, two memory start addresses are used and input image data is alternately written between the two addresses. This allows the display path to read image data from the buffer that is not being written to and avoids the “tearing effect” that may be visible when only one buffer is used. The following figure shows an example of this technique.

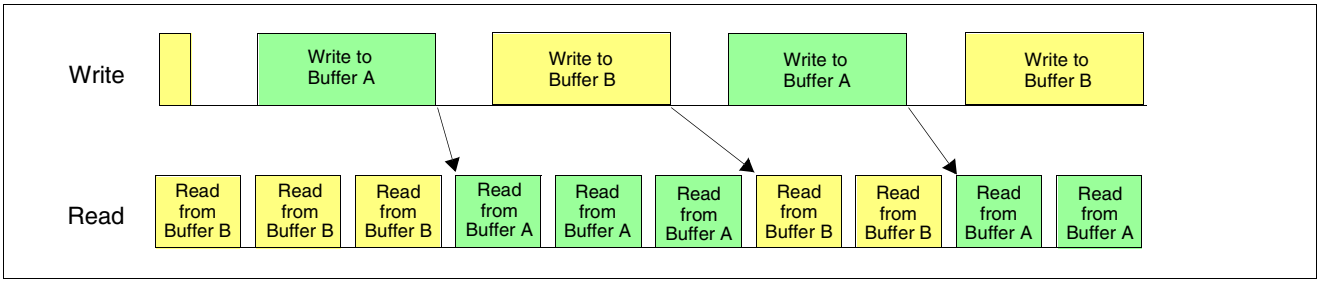


Figure 11-14: Alternating Write and Read Accesses using Double Buffering

When double buffering is enabled, a memory start address must be configured for each buffer (Buffer A and Buffer B). All other settings are shared for both buffers (see Section 11.1, “Configuring the Write Paths” on page 277).

Table 11-13: Write Path Double Buffer Memory Start Address Registers

Write Path	Buffer A	Buffer B
Main Memory	REG[0508h], REG[050Ch]	REG[0510h], REG[0514h]
Sub Memory	REG[0584h], REG[0588h]	REG[058Ch], REG[0590h]

The following figure shows the data flow from the Host or Video interface, through the write path with double buffering enabled, and out to the LCD interface. The Host can determine which buffer is currently being written using the Double Buffer Status bits (REG[0504h] bit 7 for Main Memory, REG[0580h] bit 7 for Sub Memory).

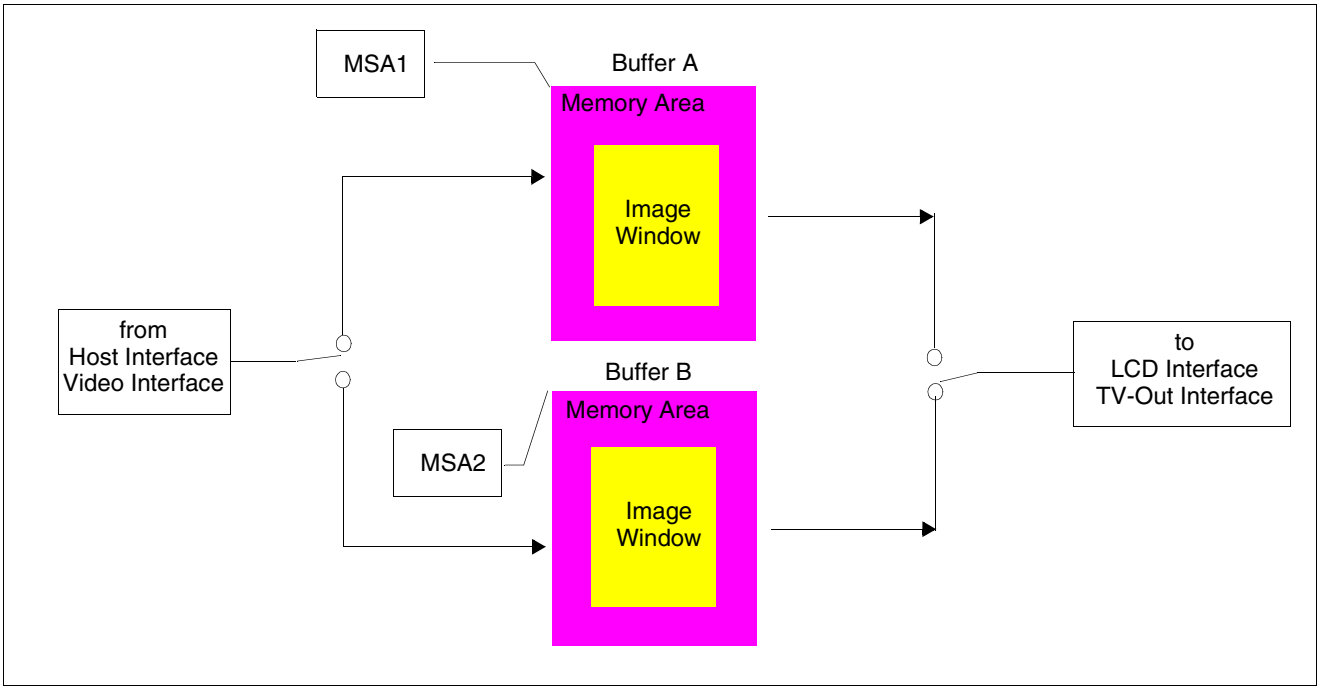


Figure 11-15: Write Path Data Flow for Double Buffering

12 Displaying Image Data from Memory

There are three paths that can be used for displaying image data from memory to the LCD and TV-Out interfaces.

- Main Window (includes Main1 and Main2)
- PIP1 Window
- PIP2 Window

All three display paths can be used simultaneously to output image data to the LCD1, LCD2, or TV-Out interface. An additional mode allows the Main Window to be output to the LCD1 interface while the PIP1 and PIP2 windows are output to the TV-Out interface. For further information on the LCD and TV-Out interfaces and supported modes, see Section 15, “LCD and TV Interface” on page 370.

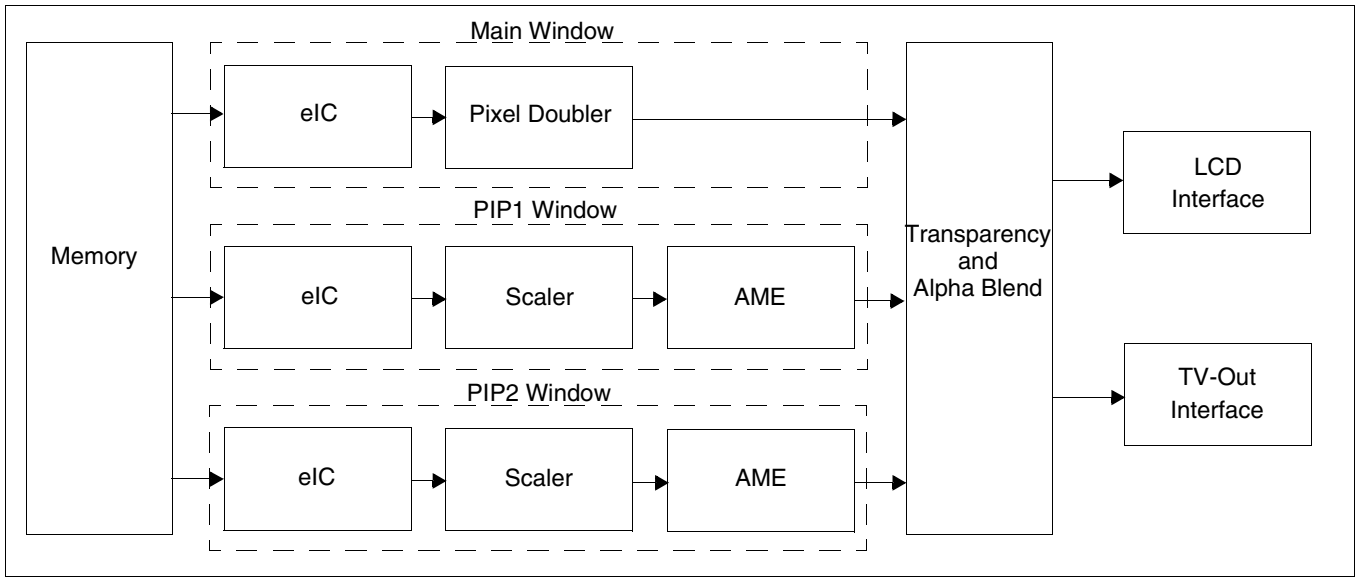


Figure 12-1: Display Path Overview

All three display paths support eIC processing (if required), transparency, and alpha blending functions. The image data for the Main window path can be expanded for output using Pixel Doubling. Pixel doubling can be controlled independently for the horizontal and vertical directions and “doubles” the size of the output image.

The image data for the PIP windows can be reduced or expanded for output using the scalers. The image data for the PIP window can also be adjusted for contrast, chroma, and gamma using AME (Auto Movie Enhancement). AME cannot be used simultaneously for both the PIP1 and PIP2 windows.

The following table summarizes the functions available for the display paths.

Table 12-1: Display Path Function Summary

Display Path	Data Formats	eIC	Scaling	AME	Transparency and Alpha Blending
Main Window (Note 1)	RGB 8:8:8, RGB 5:6:5	√	Pixel Doubling	X	√
PIP1 Window	RGB 8:8:8, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0	√	Scaler	√ (Note 2)	√
PIP2 Window	RGB 8:8:8, RGB 5:6:5, YUV 4:2:2, YUV 4:2:0	√	Scaler	√ (Note 2)	√

Note

1. Main Window settings apply for both the Main1 and Main2 windows.
2. AME cannot be used simultaneously for both the PIP1 and PIP2 windows.

12.1 Configuring the Display Paths

The size of the memory area and the image window must be configured for each display path. These settings are similar to the parameters used for configuring the Write Paths (see Section 11.1, “Configuring the Write Paths” on page 277).

The size of the memory area is configured by specifying a start address (MSA), line address offset (MAO), and vertical size (MVS). The image window is defined using a horizontal size (IHS), vertical size (IVS), and start position (XSP, YSP). These parameters must be individually set for each display path: Main1, Main2, PIP1, and PIP2.

The memory area can be set to a larger area than required for the image window. The following figure shows the display path parameters that must be configured.

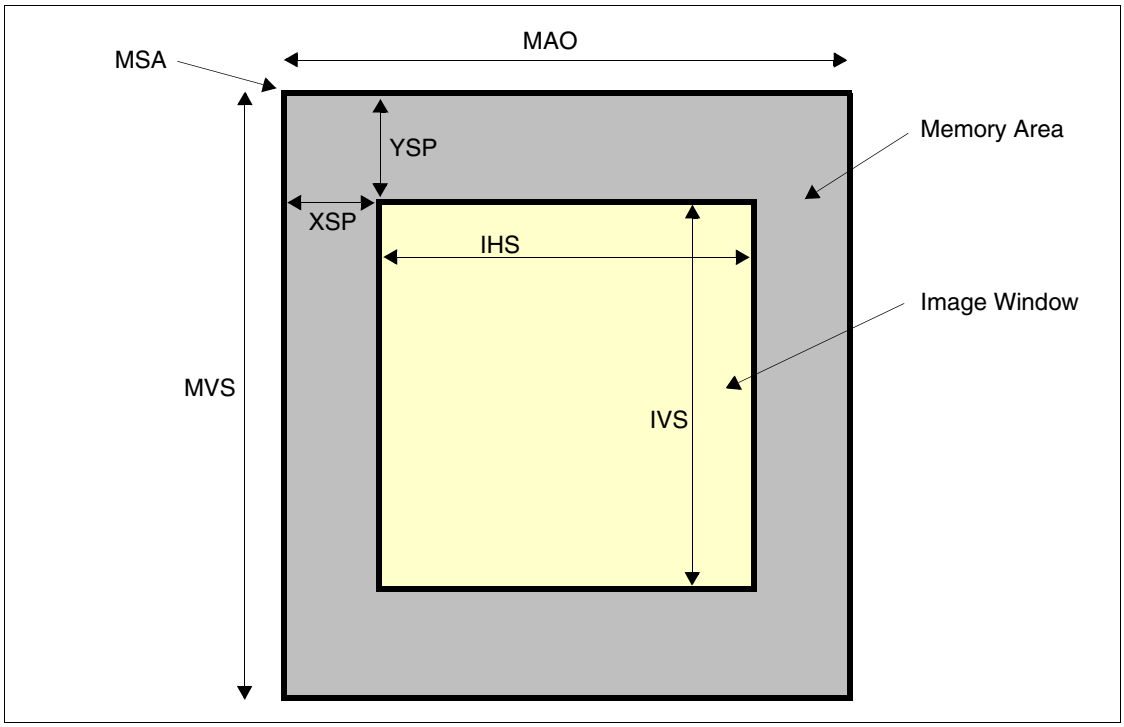


Figure 12-2: Display Path Parameters

When the display image is stored in YUV 4:2:2 or YUV 4:2:0 format, the Y and UV data are stored separately which requires two memory start addresses (MSA). For RGB format image data, only one memory start address is used. The following table provides a summary of the minimum and maximum values and registers used for display path.

Table 12-2: Display Path Parameter Summary

Symbol	Description	Min	Max	Units	Main1 Window Register	Main2 Window Register	PIP1 Window Register	PIP2 Window Register
MSA	Memory Start Address	—	—	bytes	REG[0684h]	REG[06A8h]	REG[0714h] REG[0718h]	REG[0814h] REG[0818h]
MAO	Memory Line Address Offset	64	4032	bytes	REG[0688h]	REG[06ACh]	REG[0724h]	REG[0824h]
MVS	Memory Vertical Size	4	1024	lines	REG[068Ch]	REG[06B0h]	REG[0728h]	REG[0828h]
IHS	Image Horizontal Size	16	1024	pixels	REG[0690h]	REG[06B4h]	REG[072Ch]	REG[082Ch]
IVS	Image Vertical Size	1	1024	lines	REG[0694h]	REG[06B8h]	REG[0730h]	REG[0830h]
XSP	Image X Start Position	0	1023	pixels	REG[0698h]	REG[06BCh]	REG[0734h]	REG[0834h]
YSP	Image Y Start Position	0	1023	lines	REG[069Ch]	REG[06C0h]	REG[0738h]	REG[0838h]

Many of the display path parameters have alignment or resolution restrictions that determine which values can be programmed. For all cases, the line address offset (MAO) must be 64 byte aligned and the memory vertical size (MVS) must be set to a multiple of 4 pixels. Restrictions for all other parameters are determined by the combination of data format, eIC mode, and which display path is configured. Note that Main Windows do not support YUV data formats. The following tables show the display path parameter restrictions that must be observed for each possible combination.

Table 12-3: PIP1 and PIP2 Windows: eIC Disabled

Symbol	Description	Data Format			
		RGB 8:8:8	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	2 Pixel	2 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel
XSP	Image X Start Position	2 Pixel	1 Pixel	2 Pixel	2 Pixel
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Table 12-4: PIP1 and PIP2 Windows: eIC Line Mode

Symbol	Description	Data Format			
		RGB 8:8:8	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	2 Pixel	2 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel
XSP	Image X Start Position	Note	Note	Note	Note
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Note

When eIC line mode is used, XSP must equal 0.

Table 12-5: PIP1 and PIP2 Windows: eIC Partial Mode

Symbol	Description	Data Format			
		RGB 8:8:8	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	64 byte	64 byte
MVS	Memory Vertical Size	4 Pixel	4 Pixel	4 Pixel	4 Pixel
IHS	Image Horizontal Size	2 Pixel	2 Pixel	2 Pixel	2 Pixel
IVS	Image Vertical Size	1 Pixel	1 Pixel	1 Pixel	2 Pixel
XSP	Image X Start Position	4 Pixel	5 Pixel	8 Pixel	8 Pixel
YSP	Image Y Start Position	1 Pixel	1 Pixel	1 Pixel	2 Pixel

Table 12-6: Main Windows: eIC Disabled

Symbol	Description	Data Format			
		RGB 8:8:8	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	—	—
MVS	Memory Vertical Size	4 Pixel	4 Pixel	—	—
IHS	Image Horizontal Size	1 Pixel	1 Pixel	—	—
IVS	Image Vertical Size	1 Pixel	1 Pixel	—	—
XSP	Image X Start Position	2 Pixel	1 Pixel	—	—
YSP	Image Y Start Position	1 Pixel	1 Pixel	—	—

Table 12-7: Main Windows: eIC Line Mode

Symbol	Description	Data Format			
		RGB 8:8:8	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	—	—
MVS	Memory Vertical Size	4 Pixel	4 Pixel	—	—
IHS	Image Horizontal Size	1 Pixel	1 Pixel	—	—
IVS	Image Vertical Size	1 Pixel	1 Pixel	—	—
XSP	Image X Start Position	Note	Note	—	—
YSP	Image Y Start Position	1 Pixel	1 Pixel	—	—

Note
When eIC line mode is used, XSP must equal 0.

Table 12-8: Main Windows: eIC Partial Mode

Symbol	Description	Data Format			
		RGB 8:8:8	RGB 5:6:5	YUV 4:2:2	YUV 4:2:0
MA0	Memory Line Address Offset	64 byte	64 byte	—	—
MVS	Memory Vertical Size	4 Pixel	4 Pixel	—	—
IHS	Image Horizontal Size	1 Pixel	1 Pixel	—	—
IVS	Image Vertical Size	1 Pixel	1 Pixel	—	—
XSP	Image X Start Position	4 Pixel	5 Pixel	—	—
YSP	Image Y Start Position	1 Pixel	1 Pixel	—	—

12.2 Main Window

The S1D13774 Main window can consist of up to two windows (Main1 and Main2). The windows cannot overlap and must observe the restrictions shown in Section 12.2.1, "Main Window Restrictions" on page 299. Each window is independently configured using an x,y coordinate to determine the location of the window relative to the top left corner of the panel (0,0), and height and width registers to specify the size of each window.

The size of the entire display image is determined by the HDP (Horizontal Display Period) and VDP (Vertical Display Period) settings. Any portion of the display not covered is set to the background color.

The main window(s) image data is stored in display memory in either RGB 8:8:8 or RGB 5:6:5 format starting at the specified display start address.

The Main window image data can also be expanded during output using the Pixel Doubling function. For more information, see Section 12.2.3, "Pixel Doubling" on page 300.

The following figure shows the registers used to configure the x,y start positions and sizes of the Main windows.

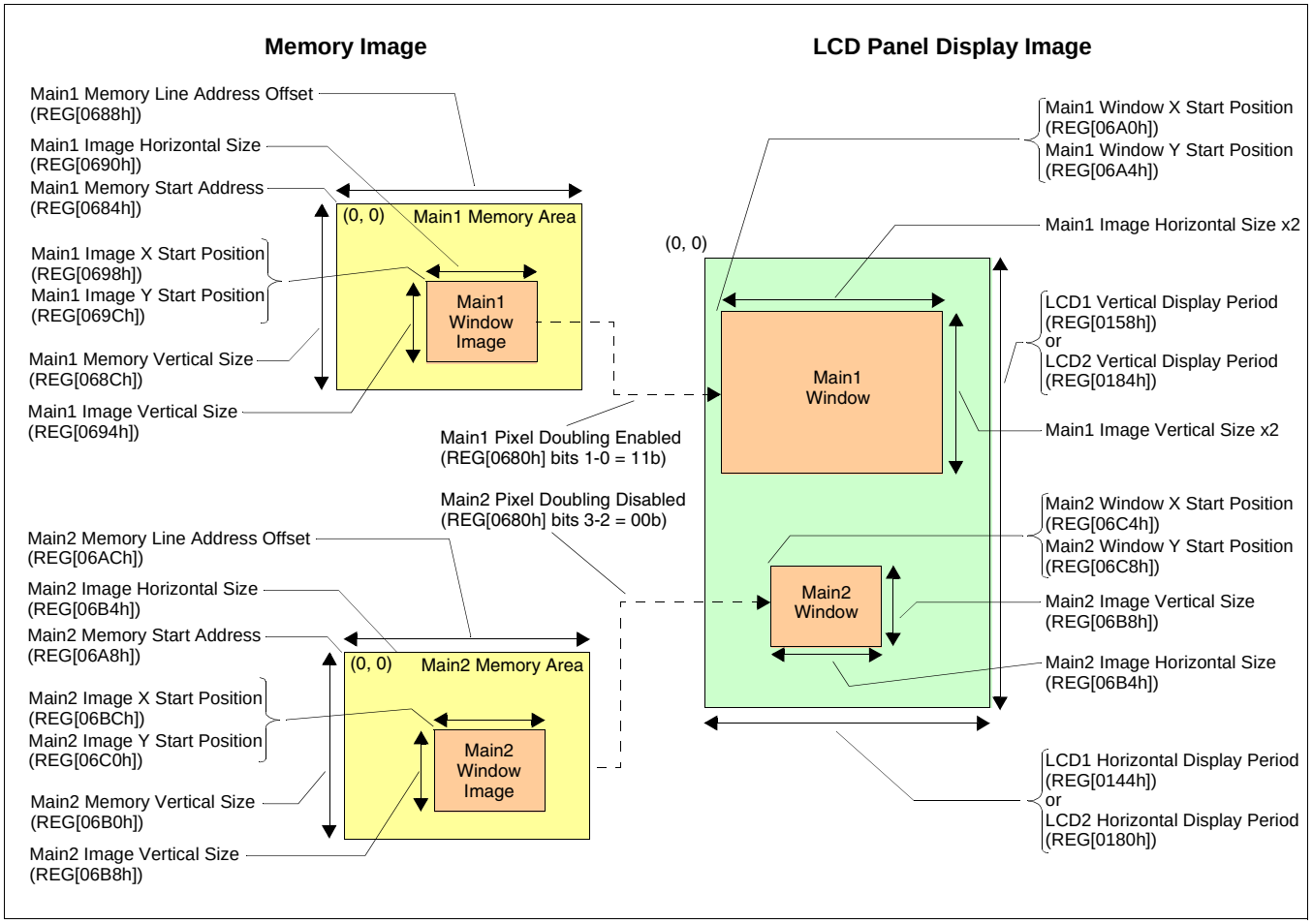


Figure 12-3: Configuring the Main Window

12.2.1 Main Window Restrictions

The following restrictions must be considered when configuring the Main windows.

- The right edge of the main window (Main1 or Main2) must not exceed the width of the display panel as defined by HDP, in pixels.
- The bottom edge of the main window (Main1 or Main2) must not exceed the height of the display panel as defined by VDP, in lines.
- The bottom edge of the Main1 window must not exceed the top edge of the Main2 window, in lines.

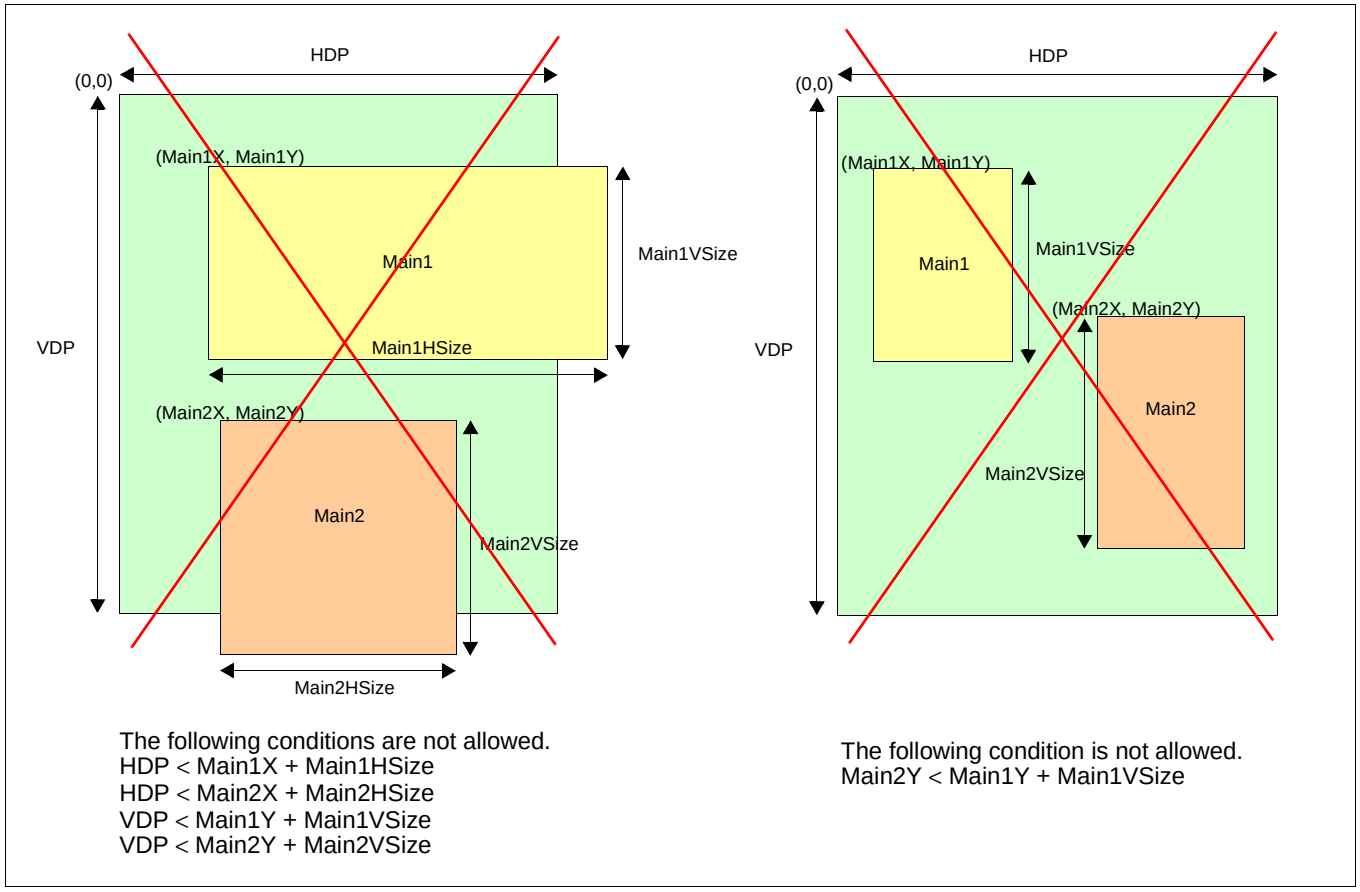


Figure 12-4: Main Window Restrictions

12.2.2 Main Window Input Format

The image data for the Main windows is stored as either RGB 8:8:8 or RGB 5:6:5 format. If the image data is stored in RGB 5:6:5 format, it is converted into RGB 8:8:8 before being processed.

Table 12-9: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5							RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

12.2.3 Pixel Doubling

The image data for both main windows can be expanded using Pixel Doubling allowing easy migration to larger panel sizes using existing image data. The following figure shows an example where pixel doubling is enabled for the Main1 Window.

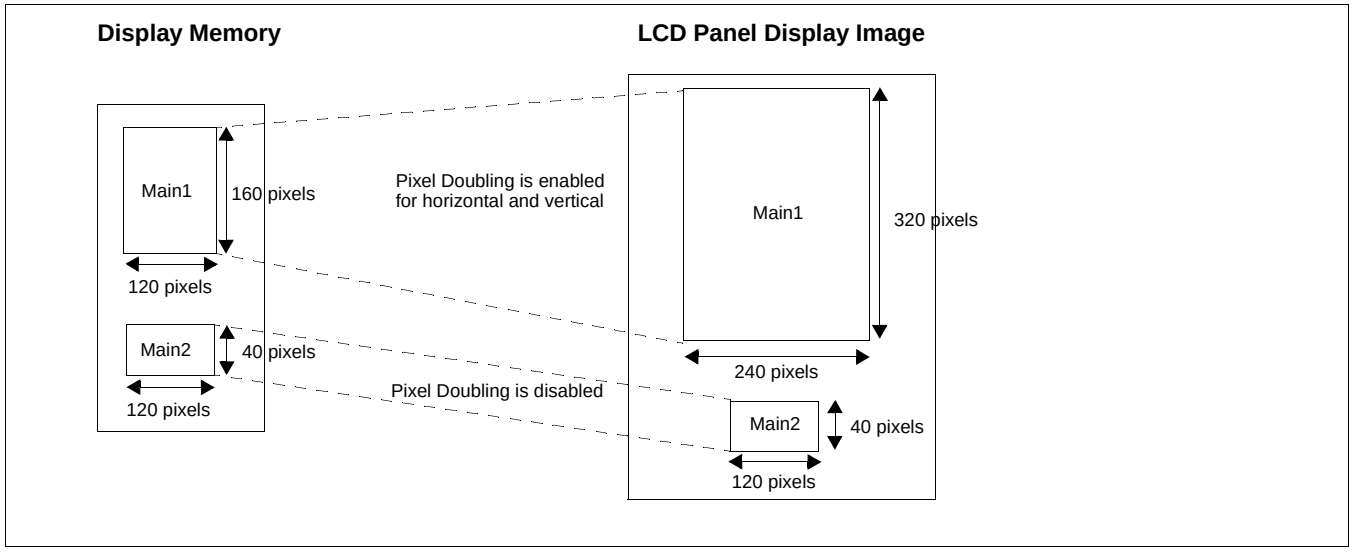


Figure 12-5: Main Window Pixel Doubling Example

Note

The Main window restrictions contained in Section 12.2.1, “Main Window Restrictions” on page 299 apply to the “Pixel Doubled” dimensions. For example, enabling horizontal pixel doubling cannot cause the right edge of the Main1 window to exceed the HDP.

Pixel Doubling can be independently controlled in both the horizontal and vertical directions for each Main window using the following registers. For further information on each bit, refer to the bit descriptions in Section 9.4.15, "Main Window Configuration Registers" on page 208

Table 12-10: Main Window Pixel Doubling Registers

Main Window	Horizontal Enable	Vertical Enable
Main 1	REG[0680h] bit 0	REG[0680h] bit 1
Main 2	REG[0680h] bit 2	REG[0680h] bit 3

12.3 PIP Windows

The S1D13774 supports two PIP Windows (PIP1 and PIP2). Each window can overlap the other PIP window and the Main windows. The PIP windows must observe the restrictions shown in Section 12.3.1, "PIP Window Restrictions" on page 303. Each PIP window is independently configured by defining the start and end x,y coordinates of the window relative to the top left corner of the panel (0,0).

The size of the entire display image is determined by the HDP (Horizontal Display Period) and VDP (Vertical Display Period) settings. Any portion of the display not covered by a PIP window or the Main window (see Section 12.2, "Main Window" on page 298), is set to the background color.

The image data for the PIP windows is stored in display memory as RGB 8:8:8, RGB 5:6:5 YUV 4:2:2, or YUV 4:2:0 format starting at the specified display start address. Before display output all image data is converted to RGB 8:8:8. For details on the conversion process, see Section 12.3.2, "PIP Window Input Format" on page 303.

The PIP windows also support the following features.

- Scaling allows expansion or reduction of the PIP window image data.
- AME (Auto Movie Enhancement) provides chroma, contrast, and gamma adjustments for the PIP window image data. Note that AME cannot be used for both PIP and PIP2 simultaneously.
- Double buffering reduces the tearing effect for streaming image data displayed in the PIP windows.
- Panorama Scaling allows a separate expansion rate to be set for up to five areas in the vertical direction or the horizontal direction. Note that Panorama Scaling is available only for the PIP2 window.

The following figure shows the registers used to configure the x,y start positions and sizes of the PIP windows.

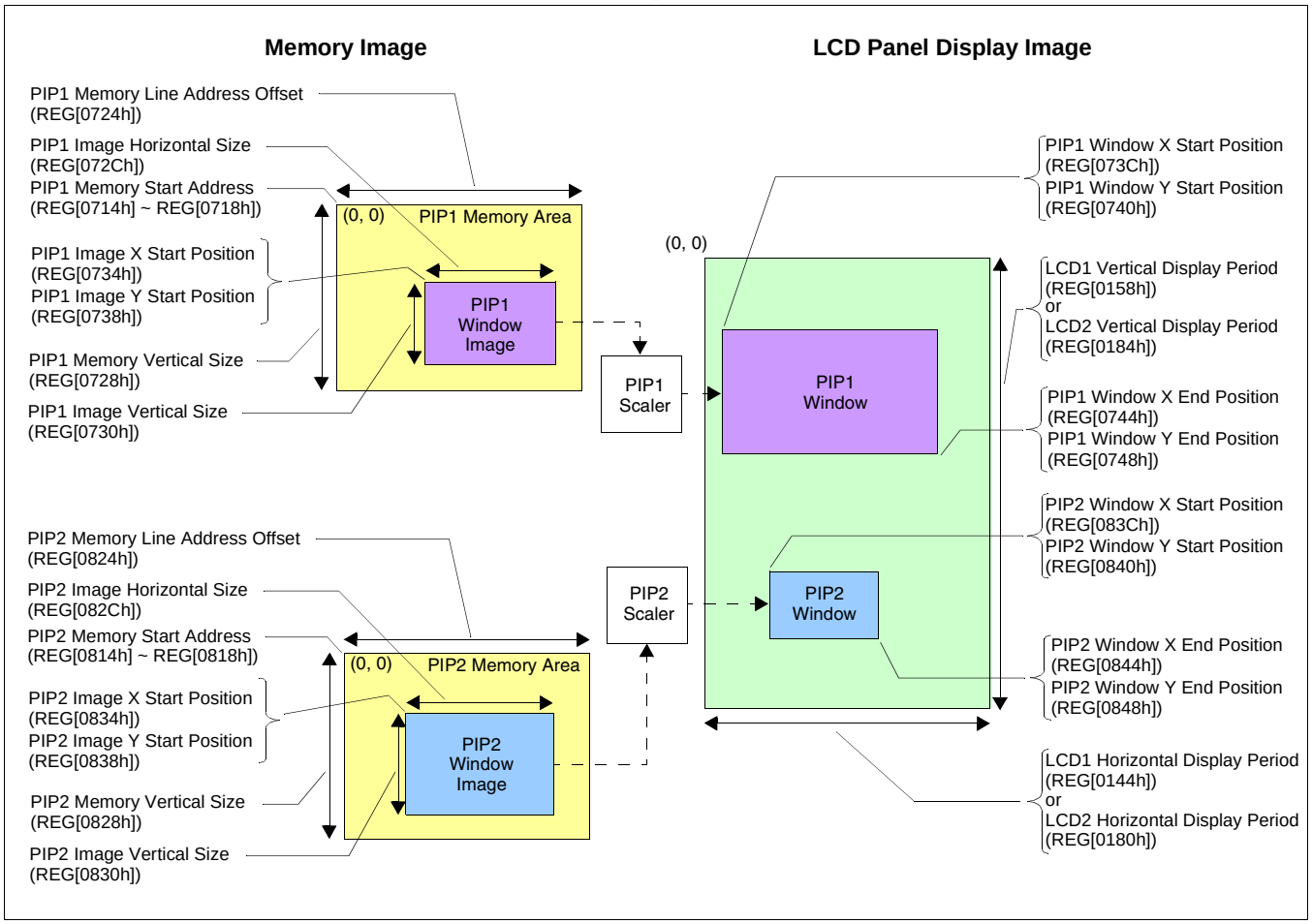


Figure 12-6: Configuring the PIP Windows

12.3.1 PIP Window Restrictions

The following restrictions must be considered when configuring the PIP windows.

- The right edge of the PIP window (PIP1 or PIP2) must not exceed the total width of the display panel as defined by HDP, in pixels.
- The bottom edge of the PIP window (PIP1 or PIP2) must not exceed the total height of the display panel as defined by VDP, in lines.

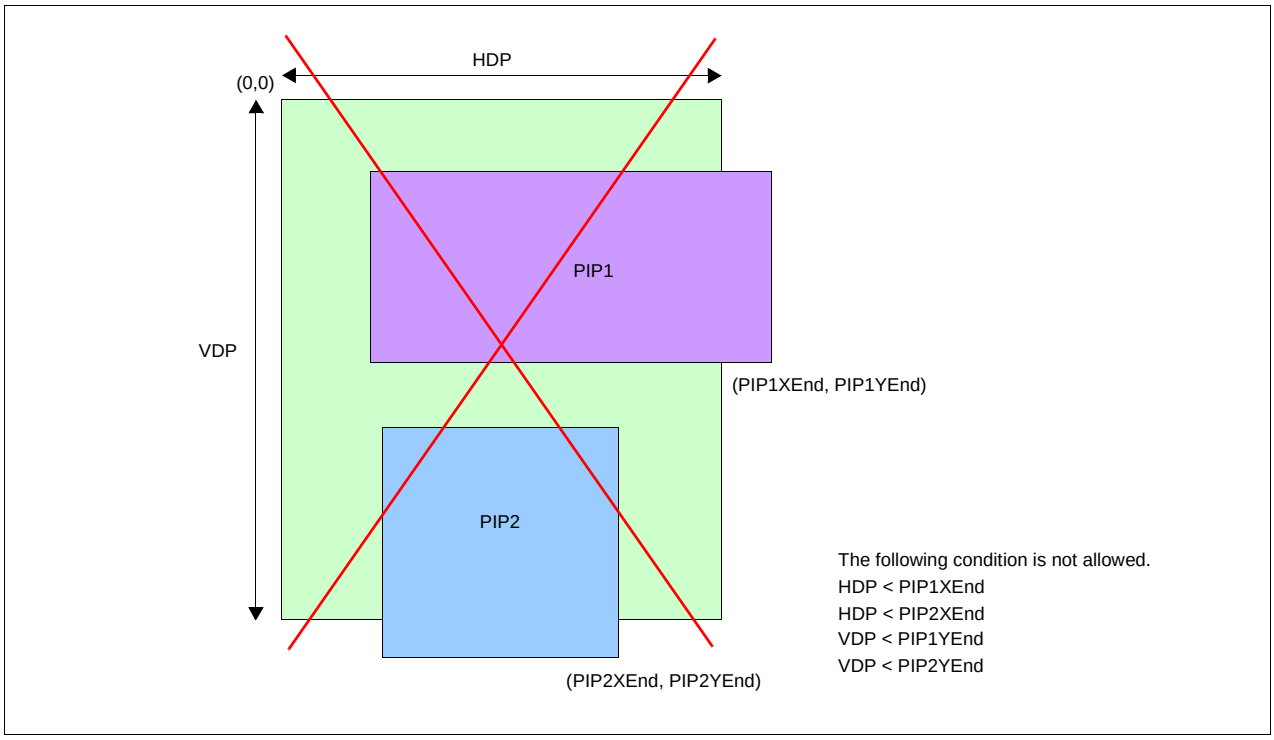


Figure 12-7: PIP Window Restrictions

12.3.2 PIP Window Input Format

The image data for the PIP windows is stored as either RGB 8:8:8, RGB 5:6:5, YUV 4:2:2, or YUV 4:2:0 format. If the image data is stored in RGB 5:6:5 format, it is converted into RGB 8:8:8 before being output to the display.

Table 12-11: RGB 5:6:5 to RGB 8:8:8 Conversion

RGB 5:6:5							RGB 8:8:8							
R4	R3	R2	R1	R0		→	R4	R3	R2	R1	R0	R4	R3	R2
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B4	B3	B2	B1	B0		→	B4	B3	B2	B1	B0	B4	B3	B2

YUV 4:2:2 and YUV 4:2:0 are converted to RGB according to the ITU-R BT.470-6 System B and G conversion type recommendation using the following expressions.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1.000 & 0.000 & 1.402 \\ 1.000 & -0.344 & -0.714 \\ 1.000 & 1.772 & 0.000 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

Note
When YUV offset data is stored in memory, the YUV offset data is converted to YUV no offset data before it is converted to RGB.

12.3.3 Scaling

The PIP1 and PIP2 windows each include an independent scaler which can be used to expand or reduce the PIP window source image data. The Filter Scaling Mode determines whether the scaler performs over/down sample scaling, or bi-cubic scaling.

Over/down sample scaling reduces the size of an image by removing pixels and expands the size of an image by inserting pixels. When over/down sample scaling is selected, the source image data can be expanded up to 8x or reduced down to 1/8x.

Bi-cubic scaling uses an interpolation method to reduce artifacting caused by large scaling. When bi-cubic scaling is selected, the source image data can be expanded up to 8x or reduced down to 1/2x. Also available for this mode is the Edge Enhance function. Edge enhance sharpens the image by automatically detecting the outline of objects in the image. The strength of edge enhancing can be controlled by software.

The following restrictions must be observed when configuring both the PIP1 and PIP2 scalers.

- The minimum source image size is 4x4 pixels.
- The maximum source image size is 864x1024 pixels.

The PIP2 window also supports Panorama Scaling (or wide scaling mode). Panorama scaling allows scaling with a variable scaling ratio in either the horizontal or vertical direction. Panorama scaling does not support simultaneous horizontal/vertical scaling. For further information on panorama scaling, see Section 12.6, “PIP2 Panorama Scaling” on page 327.

The following table summarizes the available PIP window scaler functions.

Table 12-12: PIP Window Scaler Function Summary

Scaling Method	Magnification	Panorama Scaling (Note 1)	Edge Enhance	For Interlace (Note 2)
Bi-Cubic	8x ~ 1/2x	√ (Horizontal or Vertical)	√	x
Over/Down Sample	8x ~ 1/8x	√ (Horizontal Only)	x	√

Note

1. Panorama scaling is available for the PIP2 window only.
2. When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b), bi-cubic scaling cannot be used.

When using the scaler, three sizes are important: the Source Image size, the Resulting Image size, and the PIP window size. The horizontal and vertical scaling is applied to the source image to produce the resulting image which is displayed in the PIP window. Depending on the relationship between the resulting size and the PIP window size, the following cases are possible.

- Case 1 - The resulting image is the same size as the defined PIP window. In this case, the PIP image is positioned at coordinate 0,0 of the PIP window and fills the entire area of the PIP window. This case takes place when both of the following formulas are true.

  PIP Image Horizontal Size = (PIP Window X End Position - PIP Window X Start Position)
  PIP Image Vertical Size = (PIP Window Y End Position - PIP Window Y Start Position)

- Case 2 - The resulting image is larger than the defined PIP window. In this case, the PIP image is positioned at coordinate 0,0 of the PIP window, but it is trimmed to the size of the PIP window. Any image data outside of the PIP window is not displayed. This case takes place when either of the following formulas are true.

  PIP Image Horizontal Size > (PIP Window X End Position - PIP Window X Start Position)
  PIP Image Vertical Size > (PIP Window Y End Position - PIP Window Y Start Position)

The following figure shows examples for each case.

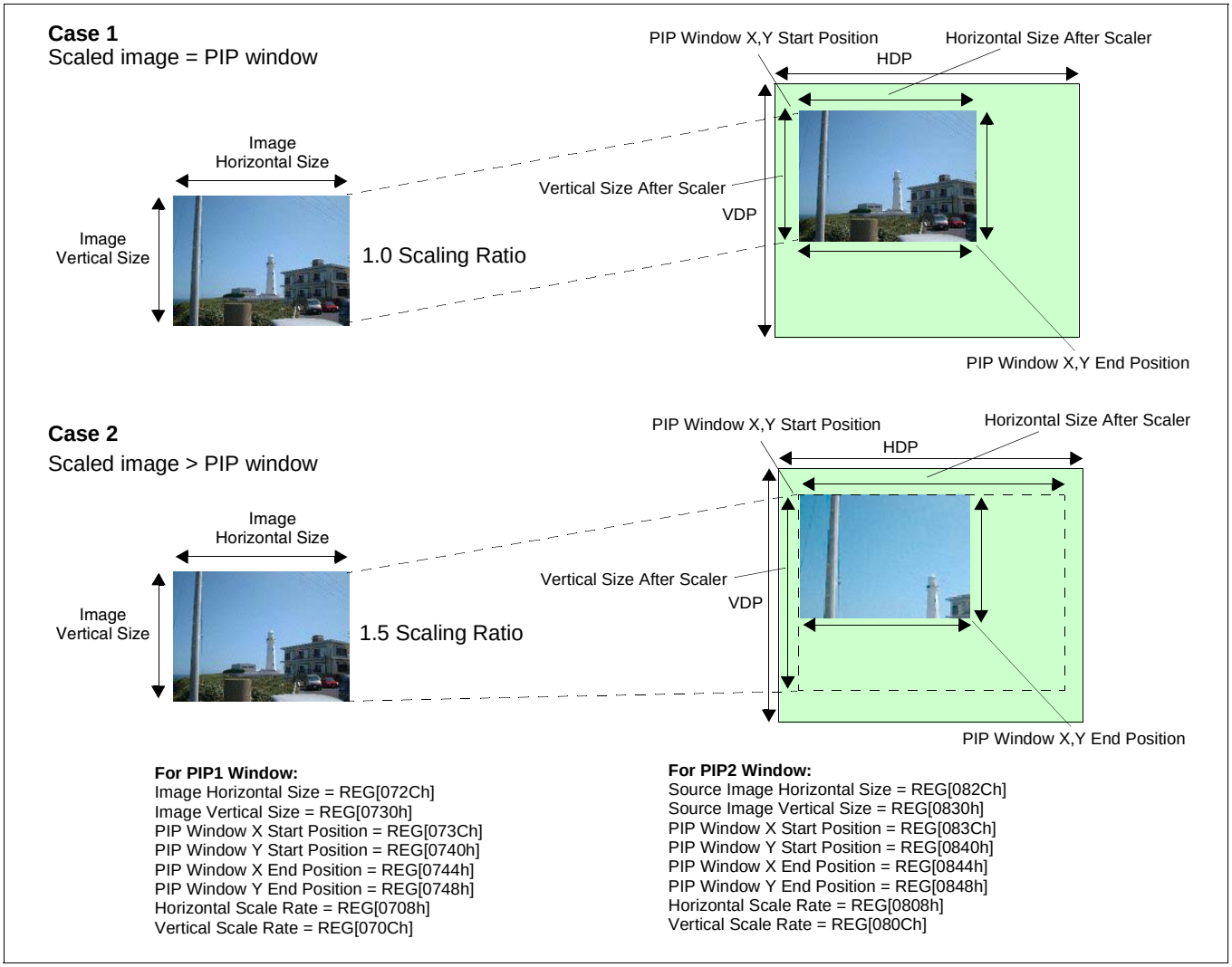


Figure 12-8: Displaying Scaled Images in a PIP Window

To scale the source image display in the PIP window use the following procedure.

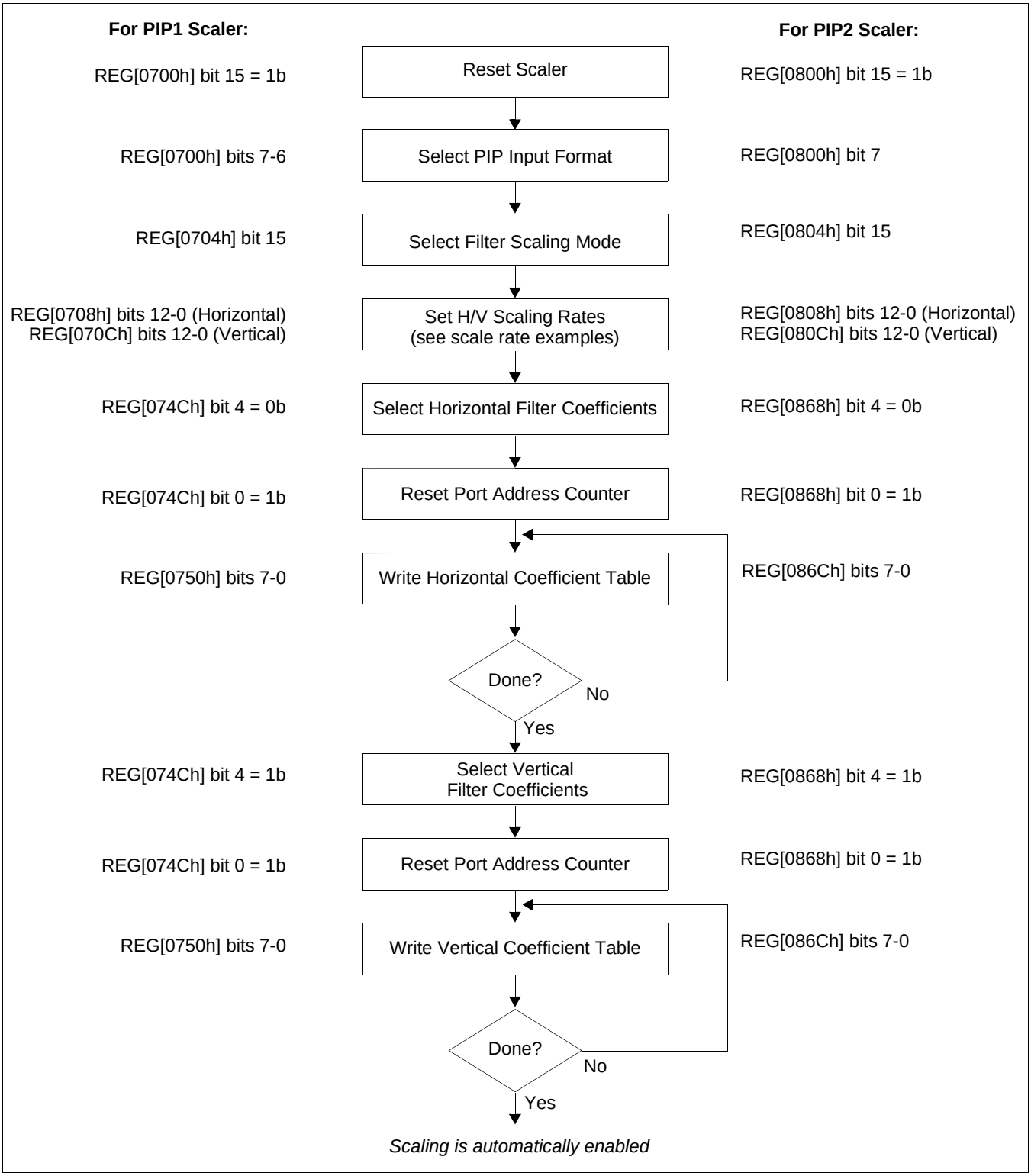


Figure 12-9: Scaler Programming Procedure

The PIP1 and PIP2 scalers support independent scaling rates for both the horizontal and vertical directions. The following calculations provides examples for scale-down and scale-up operations.

Horizontal Scale Rate

To scale-down the source image using a scaling ratio of 0.7, program the Horizontal Scale Rate register (REG[0708h] for PIP1, REG[0808h] for PIP2) as follows.

Horizontal Scale Rate = 1024 x (1 ÷ 0.7)
= 1462
= 5B6h

To scale-up the source image using a scaling ratio of 1.5, program the Horizontal Scale Rate register (REG[0708h] for PIP1, REG[0808h] for PIP2) as follows.

Horizontal Scale Rate = 1024 x (1 ÷ 1.5)
= 682
= 2AAh

Vertical Scale Rate

To scale-down the source image using a scaling ratio of 0.7, program the Vertical Scale Rate register (REG[070Ch] for PIP1, REG[080Ch] for PIP2) as follows.

Vertical Scale Rate = 1024 x (1 ÷ 0.7)
= 1462
= 5B6h

To scale-up the source image using a scaling ratio of 1.5, program the Horizontal Scale Rate register (REG[070Ch] for PIP1, REG[080Ch] for PIP2) as follows.

Vertical Scale Rate = 1024 x (1 ÷ 1.5)
= 682
= 2AAh

12.4 Alpha Blend and Transparency

12.4.1 Alpha Blend and Transparency using Main, PIP1, PIP2 Windows

When the display output port is configured for single display LCD1, LCD2, or TV-Out modes (REG[0604h] bits 15-12 ≠ 1011b), the Main, PIP1, and PIP2 can be combined using the Alpha Blend and Transparency functions. The following table shows the available configurations.

Table 12-13: Main, PIP1, and PIP2 Window Alpha Blending

Case	Top Layer	Middle Layer	Bottom Layer	REG[0604h]			
				bits 6-5	bit 3	bit 2	bit 1 / bit 0
				Layer Mode	PIP2 Enable	PIP1 Enable	Main1 or Main2 Enable
Case1	Main Window	PIP1 Window		X0b	0b	1b	1b
Case2	PIP1 Window	Main Window		X1b	0b	1b	1b
Case3	Main Window	PIP2 Window		X0b	1b	0b	1b
Case4	PIP2 Window	Main Window		X1b	1b	0b	1b
Case5	Main Window	PIP1 Window	PIP2 Window	00b	1b	1b	1b
Case6	Main Window	PIP2 Window	PIP1 Window	10b	1b	1b	1b
Case7	PIP1 Window	PIP2 Window	Main Window	01b	1b	1b	1b
Case8	PIP2 Window	PIP1 Window	Main Window	11b	1b	1b	1b

Alpha Blending

When the Main window is on top of the PIP windows, the S1D13774 can perform alpha blending on the pixel data of the selected windows. Four independently enabled key colors are available, each supporting a blend ratio from 0% to 100% in increments of 12.5%.

The Alpha Blend Mode Select bit (REG[0608h] bit 7) determines which windows are alpha blended. When alpha blending between the Main window and the PIP windows is selected (REG[0608h] bit 7 = 0b), the pixel data from the PIP window that is overlapped by the Main window key color is alpha blended with the pixel data from the Main window at the selected alpha blend ratio. If the PIP Transparency for the “top” PIP window is enabled and the key color is matched, the main window pixel data is alpha blended with the “bottom” PIP window instead of the top PIP window.

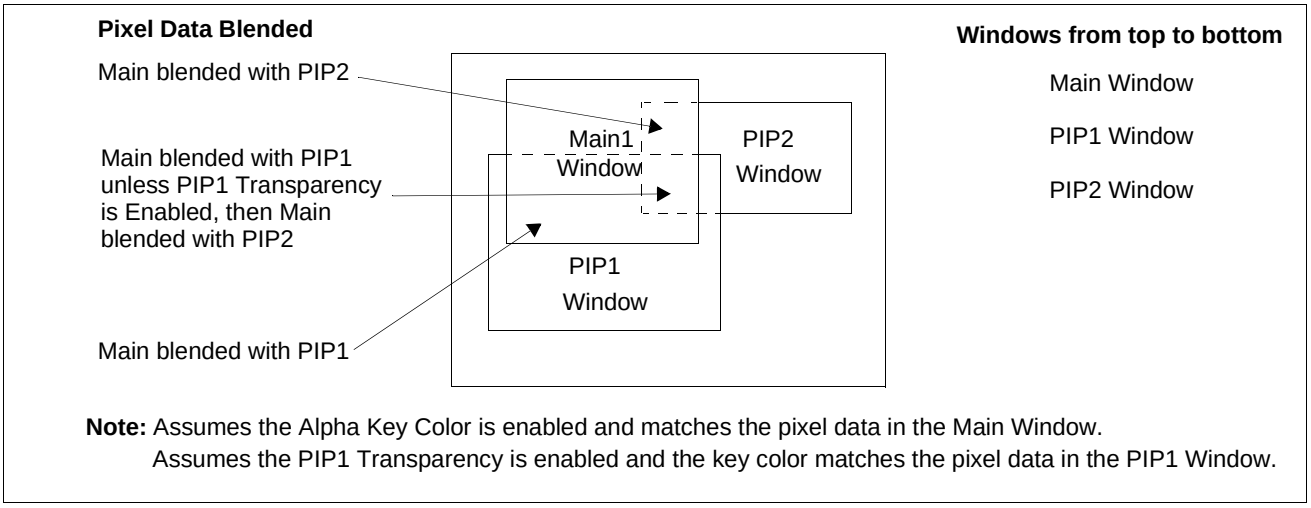


Figure 12-10: Main Window and PIP Windows Alpha Blending Example 1

When alpha blending between the PIP windows is selected (REG[0608h] bit 7 = 1b), the pixel data from the PIP windows that are overlapped by the Main window key color are alpha blended at the selected alpha blend ratio. If the PIP windows do not overlap, the PIP1 or PIP2 pixel data will "show through" the Main window key color similar to a transparency effect.

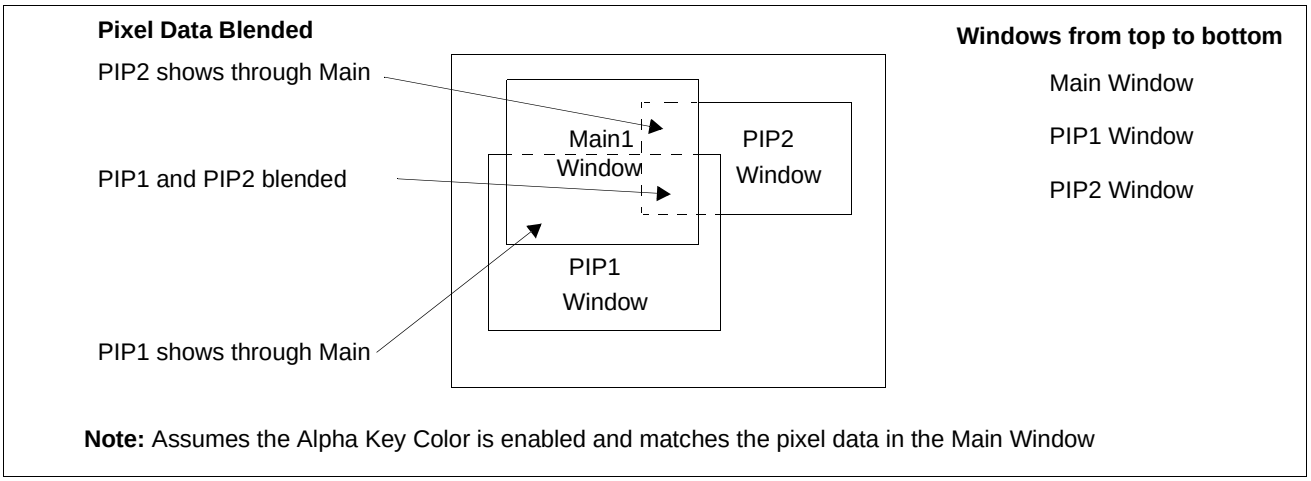


Figure 12-11: Main Window and PIP Windows Alpha Blending Example 2

The following registers are used to control and configure each Alpha Blend Key Color.

Table 12-14: Alpha Blend Register Summary

Alpha Blend	Enable	Blend Ratio	Key Color
1	REG[0608h] bit 8	REG[0614h] bits 3-0	REG[0628h] ~ REG[062Ch]
2	REG[0608h] bit 9	REG[0614h] bits 7-4	REG[0630h] ~ REG[0634h]
3	REG[0608h] bit 10	REG[0614h] bits 11-8	REG[0638h] ~ REG[063Ch]
4	REG[0608h] bit 11	REG[0614h] bits 15-12	REG[0640h] ~ REG[0644h]

Transparency

Both PIP windows have a transparency function. When the PIP window transparency is enabled, the PIP window becomes transparent where the pixel data matches the key color. This function can be used to allow pixel data to "show through" an overlapping PIP window, or allow Main window pixel data to "show through" when the PIP windows are on top of the Main window.

The following registers are used to control and configure PIP window transparency.

Table 12-15: PIP Window Transparency Register Summary

PIP Window	Enable	Key Color
PIP1 Window	REG[0608h] bit 1	REG[0618h] ~ REG[061Ch]
PIP2 Window	REG[0608h] bit 2	REG[0620h] ~ REG[0624h]

When alpha blending is enabled, the PIP transparency may be used to allow pixel data to be blended with a PIP window that is on the bottom.

Case1 Display using Main and PIP1 Window

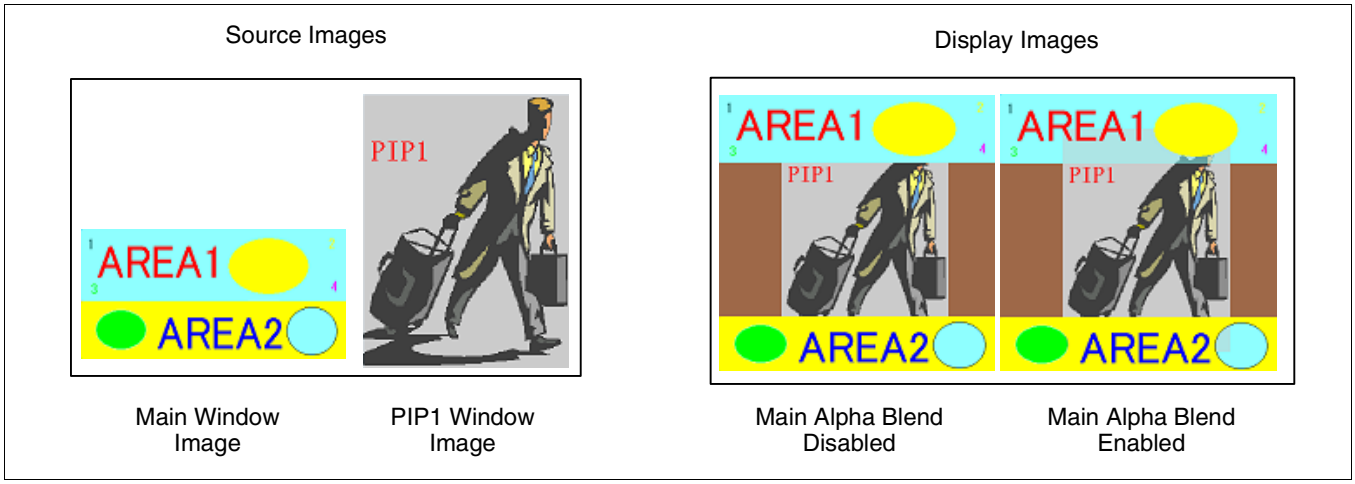


Figure 12-12: Main (top) and PIP1 (bottom) Window Display Example

Table 12-16: Main (top) and PIP1 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	0b: off
REG[0604h] bits 6-5	Layer Mode Select	X0b: Main on PIP1
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b: off
REG[0608h] bit 7	Alpha Blend Mode Select	0b: Main and PIP
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b or 1b
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	4h: 50%
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	—
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	—
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case2 Display using Main and PIP1 Window

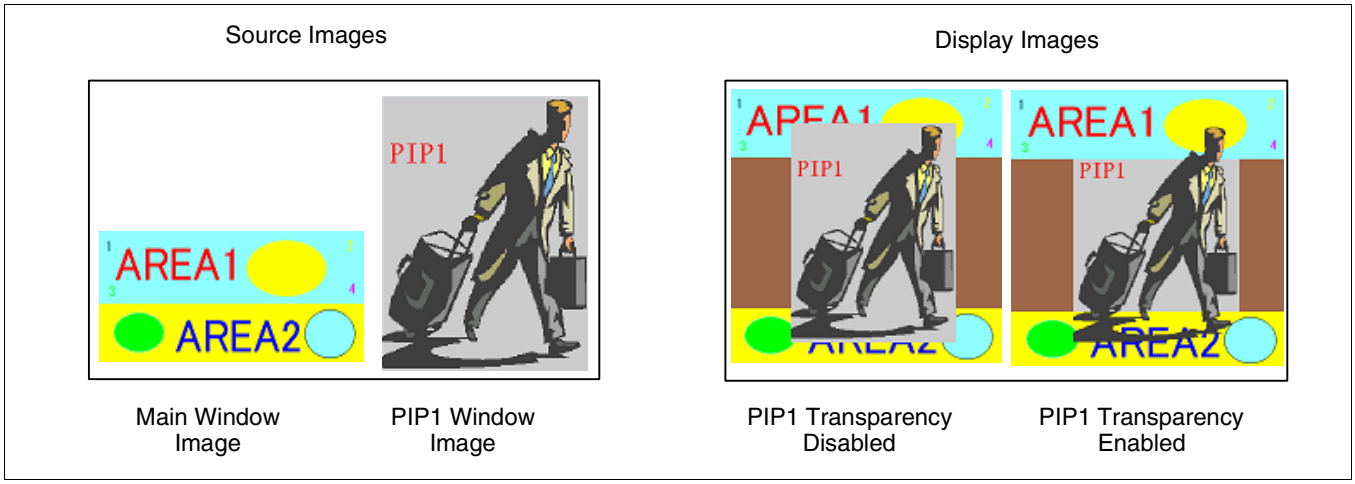


Figure 12-13: PIP1 (top) and Main (bottom) Window Display Example

Table 12-17: PIP1 (top) and Main (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	0b: off
REG[0604h] bits 6-5	Layer Mode Select	X1b: PIP1 on Main
REG[0608h] bit 1	PIP1 Transparency Enable	0b or 1b
REG[0608h] bit 2	PIP2 Transparency Enable	0b: off
REG[0608h] bit 7	Alpha Blend Mode Select	—
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b: off
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	—
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	—
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	—
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	-
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	-

Case3 Display using Main and PIP2 Window

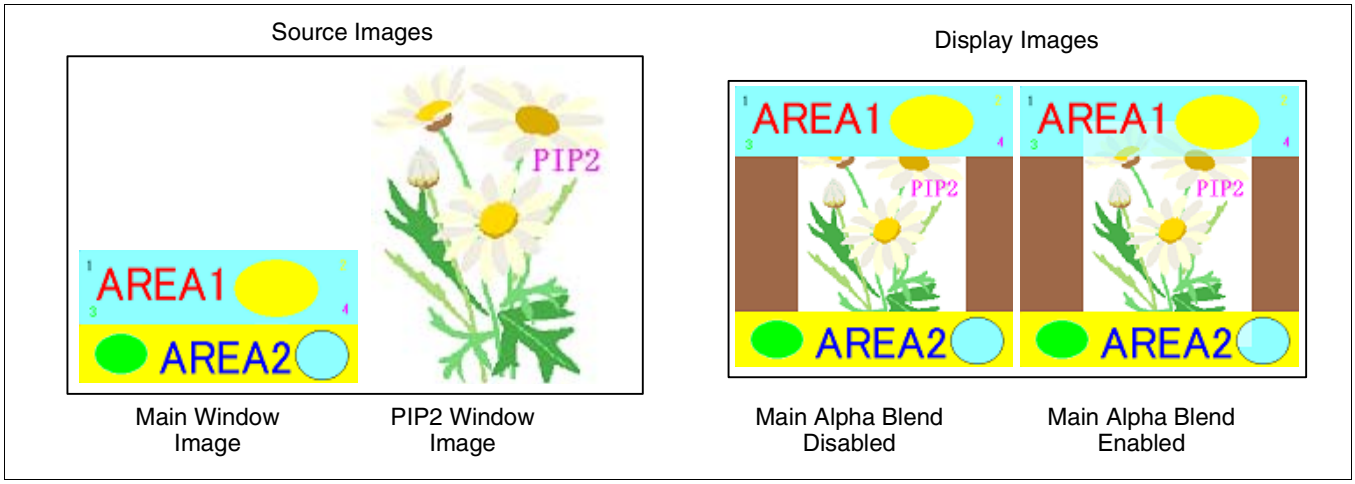


Figure 12-14: Main (top) and PIP2 (bottom) Window Display Example

Table 12-18: Main (top) and PIP2 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	0b: off
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	X0b: Main on PIP2
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b: off
REG[0608h] bit 7	Alpha Blend Mode Select	0b: Main and PIP
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b or 1b
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	4h: 50%
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	—
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	—
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case4 Display using Main and PIP2 Window

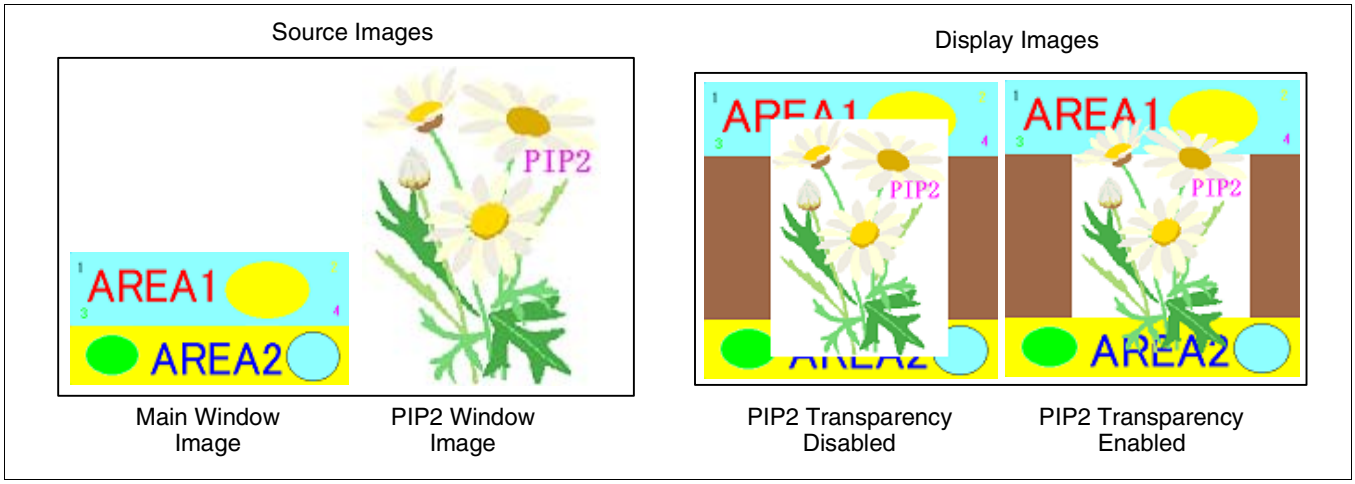


Figure 12-15: PIP2 (top) and Main (bottom) Window Display Example

Table 12-19: PIP2 (top) and Main (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	0b: off
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	X1b: PIP2 on Main
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b or 1b
REG[0608h] bit 7	Alpha Blend Mode Select	—
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b: off
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	—
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	—
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	—
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case5 1 Display using Main, PIP1 and PIP2 Window

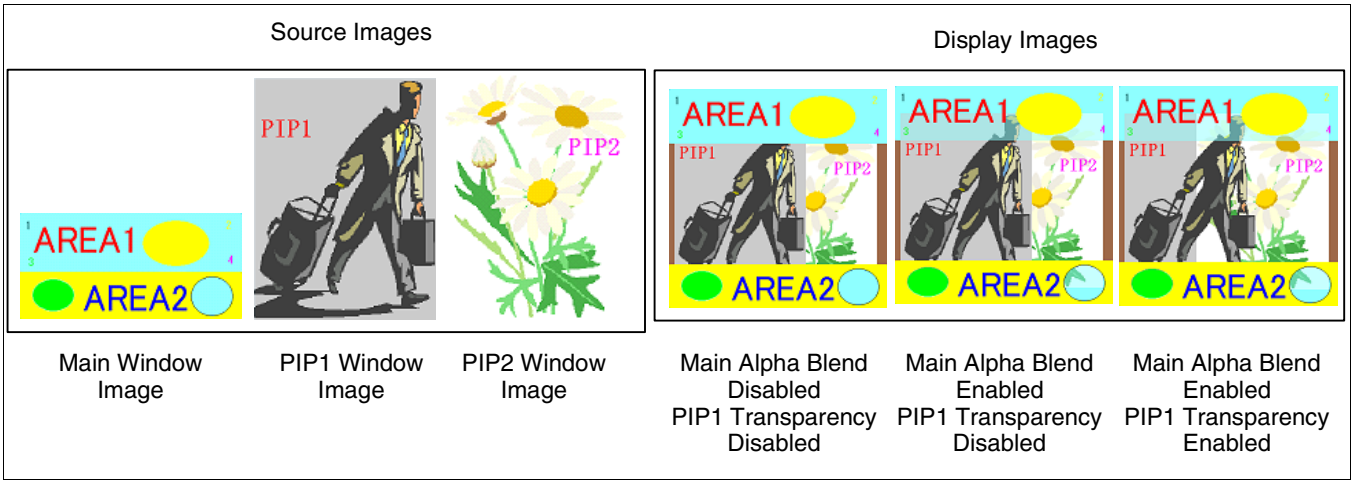


Figure 12-16: Main (top), PIP1 (middle) and PIP2 (bottom) Window Display Example

Figure 12-17: Main (top), PIP1 (middle) and PIP2 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	00b: Main(top), PIP1, PIP2(bottom)
REG[0608h] bit 1	PIP1 Transparency Enable	0b or 1b
REG[0608h] bit 2	PIP2 Transparency Enable	0b: off
REG[0608h] bit 7	Alpha Blend Mode Select	0b: Main and PIP
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b or 1b
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	4h: 50%
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	—
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case5 2 Display using Main, PIP1 and PIP2 Window

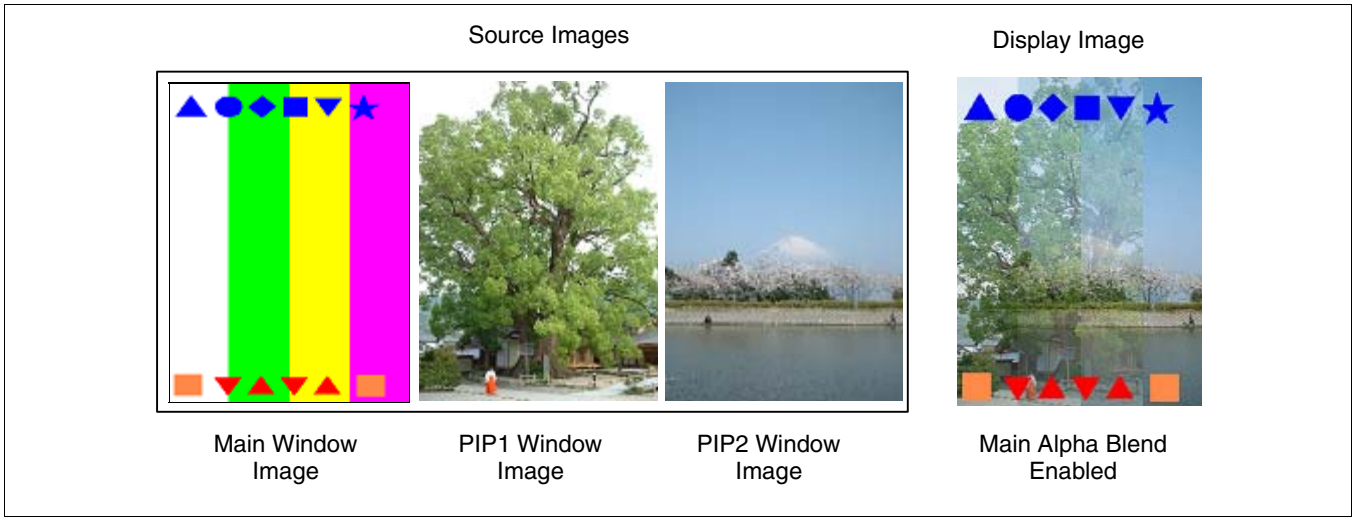


Figure 12-18: Main (top), PIP1 (middle) and PIP2 (bottom) Window Display Example

Table 12-20: Main (top), PIP1 (middle) and PIP2 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	0b: off
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	00b: Main(top), PIP1, PIP2(bottom)
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b: off
REG[0608h] bit 7	Alpha Blend Mode Select	1b: PIP1 and PIP2
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	1b
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	1b
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	1b
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	1b
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	—
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	2h: 25%
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	4h: 50%
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	6h: 75%
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	8h: 100%
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	—
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	—
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	

Case6 Display using Main, PIP1 and PIP2 Window

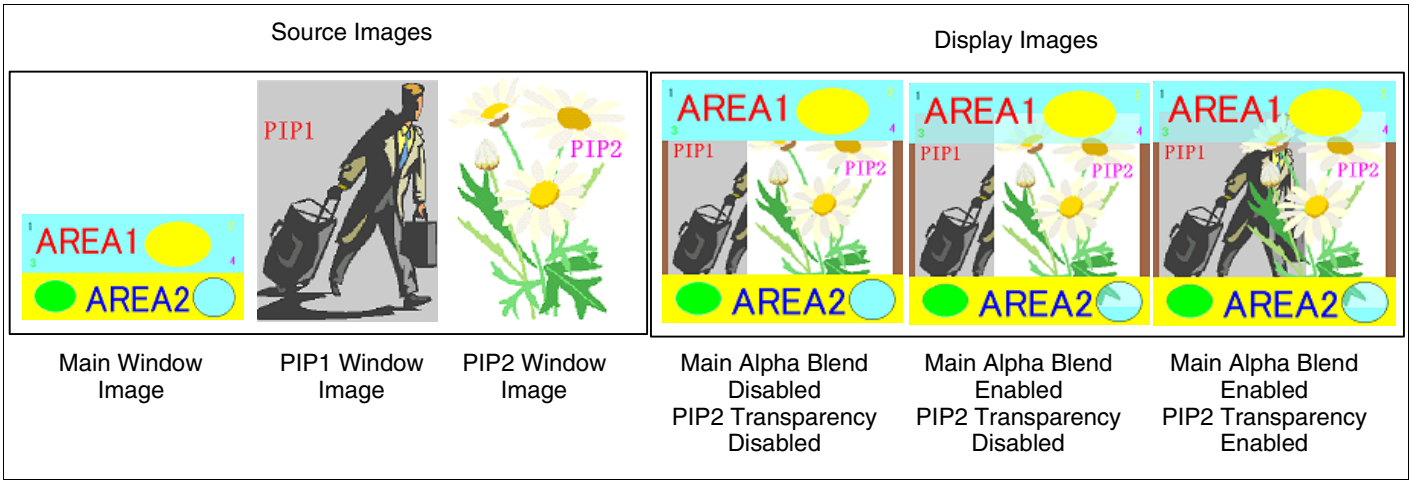


Figure 12-19: Main (top), PIP2 (middle) and PIP1 (bottom) Window Display Example

Table 12-21: Main (top), PIP2 (middle) and PIP1 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	10b: Main(top), PIP2, PIP1(bottom)
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b or 1b
REG[0608h] bit 7	Alpha Blend Mode Select	0b: Main and PIP
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b or 1b
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	4h: 50%
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	—
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case7 Display using Main, PIP1 and PIP2 Window

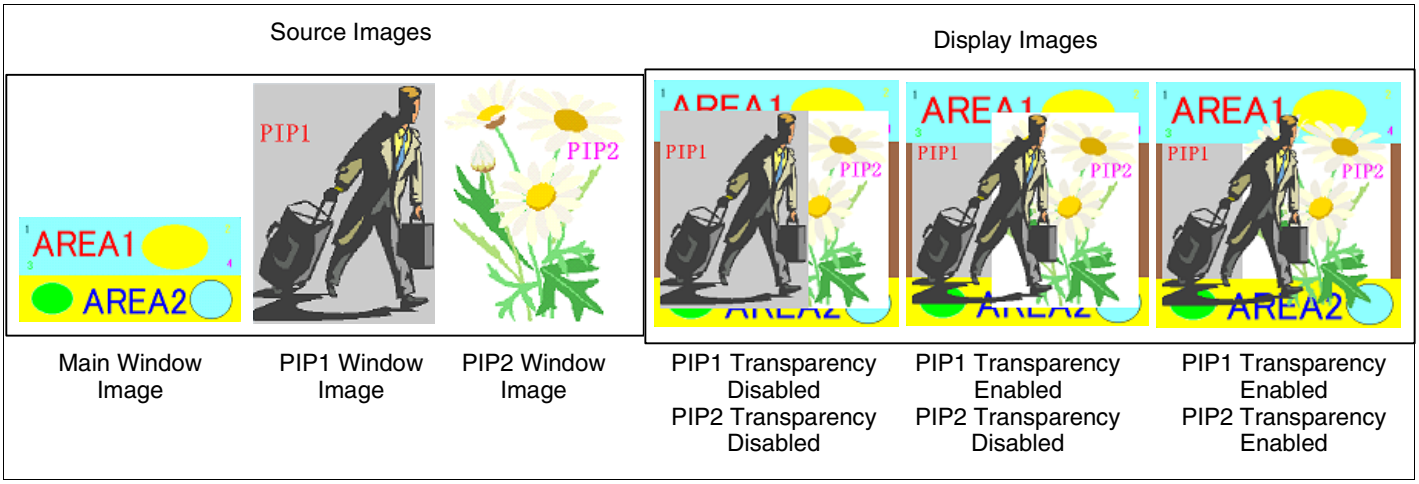


Figure 12-20: PIP1 (top), PIP2 (middle) and Main (bottom) Window Display Example

Table 12-22: PIP1 (top), PIP2 (middle) and Main (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	10b: PIP1(top), PIP2, Main (bottom)
REG[0608h] bit 1	PIP1 Transparency Enable	0b or 1b
REG[0608h] bit 2	PIP2 Transparency Enable	0b or 1b
REG[0608h] bit 7	Alpha Blend Mode Select	—
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b: off
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	—
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	—
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case8 Display using Main, PIP1 and PIP2 Window

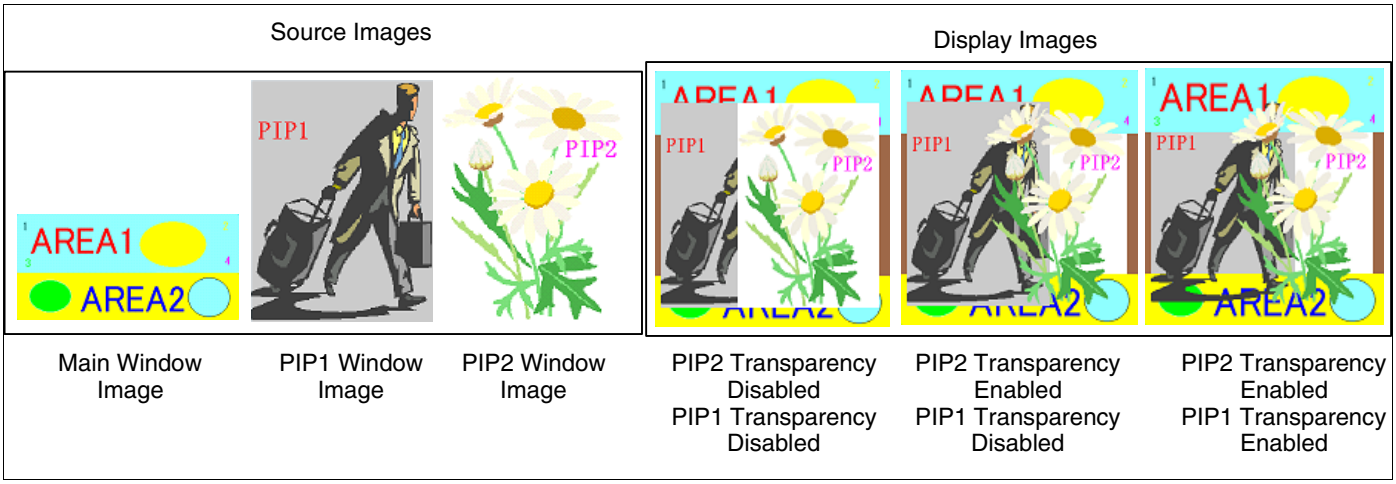


Figure 12-21: PIP2 (top), PIP1 (middle) and Main (bottom) Window Display Example

Table 12-23: PIP2 (top), PIP1 (middle) and Main (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	1b: on
REG[0604h] bit 1	Main2 Window Display Enable	1b: on
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	11b: PIP2(top), PIP1, Main (bottom)
REG[0608h] bit 1	PIP1 Transparency Enable	0b or 1b
REG[0608h] bit 2	PIP2 Transparency Enable	0b or 1b
REG[0608h] bit 7	Alpha Blend Mode Select	—
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b: off
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	—
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	—
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

12.4.2 Alpha Blend and Transparency using the PIP1 and PIP2 Windows

When the display output port is configured for LCD1 + TV-Out (REG[0604h] bits 15-12 = 1011b), the Alpha Blend Mode Select bit (REG[0608h] bit 7) should be set to perform alpha blending on the PIP1 and PIP2 windows. This is because the Main window is displayed on LCD1 and the PIP1/PIP2 windows are displayed on the TV-Out interface. For these cases, only the PIP windows are on the same display and can be alpha blended. The following table shows the available configurations.

Table 12-24: PIP1 and PIP2 Alpha Blending

Case	Top Layer	Bottom Layer	REG[0604h]		
			bits 6-5	bit 3	bit 2
Case1	PIP1 Window	PIP2 Window	00b	1b	1b
Case2	PIP2 Window	PIP1 Window	11b	1b	1b

Alpha Blend

When the PIP1 window is on top of the PIP2 window, the S1D13774 can perform alpha blending on the pixel data of the windows. Four independently enabled key colors are available, each supporting a blend ratio from 0% to 100% in increments of 12.5%.

For this case, alpha blending between the PIP windows must be selected (REG[0608h] bit 7 = 1b), the pixel data from the PIP2 window that is overlapped by the PIP1 window key color is alpha blended at the selected alpha blend ratio.

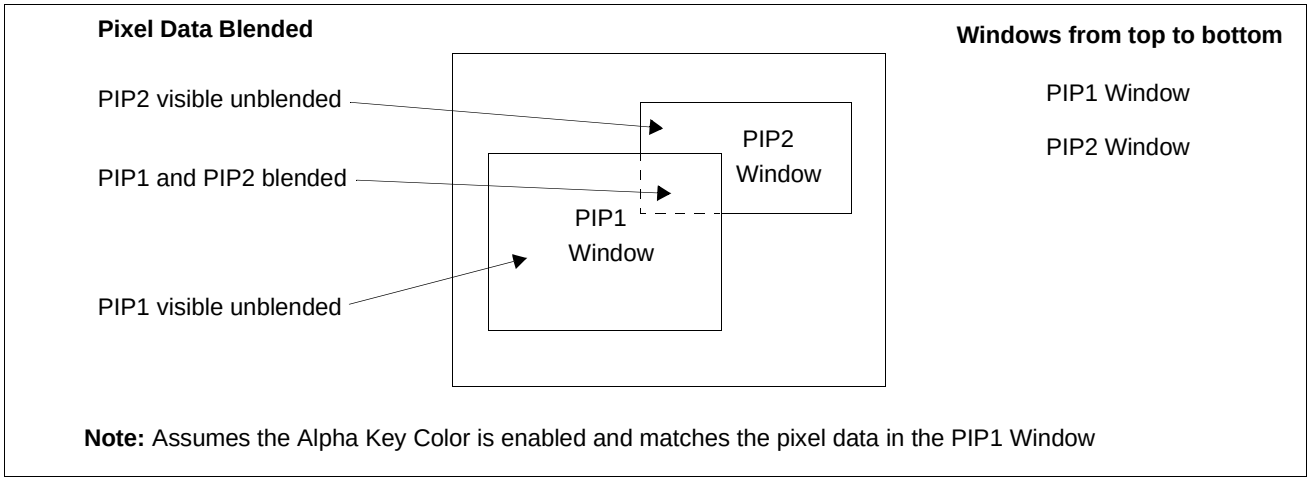


Figure 12-22: PIP1 Window and PIP2 Window Alpha Blending Example

The following registers are used to control and configure each Alpha Blend Key Color.

Table 12-25: Alpha Blend Register Summary

Alpha Blend	Enable	Blend Ratio	Key Color
1	REG[0608h] bit 8	REG[0614h] bits 3-0	REG[0628h] ~ REG[062Ch]
2	REG[0608h] bit 9	REG[0614h] bits 7-4	REG[0630h] ~ REG[0634h]
3	REG[0608h] bit 10	REG[0614h] bits 11-8	REG[0638h] ~ REG[063Ch]
4	REG[0608h] bit 11	REG[0614h] bits 15-12	REG[0640h] ~ REG[0644h]

Transparency

For these cases, the PIP2 transparency function is available when the PIP2 window is on top of the PIP1 window. When the PIP2 window transparency is enabled, the PIP window becomes transparent where the pixel data matches the key color. This function can be used to allow pixel data to from the PIP1 window to “show through” the overlapping PIP2 window. The following registers are used to control and configure PIP2 window transparency.

Table 12-26: PIP2 Window Transparency Register Summary

PIP Window	Enable	Key Color
PIP2 Window	REG[0608h] bit 2	REG[0620h] ~ REG[0624h]

Case1 Display using PIP1 and PIP2 Window

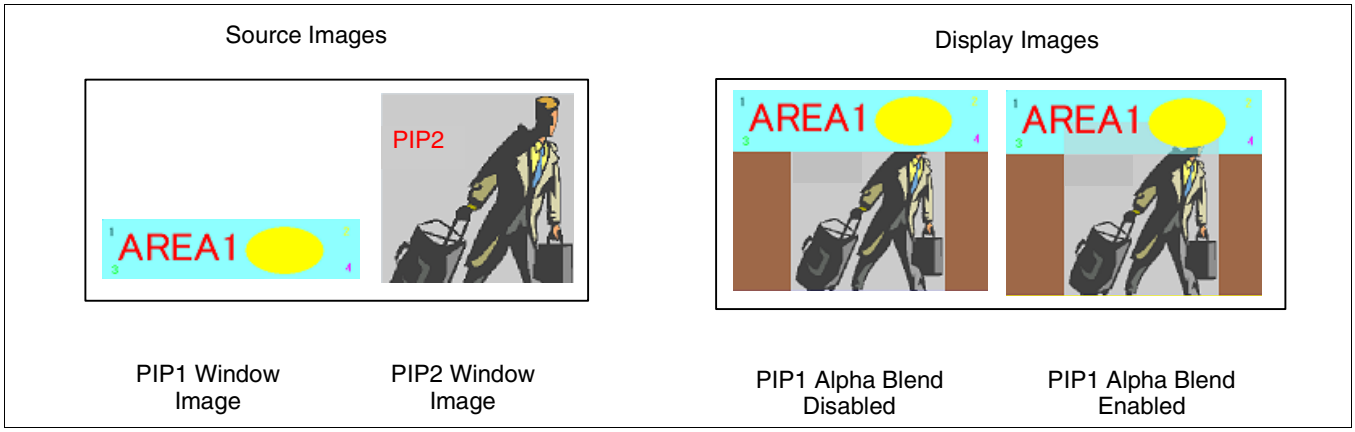


Figure 12-23: PIP1 (top) and PIP2 (bottom) Window Display Example

Table 12-27: PIP1 (top) and PIP2 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	—
REG[0604h] bit 1	Main2 Window Display Enable	—
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	00b: PIP1 on PIP2
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b: off
REG[0608h] bit 7	Alpha Blend Mode Select	1b:
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b or 1b
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0b: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	4h: 50%
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	Unavailable
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	—
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

Case2 Display using PIP1 and PIP2 Window

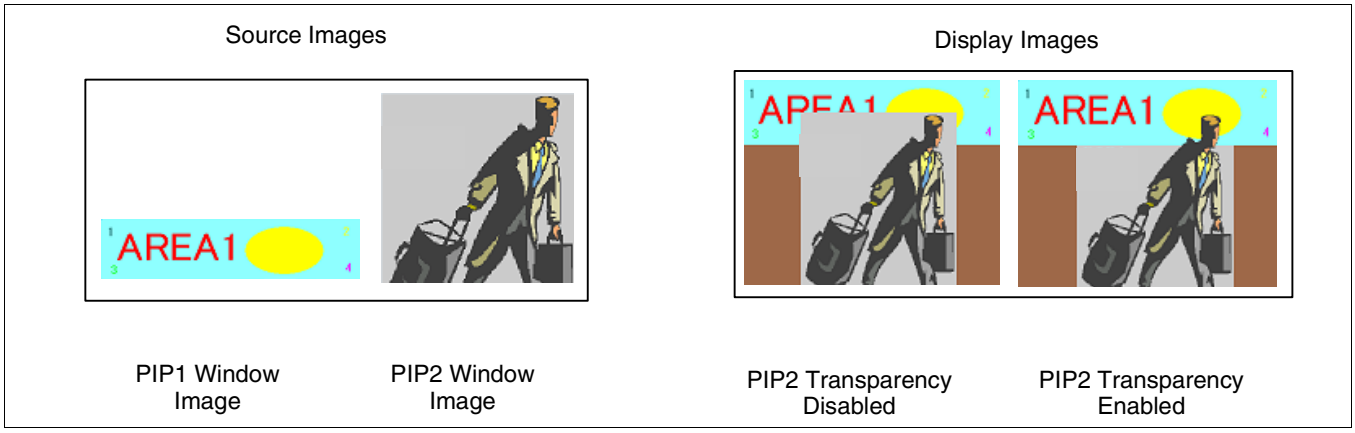


Figure 12-24: PIP2 (top) and PIP1 (bottom) Window Display Example

Table 12-28: PIP2 (top) and PIP1 (bottom) Window Register Setting Example

REG[0604h] bit 0	Main1 Window Display Enable	—
REG[0604h] bit 1	Main2 Window Display Enable	—
REG[0604h] bit 2	PIP1 Window Display Enable	1b: on
REG[0604h] bit 3	PIP2 Window Display Enable	1b: on
REG[0604h] bits 6-5	Layer Mode Select	11b: PIP2 on PIP1
REG[0608h] bit 1	PIP1 Transparency Enable	0b: off
REG[0608h] bit 2	PIP2 Transparency Enable	0b or 1b
REG[0608h] bit 7	Alpha Blend Mode Select	—
REG[0608h] bit 8	Alpha Blend 1 Key Color Enable	0b: off
REG[0608h] bit 9	Alpha Blend 2 Key Color Enable	0b: off
REG[0608h] bit 10	Alpha Blend 3 Key Color Enable	0b: off
REG[0608h] bit 11	Alpha Blend 4 Key Color Enable	0: off
REG[060Ch] bits 15-0 ~ REG[0610h] bits 7-0	Background Color	
REG[0614h] bits 3-0	Alpha Blend 1 Ratio	—
REG[0614h] bits 7-4	Alpha Blend 2 Ratio	—
REG[0614h] bits 11-8	Alpha Blend 3 Ratio	—
REG[0614h] bits 15-12	Alpha Blend 4 Ratio	—
REG[0618h] bits 15-0 ~ REG[061Ch] bits 15-0	PIP1 Transparency Key Color	Unavailable
REG[0620h] bits 15-0 ~ REG[0624h] bits 15-0	PIP2 Transparency Key Color	
REG[0628h] bits 15-0 ~ REG[062Ch] bits 15-0	Alpha Blend 1 Key Color	—
REG[0630h] bits 15-0 ~ REG[0634h] bits 15-0	Alpha Blend 2 Key Color	—
REG[0638h] bits 15-0 ~ REG[063Ch] bits 15-0	Alpha Blend 3 Key Color	—
REG[0640h] bits 15-0 ~ REG[0644h] bits 15-0	Alpha Blend 4 Key Color	—

12.5 AME

AME (Auto Movie Enhancement) provides functions that allow the chroma, contrast, and gamma of image data to be adjusted. This function can be configured for either the PIP1 or the PIP2 window and can be used to adjust image data for still or moving pictures (movies).

AME processing can be done on an entire image or on a selected "processing" area. The processing area can range in size from 64x64 pixels to 1024x1024 pixels and is set as shown below. There are independent adjustment levels for each of chroma, contrast, and gamma (see REG[0904h]).

The AME sampling area must be set within the processing area. The current frame sampling result is reflected in the next frame processing.

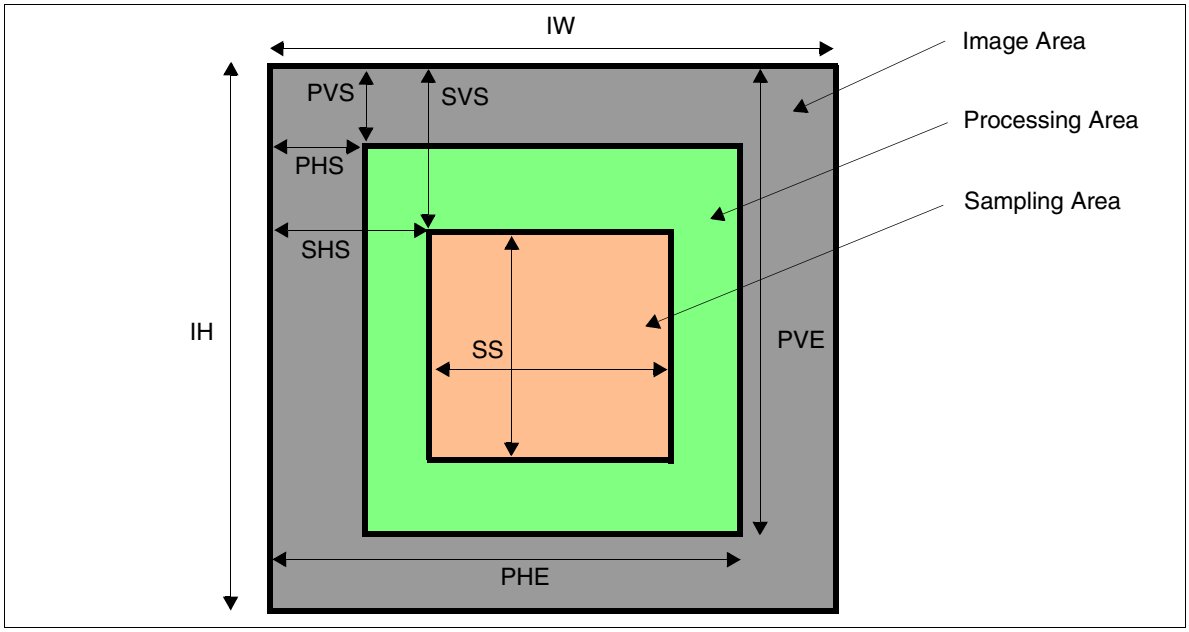


Figure 12-25: AME Processing Example

Table 12-29: AME Processing Dimension Registers

Symbol	Description	Derived From	Unit
IW	Image Width (Note 1)	REG[0908h] bits 9-0	Pixels
IH	Image Height (Note 1)	REG[090Ch] bits 9-0	Lines
PHS	Processing Horizontal Start	REG[0910h] bits 9-0	Pixels
PHE	Processing Horizontal End	REG[0914h] bits 9-0	Pixels
PVS	Processing Vertical Start	REG[0918h] bits 9-0	Lines
PVE	Processing Vertical End	REG[091Ch] bits 9-0	Lines
SVS	Sampling Vertical Start	REG[0920h] bits 9-0	Lines
SHS	Sampling Horizontal Start	REG[0924h] bits 9-0	Pixels
SS	Sampling Size	REG[0928h] bits 2-0	Pixels/Lines

1. If the image size is changed using the scaler before being processed by the AME, set the Image Width (IW) Image Height (IH) to the scaled size.

The following programming flow provides an example of how to configure and perform AME adjustment for the PIP1 or PIP2 window.

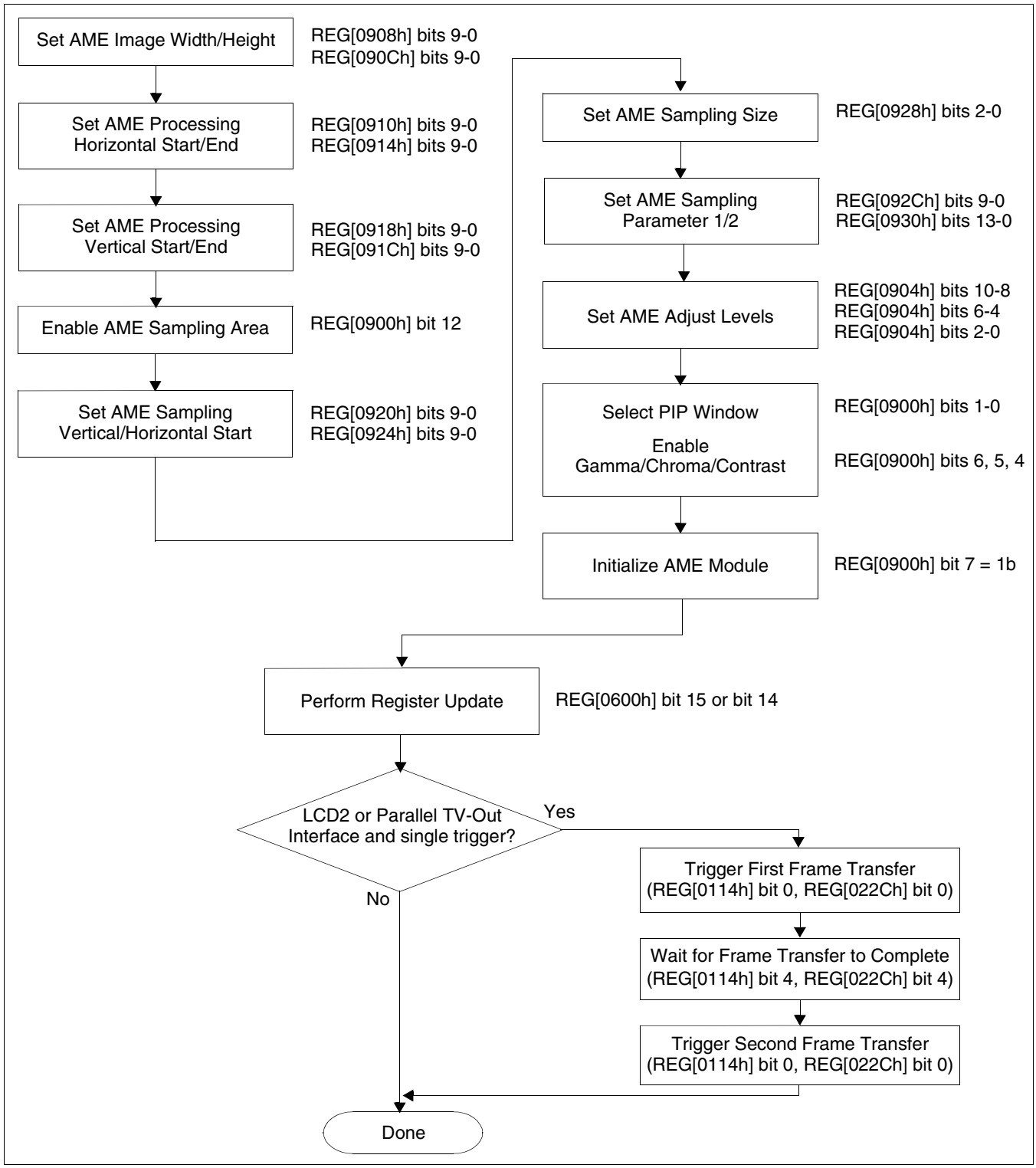


Figure 12-26: AME Programming Flow

12.6 PIP2 Panorama Scaling

The PIP2 window can be configured for Panorama scaling (or wide scaling mode) in the horizontal or the vertical direction. There are two modes, Partial and Linear, which are shown in the following examples.

12.6.1 Partial Panorama Mode

The following example shows Vertical Partial Panorama Scaling, REG[0800h] bits 2-0 = 001b. Horizontal Partial Panorama Scaling is done in a similar way, but in the horizontal direction.

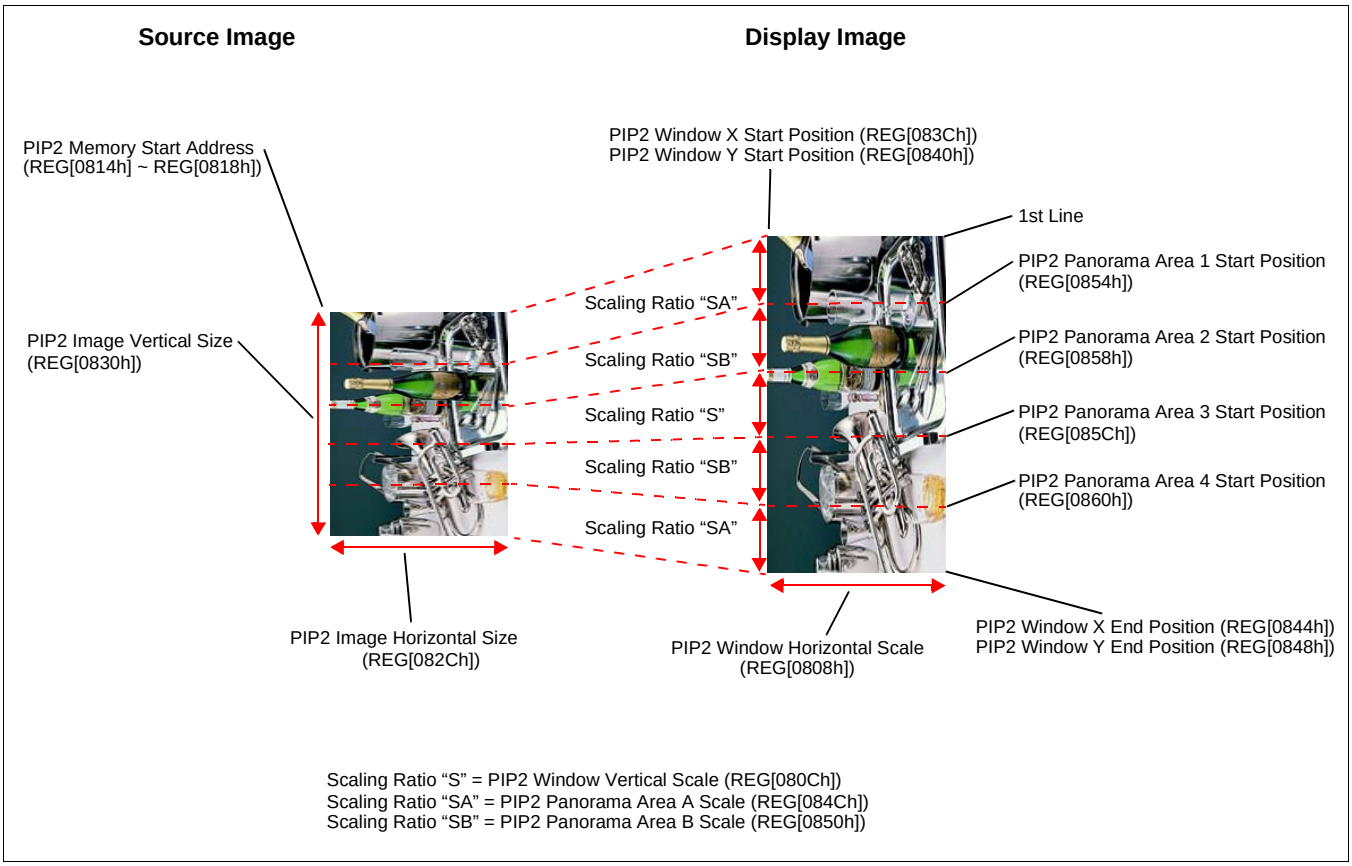


Figure 12-27: Partial Panorama Mode Example

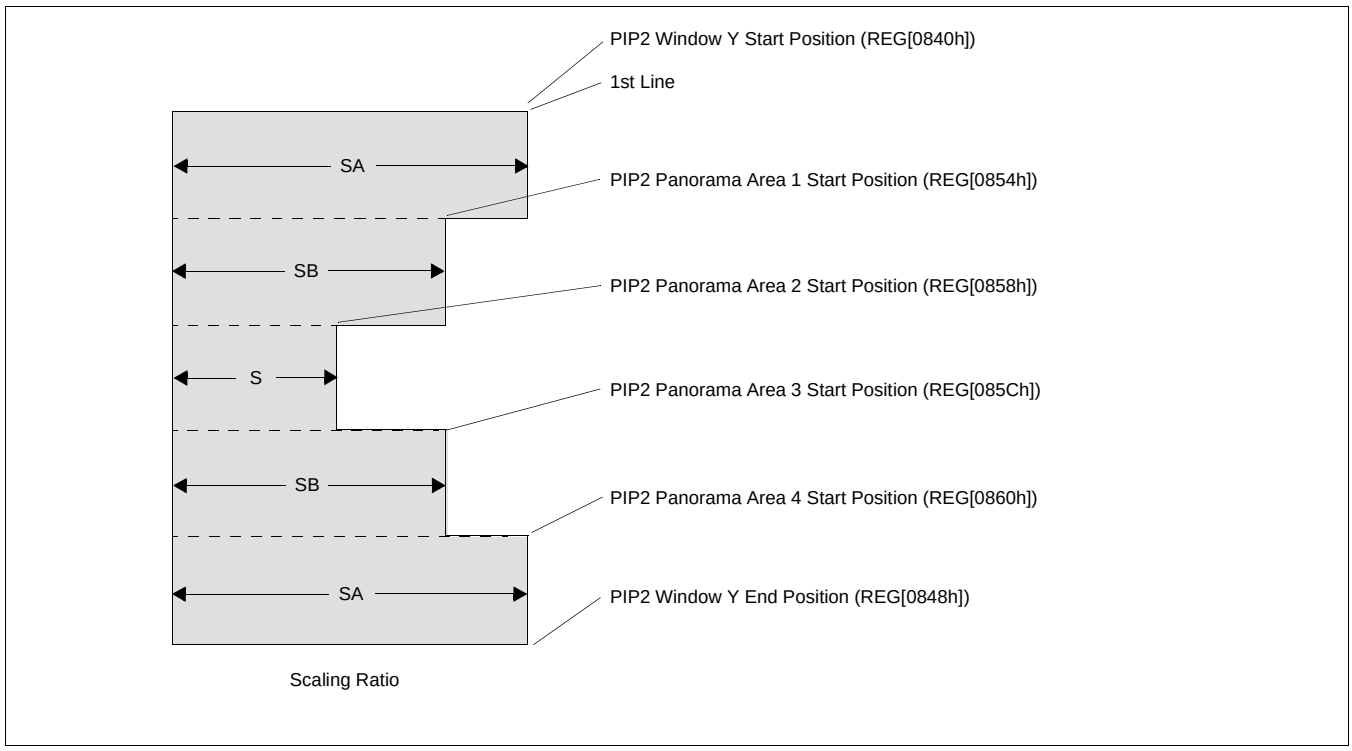


Figure 12-28: Scaling Ratios for Partial Panorama Mode

The following programming flow provides an example of how to setup the PIP2 window for Partial Panorama Scaling.

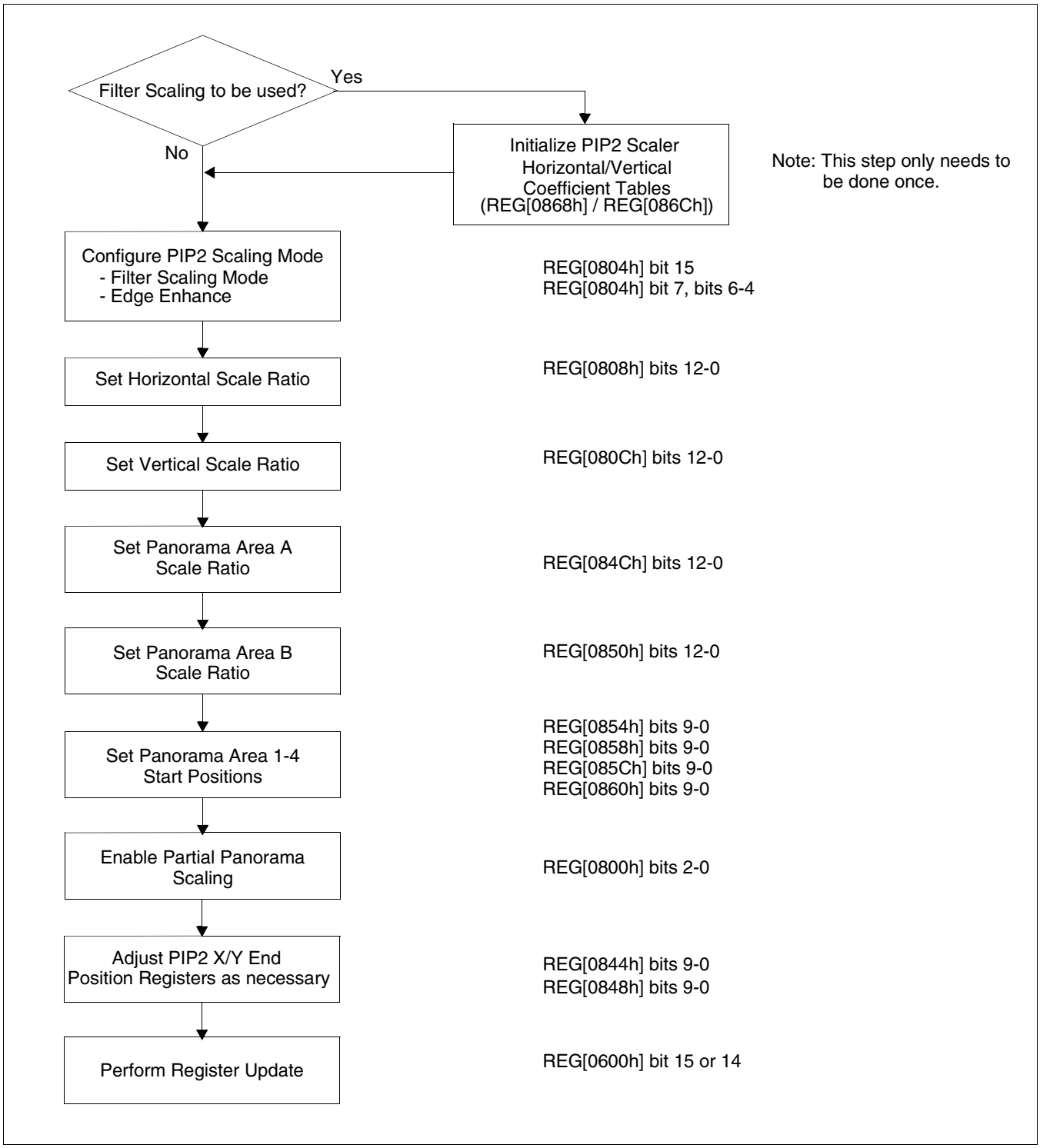


Figure 12-29: PIP2 Partial Panorama Scaling Programming Flow

The figure below shows an example of a 240x320 image scaled to 480x800 using PIP2 vertical partial panorama scaling. All dimensions are listed in pixels.

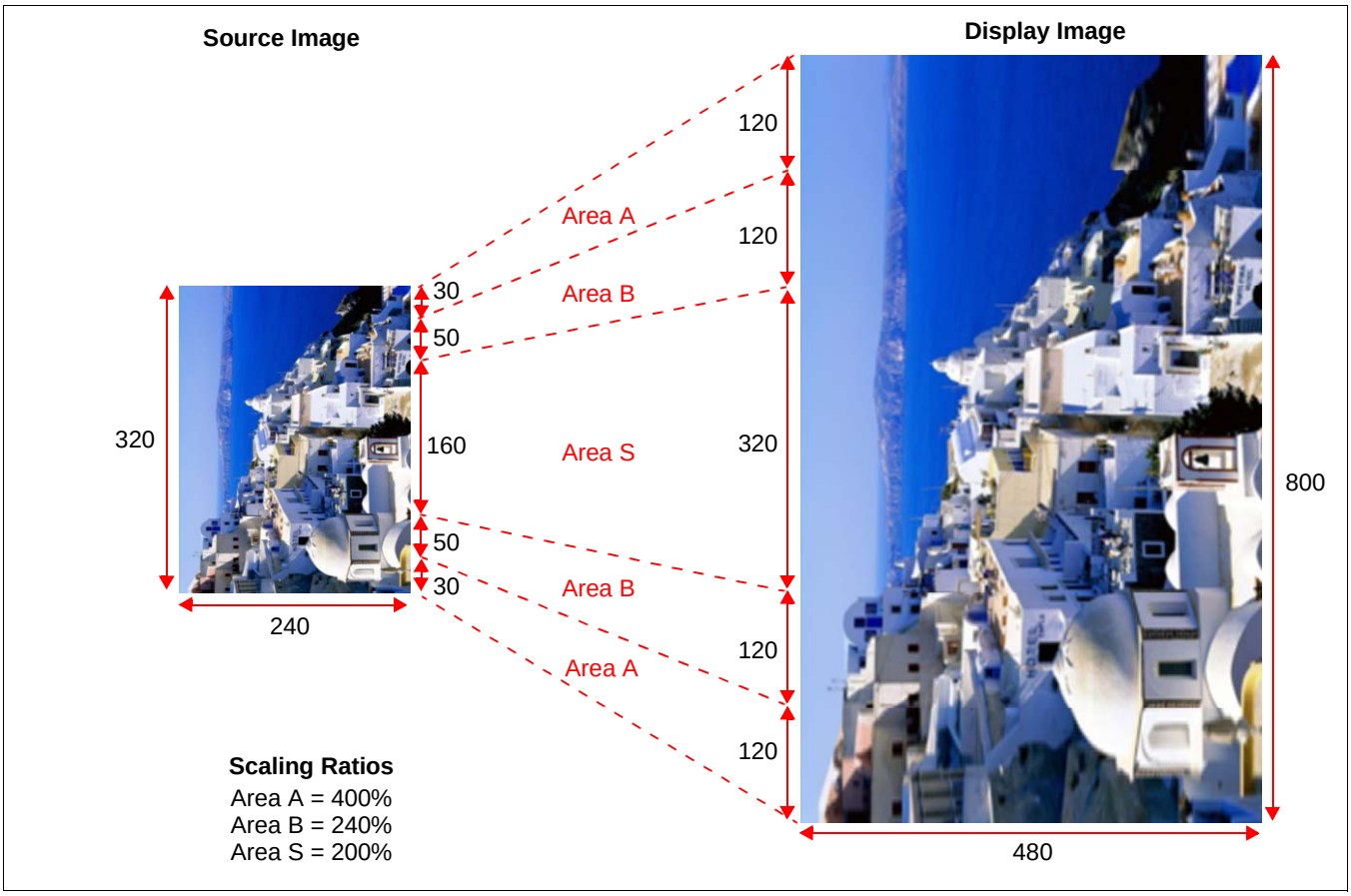


Figure 12-30: PIP2 Vertical Partial Panorama Example (240x320 scaled to 480x800)

The following steps are used to scale the 240x320 image to 480x800 using PIP2 vertical partial panorama scaling.

1. If Filter Scaling will be enabled (REG[0804h] bit 15 = 1b), initialize the PIP2 Scaler Horizontal/Vertical Coefficient Tables with the values listed in the PIP2 Window Scaler Coefficient Table Access Port register description (see REG[086Ch]).

2. Configure the scaling mode for the PIP2 window in REG[0804h].

   For this example, Filter Scaling is enabled (bit 15 = 1b) and Edge Enhance is disabled (bit 7 = 0b). Note that if Edge Enhance is enabled, the edge enhance strength must be set using bits 6-4.

   Note: REG[0804h] contains some reserved bits that must be set accordingly.

3. Set the horizontal scale ratio in REG[0808h].

   For this example the horizontal scale ratio is 200% (or 2.0x) and the value to be programmed is calculated as follows:

   REG[0808h] bits 12-0 = 1024 x (1 ÷ scaling ratio)
   = 1024 x (1 ÷ 2.0)
   = 512 (200h)

4. Set the vertical scale ratio in REG[080Ch].

   For this example the vertical scale ratio is 200% (or 2.0x) and the value to be programmed is calculated as follows:

   REG[080Ch] bits 12-0 = 1024 x (1 ÷ scaling ratio)
   = 1024 x (1 ÷ 2.0)
   = 512 (200h)

5. Set the Panorama Area A scale ratio in REG[084Ch].

   For this example the Panorama Area A scale ratio is 400% (or 4.0x) and the value to be programmed is calculated as follows:

   REG[084Ch] bits 12-0 = 1024 x (1 ÷ scaling ratio)
   = 1024 x (1 ÷ 4.0)
   = 256 (100h)

6. Set the Panorama Area B scale ratio in REG[0850h].

   For this example the Panorama Area A scale ratio is 240% (or 2.4x) and the value to be programmed is calculated as follows:

   REG[0850h] bits 12-0 = 1024 x (1 ÷ scaling ratio)
   = 1024 x (1 ÷ 2.4)
   = 426.67 (must be rounded down)
   = 426 (1AAh)

7. Set the Panorama Area 1 start position in REG[0854h].

   The start position is calculated as follows:

   REG[0854h] bits 9-0 = Area A size x scaling ratio
   = 30 x 4.0
   = 120 (078h)

8. Set the Panorama Area 2 start position in REG[0858h].

   The start position is calculated as follows:

   REG[0858h] bits 9-0 = (Panorama Area 1 size) + (Area B size x scale ratio)
   = (120) + (50 x 2.4)
   = 240 (0F0h)

9. Set the Panorama Area 3 start position in REG[085Ch].

   The start position is calculated as follows:

   REG[085Ch] bits 9-0 = (Panorama Area 2 size) + (Area S size x scale ratio)
   = (240) + (160 x 2.0)
   = 560 (230h)

10. Set the Panorama Area 4 start position in REG[0860h].

    The start position is calculated as follows:

    REG[0860h] bits 9-0 = (Panorama Area 3 size) + (Area B size x scale ratio)
    = (560) + (50 x 2.4)
    = 680 (2A8h)

11. Enable Vertical Partial Panorama scaling by setting REG[0800h] bits 2-0 = 001b.

12. Adjust the PIP2 X/Y End Position registers as necessary.

Perform a register update according to which interface the PIP2 window is displayed on by setting REG[0600h] bit 15 or bit 14.

12.6.2 Linear Panorama Mode

The following example shows Vertical Linear Panorama Scaling, REG[0800h] bits 2-0 = 010b. Horizontal Linear Panorama Scaling is done in a similar way, but in the horizontal direction.

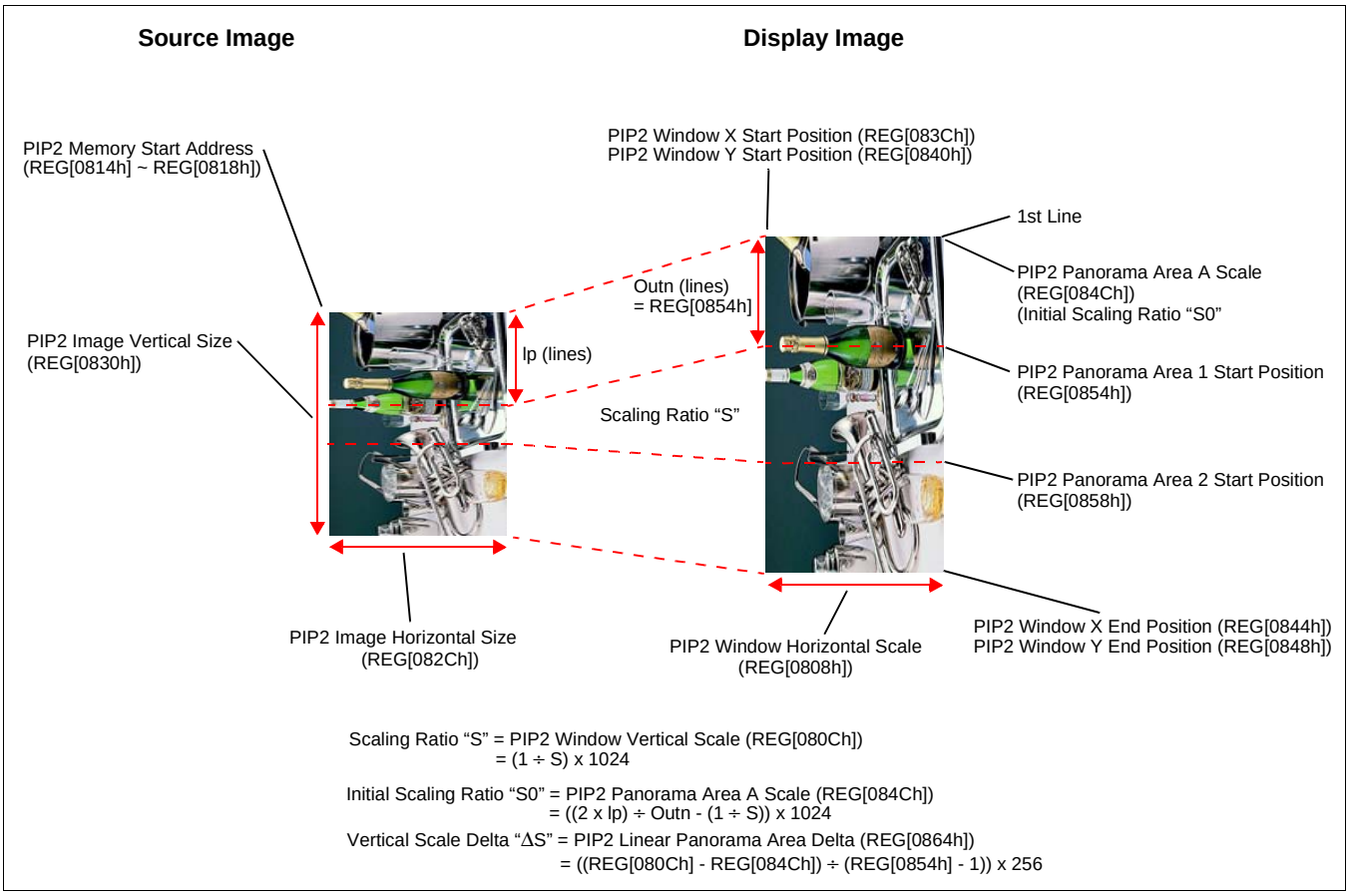


Figure 12-31: Linear Panorama Mode Example

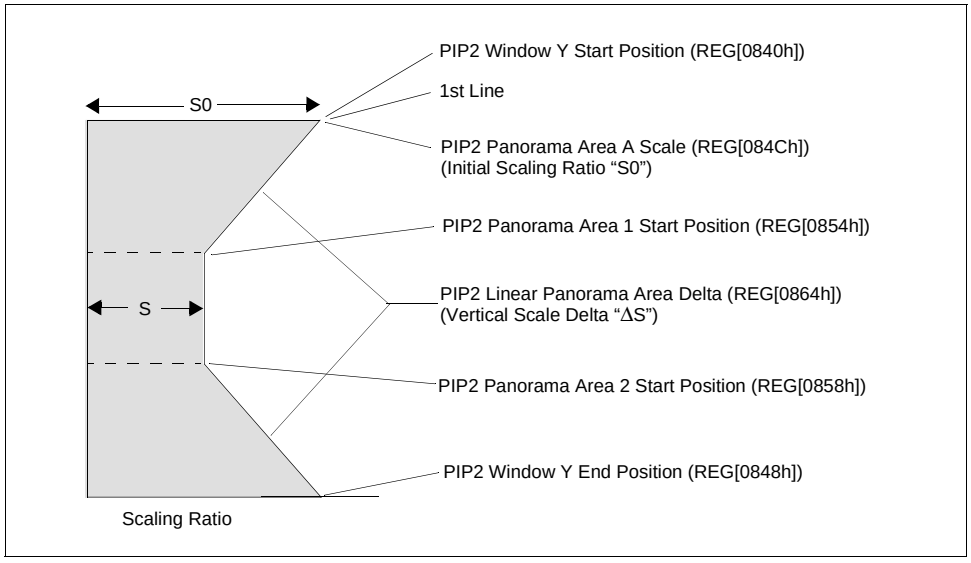


Figure 12-32: Scaling Ratio for Linear Panorama Mode

The following programming flow provides an example of how to setup the PIP2 window for Linear Panorama Scaling.

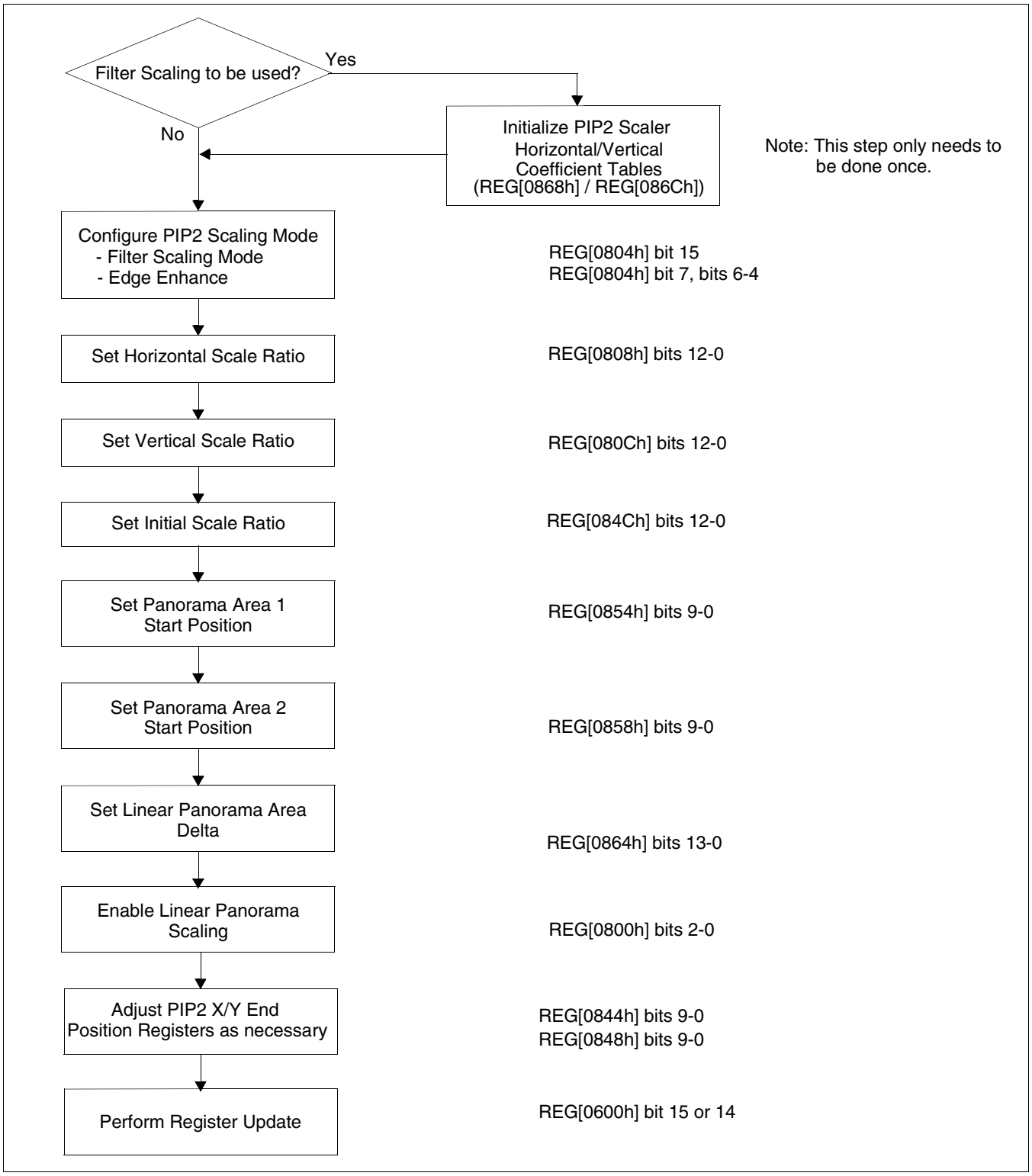


Figure 12-33: PIP2 Linear Panorama Scaling Programming Flow

The figure below shows an example of a 240x320 image scaled to 480x800 using PIP2 vertical linear panorama scaling. All dimensions are listed in pixels.

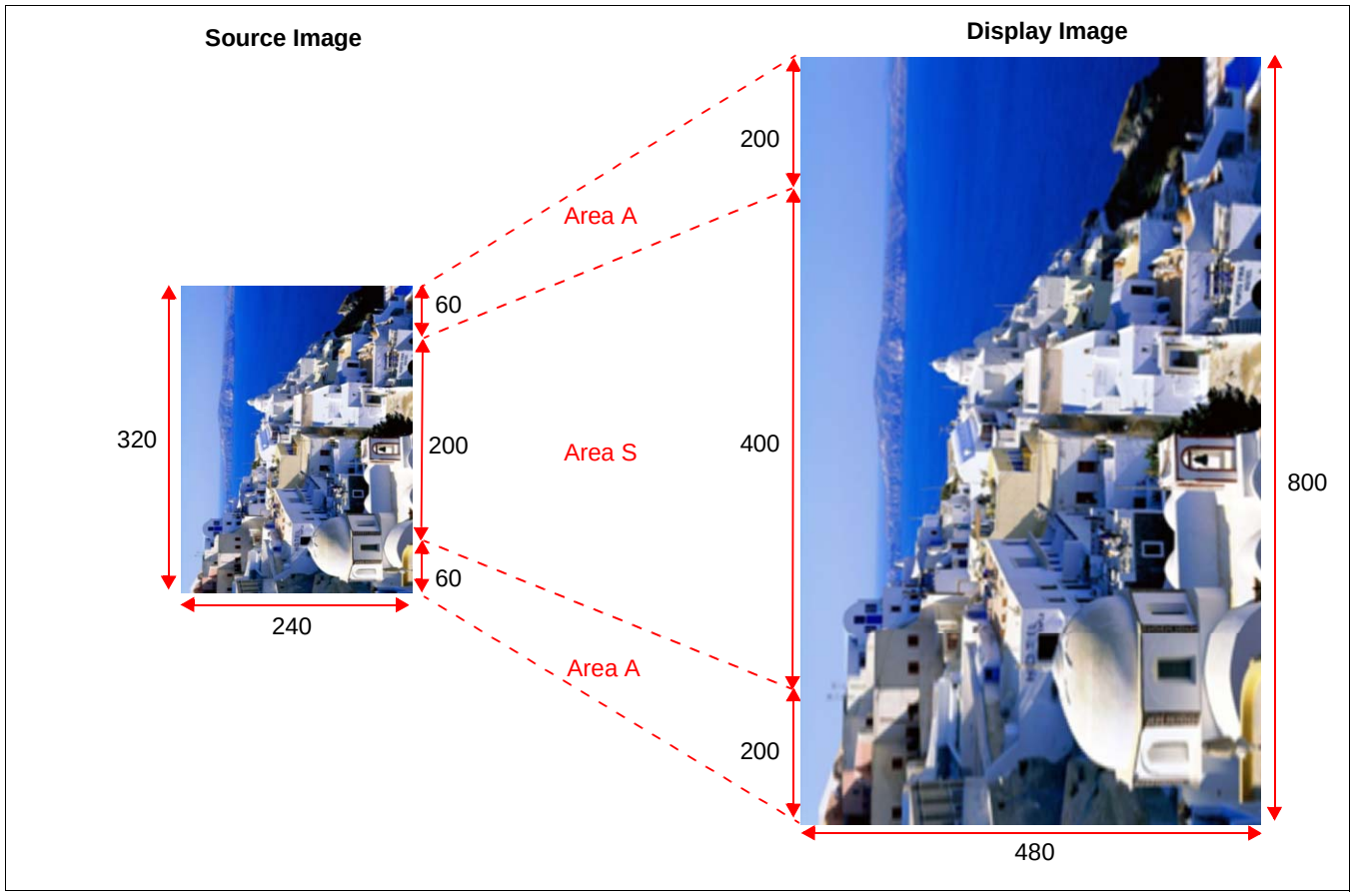


Figure 12-34: PIP2 Vertical Linear Panorama Example (240x320 scaled to 480x800)

The following steps are used to scale the 240x320 image to 480x800 using PIP2 vertical linear panorama scaling.

1. If Filter Scaling will be enabled (REG[0804h] bit 15 = 1b), initialize the PIP2 Scaler Horizontal/Vertical Coefficient Tables with the values listed in the PIP2 Window Scaler Coefficient Table Access Port register description (see REG[086Ch]).

2. Configure the scaling mode for the PIP2 window in REG[0804h].

   For this example, Filter Scaling is enabled (bit 15 = 1b) and Edge Enhance is disabled (bit 7 = 0b). Note that if Edge Enhance is enabled, the edge enhance strength must be set using bits 6-4.

   Note: REG[0804h] contains some reserved bits that must be set accordingly.

3. Set the horizontal scale ratio in REG[0808h].

   For this example the horizontal scale ratio is 200% (or 2.0x) and the value to be programmed is calculated as follows:

   REG[0808h] bits 12-0 = 1024 x (1 ÷ scaling ratio)
   = 1024 x (1 ÷ 2.0)
   = 512 (200h)

4. Set the vertical scale ratio in REG[080Ch].

   For this example the vertical scale ratio is 200% (or 2.0x) and the value to be programmed is calculated as follows:

   REG[080Ch] bits 12-0 = 1024 x (1 ÷ scaling ratio)
   = 1024 x (1 ÷ 2.0)
   = 512 (200h)

5. Set the initial scale ratio in REG[084Ch].

   The initial scale ratio is set using the Panorama Area A scale ratio register and is calculated as follows:

   REG[084Ch] bits 12-0 = ((2 x Area A input size) ÷ Area A output size - (1 ÷ Area S scaling ratio)) x 1024
   = ((2 x 60) ÷ 200) - (1 ÷ 2)) x 1024
   = ((120 / 200) - 0.5) x 1024
   = 0.1 x 1024
   = 102.4 (rounded down)
   = 102 (066h)

6. Set the Panorama Area 1 start position in REG[0854h].

   The start position is calculated as follows:

   REG[0854h] bits 9-0 = Area A output size
   = 200 (0C8h)

7. Set the Panorama Area 2 start position in REG[0858h].

   The start position is calculated as follows:

   REG[0858h] bits 9-0 = Area A output size + Area B output size
   = 200 + 400
   = 600 (20Eh)

8. Set the Linear Panorama Area Delta in REG[00864h].

   The Linear Panorama Area Delta is calculated as follows:

   REG[0864h] bits 13-0 = ((REG[080Ch] - REG[084Ch]) ÷ (REG[0854h] - 1)) x 256
   = ((512 - 102.4) ÷ (200 - 1)) x 256
   = 409.6 ÷ 199 x 256
   = 526.92 (rounded down)
   = 526 (20Eh)

9. Enable Vertical Linear Panorama scaling by setting REG[0800h] bits 2-0 = 010b.
10. Adjust the PIP2 X/Y End Position registers as necessary.
11. Perform a register update according to which interface the PIP2 window is displayed on by setting REG[0600h] bit 15 or bit 14.

12.6.3 PIP2 Panorama Scaling Restrictions

PIP2 Panorama scaling mode has some restrictions based on the selected panorama mode, whether filtering is enabled, and whether the display is interlaced. The following table summarizes the possible settings.

Table 12-30: PIP2 Wide Scaling Mode Selection

REG[0804h] bit 15	REG[0800h] bits 2-0	Scaling Mode		Non Interlace	Interlace (Note 1)
0b	000b	Non Filter Mode	Normal Scaling	Yes	Yes
	001b		Vertical Partial Panorama	No	No
	010b		Vertical Linear Panorama	No	No
	011b		Horizontal Partial Panorama	Yes (Note 2)	Yes (Note 2)
	100b		Horizontal Linear Panorama	Yes (Note 2)	Yes (Note 2)
	101b ~ 111b		Reserved	—	—
1b	000b	Filter Mode	Normal Scaling	Yes	No
	001b		Vertical Partial Panorama	Yes	No
	010b		Vertical Linear Panorama	Yes	No
	011b		Horizontal Partial Panorama	Yes	No
	100b		Horizontal Linear Panorama	Yes	No
	101b - 111b		Reserved	—	—

Note

1. When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b and REG[0604h] bits 15-12 = 0100b or 1011b), the image data is output in interlace mode.
2. For horizontal partial and linear panorama, the PIP2 Window Horizontal Scale bits must be set less than 400h.

   REG[0808h] < 400h

12.7 Image Scrolling

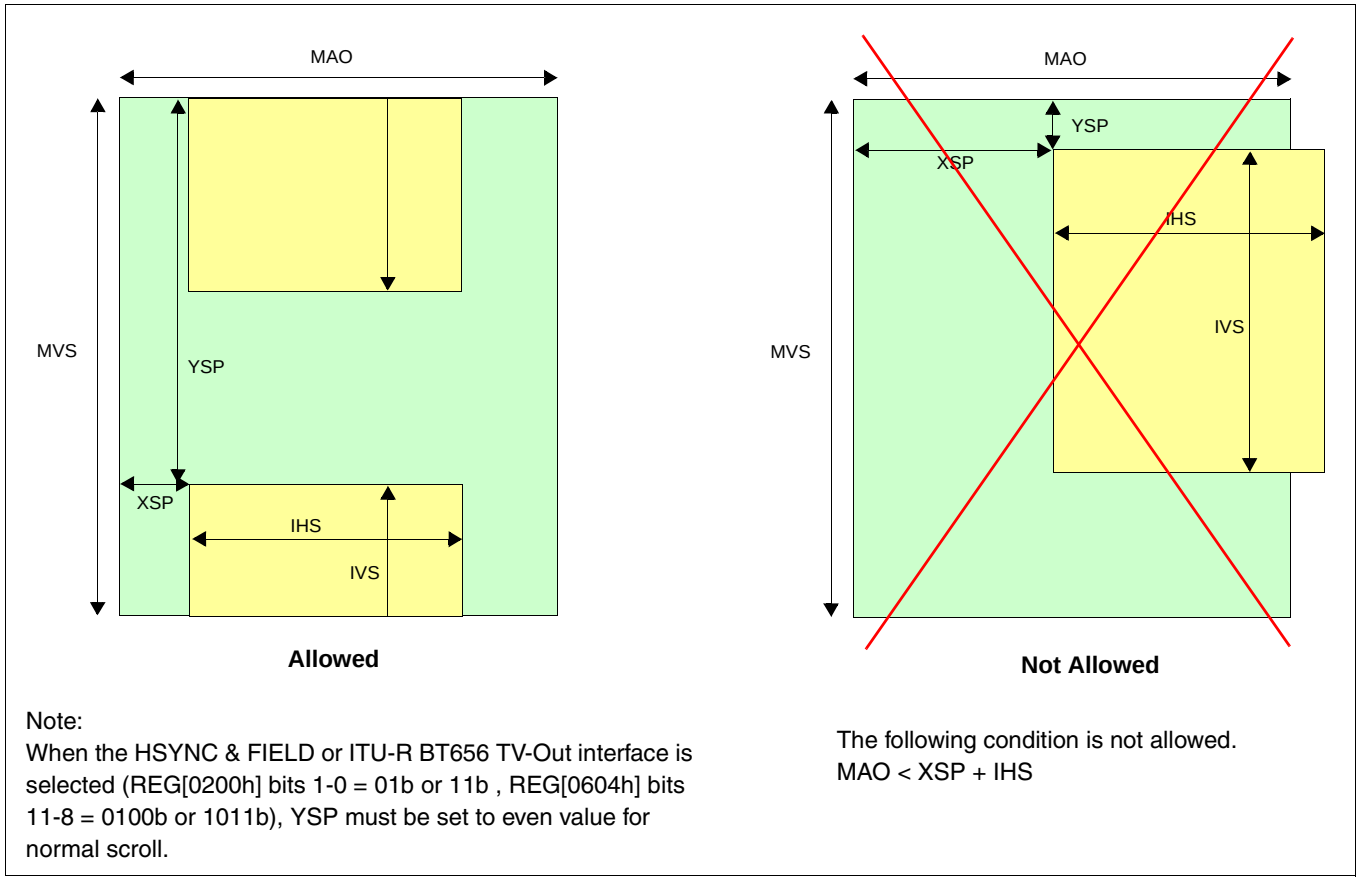
Image data can be stored in a non-contiguous memory area by allowing the image window to scroll, or "wrap around", in the vertical direction. Image scrolling automatically applies for all windows: Main, PIP1, and PIP2. There are no registers that must be programmed for this function to take effect.

Image scrolling works in the following way. When the Y start position + the image window becomes greater than the memory vertical size, the remainder of the image data is read by returning to the beginning of the memory area. The following condition causes image scrolling to occur.

YSP + Image Window > MVS

Note

1. Image scrolling in the horizontal direction is not supported.
2. When the Main1 window vertical pixel doubling is enabled (REG[0680h] bit 1 = 1b), the vertical image scrolling in the Main1 window is not supported. When the Main2 window vertical pixel doubling is enabled (REG[0680h] bit 3 = 1b), the vertical image scrolling in the Main2 window is not supported.



Note:
When the HSYNC & FIELD or ITU-R BT656 TV-Out interface is selected (REG[0200h] bits 1-0 = 01b or 11b , REG[0604h] bits 11-8 = 0100b or 1011b), YSP must be set to even value for normal scroll.

The following condition is not allowed.
MAO < XSP + IHS

Figure 12-35: Image Scrolling

13 Register Updates

When updating the configuration registers for some S1D13774 interfaces, specific procedures are required in order to ensure that the internal circuitry is updated correctly. The following interfaces require special consideration.

- Host Interface
- Video Input Interface
- LCD Interface
- TV-Out Interface

13.1 Host Interface

The Host interface can be configured to use either the Main Memory Write Path or the Sub Memory Write Path according to the setting of the Memory Write Path Select bit, REG[0500h] bit 0. When registers associated with the Host interface must be changed, the registers must be updated between the end of the current frame and the beginning of the next frame.

The Host interface register update sequence must be used when the Host interface is configured for the write path listed in the following table.

Table 13-1: Host Interface Registers Usage

REG[0500h] bit 0	Registers	Description
0b	REG[0504h] bits 13-0	Main Memory Write Path Configuration Register
	REG[0508h] ~ REG[052Ch]	Main Memory Write Path Registers
1b	REG[0580h] bits 6-0	Sub Memory Write Path Enable Register
	REG[0584h] ~ REG[05A8h]	Sub Memory Write Path Registers

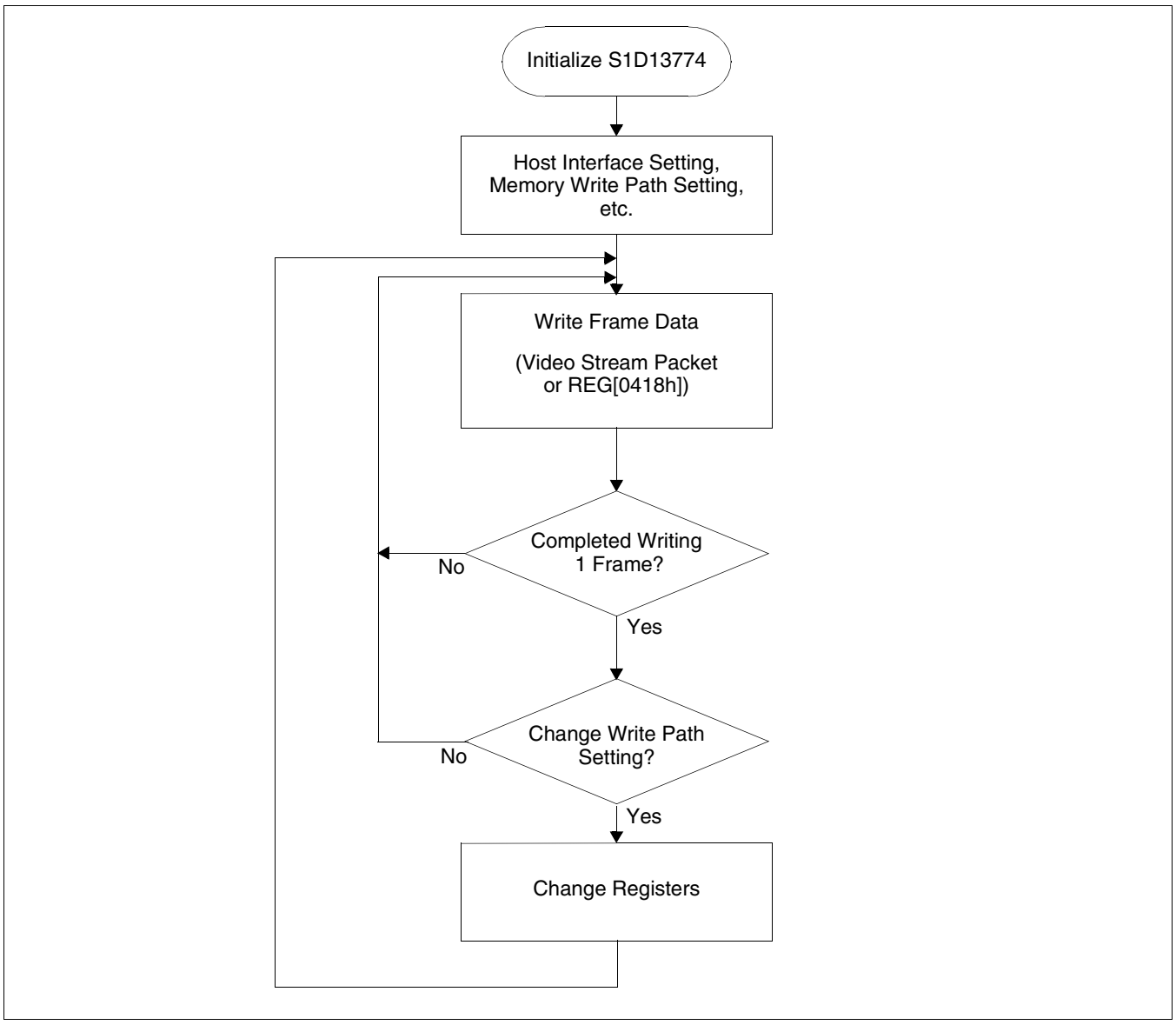


Figure 13-1: Host Interface Register Update Sequence

13.2 Video Input Interface

The Video Input interface can be configured to use either the Main Memory Write Path or the Sub Memory Write Path according to the setting of the Memory Write Path Select bit, REG[0500h] bit 0. When registers associated with the Video Input interface must be changed, update the registers and then set the corresponding Register Update bit. After the update bit is set, the updated register values will be reflected in the internal circuits synchronized with the next VSYNC of the Video Input interface.

The Video Input interface register update sequence must be used when the Video Input interface is configured for the write path listed in the following table.

Table 13-2: Video Input Interface Registers Usage

REG[0500h] bit 0	Registers	Description	Register Update Bit
0b	REG[0580h] bits 6-0	Sub Memory Write Path Enable Register	REG[0500h] bit 5
	REG[0584h] ~ REG[05A8h]	Sub Memory Write Path Registers	
1b	REG[0504h] bits 13-0	Main Memory Write Path Configuration Register	REG[0500h] bit 4
	REG[0508h] ~ REG[052Ch]	Main Memory Write Path Registers	

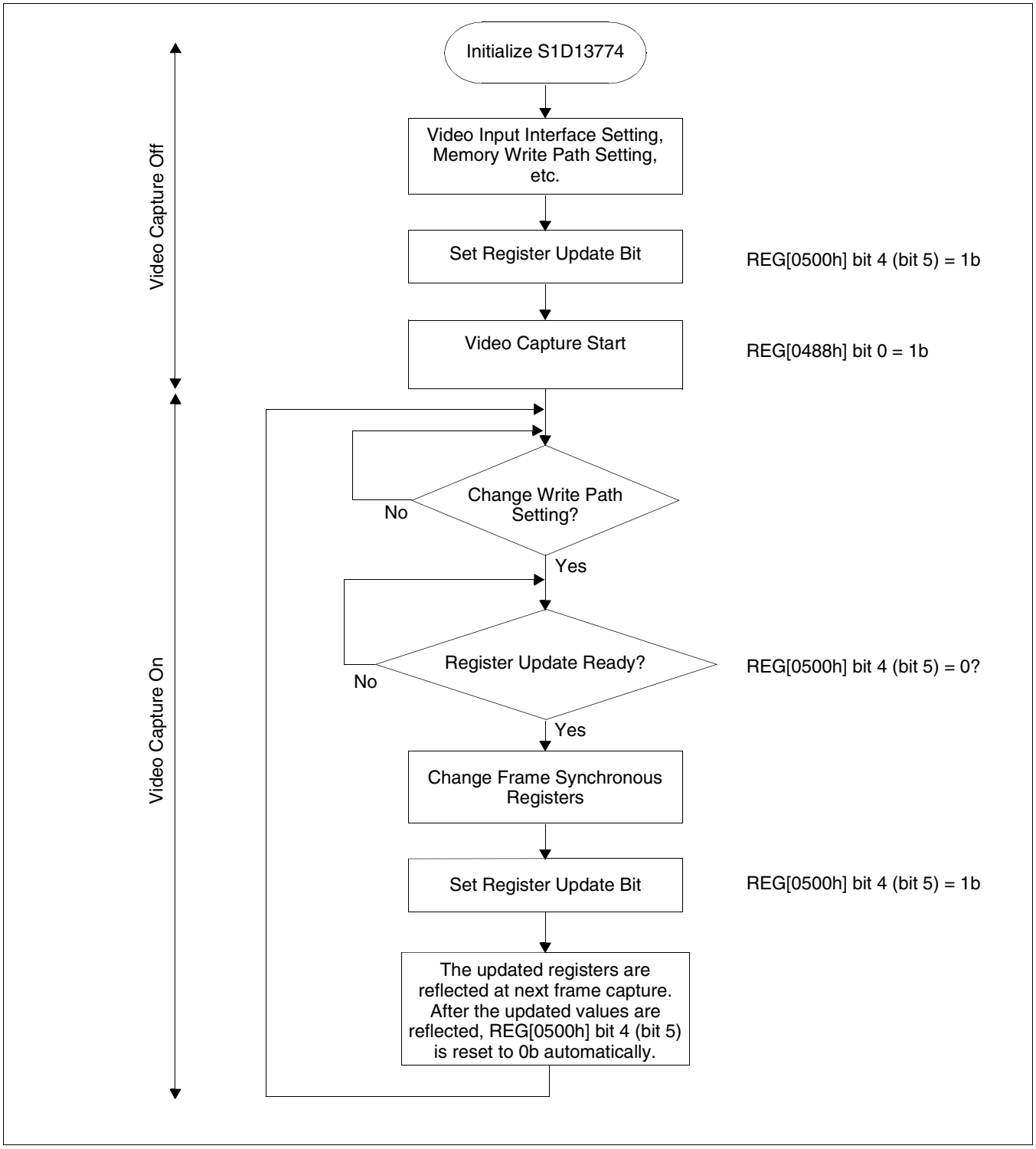


Figure 13-2: Video Input Interface Register Update Sequence

13.3 LCD Interface

When any of the registers that affect the LCD interface are changed, the LCD Interface Update Register bit (REG[0600h] bit 14) must be set before the updated values are reflected in the internal circuitry. When the update register bit is set, the updated values are reflected synchronized with VSYNC of the LCD1 interface.

The following table lists the registers that require the LCD Interface Update Register bit to be set using the register update sequences. Register update sequences are provided for LCD1, LCD2 using frame transfers, and LCD2 using auto frame transfers.

Table 13-3: LCD Frame Synchronous Registers

Address	bits	Register Name	LCD1	LCD2	LCD1 (Main Only)
			REG[0604h] bits 15-12		
			0001b	0010b	1011b
REG[0600h]	5	LUT Bypass Enable	Yes	Yes	No
REG[0604h]	0	Main1 Window Display Enable	Yes	Yes	Yes
	1	Main2 Window Display Enable	Yes	Yes	Yes
	2	PIP1 Window Display Enable	Yes	Yes	No
	3	PIP2 Window Display Enable	Yes	Yes	No
	5	Main Layer Mode Select	Yes	Yes	No
	6	PIP Layer Mode Select	Yes	Yes	No
REG[0608h]	All	Transparency and Alpha Blend Control Registers	Yes	Yes	No
REG[0614h] ~ REG[0644h]	All	Transparency and Alpha Blend Registers	Yes	Yes	No
REG[0648h]	All	Pseudo Setting Register	Yes	Yes	No
REG[0680h]	All	Main Window Registers	Yes	Yes	Yes
REG[0684h] ~ REG[06C8h]	All	Main Window Registers	Yes	Yes	Yes
REG[0700h]	All	PIP1 Window Register	Yes	Yes	No
REG[0704h] ~ REG[0748h]	All	PIP1 Window Registers	Yes	Yes	No
REG[0800h]	All	PIP2 Window Register	Yes	Yes	No
REG[0804h] ~ REG[0864h]	All	PIP2 Window Registers	Yes	Yes	No
REG[0900h] ~ REG[0930h]	All	AME Registers	Yes	Yes	No

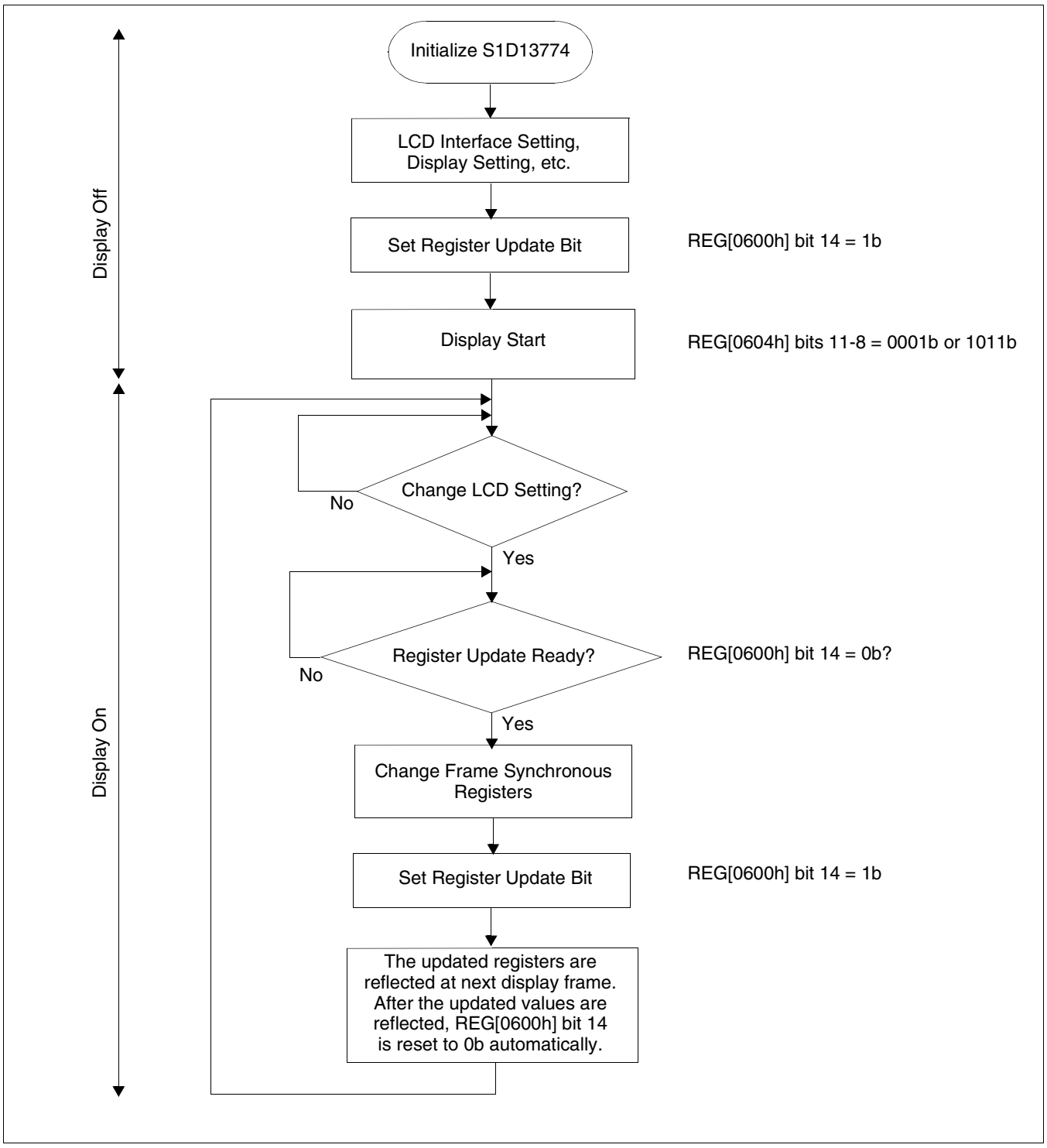


Figure 13-3: LCD1 Interface Register Update Sequence

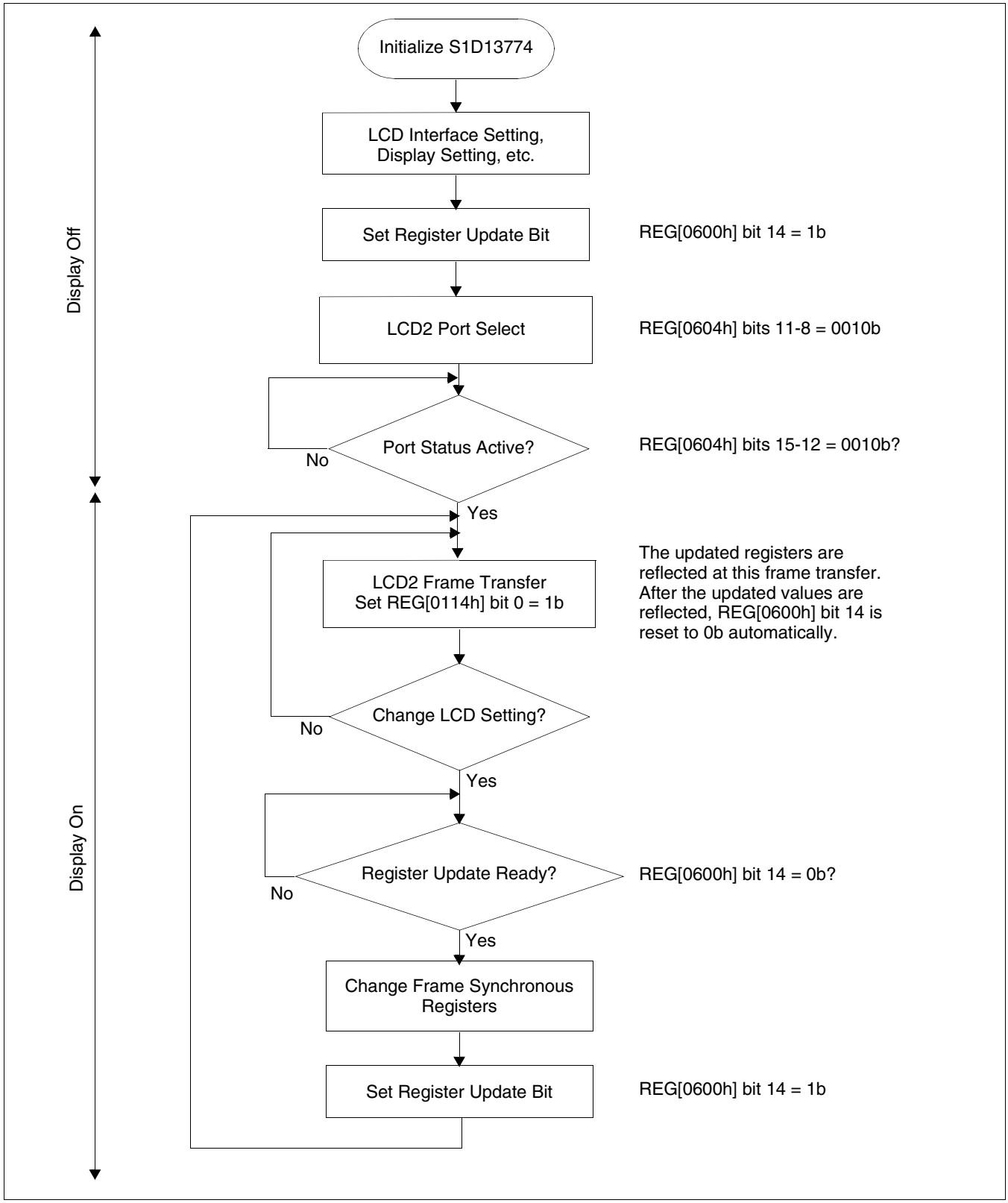


Figure 13-4: LCD2 Interface Register Update Sequence (Frame Transfer)

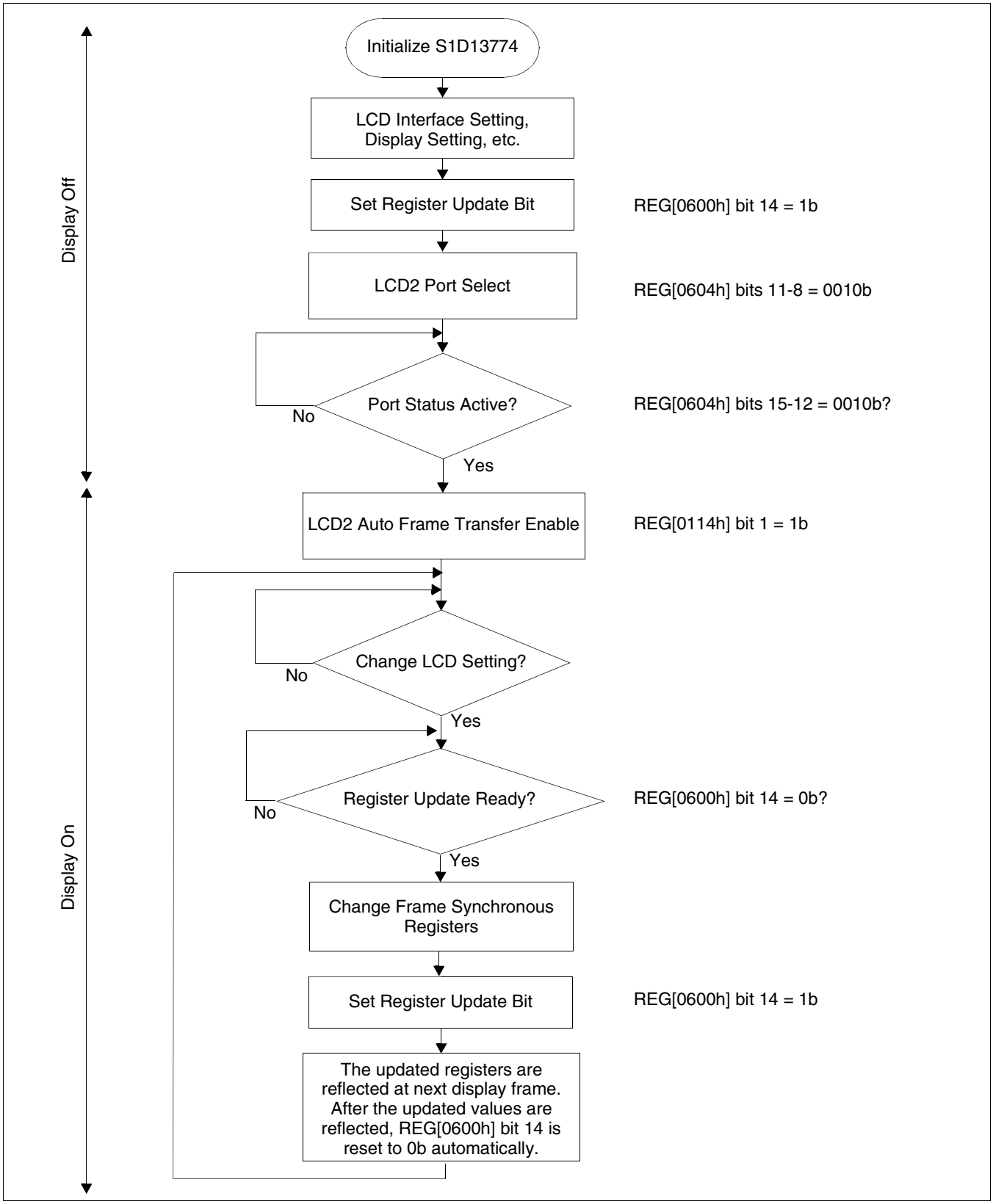


Figure 13-5: LCD2 Interface Register Update Sequence (Auto Frame Transfer)

13.4 TV-Out Interface

When any of the registers that affect the TV-Out interface are changed, the TV-Out Interface Update Register bit (REG[0600h] bit 15) must be set before the updated values are reflected in the internal circuitry. When the update register bit is set, the updated values are reflected synchronized with VSYNC of the TV-Out interface.

The following table lists the registers that require the TV-Out Interface Update Register bit to be set using the register update sequences. Register update sequences are provided for Hsync and FIELD / ITU-R BT656, Parallel using frame transfers, and Parallel using auto frame transfers.

Table 13-4: TV-Out Frame Synchronous Registers

Address	bits	Register Name	TV-Out (Main/PIP1/PIP2)	TV-Out (PIP1/PIP2)
			REG[0604h] bits 15-12	
			0100b	1011b
REG[0600h]	5	LUT Bypass Enable	Yes	Yes
REG[0604h]	0	Main1 Window Display Enable	Yes	No
	1	Main2 Window Display Enable	Yes	No
	2	PIP1 Window Display Enable	Yes	Yes
	3	PIP2 Window Display Enable	Yes	Yes
	5	Main Layer Mode Select	Yes	No
	6	PIP Layer Mode Select	Yes	Yes
REG[0608h]	1	PIP1 Transparency Enable	Yes	No
	2	PIP2 Transparency Enable	Yes	Yes
	7	Alpha Blend Mode Select	Yes	No
	11-8	Alpha Blend Key Color Enable	Yes	Yes
REG[0614h] ~ REG[0644h]	All	Transparency and Alpha Blend Control Registers	Yes	Yes
REG[0648h]	All	Pseudo Setting Register	Yes	Yes
REG[0680h]	All	Main Window Registers	Yes	No
REG[0684h] ~ REG[06C8h]	All	Main Window Registers	Yes	No
REG[0700h]	All	PIP1 Window Register	Yes	Yes
REG[0704h] ~ REG[0748h]	All	PIP1 Window Registers	Yes	Yes
REG[0800h]	All	PIP2 Window Register	Yes	Yes
REG[0804h] ~ REG[0864h]	All	PIP2 Window Registers	Yes	Yes
REG[0900h] ~ REG[0930h]	All	AME Registers	Yes	Yes

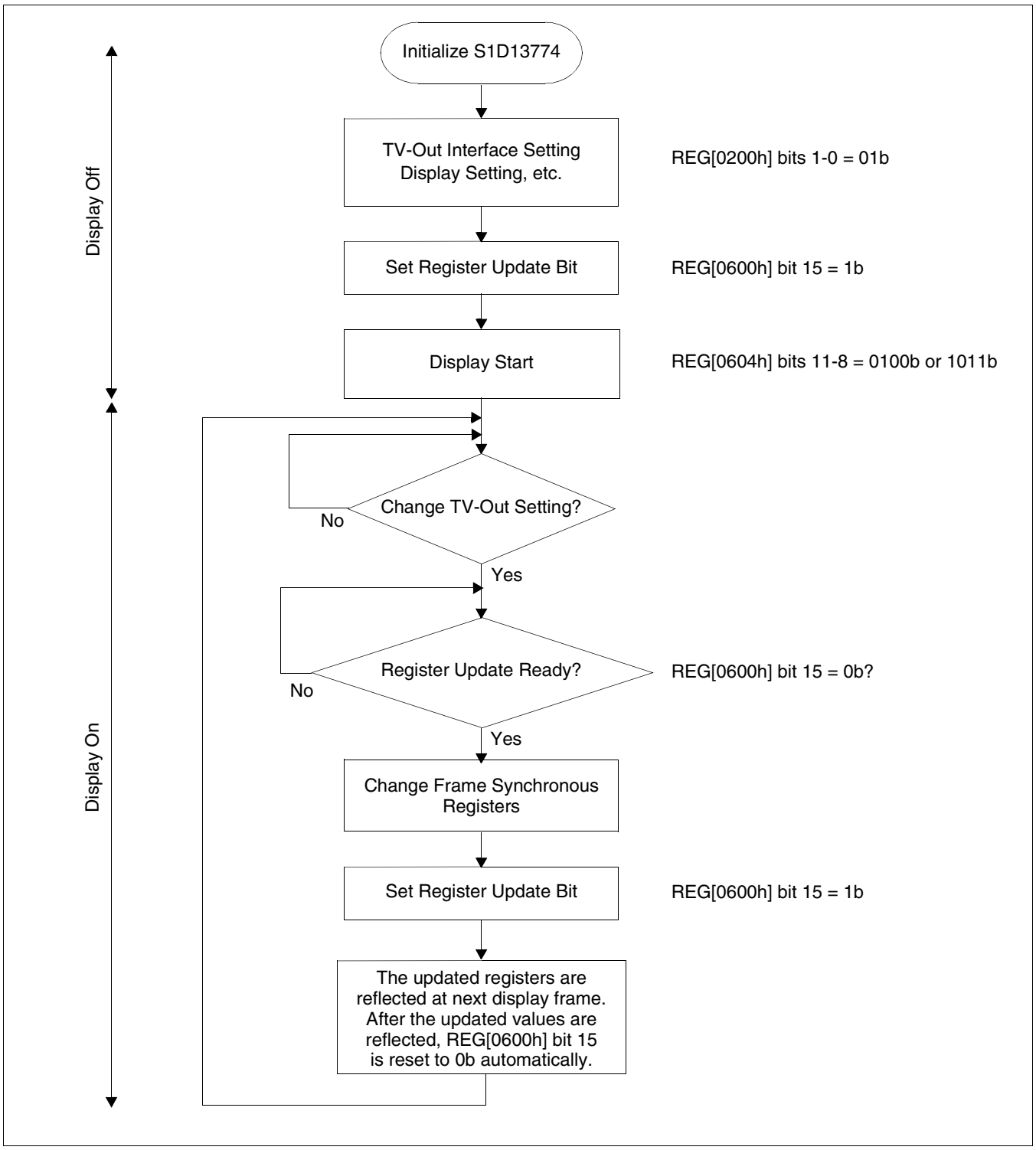


Figure 13-6: TV-Out Hsync and FIELD / ITU-R BT656 Interface Register Update Sequence

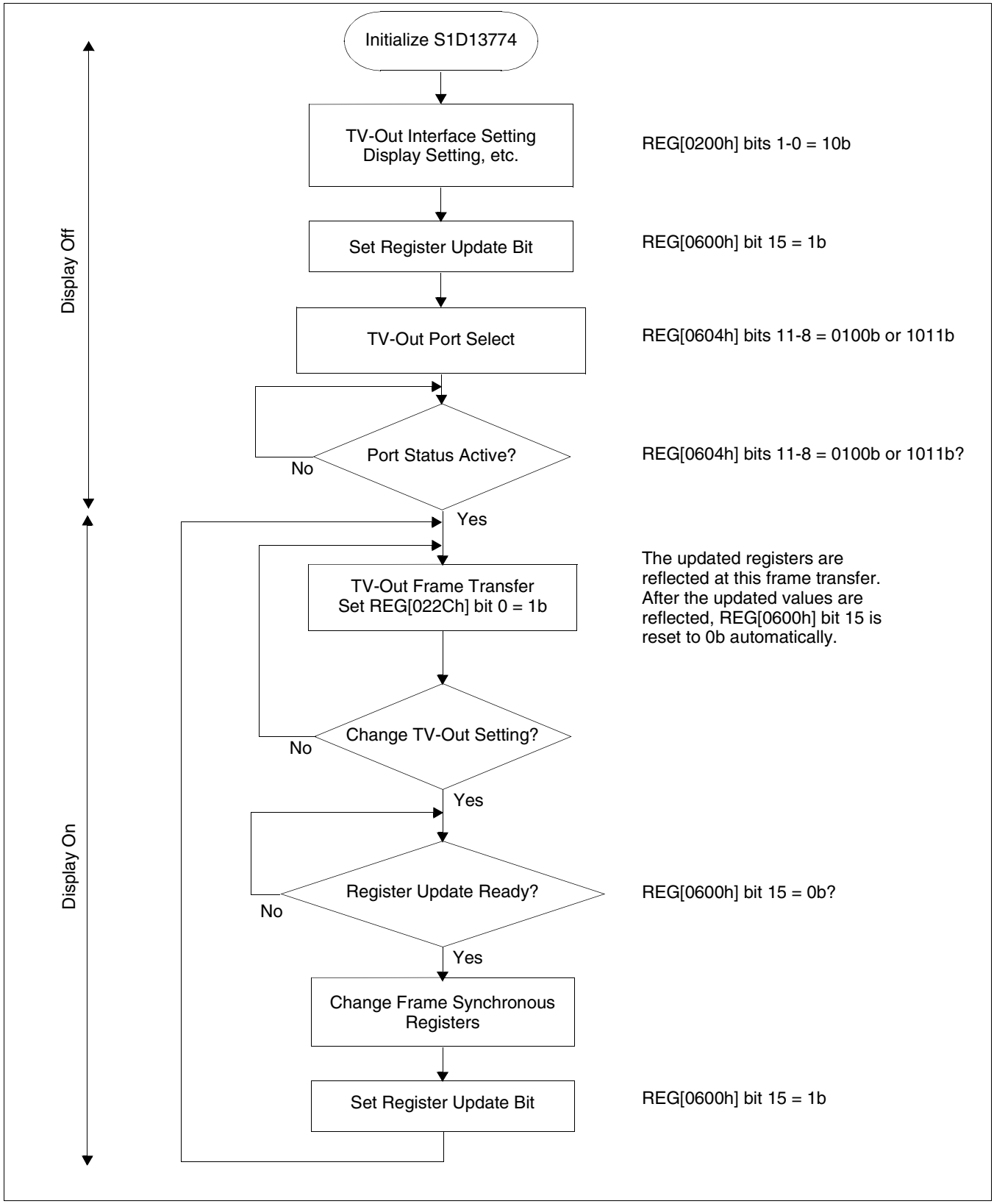


Figure 13-7: TV-Out Parallel Interface Register Update Sequence (Frame Transfer)

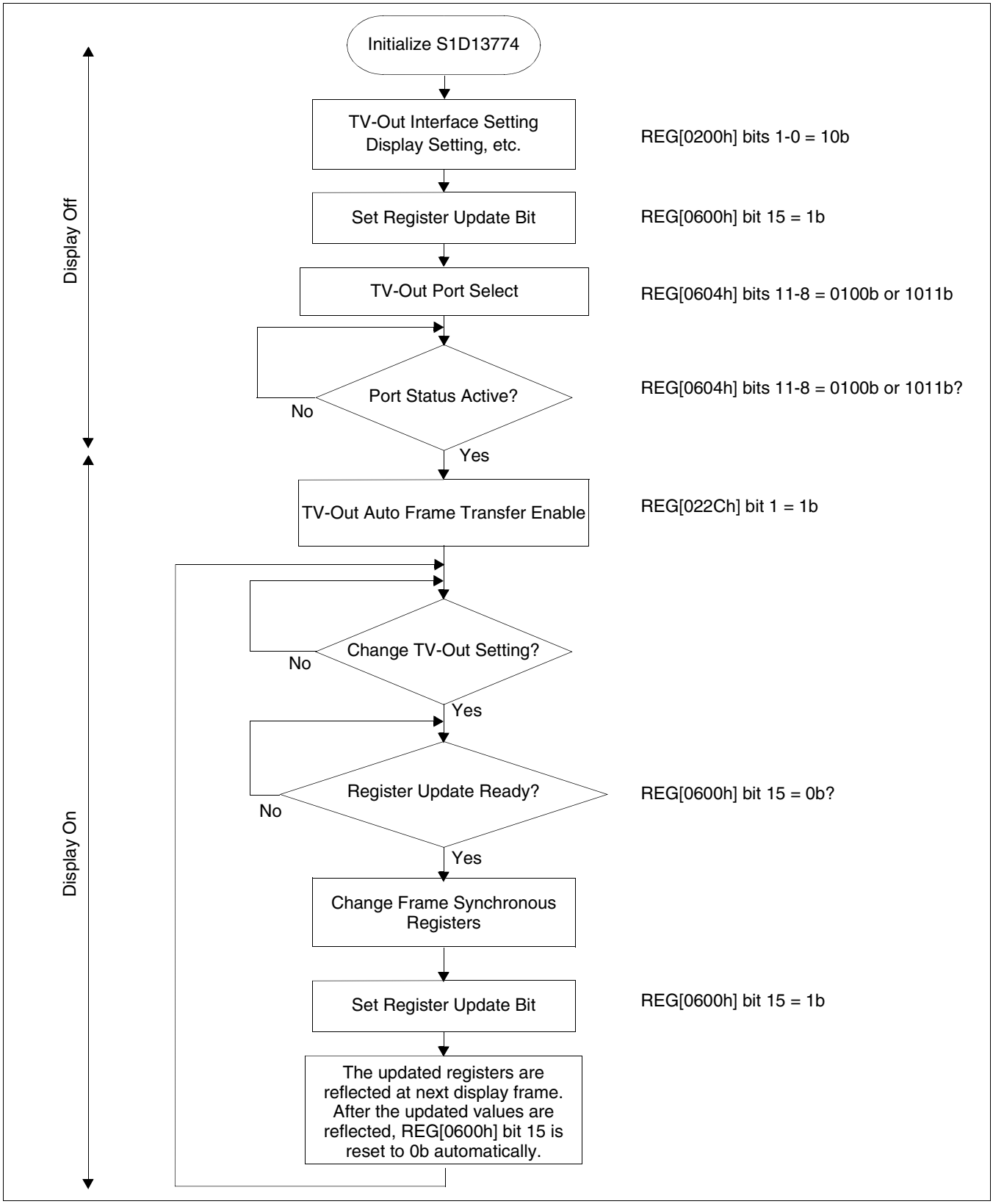


Figure 13-8: TV-Out Parallel Interface Register Update Sequence (Auto Frame Transfer)

14 Host Interface

The S1D13774 supports two Host interfaces:

- 18-bit Indirect interface
- I2C interface

Note
Although the I2C and Indirect interfaces are available at the same time, the interfaces must not be active at the same time.

14.1 Indirect Host Interface

The S1D13774 includes an 18-bit Indirect Host Interface which can be used to read/write the registers and write image data to memory. The Indirect Host Interface is selected when CNF0=1 at RESET#.

The following sections describe the Indirect Access Port and provide programming flows which show how to perform register and memory accesses.

14.1.1 Indirect Access Port

D/C# = 0b Indirect Interface Index Register
Default = 0000_0000h — Read/Write

Register Address bits 15-1															R/W Select
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-1 Register Address bits [15:1]
These bits set the register address for the indirect interface.

bit 0 R/W Select
This bit selects whether a read or a write is performed.
When this bit = 0b, a write is performed.
When this bit = 1b, a read is performed.

D/C# = 1b Indirect Interface Data Register
Default = 0000_0000h — Read/Write

Register Data bits 15-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

bits 15-0 Register Data bits [15:0]
These bits are the data port for the indirect interface.

Note
When the host interface input format is set for RGB 6:6:6 Format 5 (REG[0400h] bits 2-0 = 001b and REG[0400h] bits 6-4 = 100b), DB[17:16] are used. For details, refer to Section 14.5.9, “RGB 6:6:6 Format 5” on page 366.

14.1.2 Register Access

For register accesses by the Host, a dummy read must be added as shown in the following procedure.

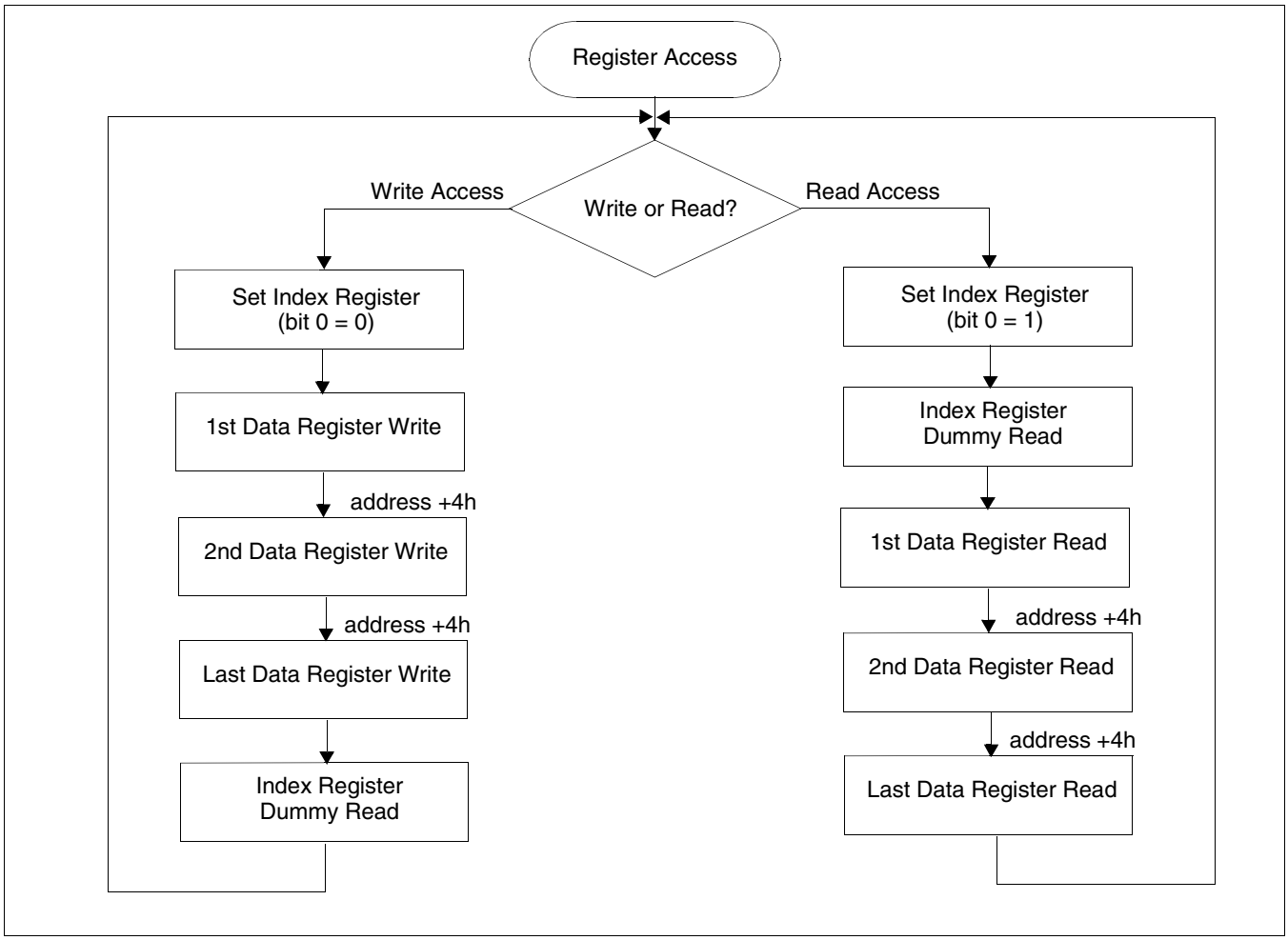


Figure 14-1: Indirect Interface Register Access

14.1.3 Memory Write Access using Main/Sub Memory Write Path

When image data is written using the Main or Sub Memory Write Path, the following procedure should be used. If the data writes to REG[0418h] are interrupted for other register accesses, the index register address must be reset to REG[0418h] once the other registers accesses are complete. Then, the remainder of the data write can be finished.

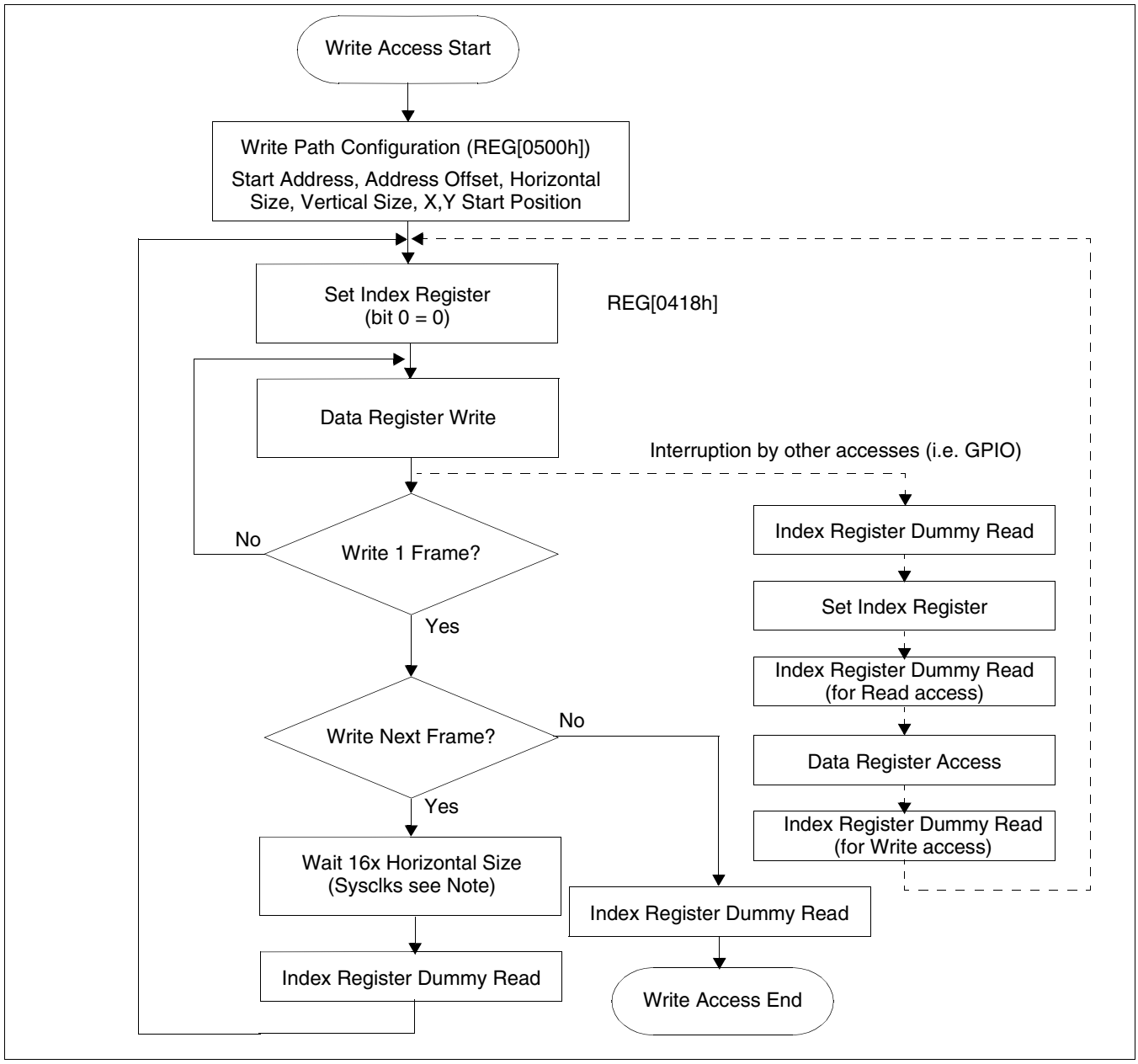


Figure 14-2: Memory Write Access using Main/Sub Memory Write Path

Note

For example if the Horizontal Size is 128 pixels, wait for 2048 sysclks or more.

14.2 I2C Interface

The S1D13774 includes I2C slave functionality which can be used to access the S1D13774 registers instead of the Indirect interface. The S1D13774 I2C slave has the following features.

- 7-bit I2C slave address support (10-bit not supported)
- supports Standard Mode (100Kbps) or Fast Mode (400Kbps) depending on the frequency of the I2C source clock

The slave address is configured using the I2C Slave Address bits, REG[0B04h] bits 14-8, and has a default value of 55h (1010101b).

Each I2C access consists of a 16-bit address (8-bit x 2) and 16 bits of data (8-bit x 2). It is possible to continuously write or read using Auto-Increment. For further information on I2C write and read accesses, see Section 14.2.3, “I2C Access Examples” on page 358.

Note
The Indirect interface must not be accessed while the I2C interface is being accessed.

There are three methods of starting the I2C interface as shown below.

Table 14-1: I2C Start-up Methods

Start-Up Trigger	I2C Source CLK		Operation in Power Save Mode (REG[002Ch] bits 1-0)	
	CNF1 = L	CNF1 = H	Sleep, Standby A, Standby B Mode	Normal Operation Mode
I2CEN pin	CLKI (Note)	OSCI/OSCO (Note)	Available	Available
Quick Enable Register REG[0030h] bit 0	CLKI (Note)	OSCI/OSCO (Note)	Available	Available
Enable Register REG[0B04h] bit 0	System Clock	Reserved	Not available	Available

Note
For Fast mode (400kbps), I2C Source Clock ≥ 24MHz.
For Standard mode (100kbps), I2C Source Clock ≥ 5.4MHz.

14.2.1 Register Access Restrictions

The following registers cannot be accessed using the I2C interface.

Table 14-2: Register Access Restrictions

REG[0030h]	I2C Quick Enable Register
REG[0418h]	Host Memory Write Access Port Register
REG[0B00h]	I2C Clock Divisor Register
REG[0B04h]	I2C Enable Register

14.2.2 I2C Example Flowcharts

Start Up using I2CEN or I2C Quick Enable Register

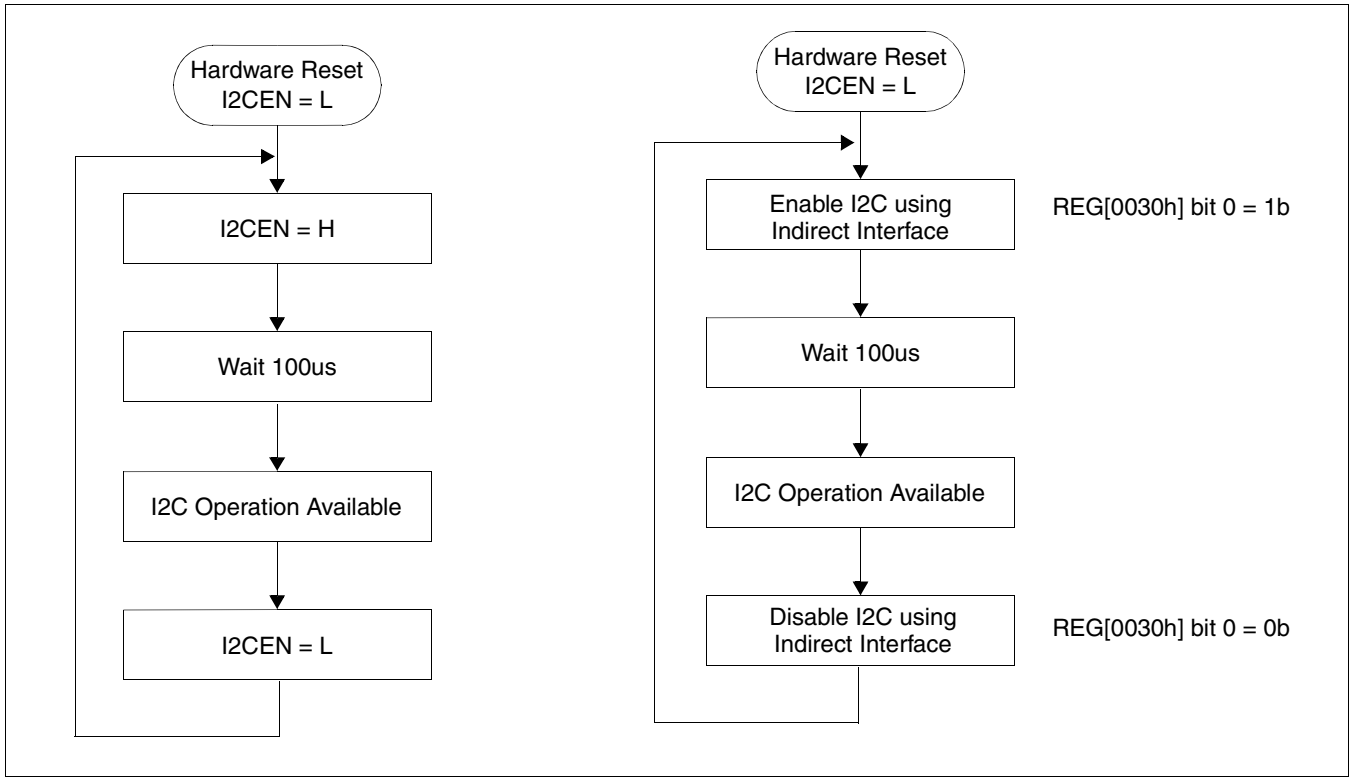


Figure 14-3: Start Up using I2CEN or I2C Quick Enable Register

Start Up using I2C Enable Register

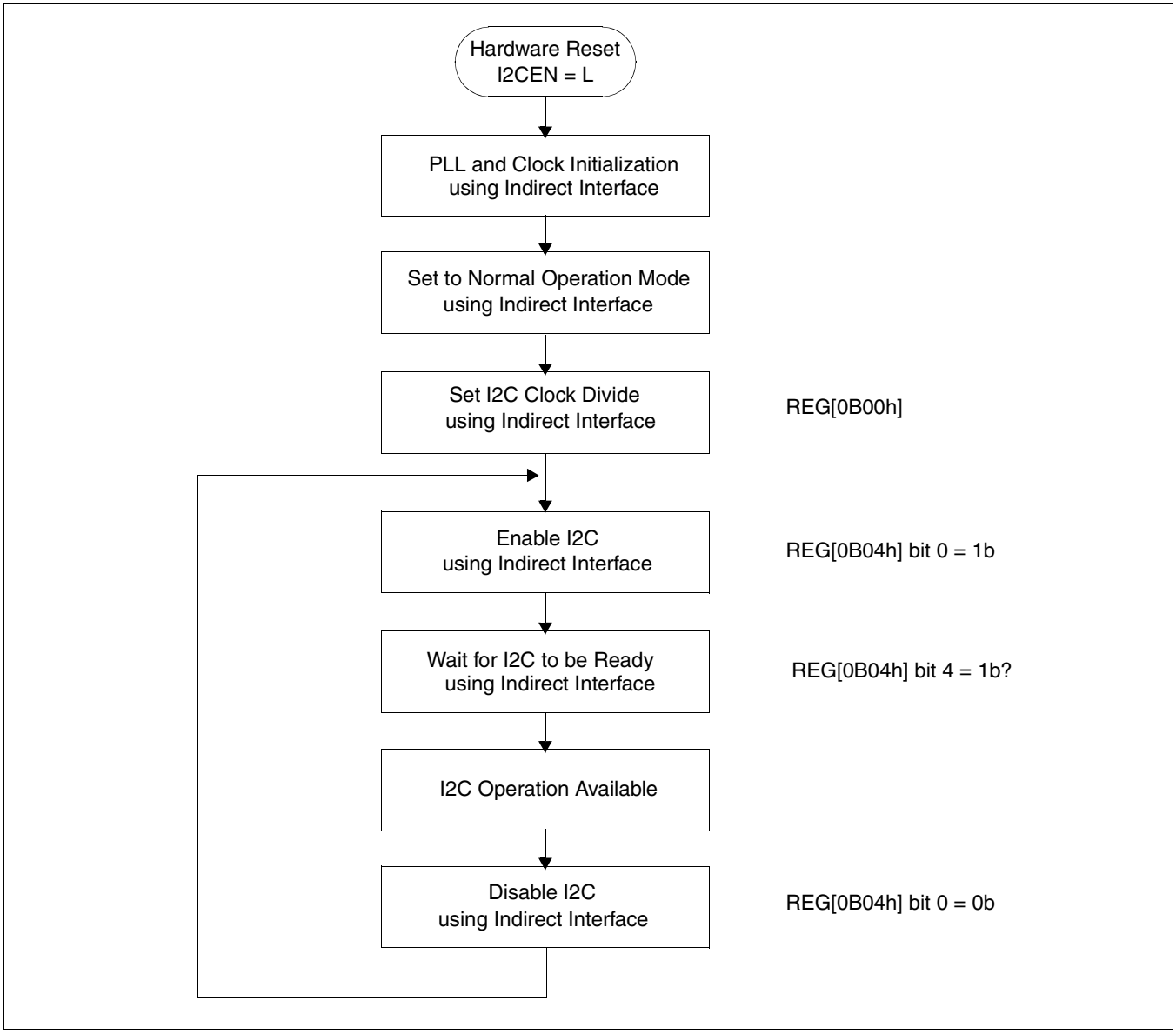


Figure 14-4: Start Up using I2C Enable Register

14.2.3 I2C Access Examples

Write Access

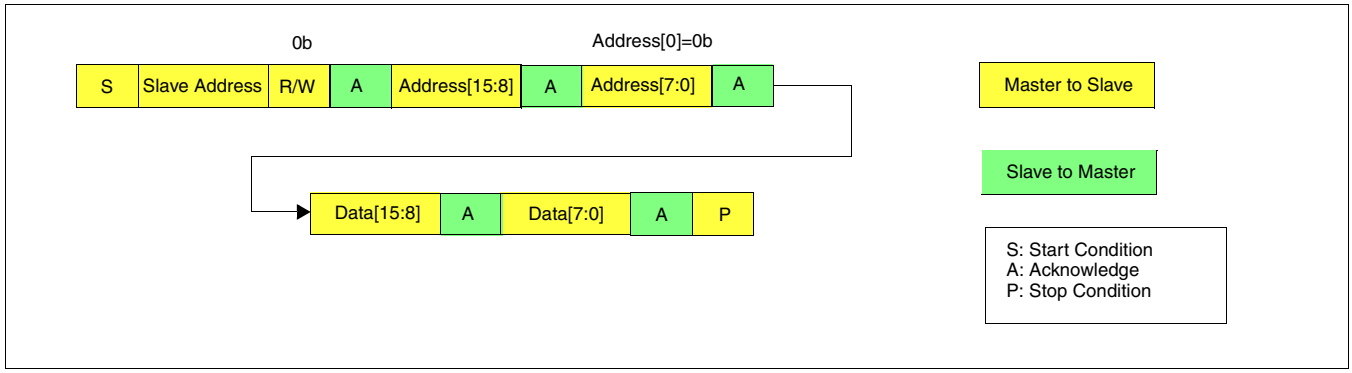


Figure 14-5: Write Access

Note

For write operations, Address[0] must be set to 0b.

Continuous Write Access (Address Auto Increment)

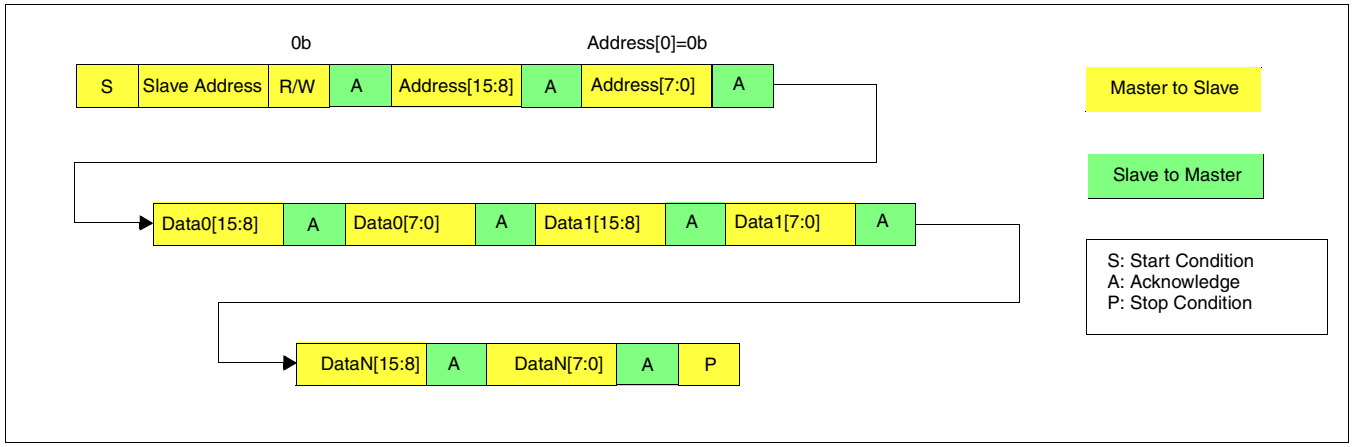


Figure 14-6: Continuous Write Access

Note

1. For write operations, Address[0] must be set to 0b.
2. If a register labeled as “Address Auto Increment Disable” is written, the address is repeatedly written until a new address is specified.

Read Access

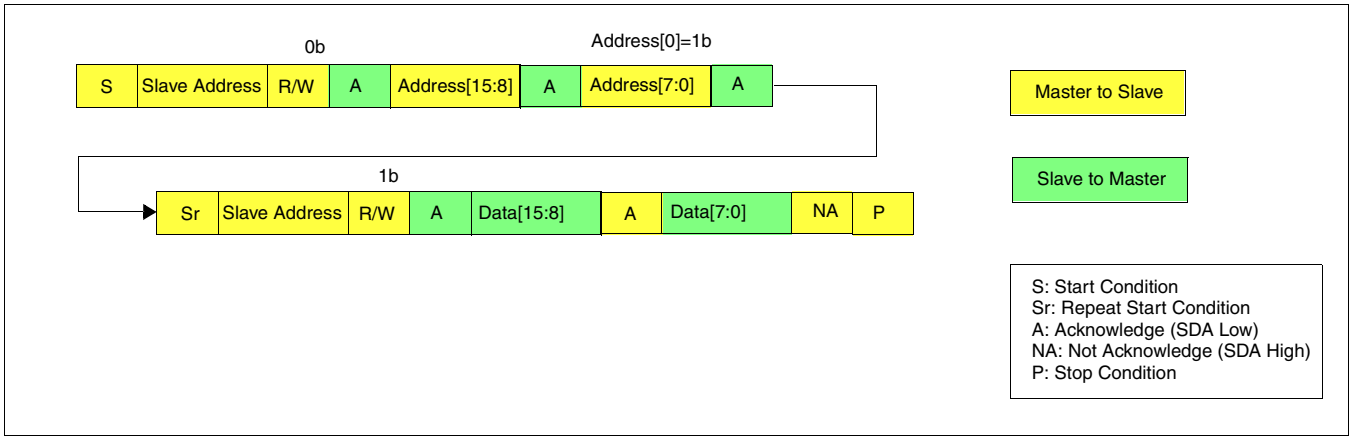


Figure 14-7: Read Access

Note

For read operations, Address[0] must be set to 1b.

Continuous Read Access (Address Auto Increment)

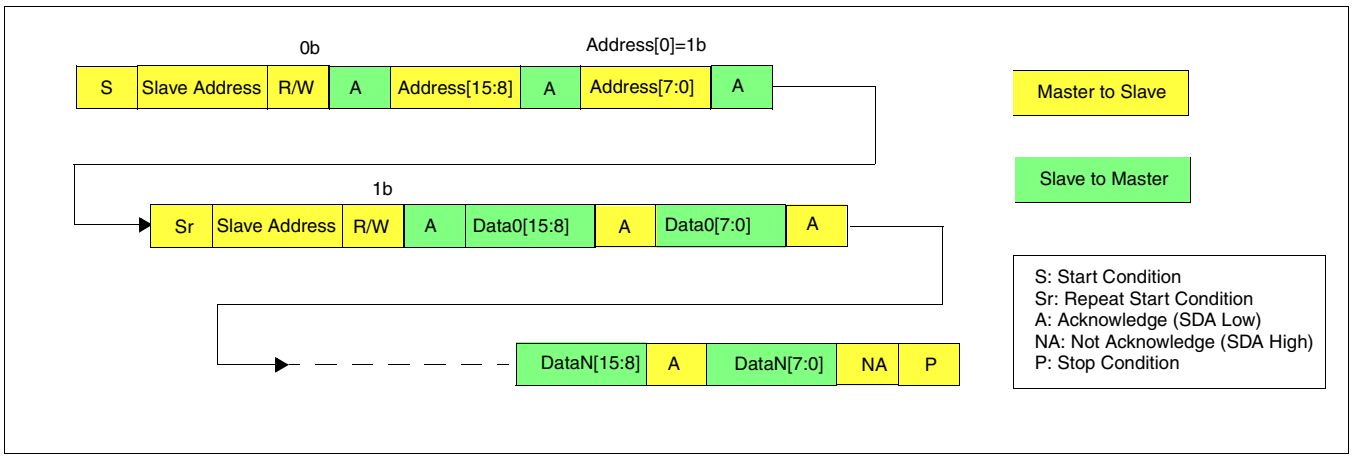


Figure 14-8: Continuous Read Access

Note

1. For read operations, Address[0] must be set to 1b.
2. If a register labeled as “Address Auto Increment Disable” is read from, the address is repeatedly read from until a new address is specified.

14.3 Register Auto Increment

The Host can perform continuous register read or write accesses using the Auto Increment function. This function allows reads or writes from/to consecutive addresses without requiring the Index register to be reset. For example, the Auto Increment function is used by I2C continuous accesses.

However, some registers do not support the Auto Increment function. These registers are identified as “Address Auto Increment Disable” in Section 9.2, “Register Set” on page 92 and in the register description headers (see Section 9.4, “Register Descriptions” on page 96). When one of these registers is reached, the register index is no longer auto incremented and the index register must be set for the next desired index.

There are also certain register boundaries that cannot be “auto incremented” across. It is not possible to auto increment between:

- REG[0230h] and REG[0300h]
- REG[0350h] and REG[0400h]
- REG[0B04h]

14.4 Host Interface VSYNC Output (Tearing Effect)

The VSYNC signal (TE) is output to the Host and can be used to indicate when it is safe to write new data from the Host in order to prevent visual tearing of an image. The source of the TE signal can be selected from four signals using the TE Source Select bits, REG[0404h] bits 11-10.

The output timing can be adjusted relative to the internally generated VSYNC of the RGB Interface and the TV-Out Interface.

- TE can be delayed by a number of lines (unit of HSYNC) relative to the internal VSYNC (see REG[0404h] bits 9-0).
- TE output rate can be set to output from once for every frame to once for every 15 frames (see REG[0404h] bits 15-12).

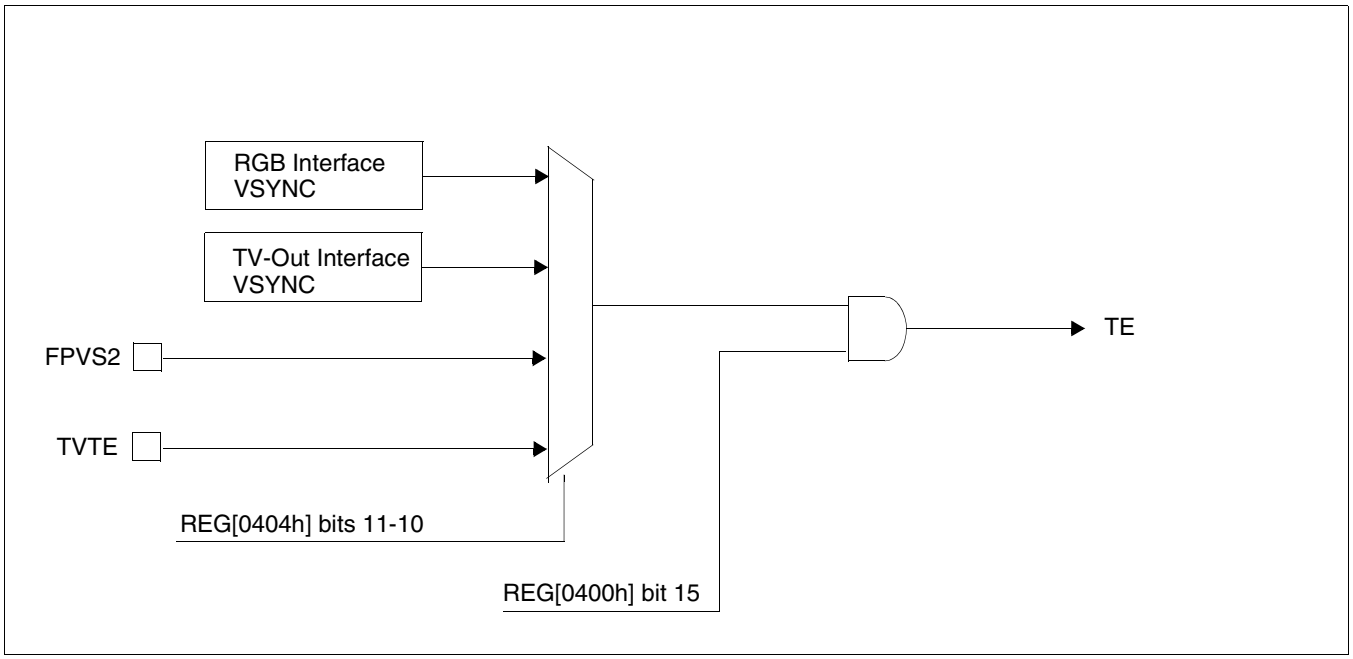


Figure 14-9: TE Output

14.5 Host Interface Input Format

The following input formats are used for the indirect interface.

The S1D13774 has no Host input resolution restrictions. However, when the width is an odd value and a 2 pixel / 3 cycle RGB format is selected (RGB 8:8:8 format 1/3 and RGB 6:6:6 format 1/3), the Host inputs the last pixel of the current line and the first pixel of the next line mixed within the same input data. If both the width and the height are odd values, the host inputs the last pixel for the frame using 2 cycles instead of 3 (the upper/lower byte of cycle 2 is ignored based on whether format 1 or format 3 is selected).

14.5.1 RGB 8:8:8 Format 1

RGB 8:8:8: REG[0400h] bits 2-0 = 010b, Format 1: REG[0400h] bits 6-4 = 000b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-3: RGB 8:8:8 Input Format 1

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$G_{(0,0)}^{7}$	$G_{(0,0)}^{6}$	$G_{(0,0)}^{5}$	$G_{(0,0)}^{4}$	$G_{(0,0)}^{3}$	$G_{(0,0)}^{2}$	$G_{(0,0)}^{1}$	$G_{(0,0)}^{0}$	$B_{(0,0)}^{7}$	$B_{(0,0)}^{6}$	$B_{(0,0)}^{5}$	$B_{(0,0)}^{4}$	$B_{(0,0)}^{3}$	$B_{(0,0)}^{2}$	$B_{(0,0)}^{1}$	$B_{(0,0)}^{0}$
2	—	—	$B_{(1,0)}^{7}$	$B_{(1,0)}^{6}$	$B_{(1,0)}^{5}$	$B_{(1,0)}^{4}$	$B_{(1,0)}^{3}$	$B_{(1,0)}^{2}$	$B_{(1,0)}^{1}$	$B_{(1,0)}^{0}$	$R_{(0,0)}^{7}$	$R_{(0,0)}^{6}$	$R_{(0,0)}^{5}$	$R_{(0,0)}^{4}$	$R_{(0,0)}^{3}$	$R_{(0,0)}^{2}$	$R_{(0,0)}^{1}$	$R_{(0,0)}^{0}$
3	—	—	$R_{(1,0)}^{7}$	$R_{(1,0)}^{6}$	$R_{(1,0)}^{5}$	$R_{(1,0)}^{4}$	$R_{(1,0)}^{3}$	$R_{(1,0)}^{2}$	$R_{(1,0)}^{1}$	$R_{(1,0)}^{0}$	$G_{(1,0)}^{7}$	$G_{(1,0)}^{6}$	$G_{(1,0)}^{5}$	$G_{(1,0)}^{4}$	$G_{(1,0)}^{3}$	$G_{(1,0)}^{2}$	$G_{(1,0)}^{1}$	$G_{(1,0)}^{0}$
	...																	
	—	—	$G_{(0,1)}^{7}$	$G_{(0,1)}^{6}$	$G_{(0,1)}^{5}$	$G_{(0,1)}^{4}$	$G_{(0,1)}^{3}$	$G_{(0,1)}^{2}$	$G_{(0,1)}^{1}$	$G_{(0,1)}^{0}$	$B_{(0,1)}^{7}$	$B_{(0,1)}^{6}$	$B_{(0,1)}^{5}$	$B_{(0,1)}^{4}$	$B_{(0,1)}^{3}$	$B_{(0,1)}^{2}$	$B_{(0,1)}^{1}$	$B_{(0,1)}^{0}$
	—	—	$B_{(1,1)}^{7}$	$B_{(1,1)}^{6}$	$B_{(1,1)}^{5}$	$B_{(1,1)}^{4}$	$B_{(1,1)}^{3}$	$B_{(1,1)}^{2}$	$B_{(1,1)}^{1}$	$B_{(1,1)}^{0}$	$R_{(0,1)}^{7}$	$R_{(0,1)}^{6}$	$R_{(0,1)}^{5}$	$R_{(0,1)}^{4}$	$R_{(0,1)}^{3}$	$R_{(0,1)}^{2}$	$R_{(0,1)}^{1}$	$R_{(0,1)}^{0}$
	—	—	$R_{(1,1)}^{7}$	$R_{(1,1)}^{6}$	$R_{(1,1)}^{5}$	$R_{(1,1)}^{4}$	$R_{(1,1)}^{3}$	$R_{(1,1)}^{2}$	$R_{(1,1)}^{1}$	$R_{(1,1)}^{0}$	$G_{(1,1)}^{7}$	$G_{(1,1)}^{6}$	$G_{(1,1)}^{5}$	$G_{(1,1)}^{4}$	$G_{(1,1)}^{3}$	$G_{(1,1)}^{2}$	$G_{(1,1)}^{1}$	$G_{(1,1)}^{0}$
	...																	

14.5.2 RGB 8:8:8 Format 2

RGB 8:8:8: REG[0400h] bits 2-0 = 010b, Format 2: REG[0400h] bits 6-4 = 001b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-4: RGB 8:8:8 Input Format 2

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$B_{(0,0)}^{7}$	$B_{(0,0)}^{6}$	$B_{(0,0)}^{5}$	$B_{(0,0)}^{4}$	$B_{(0,0)}^{3}$	$B_{(0,0)}^{2}$	$B_{(0,0)}^{1}$	$B_{(0,0)}^{0}$	—	—	—	—	—	—	—	—
2	—	—	$R_{(0,0)}^{7}$	$R_{(0,0)}^{6}$	$R_{(0,0)}^{5}$	$R_{(0,0)}^{4}$	$R_{(0,0)}^{3}$	$R_{(0,0)}^{2}$	$R_{(0,0)}^{1}$	$R_{(0,0)}^{0}$	$G_{(0,0)}^{7}$	$G_{(0,0)}^{6}$	$G_{(0,0)}^{5}$	$G_{(0,0)}^{4}$	$G_{(0,0)}^{3}$	$G_{(0,0)}^{2}$	$G_{(0,0)}^{1}$	$G_{(0,0)}^{0}$
3	—	—	$B_{(1,0)}^{7}$	$B_{(1,0)}^{6}$	$B_{(1,0)}^{5}$	$B_{(1,0)}^{4}$	$B_{(1,0)}^{3}$	$B_{(1,0)}^{2}$	$B_{(1,0)}^{1}$	$B_{(1,0)}^{0}$	—	—	—	—	—	—	—	—
4			$R_{(1,0)}^{7}$	$R_{(1,0)}^{6}$	$R_{(1,0)}^{5}$	$R_{(1,0)}^{4}$	$R_{(1,0)}^{3}$	$R_{(1,0)}^{2}$	$R_{(1,0)}^{1}$	$R_{(1,0)}^{0}$	$G_{(1,0)}^{7}$	$G_{(1,0)}^{6}$	$G_{(1,0)}^{5}$	$G_{(1,0)}^{4}$	$G_{(1,0)}^{3}$	$G_{(1,0)}^{2}$	$G_{(1,0)}^{1}$	$G_{(1,0)}^{0}$
	...																	
	—	—	$B_{(0,1)}^{7}$	$B_{(0,1)}^{6}$	$B_{(0,1)}^{5}$	$B_{(0,1)}^{4}$	$B_{(0,1)}^{3}$	$B_{(0,1)}^{2}$	$B_{(0,1)}^{1}$	$B_{(0,1)}^{0}$	—	—	—	—	—	—	—	—
	—	—	$R_{(0,1)}^{7}$	$R_{(0,1)}^{6}$	$R_{(0,1)}^{5}$	$R_{(0,1)}^{4}$	$R_{(0,1)}^{3}$	$R_{(0,1)}^{2}$	$R_{(0,1)}^{1}$	$R_{(0,1)}^{0}$	$G_{(0,1)}^{7}$	$G_{(0,1)}^{6}$	$G_{(0,1)}^{5}$	$G_{(0,1)}^{4}$	$G_{(0,1)}^{3}$	$G_{(0,1)}^{2}$	$G_{(0,1)}^{1}$	$G_{(0,1)}^{0}$
	—	—	$B_{(1,1)}^{7}$	$B_{(1,1)}^{6}$	$B_{(1,1)}^{5}$	$B_{(1,1)}^{4}$	$B_{(1,1)}^{3}$	$B_{(1,1)}^{2}$	$B_{(1,1)}^{1}$	$B_{(1,1)}^{0}$	—	—	—	—	—	—	—	—
			$R_{(1,1)}^{7}$	$R_{(1,1)}^{6}$	$R_{(1,1)}^{5}$	$R_{(1,1)}^{4}$	$R_{(1,1)}^{3}$	$R_{(1,1)}^{2}$	$R_{(1,1)}^{1}$	$R_{(1,1)}^{0}$	$G_{(1,1)}^{7}$	$G_{(1,1)}^{6}$	$G_{(1,1)}^{5}$	$G_{(1,1)}^{4}$	$G_{(1,1)}^{3}$	$G_{(1,1)}^{2}$	$G_{(1,1)}^{1}$	$G_{(1,1)}^{0}$
	...																	

14.5.3 RGB 8:8:8 Format 3

RGB 8:8:8: REG[0400h] bits 2-0 = 010b, Format 3: REG[0400h] bits 6-4 = 010b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-5: RGB 8:8:8 Input Format 3

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$R_{(0,0)}^{7}$	$R_{(0,0)}^{6}$	$R_{(0,0)}^{5}$	$R_{(0,0)}^{4}$	$R_{(0,0)}^{3}$	$R_{(0,0)}^{2}$	$R_{(0,0)}^{1}$	$R_{(0,0)}^{0}$	$G_{(0,0)}^{7}$	$G_{(0,0)}^{6}$	$G_{(0,0)}^{5}$	$G_{(0,0)}^{4}$	$G_{(0,0)}^{3}$	$G_{(0,0)}^{2}$	$G_{(0,0)}^{1}$	$G_{(0,0)}^{0}$
2	—	—	$B_{(0,0)}^{7}$	$B_{(0,0)}^{6}$	$B_{(0,0)}^{5}$	$B_{(0,0)}^{4}$	$B_{(0,0)}^{3}$	$B_{(0,0)}^{2}$	$B_{(0,0)}^{1}$	$B_{(0,0)}^{0}$	$R_{(1,0)}^{7}$	$R_{(1,0)}^{6}$	$R_{(1,0)}^{5}$	$R_{(1,0)}^{4}$	$R_{(1,0)}^{3}$	$R_{(1,0)}^{2}$	$R_{(1,0)}^{1}$	$R_{(1,0)}^{0}$
3	—	—	$G_{(1,0)}^{7}$	$G_{(1,0)}^{6}$	$G_{(1,0)}^{5}$	$G_{(1,0)}^{4}$	$G_{(1,0)}^{3}$	$G_{(1,0)}^{2}$	$G_{(1,0)}^{1}$	$G_{(1,0)}^{0}$	$B_{(1,0)}^{7}$	$B_{(1,0)}^{6}$	$B_{(1,0)}^{5}$	$B_{(1,0)}^{4}$	$B_{(1,0)}^{3}$	$B_{(1,0)}^{2}$	$B_{(1,0)}^{1}$	$B_{(1,0)}^{0}$
	...																	
	—	—	$R_{(0,1)}^{7}$	$R_{(0,1)}^{6}$	$R_{(0,1)}^{5}$	$R_{(0,1)}^{4}$	$R_{(0,1)}^{3}$	$R_{(0,1)}^{2}$	$R_{(0,1)}^{1}$	$R_{(0,1)}^{0}$	$G_{(0,1)}^{7}$	$G_{(0,1)}^{6}$	$G_{(0,1)}^{5}$	$G_{(0,1)}^{4}$	$G_{(0,1)}^{3}$	$G_{(0,1)}^{2}$	$G_{(0,1)}^{1}$	$G_{(0,1)}^{0}$
	—	—	$B_{(0,1)}^{7}$	$B_{(0,1)}^{6}$	$B_{(0,1)}^{5}$	$B_{(0,1)}^{4}$	$B_{(0,1)}^{3}$	$B_{(0,1)}^{2}$	$B_{(0,1)}^{1}$	$B_{(0,1)}^{0}$	$R_{(1,1)}^{7}$	$R_{(1,1)}^{6}$	$R_{(1,1)}^{5}$	$R_{(1,1)}^{4}$	$R_{(1,1)}^{3}$	$R_{(1,1)}^{2}$	$R_{(1,1)}^{1}$	$R_{(1,1)}^{0}$
	—	—	$G_{(1,1)}^{7}$	$G_{(1,1)}^{6}$	$G_{(1,1)}^{5}$	$G_{(1,1)}^{4}$	$G_{(1,1)}^{3}$	$G_{(1,1)}^{2}$	$G_{(1,1)}^{1}$	$G_{(1,1)}^{0}$	$B_{(1,1)}^{7}$	$B_{(1,1)}^{6}$	$B_{(1,1)}^{5}$	$B_{(1,1)}^{4}$	$B_{(1,1)}^{3}$	$B_{(1,1)}^{2}$	$B_{(1,1)}^{1}$	$B_{(1,1)}^{0}$
	...																	

14.5.4 RGB 8:8:8 Format 4

RGB 8:8:8: REG[0400h] bits 2-0 = 010b, Format 4: REG[0400h] bits 6-4 = 011b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-6: RGB 8:8:8 Input Format 4

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	—	—	—	—	—	—	—	—	$R_{(0,0)}^{7}$	$R_{(0,0)}^{6}$	$R_{(0,0)}^{5}$	$R_{(0,0)}^{4}$	$R_{(0,0)}^{3}$	$R_{(0,0)}^{2}$	$R_{(0,0)}^{1}$	$R_{(0,0)}^{0}$
2	—	—	$G_{(0,0)}^{7}$	$G_{(0,0)}^{6}$	$G_{(0,0)}^{5}$	$G_{(0,0)}^{4}$	$G_{(0,0)}^{3}$	$G_{(0,0)}^{2}$	$G_{(0,0)}^{1}$	$G_{(0,0)}^{0}$	$B_{(0,0)}^{7}$	$B_{(0,0)}^{6}$	$B_{(0,0)}^{5}$	$B_{(0,0)}^{4}$	$B_{(0,0)}^{3}$	$B_{(0,0)}^{2}$	$B_{(0,0)}^{1}$	$B_{(0,0)}^{0}$
3	—	—	—	—	—	—	—	—	—	—	$R_{(1,0)}^{7}$	$R_{(1,0)}^{6}$	$R_{(1,0)}^{5}$	$R_{(1,0)}^{4}$	$R_{(1,0)}^{3}$	$R_{(1,0)}^{2}$	$R_{(1,0)}^{1}$	$R_{(1,0)}^{0}$
4			$G_{(1,0)}^{7}$	$G_{(1,0)}^{6}$	$G_{(1,0)}^{5}$	$G_{(1,0)}^{4}$	$G_{(1,0)}^{3}$	$G_{(1,0)}^{2}$	$G_{(1,0)}^{1}$	$G_{(1,0)}^{0}$	$B_{(1,0)}^{7}$	$B_{(1,0)}^{6}$	$B_{(1,0)}^{5}$	$B_{(1,0)}^{4}$	$B_{(1,0)}^{3}$	$B_{(1,0)}^{2}$	$B_{(1,0)}^{1}$	$B_{(1,0)}^{0}$
	...																	
	—	—	—	—	—	—	—	—	—	—	$R_{(0,1)}^{7}$	$R_{(0,1)}^{6}$	$R_{(0,1)}^{5}$	$R_{(0,1)}^{4}$	$R_{(0,1)}^{3}$	$R_{(0,1)}^{2}$	$R_{(0,1)}^{1}$	$R_{(0,1)}^{0}$
	—	—	$G_{(0,1)}^{7}$	$G_{(0,1)}^{6}$	$G_{(0,1)}^{5}$	$G_{(0,1)}^{4}$	$G_{(0,1)}^{3}$	$G_{(0,1)}^{2}$	$G_{(0,1)}^{1}$	$G_{(0,1)}^{0}$	$B_{(0,1)}^{7}$	$B_{(0,1)}^{6}$	$B_{(0,1)}^{5}$	$B_{(0,1)}^{4}$	$B_{(0,1)}^{3}$	$B_{(0,1)}^{2}$	$B_{(0,1)}^{1}$	$B_{(0,1)}^{0}$
	—	—	—	—	—	—	—	—	—	—	$R_{(1,1)}^{7}$	$R_{(1,1)}^{6}$	$R_{(1,1)}^{5}$	$R_{(1,1)}^{4}$	$R_{(1,1)}^{3}$	$R_{(1,1)}^{2}$	$R_{(1,1)}^{1}$	$R_{(1,1)}^{0}$
			$G_{(1,1)}^{7}$	$G_{(1,1)}^{6}$	$G_{(1,1)}^{5}$	$G_{(1,1)}^{4}$	$G_{(1,1)}^{3}$	$G_{(1,1)}^{2}$	$G_{(1,1)}^{1}$	$G_{(1,1)}^{0}$	$B_{(1,1)}^{7}$	$B_{(1,1)}^{6}$	$B_{(1,1)}^{5}$	$B_{(1,1)}^{4}$	$B_{(1,1)}^{3}$	$B_{(1,1)}^{2}$	$B_{(1,1)}^{1}$	$B_{(1,1)}^{0}$
	...																	

14.5.5 RGB 6:6:6 Format 1

RGB 6:6:6: REG[0400h] bits 2-0 = 001b, Format 1: REG[0400h] bits 6-4 = 000b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-7: RGB 6:6:6 Input Format 1

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$G_{(0,0)}^{5}$	$G_{(0,0)}^{4}$	$G_{(0,0)}^{3}$	$G_{(0,0)}^{2}$	$G_{(0,0)}^{1}$	$G_{(0,0)}^{0}$	—	—	$B_{(0,0)}^{5}$	$B_{(0,0)}^{4}$	$B_{(0,0)}^{3}$	$B_{(0,0)}^{2}$	$B_{(0,0)}^{1}$	$B_{(0,0)}^{0}$	—	—
2	—	—	$B_{(1,0)}^{5}$	$B_{(1,0)}^{4}$	$B_{(1,0)}^{3}$	$B_{(1,0)}^{2}$	$B_{(1,0)}^{1}$	$B_{(1,0)}^{0}$	—	—	$R_{(0,0)}^{5}$	$R_{(0,0)}^{4}$	$R_{(0,0)}^{3}$	$R_{(0,0)}^{2}$	$R_{(0,0)}^{1}$	$R_{(0,0)}^{0}$	—	—
3	—	—	$R_{(1,0)}^{5}$	$R_{(1,0)}^{4}$	$R_{(1,0)}^{3}$	$R_{(1,0)}^{2}$	$R_{(1,0)}^{1}$	$R_{(1,0)}^{0}$	—	—	$G_{(1,0)}^{5}$	$G_{(1,0)}^{4}$	$G_{(1,0)}^{3}$	$G_{(1,0)}^{2}$	$G_{(1,0)}^{1}$	$G_{(1,0)}^{0}$	—	—
	...																	
	—	—	$G_{(0,1)}^{5}$	$G_{(0,1)}^{4}$	$G_{(0,1)}^{3}$	$G_{(0,1)}^{2}$	$G_{(0,1)}^{1}$	$G_{(0,1)}^{0}$	—	—	$B_{(0,1)}^{5}$	$B_{(0,1)}^{4}$	$B_{(0,1)}^{3}$	$B_{(0,1)}^{2}$	$B_{(0,1)}^{1}$	$B_{(0,1)}^{0}$	—	—
	—	—	$B_{(1,1)}^{5}$	$B_{(1,1)}^{4}$	$B_{(1,1)}^{3}$	$B_{(1,1)}^{2}$	$B_{(1,1)}^{1}$	$B_{(1,1)}^{0}$	—	—	$R_{(0,1)}^{5}$	$R_{(0,1)}^{4}$	$R_{(0,1)}^{3}$	$R_{(0,1)}^{2}$	$R_{(0,1)}^{1}$	$R_{(0,1)}^{0}$	—	—
	—	—	$R_{(1,1)}^{5}$	$R_{(1,1)}^{4}$	$R_{(1,1)}^{3}$	$R_{(1,1)}^{2}$	$R_{(1,1)}^{1}$	$R_{(1,1)}^{0}$	—	—	$G_{(1,1)}^{5}$	$G_{(1,1)}^{4}$	$G_{(1,1)}^{3}$	$G_{(1,1)}^{2}$	$G_{(1,1)}^{1}$	$G_{(1,1)}^{0}$	—	—
	...																	

14.5.6 RGB 6:6:6 Format 2

RGB 6:6:6: REG[0400h] bits 2-0 = 001b, Format 2: REG[0400h] bits 6-4 = 001b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-8: RGB 6:6:6 Input Format 2

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$B_{(0,0)}^5$	$B_{(0,0)}^4$	$B_{(0,0)}^3$	$B_{(0,0)}^2$	$B_{(0,0)}^1$	$B_{(0,0)}^0$	—	—	—	—	—	—	—	—	—	—
2	—	—	$R_{(0,0)}^5$	$R_{(0,0)}^4$	$R_{(0,0)}^3$	$R_{(0,0)}^2$	$R_{(0,0)}^1$	$R_{(0,0)}^0$	—	—	$G_{(0,0)}^5$	$G_{(0,0)}^4$	$G_{(0,0)}^3$	$G_{(0,0)}^2$	$G_{(0,0)}^1$	$G_{(0,0)}^0$	—	—
3	—	—	$B_{(1,0)}^5$	$B_{(1,0)}^4$	$B_{(1,0)}^3$	$B_{(1,0)}^2$	$B_{(1,0)}^1$	$B_{(1,0)}^0$	—	—	—	—	—	—	—	—	—	—
4			$R_{(1,0)}^5$	$R_{(1,0)}^4$	$R_{(1,0)}^3$	$R_{(1,0)}^2$	$R_{(1,0)}^1$	$R_{(1,0)}^0$			$G_{(1,0)}^5$	$G_{(1,0)}^4$	$G_{(1,0)}^3$	$G_{(1,0)}^2$	$G_{(1,0)}^1$	$G_{(1,0)}^0$		
	...																	
	—	—	$B_{(0,1)}^5$	$B_{(0,1)}^4$	$B_{(0,1)}^3$	$B_{(0,1)}^2$	$B_{(0,1)}^1$	$B_{(0,1)}^0$	—	—	—	—	—	—	—	—	—	—
	—	—	$R_{(0,1)}^5$	$R_{(0,1)}^4$	$R_{(0,1)}^3$	$R_{(0,1)}^2$	$R_{(0,1)}^1$	$R_{(0,1)}^0$	—	—	$G_{(0,1)}^5$	$G_{(0,1)}^4$	$G_{(0,1)}^3$	$G_{(0,1)}^2$	$G_{(0,1)}^1$	$G_{(0,1)}^0$	—	—
	—	—	$B_{(1,1)}^5$	$B_{(1,1)}^4$	$B_{(1,1)}^3$	$B_{(1,1)}^2$	$B_{(1,1)}^1$	$B_{(1,1)}^0$	—	—	—	—	—	—	—	—	—	—
			$R_{(1,1)}^5$	$R_{(1,1)}^4$	$R_{(1,1)}^3$	$R_{(1,1)}^2$	$R_{(1,1)}^1$	$R_{(1,1)}^0$			$G_{(1,1)}^5$	$G_{(1,1)}^4$	$G_{(1,1)}^3$	$G_{(1,1)}^2$	$G_{(1,1)}^1$	$G_{(1,1)}^0$		
	...																	

14.5.7 RGB 6:6:6 Format 3

RGB 6:6:6: REG[0400h] bits 2-0 = 001b, Format 3: REG[0400h] bits 6-4 = 010b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-9: RGB 6:6:6 Input Format 3

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$R_{(0,0)}^5$	$R_{(0,0)}^4$	$R_{(0,0)}^3$	$R_{(0,0)}^2$	$R_{(0,0)}^1$	$R_{(0,0)}^0$	—	—	$G_{(0,0)}^5$	$G_{(0,0)}^4$	$G_{(0,0)}^3$	$G_{(0,0)}^2$	$G_{(0,0)}^1$	$G_{(0,0)}^0$	—	—
2	—	—	$B_{(0,0)}^5$	$B_{(0,0)}^4$	$B_{(0,0)}^3$	$B_{(0,0)}^2$	$B_{(0,0)}^1$	$B_{(0,0)}^0$	—	—	$R_{(1,0)}^5$	$R_{(1,0)}^4$	$R_{(1,0)}^3$	$R_{(1,0)}^2$	$R_{(1,0)}^1$	$R_{(1,0)}^0$	—	—
3	—	—	$G_{(1,0)}^5$	$G_{(1,0)}^4$	$G_{(1,0)}^3$	$G_{(1,0)}^2$	$G_{(1,0)}^1$	$G_{(1,0)}^0$	—	—	$B_{(1,0)}^5$	$B_{(1,0)}^4$	$B_{(1,0)}^3$	$B_{(1,0)}^2$	$B_{(1,0)}^1$	$B_{(1,0)}^0$	—	—
	...																	
	—	—	$R_{(0,1)}^5$	$R_{(0,1)}^4$	$R_{(0,1)}^3$	$R_{(0,1)}^2$	$R_{(0,1)}^1$	$R_{(0,1)}^0$	—	—	$G_{(0,1)}^5$	$G_{(0,1)}^4$	$G_{(0,1)}^3$	$G_{(0,1)}^2$	$G_{(0,1)}^1$	$G_{(0,1)}^0$	—	—
	—	—	$B_{(0,1)}^5$	$B_{(0,1)}^4$	$B_{(0,1)}^3$	$B_{(0,1)}^2$	$B_{(0,1)}^1$	$B_{(0,1)}^0$	—	—	$R_{(1,1)}^5$	$R_{(1,1)}^4$	$R_{(1,1)}^3$	$R_{(1,1)}^2$	$R_{(1,1)}^1$	$R_{(1,1)}^0$	—	—
	—	—	$G_{(1,1)}^5$	$G_{(1,1)}^4$	$G_{(1,1)}^3$	$G_{(1,1)}^2$	$G_{(1,1)}^1$	$G_{(1,1)}^0$	—	—	$B_{(1,1)}^5$	$B_{(1,1)}^4$	$B_{(1,1)}^3$	$B_{(1,1)}^2$	$B_{(1,1)}^1$	$B_{(1,1)}^0$	—	—
	...																	

14.5.8 RGB 6:6:6 Format 4

RGB 6:6:6: REG[0400h] bits 2-0 = 001b, Format 4: REG[0400h] bits 6-4 = 011b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-10: RGB 6:6:6 Input Format 4

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	—	—	—	—	—	—	—	—	$R_{(0,0)}^5$	$R_{(0,0)}^4$	$R_{(0,0)}^3$	$R_{(0,0)}^2$	$R_{(0,0)}^1$	$R_{(0,0)}^0$	—	—
2	—	—	$G_{(0,0)}^5$	$G_{(0,0)}^4$	$G_{(0,0)}^3$	$G_{(0,0)}^2$	$G_{(0,0)}^1$	$G_{(0,0)}^0$	—	—	$B_{(0,0)}^5$	$B_{(0,0)}^4$	$B_{(0,0)}^3$	$B_{(0,0)}^2$	$B_{(0,0)}^1$	$B_{(0,0)}^0$	—	—
3	—	—	—	—	—	—	—	—	—	—	$R_{(1,0)}^5$	$R_{(1,0)}^4$	$R_{(1,0)}^3$	$R_{(1,0)}^2$	$R_{(1,0)}^1$	$R_{(1,0)}^0$	—	—
4			$G_{(1,0)}^5$	$G_{(1,0)}^4$	$G_{(1,0)}^3$	$G_{(1,0)}^2$	$G_{(1,0)}^1$	$G_{(1,0)}^0$			$B_{(1,0)}^5$	$B_{(1,0)}^4$	$B_{(1,0)}^3$	$B_{(1,0)}^2$	$B_{(1,0)}^1$	$B_{(1,0)}^0$		
	...																	
	—	—	—	—	—	—	—	—	—	—	$R_{(0,1)}^5$	$R_{(0,1)}^4$	$R_{(0,1)}^3$	$R_{(0,1)}^2$	$R_{(0,1)}^1$	$R_{(0,1)}^0$	—	—
	—	—	$G_{(0,1)}^5$	$G_{(0,1)}^4$	$G_{(0,1)}^3$	$G_{(0,1)}^2$	$G_{(0,1)}^1$	$G_{(0,1)}^0$	—	—	$B_{(0,1)}^5$	$B_{(0,1)}^4$	$B_{(0,1)}^3$	$B_{(0,1)}^2$	$B_{(0,1)}^1$	$B_{(0,1)}^0$	—	—
	—	—	—	—	—	—	—	—	—	—	$R_{(1,1)}^5$	$R_{(1,1)}^4$	$R_{(1,1)}^3$	$R_{(1,1)}^2$	$R_{(1,1)}^1$	$R_{(1,1)}^0$	—	—
			$G_{(1,1)}^5$	$G_{(1,1)}^4$	$G_{(1,1)}^3$	$G_{(1,1)}^2$	$G_{(1,1)}^1$	$G_{(1,1)}^0$			$B_{(1,1)}^5$	$B_{(1,1)}^4$	$B_{(1,1)}^3$	$B_{(1,1)}^2$	$B_{(1,1)}^1$	$B_{(1,1)}^0$		
	...																	

14.5.9 RGB 6:6:6 Format 5

RGB 6:6:6: REG[0400h] bits 2-0 = 001b, Format 5: REG[0400h] bits 6-4 = 100b.

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-11: RGB 6:6:6 Input Format 5

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	$R_{(0,0)}^5$	$R_{(0,0)}^4$	$R_{(0,0)}^3$	$R_{(0,0)}^2$	$R_{(0,0)}^1$	$R_{(0,0)}^0$	$G_{(0,0)}^5$	$G_{(0,0)}^4$	$G_{(0,0)}^3$	$G_{(0,0)}^2$	$G_{(0,0)}^1$	$G_{(0,0)}^0$	$B_{(0,0)}^5$	$B_{(0,0)}^4$	$B_{(0,0)}^3$	$B_{(0,0)}^2$	$B_{(0,0)}^1$	$B_{(0,0)}^0$
2	$R_{(1,0)}^5$	$R_{(1,0)}^4$	$R_{(1,0)}^3$	$R_{(1,0)}^2$	$R_{(1,0)}^1$	$R_{(1,0)}^0$	$G_{(1,0)}^5$	$G_{(1,0)}^4$	$G_{(1,0)}^3$	$G_{(1,0)}^2$	$G_{(1,0)}^1$	$G_{(1,0)}^0$	$B_{(1,0)}^5$	$B_{(1,0)}^4$	$B_{(1,0)}^3$	$B_{(1,0)}^2$	$B_{(1,0)}^1$	$B_{(1,0)}^0$
3	$R_{(2,0)}^5$	$R_{(2,0)}^4$	$R_{(2,0)}^3$	$R_{(2,0)}^2$	$R_{(2,0)}^1$	$R_{(2,0)}^0$	$G_{(2,0)}^5$	$G_{(2,0)}^4$	$G_{(2,0)}^3$	$G_{(2,0)}^2$	$G_{(2,0)}^1$	$G_{(2,0)}^0$	$B_{(2,0)}^5$	$B_{(2,0)}^4$	$B_{(2,0)}^3$	$B_{(2,0)}^2$	$B_{(2,0)}^1$	$B_{(2,0)}^0$
4	$R_{(3,0)}^5$	$R_{(3,0)}^4$	$R_{(3,0)}^3$	$R_{(3,0)}^2$	$R_{(3,0)}^1$	$R_{(3,0)}^0$	$G_{(3,0)}^5$	$G_{(3,0)}^4$	$G_{(3,0)}^3$	$G_{(3,0)}^2$	$G_{(3,0)}^1$	$G_{(3,0)}^0$	$B_{(3,0)}^5$	$B_{(3,0)}^4$	$B_{(3,0)}^3$	$B_{(3,0)}^2$	$B_{(3,0)}^1$	$B_{(3,0)}^0$
	...																	
	$R_{(0,1)}^5$	$R_{(0,1)}^4$	$R_{(0,1)}^3$	$R_{(0,1)}^2$	$R_{(0,1)}^1$	$R_{(0,1)}^0$	$G_{(0,1)}^5$	$G_{(0,1)}^4$	$G_{(0,1)}^3$	$G_{(0,1)}^2$	$G_{(0,1)}^1$	$G_{(0,1)}^0$	$B_{(0,1)}^5$	$B_{(0,1)}^4$	$B_{(0,1)}^3$	$B_{(0,1)}^2$	$B_{(0,1)}^1$	$B_{(0,1)}^0$
	$R_{(1,1)}^5$	$R_{(1,1)}^4$	$R_{(1,1)}^3$	$R_{(1,1)}^2$	$R_{(1,1)}^1$	$R_{(1,1)}^0$	$G_{(1,1)}^5$	$G_{(1,1)}^4$	$G_{(1,1)}^3$	$G_{(1,1)}^2$	$G_{(1,1)}^1$	$G_{(1,1)}^0$	$B_{(1,1)}^5$	$B_{(1,1)}^4$	$B_{(1,1)}^3$	$B_{(1,1)}^2$	$B_{(1,1)}^1$	$B_{(1,1)}^0$
	$R_{(2,1)}^5$	$R_{(2,1)}^4$	$R_{(2,1)}^3$	$R_{(2,1)}^2$	$R_{(2,1)}^1$	$R_{(2,1)}^0$	$G_{(2,1)}^5$	$G_{(2,1)}^4$	$G_{(2,1)}^3$	$G_{(2,1)}^2$	$G_{(2,1)}^1$	$G_{(2,1)}^0$	$B_{(2,1)}^5$	$B_{(2,1)}^4$	$B_{(2,1)}^3$	$B_{(2,1)}^2$	$B_{(2,1)}^1$	$B_{(2,1)}^0$
	$R_{(3,1)}^5$	$R_{(3,1)}^4$	$R_{(3,1)}^3$	$R_{(3,1)}^2$	$R_{(3,1)}^1$	$R_{(3,1)}^0$	$G_{(3,1)}^5$	$G_{(3,1)}^4$	$G_{(3,1)}^3$	$G_{(3,1)}^2$	$G_{(3,1)}^1$	$G_{(3,1)}^0$	$B_{(3,1)}^5$	$B_{(3,1)}^4$	$B_{(3,1)}^3$	$B_{(3,1)}^2$	$B_{(3,1)}^1$	$B_{(3,1)}^0$
	...																	

14.5.10 RGB 6:6:6 to RGB 8:8:8 Conversion

RGB 6:6:6 input data is expanded to RGB 8:8:8 before it is stored in memory. The following conversion method is used.

Table 14-12: RGB 6:6:6 to RGB 8:8:8 Conversion

RGB 6:6:6 (Input)							RGB 8:8:8 (Memory)							
R5	R4	R3	R2	R1	R0	→	R5	R4	R3	R2	R1	R0	R5	R4
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B5	B4	B3	B2	B1	B0	→	B5	B4	B3	B2	B1	B0	B5	B4

14.5.11 RGB 5:6:5

RGB 5:6:5: REG[0400h] bits 2-0 = 000b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-13: RGB 5:6:5 Input Format

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$R_{(0,0)}^4$	$R_{(0,0)}^3$	$R_{(0,0)}^2$	$R_{(0,0)}^1$	$R_{(0,0)}^0$	$G_{(0,0)}^5$	$G_{(0,0)}^4$	$G_{(0,0)}^3$	$G_{(0,0)}^2$	$G_{(0,0)}^1$	$G_{(0,0)}^0$	$B_{(0,0)}^4$	$B_{(0,0)}^3$	$B_{(0,0)}^2$	$B_{(0,0)}^1$	$B_{(0,0)}^0$
2	—	—	$R_{(1,0)}^4$	$R_{(1,0)}^3$	$R_{(1,0)}^2$	$R_{(1,0)}^1$	$R_{(1,0)}^0$	$G_{(1,0)}^5$	$G_{(1,0)}^4$	$G_{(1,0)}^3$	$G_{(1,0)}^2$	$G_{(1,0)}^1$	$G_{(1,0)}^0$	$B_{(1,0)}^4$	$B_{(1,0)}^3$	$B_{(1,0)}^2$	$B_{(1,0)}^1$	$B_{(1,0)}^0$
3	—	—	$R_{(2,0)}^4$	$R_{(2,0)}^3$	$R_{(2,0)}^2$	$R_{(2,0)}^1$	$R_{(2,0)}^0$	$G_{(2,0)}^5$	$G_{(2,0)}^4$	$G_{(2,0)}^3$	$G_{(2,0)}^2$	$G_{(2,0)}^1$	$G_{(2,0)}^0$	$B_{(2,0)}^4$	$B_{(2,0)}^3$	$B_{(2,0)}^2$	$B_{(2,0)}^1$	$B_{(2,0)}^0$
4			$R_{(3,0)}^4$	$R_{(3,0)}^3$	$R_{(3,0)}^2$	$R_{(3,0)}^1$	$R_{(3,0)}^0$	$G_{(3,0)}^5$	$G_{(3,0)}^4$	$G_{(3,0)}^3$	$G_{(3,0)}^2$	$G_{(3,0)}^1$	$G_{(3,0)}^0$	$B_{(3,0)}^4$	$B_{(3,0)}^3$	$B_{(3,0)}^2$	$B_{(3,0)}^1$	$B_{(3,0)}^0$
	...																	
	—	—	$R_{(0,1)}^4$	$R_{(0,1)}^3$	$R_{(0,1)}^2$	$R_{(0,1)}^1$	$R_{(0,1)}^0$	$G_{(0,1)}^5$	$G_{(0,1)}^4$	$G_{(0,1)}^3$	$G_{(0,1)}^2$	$G_{(0,1)}^1$	$G_{(0,1)}^0$	$B_{(0,1)}^4$	$B_{(0,1)}^3$	$B_{(0,1)}^2$	$B_{(0,1)}^1$	$B_{(0,1)}^0$
	—	—	$R_{(1,1)}^4$	$R_{(1,1)}^3$	$R_{(1,1)}^2$	$R_{(1,1)}^1$	$R_{(1,1)}^0$	$G_{(1,1)}^5$	$G_{(1,1)}^4$	$G_{(1,1)}^3$	$G_{(1,1)}^2$	$G_{(1,1)}^1$	$G_{(1,1)}^0$	$B_{(1,1)}^4$	$B_{(1,1)}^3$	$B_{(1,1)}^2$	$B_{(1,1)}^1$	$B_{(1,1)}^0$
	—	—	$R_{(2,1)}^4$	$R_{(2,1)}^3$	$R_{(2,1)}^2$	$R_{(2,1)}^1$	$R_{(2,1)}^0$	$G_{(2,1)}^5$	$G_{(2,1)}^4$	$G_{(2,1)}^3$	$G_{(2,1)}^2$	$G_{(2,1)}^1$	$G_{(2,1)}^0$	$B_{(2,1)}^4$	$B_{(2,1)}^3$	$B_{(2,1)}^2$	$B_{(2,1)}^1$	$B_{(2,1)}^0$
			$R_{(3,1)}^4$	$R_{(3,1)}^3$	$R_{(3,1)}^2$	$R_{(3,1)}^1$	$R_{(3,1)}^0$	$G_{(3,1)}^5$	$G_{(3,1)}^4$	$G_{(3,1)}^3$	$G_{(3,1)}^2$	$G_{(3,1)}^1$	$G_{(3,1)}^0$	$B_{(3,1)}^4$	$B_{(3,1)}^3$	$B_{(3,1)}^2$	$B_{(3,1)}^1$	$B_{(3,1)}^0$
	...																	

14.5.12 YUV 4:2:2 Format 1

YUV 4:2:2: REG[0400h] bits 2-0 = 100b, Format 1: REG[0400h] bits 6-4 = 000b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-14: YUV 4:2:2 Input Format 1

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$Y_{(0,0)}^{7}$	$Y_{(0,0)}^{6}$	$Y_{(0,0)}^{5}$	$Y_{(0,0)}^{4}$	$Y_{(0,0)}^{3}$	$Y_{(0,0)}^{2}$	$Y_{(0,0)}^{1}$	$Y_{(0,0)}^{0}$	$U_{(0,0)}^{7}$	$U_{(0,0)}^{6}$	$U_{(0,0)}^{5}$	$U_{(0,0)}^{4}$	$U_{(0,0)}^{3}$	$U_{(0,0)}^{2}$	$U_{(0,0)}^{1}$	$U_{(0,0)}^{0}$
2	—	—	$Y_{(1,0)}^{7}$	$Y_{(1,0)}^{6}$	$Y_{(1,0)}^{5}$	$Y_{(1,0)}^{4}$	$Y_{(1,0)}^{3}$	$Y_{(1,0)}^{2}$	$Y_{(1,0)}^{1}$	$Y_{(1,0)}^{0}$	$V_{(0,0)}^{7}$	$V_{(0,0)}^{6}$	$V_{(0,0)}^{5}$	$V_{(0,0)}^{4}$	$V_{(0,0)}^{3}$	$V_{(0,0)}^{2}$	$V_{(0,0)}^{1}$	$V_{(0,0)}^{0}$
3	—	—	$Y_{(2,0)}^{7}$	$Y_{(2,0)}^{6}$	$Y_{(2,0)}^{5}$	$Y_{(2,0)}^{4}$	$Y_{(2,0)}^{3}$	$Y_{(2,0)}^{2}$	$Y_{(2,0)}^{1}$	$Y_{(2,0)}^{0}$	$U_{(2,0)}^{7}$	$U_{(2,0)}^{6}$	$U_{(2,0)}^{5}$	$U_{(2,0)}^{4}$	$U_{(2,0)}^{3}$	$U_{(2,0)}^{2}$	$U_{(2,0)}^{1}$	$U_{(2,0)}^{0}$
4			$Y_{(3,0)}^{7}$	$Y_{(3,0)}^{6}$	$Y_{(3,0)}^{5}$	$Y_{(3,0)}^{4}$	$Y_{(3,0)}^{3}$	$Y_{(3,0)}^{2}$	$Y_{(3,0)}^{1}$	$Y_{(3,0)}^{0}$	$V_{(2,0)}^{7}$	$V_{(2,0)}^{6}$	$V_{(2,0)}^{5}$	$V_{(2,0)}^{4}$	$V_{(2,0)}^{3}$	$V_{(2,0)}^{2}$	$V_{(2,0)}^{1}$	$V_{(2,0)}^{0}$
	...																	
	—	—	$Y_{(0,1)}^{7}$	$Y_{(0,1)}^{6}$	$Y_{(0,1)}^{5}$	$Y_{(0,1)}^{4}$	$Y_{(0,1)}^{3}$	$Y_{(0,1)}^{2}$	$Y_{(0,1)}^{1}$	$Y_{(0,1)}^{0}$	$U_{(0,1)}^{7}$	$U_{(0,1)}^{6}$	$U_{(0,1)}^{5}$	$U_{(0,1)}^{4}$	$U_{(0,1)}^{3}$	$U_{(0,1)}^{2}$	$U_{(0,1)}^{1}$	$U_{(0,1)}^{0}$
	—	—	$Y_{(1,1)}^{7}$	$Y_{(1,1)}^{6}$	$Y_{(1,1)}^{5}$	$Y_{(1,1)}^{4}$	$Y_{(1,1)}^{3}$	$Y_{(1,1)}^{2}$	$Y_{(1,1)}^{1}$	$Y_{(1,1)}^{0}$	$V_{(0,1)}^{7}$	$V_{(0,1)}^{6}$	$V_{(0,1)}^{5}$	$V_{(0,1)}^{4}$	$V_{(0,1)}^{3}$	$V_{(0,1)}^{2}$	$V_{(0,1)}^{1}$	$V_{(0,1)}^{0}$
	—	—	$Y_{(2,1)}^{7}$	$Y_{(2,1}^{6}$	$Y_{(2,1)}^{5}$	$Y_{(2,1)}^{4}$	$Y_{(2,1)}^{3}$	$Y_{(2,1)}^{2}$	$Y_{(2,1)}^{1}$	$Y_{(2,1)}^{0}$	$U_{(2,1)}^{7}$	$U_{(2,1)}^{6}$	$U_{(2,1)}^{5}$	$U_{(2,1)}^{4}$	$U_{(2,1)}^{3}$	$U_{(2,1)}^{2}$	$U_{(2,1)}^{1}$	$U_{(2,1)}^{0}$
			$Y_{(3,1)}^{7}$	$Y_{(3,1)}^{6}$	$Y_{(3,1)}^{5}$	$Y_{(3,1)}^{4}$	$Y_{(3,1)}^{3}$	$Y_{(3,1)}^{2}$	$Y_{(3,1)}^{1}$	$Y_{(3,1)}^{0}$	$V_{(2,1)}^{7}$	$V_{(2,1)}^{6}$	$V_{(2,1)}^{5}$	$V_{(2,1)}^{4}$	$V_{(2,1)}^{3}$	$V_{(2,1)}^{2}$	$V_{(2,1)}^{1}$	$V_{(2,1)}^{0}$
	...																	

14.5.13 YUV 4:2:2 Format 2

YUV 4:2:2: REG[0400h] bits 2-0 = 100b, Format 2: REG[0400h] bits 6-4 = 001b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-15: YUV 4:2:2 Input Format 2

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$U_{(0,0)}^{7}$	$U_{(0,0)}^{6}$	$U_{(0,0)}^{5}$	$U_{(0,0)}^{4}$	$U_{(0,0)}^{3}$	$U_{(0,0)}^{2}$	$U_{(0,0)}^{1}$	$U_{(0,0)}^{0}$	$Y_{(0,0)}^{7}$	$Y_{(0,0)}^{6}$	$Y_{(0,0)}^{5}$	$Y_{(0,0)}^{4}$	$Y_{(0,0)}^{3}$	$Y_{(0,0)}^{2}$	$Y_{(0,0)}^{1}$	$Y_{(0,0)}^{0}$
2	—	—	$V_{(0,0)}^{7}$	$V_{(0,0)}^{6}$	$V_{(0,0)}^{5}$	$V_{(0,0)}^{4}$	$V_{(0,0)}^{3}$	$V_{(0,0)}^{2}$	$V_{(0,0)}^{1}$	$V_{(0,0)}^{0}$	$Y_{(1,0)}^{7}$	$Y_{(1,0)}^{6}$	$Y_{(1,0)}^{5}$	$Y_{(1,0)}^{4}$	$Y_{(1,0)}^{3}$	$Y_{(1,0)}^{2}$	$Y_{(1,0)}^{1}$	$Y_{(1,0)}^{0}$
3	—	—	$U_{(2,0)}^{7}$	$U_{(2,0)}^{6}$	$U_{(2,0)}^{5}$	$U_{(2,0)}^{4}$	$U_{(2,0)}^{3}$	$U_{(2,0)}^{2}$	$U_{(2,0)}^{1}$	$U_{(2,0)}^{0}$	$Y_{(2,0)}^{7}$	$Y_{(2,0)}^{6}$	$Y_{(2,0)}^{5}$	$Y_{(2,0)}^{4}$	$Y_{(2,0)}^{3}$	$Y_{(2,0)}^{2}$	$Y_{(2,0)}^{1}$	$Y_{(2,0)}^{0}$
4			$V_{(2,0)}^{7}$	$V_{(2,0)}^{6}$	$V_{(2,0)}^{5}$	$V_{(2,0)}^{4}$	$V_{(2,0)}^{3}$	$V_{(2,0)}^{2}$	$V_{(2,0)}^{1}$	$V_{(2,0)}^{0}$	$Y_{(3,0)}^{7}$	$Y_{(3,0)}^{6}$	$Y_{(3,0)}^{5}$	$Y_{(3,0)}^{4}$	$Y_{(3,0)}^{3}$	$Y_{(3,0)}^{2}$	$Y_{(3,0)}^{1}$	$Y_{(3,0)}^{0}$
	...																	
	—	—	$U_{(0,1)}^{7}$	$U_{(0,1)}^{6}$	$U_{(0,1)}^{5}$	$U_{(0,1)}^{4}$	$U_{(0,1)}^{3}$	$U_{(0,1)}^{2}$	$U_{(0,1)}^{1}$	$U_{(0,1)}^{0}$	$Y_{(0,1)}^{7}$	$Y_{(0,1)}^{6}$	$Y_{(0,1)}^{5}$	$Y_{(0,1)}^{4}$	$Y_{(0,1)}^{3}$	$Y_{(0,1)}^{2}$	$Y_{(0,1)}^{1}$	$Y_{(0,1)}^{0}$
	—	—	$V_{(0,1)}^{7}$	$V_{(0,1)}^{6}$	$V_{(0,1)}^{5}$	$V_{(0,1)}^{4}$	$V_{(0,1)}^{3}$	$V_{(0,1)}^{2}$	$V_{(0,1)}^{1}$	$V_{(0,1)}^{0}$	$Y_{(1,1)}^{7}$	$Y_{(1,1)}^{6}$	$Y_{(1,1)}^{5}$	$Y_{(1,1)}^{4}$	$Y_{(1,1)}^{3}$	$Y_{(1,1)}^{2}$	$Y_{(1,1)}^{1}$	$Y_{(1,1)}^{0}$
	—	—	$U_{(2,1)}^{7}$	$U_{(2,1)}^{6}$	$U_{(2,1)}^{5}$	$U_{(2,1)}^{4}$	$U_{(2,1)}^{3}$	$U_{(2,1)}^{2}$	$U_{(2,1)}^{1}$	$U_{(2,1)}^{0}$	$Y_{(2,1)}^{7}$	$Y_{(2,1}^{6}$	$Y_{(2,1)}^{5}$	$Y_{(2,1)}^{4}$	$Y_{(2,1)}^{3}$	$Y_{(2,1)}^{2}$	$Y_{(2,1)}^{1}$	$Y_{(2,1)}^{0}$
			$V_{(2,1)}^{7}$	$V_{(2,1)}^{6}$	$V_{(2,1)}^{5}$	$V_{(2,1)}^{4}$	$V_{(2,1)}^{3}$	$V_{(2,1)}^{2}$	$V_{(2,1)}^{1}$	$V_{(2,1)}^{0}$	$Y_{(3,1)}^{7}$	$Y_{(3,1)}^{6}$	$Y_{(3,1)}^{5}$	$Y_{(3,1)}^{4}$	$Y_{(3,1)}^{3}$	$Y_{(3,1)}^{2}$	$Y_{(3,1)}^{1}$	$Y_{(3,1)}^{0}$
	...																	

14.5.14 YUV 4:2:0 Format 1

YUV 4:2:0: REG[0400h] bits 2-0 = 110b, Format 1: REG[0400h] bits 6-4 = 000b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-16: YUV 4:2:0 Input Format 1

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$Y_{(0,0)}{}^{7}$	$Y_{(0,0)}{}^{6}$	$Y_{(0,0)}{}^{5}$	$Y_{(0,0)}{}^{4}$	$Y_{(0,0)}{}^{3}$	$Y_{(0,0)}{}^{2}$	$Y_{(0,0)}{}^{1}$	$Y_{(0,0)}{}^{0}$	$U_{(0,0)}{}^{7}$	$U_{(0,0)}{}^{6}$	$U_{(0,0)}{}^{5}$	$U_{(0,0)}{}^{4}$	$U_{(0,0)}{}^{3}$	$U_{(0,0)}{}^{2}$	$U_{(0,0)}{}^{1}$	$U_{(0,0)}{}^{0}$
2	—	—	$Y_{(1,0)}{}^{7}$	$Y_{(1,0)}{}^{6}$	$Y_{(1,0)}{}^{5}$	$Y_{(1,0)}{}^{4}$	$Y_{(1,0)}{}^{3}$	$Y_{(1,0)}{}^{2}$	$Y_{(1,0)}{}^{1}$	$Y_{(1,0)}{}^{0}$	$V_{(0,0)}{}^{7}$	$V_{(0,0)}{}^{6}$	$V_{(0,0)}{}^{5}$	$V_{(0,0)}{}^{4}$	$V_{(0,0)}{}^{3}$	$V_{(0,0)}{}^{2}$	$V_{(0,0)}{}^{1}$	$V_{(0,0)}{}^{0}$
3	—	—	$Y_{(2,0)}{}^{7}$	$Y_{(2,0)}{}^{6}$	$Y_{(2,0)}{}^{5}$	$Y_{(2,0)}{}^{4}$	$Y_{(2,0)}{}^{3}$	$Y_{(2,0)}{}^{2}$	$Y_{(2,0)}{}^{1}$	$Y_{(2,0)}{}^{0}$	$U_{(2,0)}{}^{7}$	$U_{(2,0)}{}^{6}$	$U_{(2,0)}{}^{5}$	$U_{(2,0)}{}^{4}$	$U_{(2,0)}{}^{3}$	$U_{(2,0)}{}^{2}$	$U_{(2,0)}{}^{1}$	$U_{(2,0)}{}^{0}$
4			$Y_{(3,0)}{}^{7}$	$Y_{(3,0)}{}^{6}$	$Y_{(3,0)}{}^{5}$	$Y_{(3,0)}{}^{4}$	$Y_{(3,0)}{}^{3}$	$Y_{(3,0)}{}^{2}$	$Y_{(3,0)}{}^{1}$	$Y_{(3,0)}{}^{0}$	$V_{(2,0)}{}^{7}$	$V_{(2,0)}{}^{6}$	$V_{(2,0)}{}^{5}$	$V_{(2,0)}{}^{4}$	$V_{(2,0)}{}^{3}$	$V_{(2,0)}{}^{2}$	$V_{(2,0)}{}^{1}$	$V_{(2,0)}{}^{0}$
	...																	
	—	—	$Y_{(1,1)}{}^{7}$	$Y_{(1,1)}{}^{6}$	$Y_{(1,1)}{}^{5}$	$Y_{(1,1)}{}^{4}$	$Y_{(1,1)}{}^{3}$	$Y_{(1,1)}{}^{2}$	$Y_{(1,1)}{}^{1}$	$Y_{(1,1)}{}^{0}$	$Y_{(0,1)}{}^{7}$	$Y_{(0,1)}{}^{6}$	$Y_{(0,1)}{}^{5}$	$Y_{(0,1)}{}^{4}$	$Y_{(0,1)}{}^{3}$	$Y_{(0,1)}{}^{2}$	$Y_{(0,1)}{}^{1}$	$Y_{(0,1)}{}^{0}$
	—	—	$Y_{(3,1)}{}^{7}$	$Y_{(3,1)}{}^{6}$	$Y_{(3,1)}{}^{5}$	$Y_{(3,1)}{}^{4}$	$Y_{(3,1)}{}^{3}$	$Y_{(3,1)}{}^{2}$	$Y_{(3,1)}{}^{1}$	$Y_{(3,1)}{}^{0}$	$Y_{(2,1)}{}^{7}$	$Y_{(2,1)}{}^{6}$	$Y_{(2,1)}{}^{5}$	$Y_{(2,1)}{}^{4}$	$Y_{(2,1)}{}^{3}$	$Y_{(2,1)}{}^{2}$	$Y_{(2,1)}{}^{1}$	$Y_{(2,1)}{}^{0}$
	...																	

14.5.15 YUV 4:2:0 Format 2

YUV 4:2:0: REG[0400h] bits 2-0 = 110b, Format 2: REG[0400h] bits 6-4 = 001b

Pixel (0,0)	Pixel (1,0)	Pixel (2,0)	Pixel (3,0)	...
Pixel (0,1)	Pixel (1,1)	Pixel (2,1)	Pixel (3,1)	...
Pixel (0,2)	Pixel (1,2)	Pixel (2,2)	Pixel (3,2)	...
Pixel (0,3)	Pixel (1,3)	Pixel (2,3)	Pixel (3,3)	...
...	...	...	...	...

Table 14-17: YUV 4:2:0 Input Format 2

	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	—	—	$U_{(0,0)}{}^{7}$	$U_{(0,0)}{}^{6}$	$U_{(0,0)}{}^{5}$	$U_{(0,0)}{}^{4}$	$U_{(0,0)}{}^{3}$	$U_{(0,0)}{}^{2}$	$U_{(0,0)}{}^{1}$	$U_{(0,0)}{}^{0}$	$Y_{(0,0)}{}^{7}$	$Y_{(0,0)}{}^{6}$	$Y_{(0,0)}{}^{5}$	$Y_{(0,0)}{}^{4}$	$Y_{(0,0)}{}^{3}$	$Y_{(0,0)}{}^{2}$	$Y_{(0,0)}{}^{1}$	$Y_{(0,0)}{}^{0}$
2	—	—	$V_{(0,0)}{}^{7}$	$V_{(0,0)}{}^{6}$	$V_{(0,0)}{}^{5}$	$V_{(0,0)}{}^{4}$	$V_{(0,0)}{}^{3}$	$V_{(0,0)}{}^{2}$	$V_{(0,0)}{}^{1}$	$V_{(0,0)}{}^{0}$	$Y_{(1,0)}{}^{7}$	$Y_{(1,0)}{}^{6}$	$Y_{(1,0)}{}^{5}$	$Y_{(1,0)}{}^{4}$	$Y_{(1,0)}{}^{3}$	$Y_{(1,0)}{}^{2}$	$Y_{(1,0)}{}^{1}$	$Y_{(1,0)}{}^{0}$
3	—	—	$U_{(2,0)}{}^{7}$	$U_{(2,0)}{}^{6}$	$U_{(2,0)}{}^{5}$	$U_{(2,0)}{}^{4}$	$U_{(2,0)}{}^{3}$	$U_{(2,0)}{}^{2}$	$U_{(2,0)}{}^{1}$	$U_{(2,0)}{}^{0}$	$Y_{(2,0)}{}^{7}$	$Y_{(2,0)}{}^{6}$	$Y_{(2,0)}{}^{5}$	$Y_{(2,0)}{}^{4}$	$Y_{(2,0)}{}^{3}$	$Y_{(2,0)}{}^{2}$	$Y_{(2,0)}{}^{1}$	$Y_{(2,0)}{}^{0}$
4			$V_{(2,0)}{}^{7}$	$V_{(2,0)}{}^{6}$	$V_{(2,0)}{}^{5}$	$V_{(2,0)}{}^{4}$	$V_{(2,0)}{}^{3}$	$V_{(2,0)}{}^{2}$	$V_{(2,0)}{}^{1}$	$V_{(2,0)}{}^{0}$	$Y_{(3,0)}{}^{7}$	$Y_{(3,0)}{}^{6}$	$Y_{(3,0)}{}^{5}$	$Y_{(3,0)}{}^{4}$	$Y_{(3,0)}{}^{3}$	$Y_{(3,0)}{}^{2}$	$Y_{(3,0)}{}^{1}$	$Y_{(3,0)}{}^{0}$
	...																	
	—	—	$Y_{(0,1)}{}^{7}$	$Y_{(0,1)}{}^{6}$	$Y_{(0,1)}{}^{5}$	$Y_{(0,1)}{}^{4}$	$Y_{(0,1)}{}^{3}$	$Y_{(0,1)}{}^{2}$	$Y_{(0,1)}{}^{1}$	$Y_{(0,1)}{}^{0}$	$Y_{(1,1)}{}^{7}$	$Y_{(1,1)}{}^{6}$	$Y_{(1,1)}{}^{5}$	$Y_{(1,1)}{}^{4}$	$Y_{(1,1)}{}^{3}$	$Y_{(1,1)}{}^{2}$	$Y_{(1,1)}{}^{1}$	$Y_{(1,1)}{}^{0}$
	—	—	$Y_{(2,1)}{}^{7}$	$Y_{(2,1)}{}^{6}$	$Y_{(2,1)}{}^{5}$	$Y_{(2,1)}{}^{4}$	$Y_{(2,1)}{}^{3}$	$Y_{(2,1)}{}^{2}$	$Y_{(2,1)}{}^{1}$	$Y_{(2,1)}{}^{0}$	$Y_{(3,1)}{}^{7}$	$Y_{(3,1)}{}^{6}$	$Y_{(3,1)}{}^{5}$	$Y_{(3,1)}{}^{4}$	$Y_{(3,1)}{}^{3}$	$Y_{(3,1)}{}^{2}$	$Y_{(3,1)}{}^{1}$	$Y_{(3,1)}{}^{0}$
	...																	

15 LCD and TV Interface

15.1 Overview

The S1D13774 supports up to two panels and can provide TV-Out signals for processing via an external NTSC/PAL encoder. The LCD interface supports RGB, serial (RAM integrated), and parallel (RAM integrated) interface panels.

The S1D13774 supports three possible combinations of panel interfaces. All modes have a RGB interface panel as LCD1. LCD2 can be configured for either a serial interface, a parallel interface that shares the data bus pins with LCD1, or a parallel interface with data bus pins different than LCD1. This setting is configured using the LCD Panel Interface Select bits, REG[0104h] bits 1-0. The following table summarizes the possible panel interface configurations.

Table 15-1: Panel Interface Modes

REG[0104h] bits 1-0	Mode	LCD1	LCD2
00b	Mode 1	RGB Interface panel with Serial Command Interface	Serial Interface (RAM Integrated)
01b	Mode 2		Parallel Interface (RAM Integrated) where the LCD1 data bus and LCD2 data bus use the same pins
10b	Mode 3		Parallel Interface (RAM Integrated) where the LCD1 data bus and LCD2 data bus use different pins

For each panel interface mode, the image data in memory can be displayed on LCD1, LCD2, or sent to an external NTSC/PAL encoder using TV-Out. Additionally, the S1D13774 can display on LCD1 and a TV simultaneously by showing the Main window on LCD1 and sending the PIP1/PIP2 image data to an external NTSC/PAL encoder. Note that for simultaneous display there are some limitations due to the fact that not all windows are sent to the same display output port. The following table summarizes the display output port combinations.

Table 15-2: Display Output Port Combinations

	LCD1	LCD2	TV-Out
LCD1 Active	Main/PIP1/PIP2 Window, Transparency, Alpha Blend, LUT/Dither	Off	Off
LCD2 Active	Off	Main/PIP1/PIP2 Window, Transparency, Alpha Blend, LUT/Dither	Off
TV-Out Active	Off	Off	Main/PIP1/PIP2 Window, Transparency, Blend, LUT/Dither
LCD1 & TV-Out Active	Main Window	Off	PIP1/PIP2 Window, Transparency, Alpha Blend, LUT/Dither

Note

Programming for the LCD or TV-Out interfaces requires the contents of the LCD/TV-Out registers to updated according to a specific sequence. Example programming flows which show when the registers should be updated are available in Section 13, “Register Updates” on page 340.

In each mode, the Host interface can access the LCDs and NTSC/PAL encoder (TV-Out) directly. This is done using command accesses through the S1D13774 registers. These accesses to the LCDs and NTSC/PAL encoder by the Host interface can be used at any time as long as the display interface used doesn't forward it.

15.2 Display Modes

The following figures show the display paths for each panel interface mode (see REG[0104h] bits 1-0). For each panel interface mode, there are several possible display output port options (see REG[0604h] bits 11-8). For more information on displaying image data from memory, see Section 12, "Displaying Image Data from Memory" on page 293.

15.2.1 Mode 1

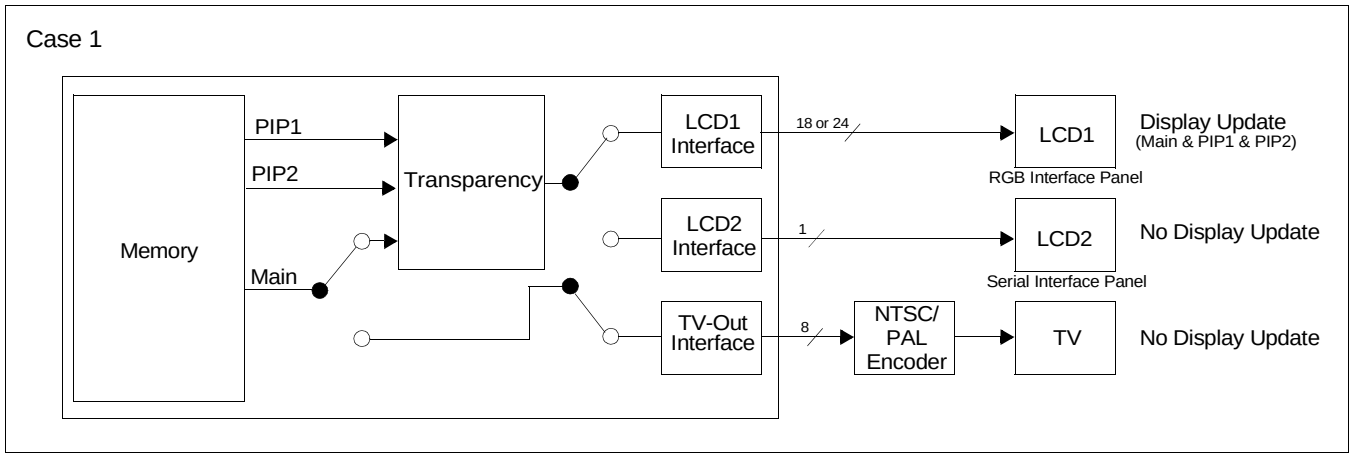


Figure 15-1: Mode 1, Case 1 - LCD1 Active (Main & PIP1 & PIP2)

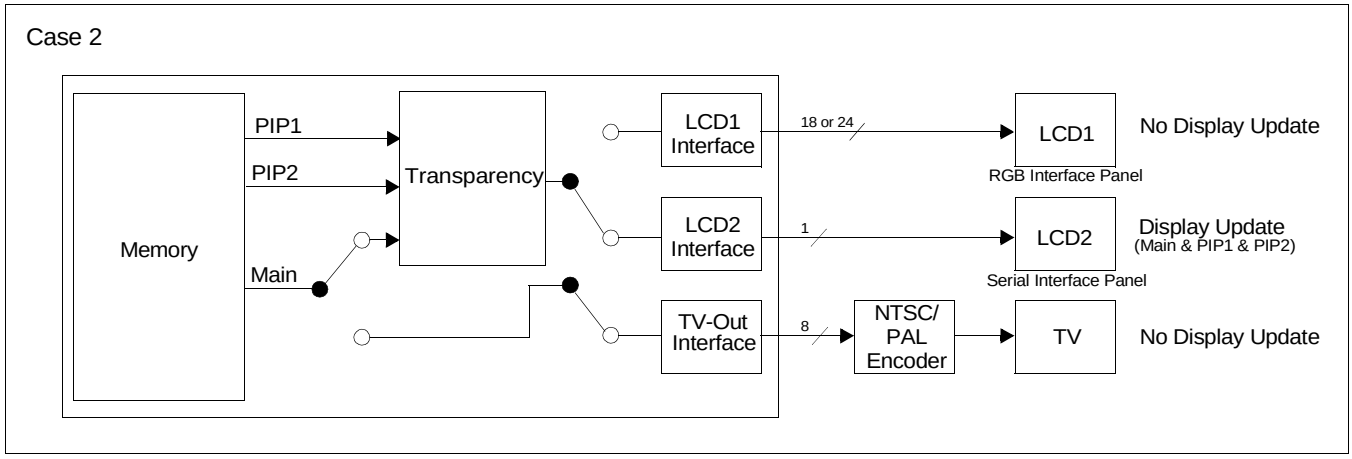


Figure 15-2: Mode 1, Case 2 - LCD2 Active (Main & PIP1 & PIP2)

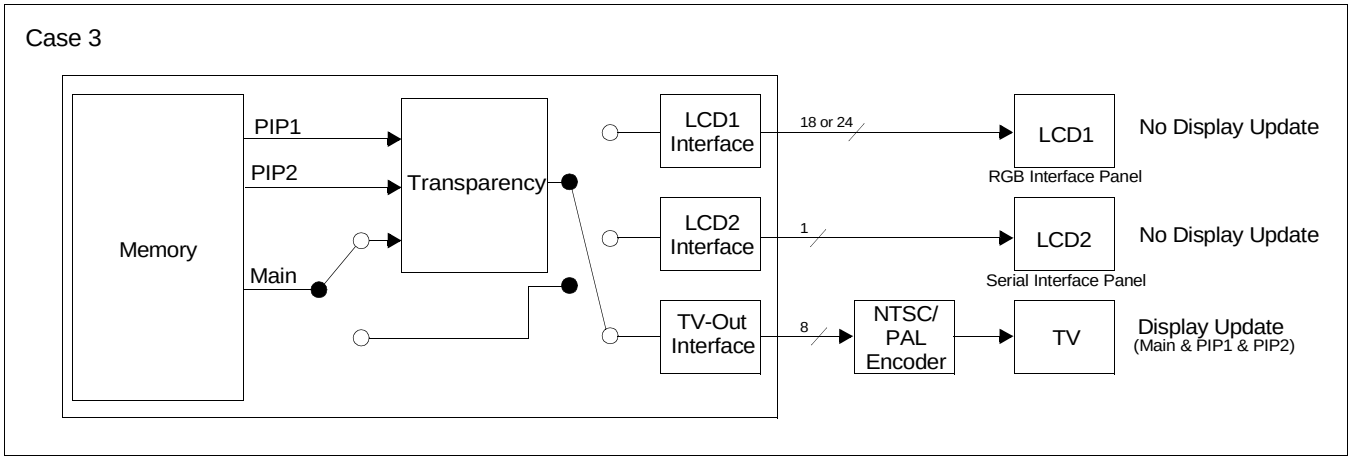


Figure 15-3: Mode 1, Case 3 - TV Active (Main & PIP1 & PIP2)

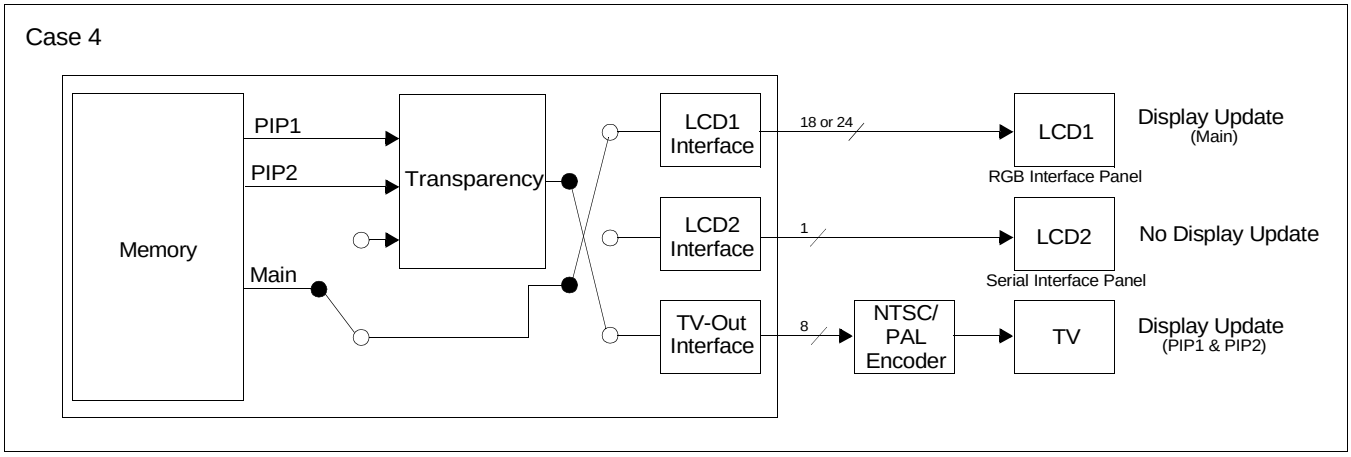


Figure 15-4: Mode 1, Case 4 - LCD1 Active (Main) and TV Active (PIP1 & PIP2)

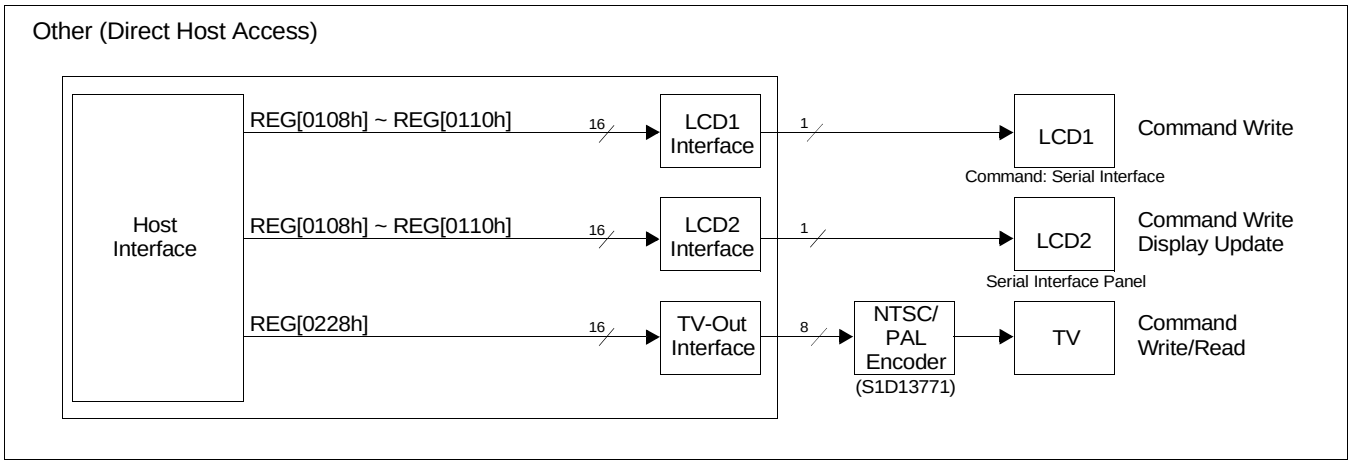


Figure 15-5: Mode 1, Direct Host Access - LCD2 Active

15.2.2 Mode 2

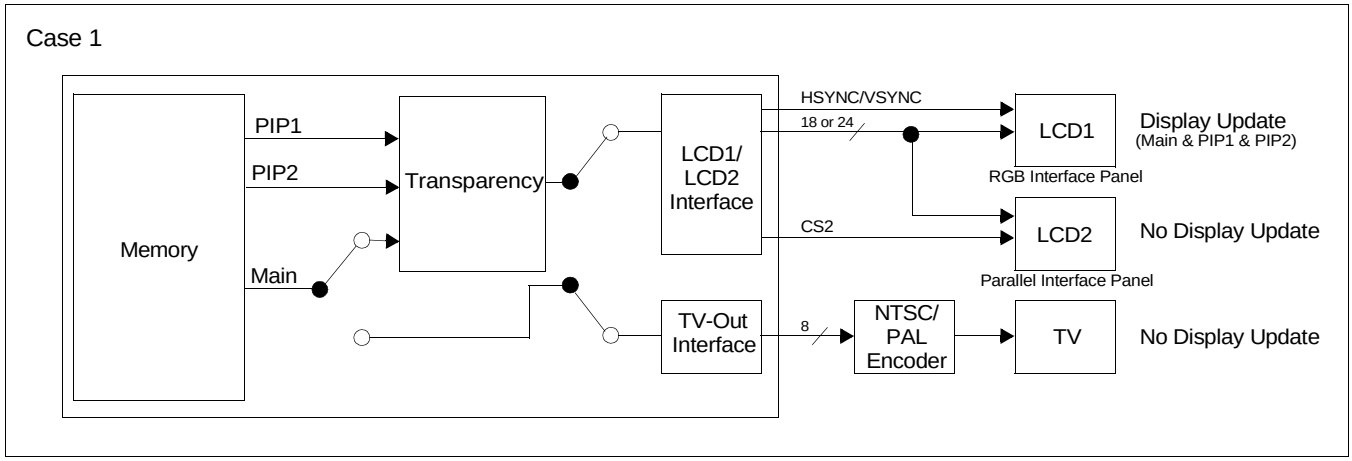


Figure 15-6: Mode 2, Case 1 - LCD1 Active (Main & PIP1 & PIP2)

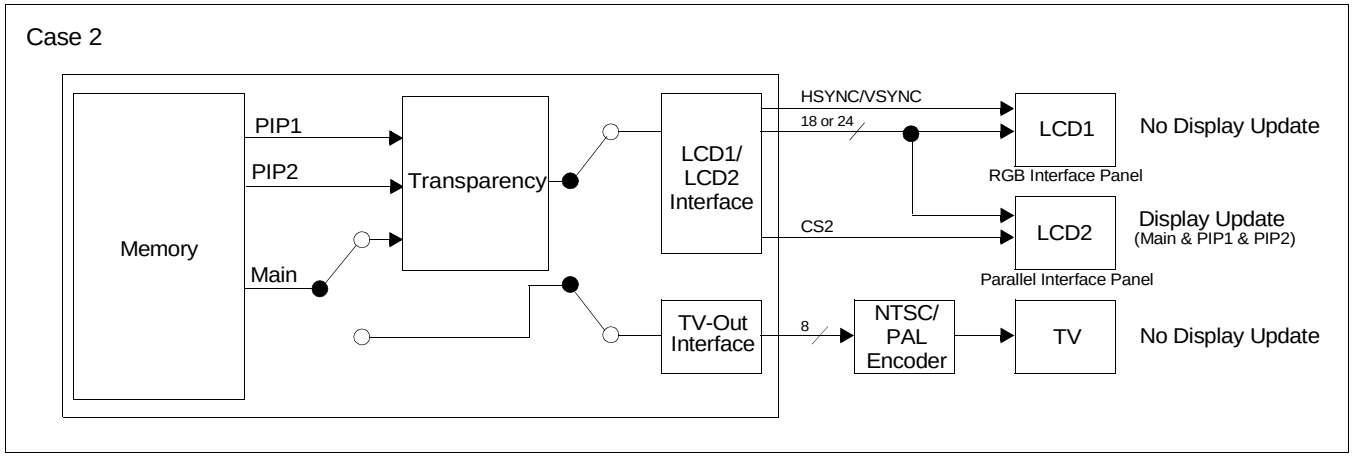


Figure 15-7: Mode 2, Case 2 - LCD2 Active (Main & PIP1 & PIP2)

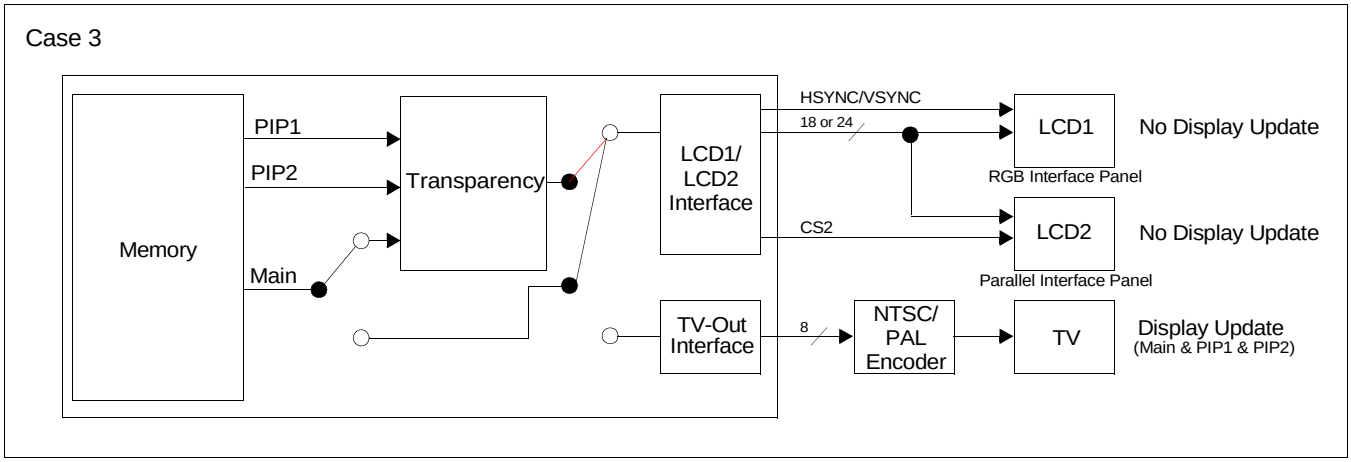


Figure 15-8: Mode 2, Case 3 - TV Active (Main & PIP1 & PIP2)

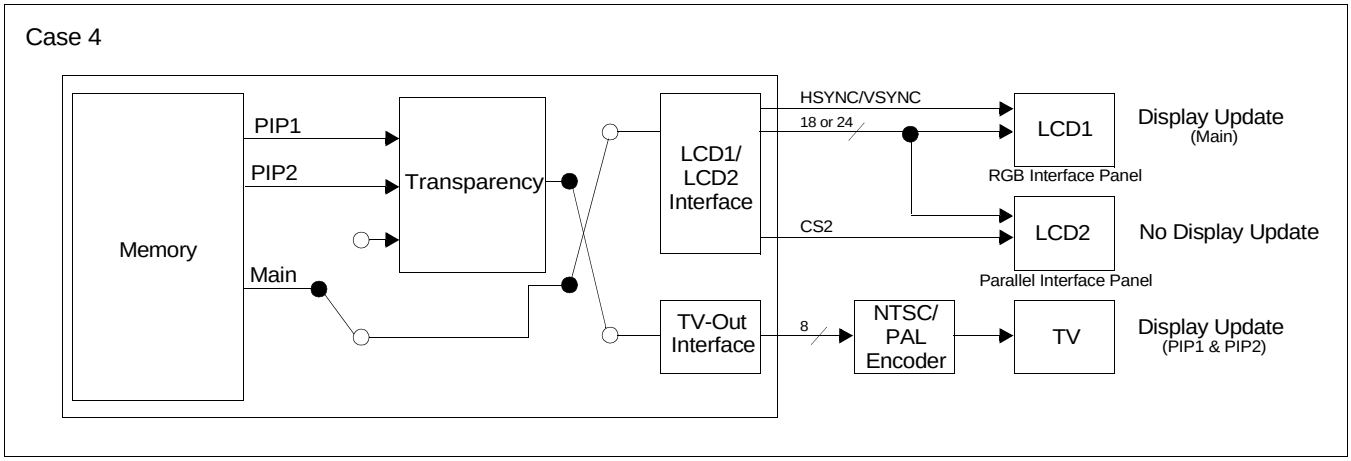


Figure 15-9: Mode 2, Case 4 - LCD1 Active (Main) and TV Active (PIP1 & PIP2)

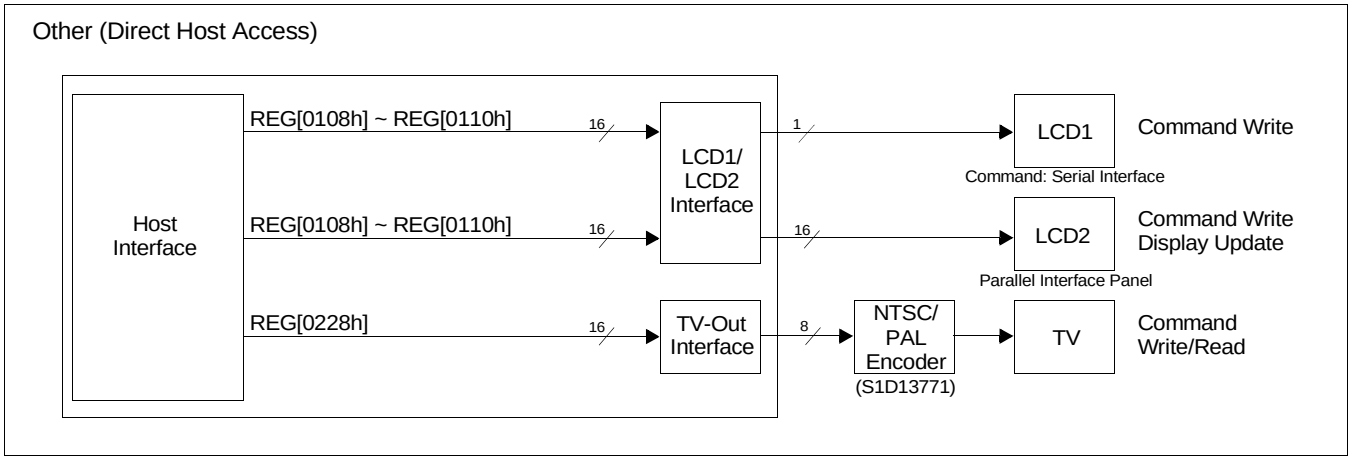


Figure 15-10: Mode 2, Direct Host Access - LCD2 Active

15.2.3 Mode 3

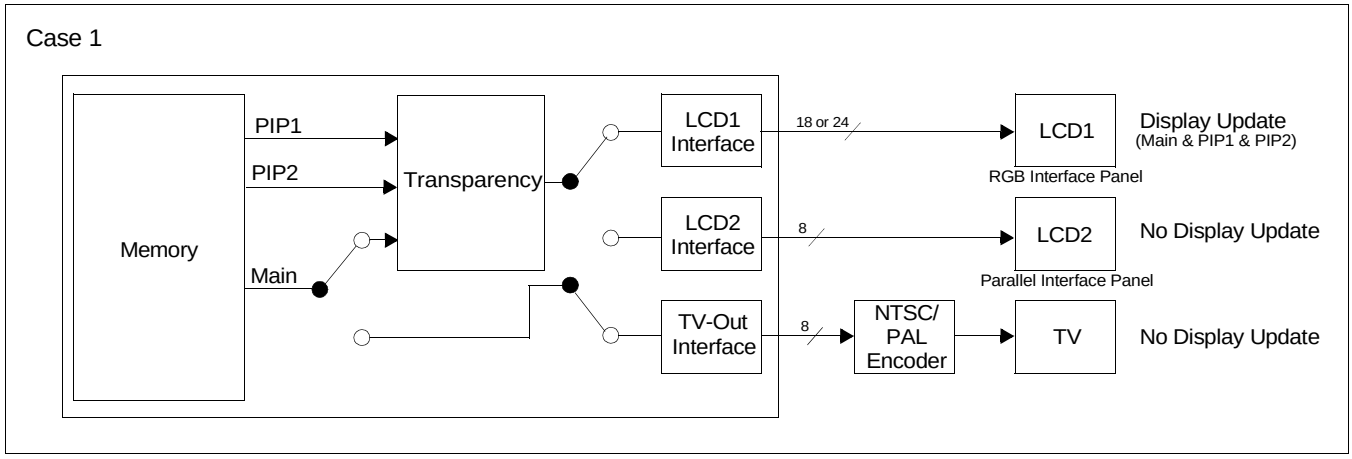


Figure 15-11: Mode 3, Case 1 - LCD1 Active (Main & PIP1 & PIP2)

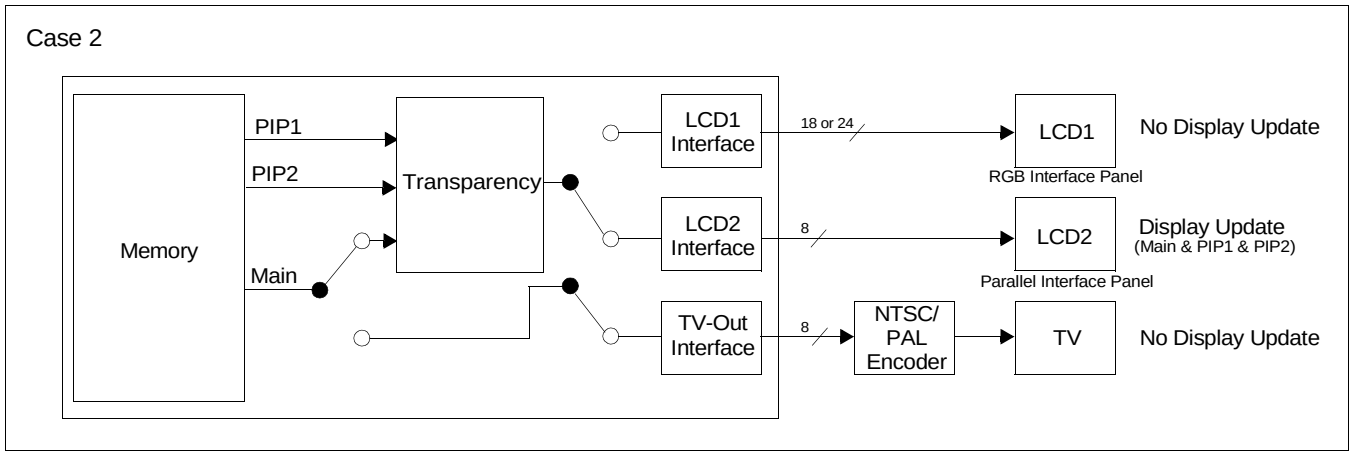


Figure 15-12: Mode 3, Case 2 - LCD2 Active (Main & PIP1 & PIP2)

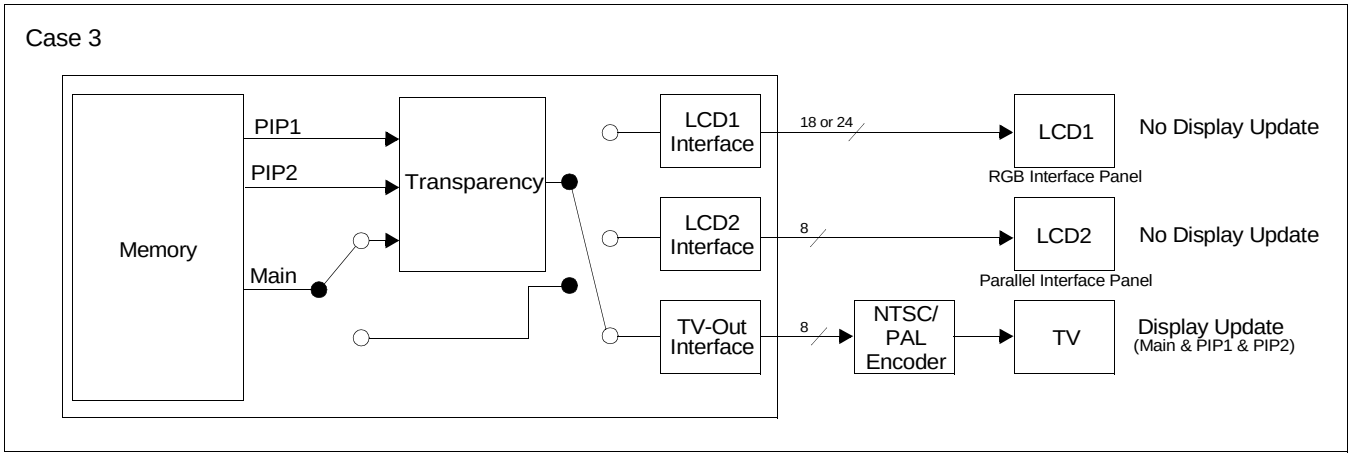


Figure 15-13: Mode 3, Case 3 - TV Active (Main & PIP1 & PIP2)

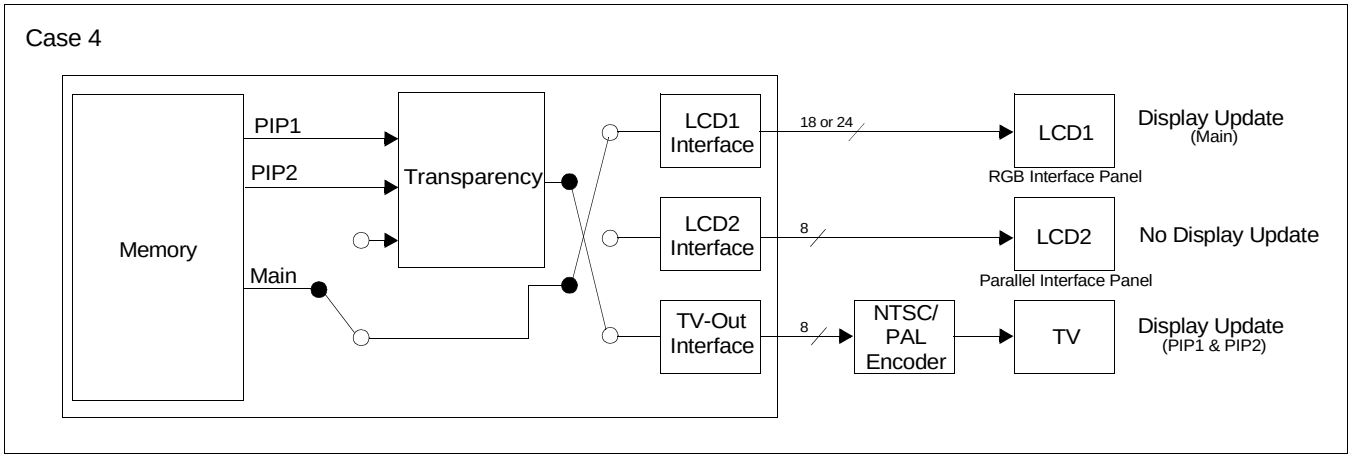


Figure 15-14: Mode 3, Case 4 - LCD1 Active (Main) and TV Active (PIP1 & PIP2)

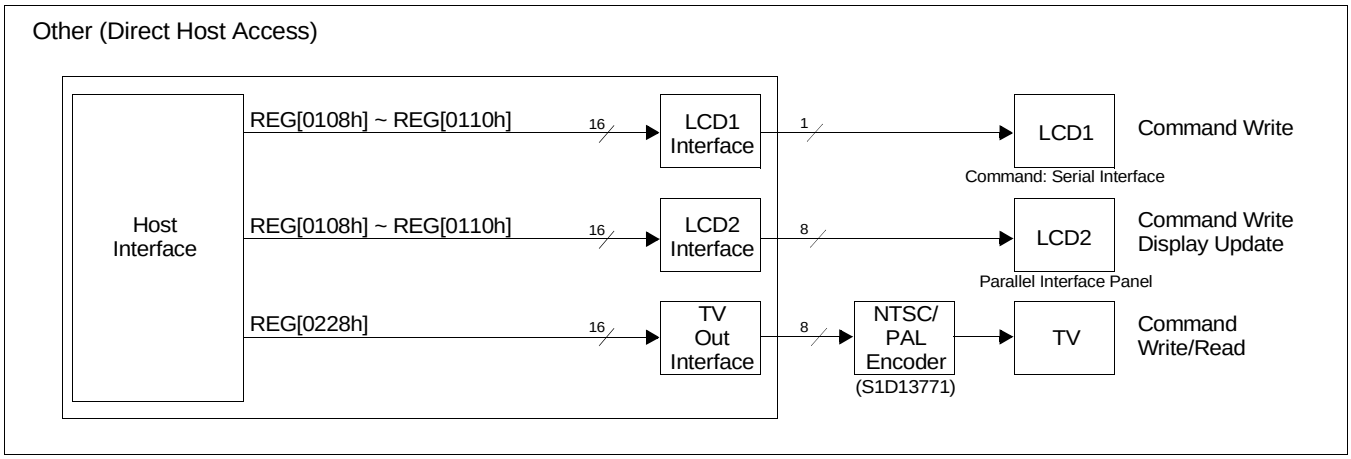


Figure 15-15: Mode 3, Direct Host Access - LCD2 Active

15.3 LCD1 Data Formats

LCD1 is always configured for a RGB panel interface (see REG[0104h] bits 1-0). The data format is determined by the data bus width as follows.

When REG[0104h] bit 5 = 0b, LCD1 is configured for an 18-bit interface and the RGB 6:6:6 data format is used.
When REG[0104h] bit 5 = 1b, LCD1 is configured for a 24-bit interface and the RGB 8:8:8 data format is used.

Table 15-3: 18/24-bit RGB Interface Data Formats

Pin	18-bit	24-bit
FPDAT0	R^7	R^7
FPDAT1	R^6	R^6
FPDAT2	R^5	R^5
FPDAT3	G^7	G^7
FPDAT4	G^6	G^6
FPDAT5	G^5	G^5
FPDAT6	B^7	B^7
FPDAT7	B^6	B^6
FPDAT8	B^5	B^5
FPDAT9	R^4	R^4
FPDAT10	R^3	R^3
FPDAT11	R^2	R^2
FPDAT12	G^4	G^4
FPDAT13	G^3	G^3
FPDAT14	G^2	G^2
FPDAT15	B^4	B^4
FPDAT16	B^3	B^3
FPDAT17	B^2	B^2
FPDAT18 (GPIOP0)	Low	R^1
FPDAT19 (GPIOP1)	Low	R^0
FPDAT20 (GPIOP2)	Low	G^1
FPDAT21 (GPIOP3)	Low	G^0
FPDAT22 (GPIOP4)	Low	B^1
FPDAT23 (GPIOP5)	Low	B^0

Note

FPDAT[18:23] are mapped on the GPIOP[0:5] pins. For detailed pin mapping, see Section 4.6, “LCD and TV-out Interface Pin Mapping” on page 34.

15.4 LCD2 Parallel Interface Data Formats

For LCD2 parallel interfaces (REG[0104h] bits 1-0 = 01b or 10b), the data format is selected by the LCD2 Parallel Data Format bits, REG[018Ch] bits 3-0.

15.4.1 8-Bit Parallel (RGB 3:3:2) Data Format

When REG[018Ch] bits 3-0 = 0000b, an 8-bit parallel interface using the RGB 3:3:2 data format is selected. This format uses 1 cycle per pixel.

Table 15-4: 8-bit Parallel (RGB 3:3:2) Data Format

Cycle Count	1	2	3	...	n+1
D7	R_0^7	R_1^7	R_2^7	...	R_n^7
D6	R_0^6	R_1^6	R_2^6	...	R_n^6
D5	R_0^5	R_1^5	R_2^5	...	R_n^5
D4	G_0^7	G_1^7	G_2^7	...	G_n^7
D3	G_0^6	G_1^6	G_2^6	...	G_n^6
D2	G_0^5	G_1^5	G_2^5	...	G_n^5
D1	B_0^7	B_1^7	B_2^7	...	B_n^7
D0	B_0^6	B_1^6	B_2^6	...	B_n^6

15.4.2 8-Bit Parallel (RGB 4:4:4) Data Format

When REG[018Ch] bits 3-0 = 0001b, an 8-bit parallel interface using the RGB 4:4:4 data format is selected. This format uses 3 cycles for every 2 pixels.

Table 15-5: 8-bit Parallel (RGB 4:4:4) Data Format

Cycle Count	1	2	3	...	3n+1	3n+2	3n+3
D7	R_0^7	B_0^7	G_1^7	...	R_n^7	B_n^7	G_{n+1}^7
D6	R_0^6	B_0^6	G_1^6	...	R_n^6	B_n^6	G_{n+1}^6
D5	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D4	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D3	G_0^7	R_1^7	B_1^7	...	G_n^7	R_{n+1}^7	B_{n+1}^7
D2	G_0^6	R_1^6	B_1^6	...	G_n^6	R_{n+1}^6	B_{n+1}^6
D1	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D0	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4

15.4.3 8-Bit Parallel (RGB 5:6:5) Data Format

When REG[018Ch] bits 3-0 = 1xxxb, an 8-bit parallel interface using RGB 5:6:5 data format is selected. This format uses 2 cycles per pixel.

Table 15-6: 8-bit Parallel (RGB 5:6:5) Data Format

Cycle Count	1	2	...	3n+1	3n+2
D7	R_0^7	G_0^4	...	R_n^7	G_n^4
D6	R_0^6	G_0^3	...	R_n^6	G_n^3
D5	R_0^5	G_0^2	...	R_n^5	G_n^2
D4	R_0^4	B_0^7	...	R_n^4	B_n^7
D3	R_0^3	B_0^6	...	R_n^3	B_n^6
D2	G_0^7	B_0^5	...	G_n^7	B_n^5
D1	G_0^6	B_0^4	...	G_n^6	B_n^4
D0	G_0^5	B_0^3	...	G_n^5	B_n^3

15.4.4 8-Bit Parallel (RGB 8:8:8) Data Format

When REG[018Ch] bits 3-0 = 0011b, an 8-bit parallel interface using RGB 8:8:8 data format is selected. This format uses 3 cycles per pixel.

Table 15-7: 8-bit Parallel (RGB 8:8:8) Data Format

Cycle Count	1	2	2	...	3n+1	3n+2	3n+2
D7	R_0^7	G_0^7	B_0^7	...	R_n^7	G_n^7	B_n^7
D6	R_0^6	G_0^6	B_0^6	...	R_n^6	G_n^6	B_n^6
D5	R_0^5	G_0^5	B_0^5	...	R_n^5	G_n^5	B_n^5
D4	R_0^4	G_0^4	B_0^4	...	R_n^4	G_n^4	B_n^4
D3	R_0^3	G_0^3	B_0^3	...	R_n^3	G_n^3	B_n^3
D2	R_0^2	G_0^2	B_0^2	...	R_n^2	G_n^2	B_n^2
D1	R_0^1	G_0^1	B_0^1	...	R_n^1	G_n^1	B_n^1
D0	R_0^0	G_0^0	B_0^0	...	R_n^0	G_n^0	B_n^0

15.4.5 16-Bit Parallel (RGB 4:4:4) Data Format

When REG[018Ch] bits 3-0 = 0101b, a 16-bit parallel interface using RGB 4:4:4 is selected. This format uses 1 cycle per pixel.

Table 15-8: 16-bit Parallel (RGB 4:4:4) Data Format

Cycle Count	1	2	3	...	n+1
D15	R_0^7	R_1^7	R_2^7	...	R_n^7
D14	R_0^6	R_1^6	R_2^6	...	R_n^6
D13	R_0^5	R_1^5	R_2^5	...	R_n^5
D12	R_0^4	R_1^4	R_2^4	...	R_n^4
D11	G_0^7	G_1^7	G_2^7	...	G_n^7
D10	G_0^6	G_1^6	G_2^6	...	G_n^6
D9	G_0^5	G_1^5	G_2^5	...	G_n^5
D8	G_0^4	G_1^4	G_2^4	...	G_n^4
D7	B_0^7	B_1^7	B_2^7	...	B_n^7
D6	B_0^6	B_1^6	B_2^6	...	B_n^6
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	—	—	—	...	—
D2	—	—	—	...	—
D1	—	—	—	...	—
D0	—	—	—	...	—

15.4.6 16-Bit Parallel (RGB 5:6:5) Data Format

When REG[018Ch] bits 3-0 = 0110b, a 16-bit parallel interface using RGB 5:6:5 is selected. This format uses 1 cycle per pixel.

Table 15-9: 16-bit Parallel (RGB 5:6:5) Data Format

Cycle Count	1	2	3	...	n+1
D15	R_0^7	R_1^7	R_2^7	...	R_n^7
D14	R_0^6	R_1^6	R_2^6	...	R_n^6
D13	R_0^5	R_1^5	R_2^5	...	R_n^5
D12	R_0^4	R_1^4	R_2^4	...	R_n^4
D11	R_0^3	R_1^3	R_2^3	...	R_n^3
D10	G_0^7	G_1^7	G_2^7	...	G_n^7
D9	G_0^6	G_1^6	G_2^6	...	G_n^6
D8	G_0^5	G_1^5	G_2^5	...	G_n^5
D7	G_0^4	G_1^4	G_2^4	...	G_n^4
D6	G_0^3	G_1^3	G_2^3	...	G_n^3
D5	$G0^2$	G_1^2	G_2^2	...	G_n^2
D4	B_0^7	B_1^7	B_2^7	...	B_n^7
D3	B_0^6	B_1^6	B_2^6	...	B_n^6
D2	B_0^5	B_1^5	B_2^5	...	B_n^5
D1	B_0^4	B_1^4	B_2^4	...	B_n^4
D0	B_0^3	B_1^3	B_2^3	...	B_n^3

15.4.7 16-Bit Parallel (RGB 8:8:8) Data Format

When REG[018Ch] bits 3-0 = 0010b, a 16-bit parallel interface using RGB 8:8:8 is selected. This format uses 3 cycles for every 2 pixels.

Table 15-10: 16-bit Parallel (RGB 8:8:8) Data Format

Cycle Count	1	2	3	...	3n+1	3n+2	3n+3
D15	R_0^7	B_0^7	G_1^7	...	R_n^7	B_n^7	G_{n+1}^7
D14	R_0^6	B_0^6	G_1^6	...	R_n^6	B_n^6	G_{n+1}^6
D13	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D12	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D11	R_0^3	B_0^3	G_1^3	...	R_n^3	B_n^3	G_{n+1}^3
D10	R_0^2	B_0^2	G_1^2	...	R_n^2	B_n^2	G_{n+1}^2
D9	R_0^1	B_0^1	G_1^1	...	R_n^1	B_n^1	G_{n+1}^1
D8	R_0^0	B_0^0	G_1^0	...	R_n^0	B_n^0	G_{n+1}^0
D7	G_0^7	R_1^7	B_1^7	...	G_n^7	R_{n+1}^7	B_{n+1}^7
D6	G_0^6	R_1^6	B_1^6	...	G_n^6	R_{n+1}^6	B_{n+1}^6
D5	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D4	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4
D3	G_0^3	R_1^3	B_1^3	...	G_n^3	R_{n+1}^3	B_{n+1}^3
D2	G_0^2	R_1^2	B_1^2	...	G_n^2	R_{n+1}^2	B_{n+1}^2
D1	G_0^1	R_1^1	B_1^1	...	G_n^1	R_{n+1}^1	B_{n+1}^1
D0	G_0^0	R_1^0	B_1^0	...	G_n^0	R_{n+1}^0	B_{n+1}^0

15.4.8 18-Bit Parallel (RGB 6:6:6) Data Format

When REG[018Ch] bits 3-0 = 0111b, an 18-bit parallel interface using RGB 6:6:6 is selected. This format uses 1 cycle per pixel.

Table 15-11: 18-bit Parallel (RGB 6:6:6) Data Format

Cycle Count	1	2	3	...	n+1
D17	R_0^7	R_1^7	R_2^7	...	R_n^7
D16	R_0^6	R_1^6	R_2^6	...	R_n^6
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	G_0^7	G_1^7	G_2^7	...	G_n^7
D10	G_0^6	G_1^6	G_2^6	...	G_n^6
D9	G_0^5	G_1^5	G_2^5	...	G_n^5
D8	G_0^4	G_1^4	G_2^4	...	G_n^4
D7	G_0^3	G_1^3	G_2^3	...	G_n^3
D6	G_0^2	G_1^2	G_2^2	...	G_n^2
D5	B_0^7	B_1^7	B_2^7	...	B_n^7
D4	B_0^6	B_1^6	B_2^6	...	B_n^6
D3	B_0^5	B_1^5	B_2^5	...	B_n^5
D2	B_0^4	B_1^4	B_2^4	...	B_n^4
D1	B_0^3	B_1^3	B_2^3	...	B_n^3
D0	B_0^2	B_1^2	B_2^2	...	B_n^2

15.4.9 24-Bit Parallel (RGB 8:8:8) Data Format

When REG[018Ch] bits 3-0 = 0100b, a 24-bit parallel interface using RGB 8:8:8 is selected. This format uses 1 cycle per pixel.

Table 15-12: 24-bit Parallel (RGB 8:8:8) Data Format

Cycle Count	1	2	3	...	n+1
D23	R_0^7	R_1^7	R_2^7	...	R_n^7
D22	R_0^6	R_1^6	R_2^6	...	R_n^6
D21	R_0^5	R_1^5	R_2^5	...	R_n^5
D20	R_0^4	R_1^4	R_2^4	...	R_n^4
D19	R_0^3	R_1^3	R_2^3	...	R_n^3
D18	R_0^2	R_1^2	R_2^2	...	R_n^2
D17	R_0^1	R_1^1	R_2^1	...	R_n^1
D16	R_0^0	R_1^0	R_2^0	...	R_n^0
D15	G_0^7	G_1^7	G_2^7	...	G_n^7
D14	G_0^6	G_1^6	G_2^6	...	G_n^6
D13	G_0^5	G_1^5	G_2^5	...	G_n^5
D12	G_0^4	G_1^4	G_2^4	...	G_n^4
D11	G_0^3	G_1^3	G_2^3	...	G_n^3
D10	G_0^2	G_1^2	G_2^2	...	G_n^2
D9	G_0^1	G_1^1	G_2^1	...	G_n^1
D8	G_0^0	G_1^0	G_2^0	...	G_n^0
D7	B_0^7	B_1^7	B_2^7	...	B_n^7
D6	B_0^6	B_1^6	B_2^6	...	B_n^6
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	B_0^3	B_1^3	B_2^3	...	B_n^3
D2	B_0^2	B_1^2	B_2^2	...	B_n^2
D1	B_0^1	B_1^1	B_2^1	...	B_n^1
D0	B_0^0	B_1^0	B_2^0	...	B_n^0

15.5 LCD2 Serial Interface Data Formats

For LCD2 serial interfaces (REG[0104h] bits 1-0 = 00b), the data format is selected by REG[0188h] bit 7 and the LCD2 Serial Data Format bits, REG[0188h] bits 3-2.

15.5.1 8-Bit Serial (RGB 3:3:2) Data Format

When REG[0188h] bit 7 = 0b and REG[0188h] bits 3-2 = 00b, an 8-bit serial interface using RGB 3:3:2 is selected.

Table 15-13: 8-bit Serial (RGB 3:3:2) Data Format

Cycle Count	1	2	3	...	n+1
D7	R_0^7	R_1^7	R_2^7	...	R_n^7
D6	R_0^6	R_1^6	R_2^6	...	R_n^6
D5	R_0^5	R_1^5	R_2^5	...	R_n^5
D4	G_0^7	G_1^7	G_2^7	...	G_n^7
D3	G_0^6	G_1^6	G_2^6	...	G_n^6
D2	G_0^5	G_1^5	G_2^5	...	G_n^5
D1	B_0^7	B_1^7	B_2^7	...	B_n^7
D0	B_0^6	B_1^6	B_2^6	...	B_n^6

15.5.2 8-Bit Serial (RGB 4:4:4) Data Format

When REG[0188h] bit 7 = 0b and REG[0188h] bits 3-2 = 01b, an 8-bit serial interface using RGB 4:4:4 is selected.

Table 15-14: 8-bit Serial (RGB 4:4:4) Data Format

Cycle Count	1	2	3	...	3n+1	3n+2	3n+3
D7	R_0^7	B_0^7	G_1^7	...	R_n^7	B_n^7	G_{n+1}^7
D6	R_0^6	B_0^6	G_1^6	...	R_n^6	B_n^6	G_{n+1}^6
D5	R_0^5	B_0^5	G_1^5	...	R_n^5	B_n^5	G_{n+1}^5
D4	R_0^4	B_0^4	G_1^4	...	R_n^4	B_n^4	G_{n+1}^4
D3	G_0^7	R_1^7	B_1^7	...	G_n^7	R_{n+1}^7	B_{n+1}^7
D2	G_0^6	R_1^6	B_1^6	...	G_n^6	R_{n+1}^6	B_{n+1}^6
D1	G_0^5	R_1^5	B_1^5	...	G_n^5	R_{n+1}^5	B_{n+1}^5
D0	G_0^4	R_1^4	B_1^4	...	G_n^4	R_{n+1}^4	B_{n+1}^4

15.5.3 16-Bit Serial (RGB 4:4:4) LSB unused Data Format

When REG[0188h] bit 7 = 1b and REG[0188h] bits 3-2 = 00b, a 16-bit serial interface using RGB 4:4:4 LSB unused is selected.

Table 15-15: 16-bit Serial (RGB 4:4:4) LSB Un-used Data Format

Cycle Count	1	2	3	...	n
D15	R_0^7	R_1^7	R_2^7	...	R_n^7
D14	R_0^6	R_1^6	R_2^6	...	R_n^6
D13	R_0^5	R_1^5	R_2^5	...	R_n^5
D12	R_0^4	R_1^4	R_2^4	...	R_n^4
D11	G_0^7	G_1^7	G_2^7	...	G_n^7
D10	G_0^6	G_1^6	G_2^6	...	G_n^6
D9	G_0^5	G_1^5	G_2^5	...	G_n^5
D8	G_0^4	G_1^4	G_2^4	...	G_n^4
D7	B_0^7	B_1^7	B_2^7	...	B_n^7
D6	B_0^6	B_1^6	B_2^6	...	B_n^6
D5	B_0^5	B_1^5	B_2^5	...	B_n^5
D4	B_0^4	B_1^4	B_2^4	...	B_n^4
D3	—	—	—	...	—
D2	—	—	—	...	—
D1	—	—	—	...	—
D0	—	—	—	...	—

15.5.4 16-Bit Serial (RGB 4:4:4) MSB unused Data Format

When REG[0188h] bit 7 = 1b and REG[0188h] bits 3-2 = 01b, a 16-bit serial interface using RGB 4:4:4 MSB unused is selected.

Table 15-16: 16-bit Serial (RGB 4:4:4) MSB Un-used Data Format

Cycle Count	1	2	3	...	n+1
D15	—	—	—	...	—
D14	—	—	—	...	—
D13	—	—	—	...	—
D12	—	—	—	...	—
D11	R_0^7	R_1^7	R_2^7	...	R_n^7
D10	R_0^6	R_1^6	R_2^6	...	R_n^6
D9	R_0^5	R_1^5	R_2^5	...	R_n^5
D8	R_0^4	R_1^4	R_2^4	...	R_n^4
D7	G_0^7	G_1^7	G_2^7	...	G_n^7
D6	G_0^6	G_1^6	G_2^6	...	G_n^6
D5	G_0^5	G_1^5	G_2^5	...	G_n^5
D4	G_0^4	G_1^4	G_2^4	...	G_n^4
D3	B_0^7	B_1^7	B_2^7	...	B_n^7
D2	B_0^6	B_1^6	B_2^6	...	B_n^6
D1	B_0^5	B_1^5	B_2^5	...	B_n^5
D0	B_0^4	B_1^4	B_2^4	...	B_n^4

15.5.5 16-Bit Serial (RGB 5:6:5) Data Format

When REG[0188h] bit 7 = 1b and REG[0188h] bits 3-2 = 10b, a 16-bit serial interface using RGB 5:6:5 is selected.

Table 15-17: 16-bit Serial (RGB 5:6:5) Data Format

Cycle Count	1	2	3	...	n+1
D15	R_0^7	R_1^7	R_2^7	...	R_n^7
D14	R_0^6	R_1^6	R_2^6	...	R_n^6
D13	R_0^5	R_1^5	R_2^5	...	R_n^5
D12	R_0^4	R_1^4	R_2^4	...	R_n^4
D11	R_0^3	R_1^3	R_2^3	...	R_n^3
D10	G_0^7	G_1^7	G_2^7	...	G_n^7
D9	G_0^6	G_1^6	G_2^6	...	G_n^6
D8	G_0^5	G_1^5	G_2^5	...	G_n^5
D7	G_0^4	G_1^4	G_2^4	...	G_n^4
D6	G_0^3	G_1^3	G_2^3	...	G_n^3
D5	G_0^2	G_1^2	G_2^2	...	G_n^2
D4	B_0^7	B_1^7	B_2^7	...	B_n^7
D3	B_0^6	B_1^6	B_2^6	...	B_n^6
D2	B_0^5	B_1^5	B_2^5	...	B_n^5
D1	B_0^4	B_1^4	B_2^4	...	B_n^4
D0	B_0^3	B_1^3	B_2^3	...	B_n^3

15.5.6 18-Bit Serial (RGB 6:6:6) Data Format

When REG[0188h] bit 7 = 1b and REG[0188h] bits 3-2 = 11b, an 18-bit serial interface using RGB 6:6:6 is selected.

Table 15-18: 18-bit Serial (RGB 6:6:6) Data Format

Cycle Count	1	2	3	...	n+1
D17	R_0^7	R_1^7	R_2^7		R_n^7
D16	R_0^6	R_1^6	R_2^6		R_n^6
D15	R_0^5	R_1^5	R_2^5	...	R_n^5
D14	R_0^4	R_1^4	R_2^4	...	R_n^4
D13	R_0^3	R_1^3	R_2^3	...	R_n^3
D12	R_0^2	R_1^2	R_2^2	...	R_n^2
D11	G_0^7	G_1^7	G_2^7	...	G_n^7
D10	G_0^6	G_1^6	G_2^6	...	G_n^6
D9	G_0^5	G_1^5	G_2^5	...	G_n^5
D8	G_0^4	G_1^4	G_2^4	...	G_n^4
D7	G_0^3	G_1^3	G_2^3	...	G_n^3
D6	G_0^2	G_1^2	G_2^2	...	G_n^2
D5	B_0^7	B_1^7	B_2^7	...	B_n^7
D4	B_0^6	B_1^6	B_2^6	...	B_n^6
D3	B_0^5	B_1^5	B_2^5	...	B_n^5
D2	B_0^4	B_1^4	B_2^4	...	B_n^4
D1	B_0^3	B_1^3	B_2^3	...	B_n^3
D0	B_0^2	B_1^2	B_2^2	...	B_n^2

15.6 LCD2 Parallel Command/Parameter Format

15.6.1 LCD2 Parallel Command/Parameter Format 1

When panel interface Mode 2 is selected (REG[0104h] bits 1-0 = 01b), the following parallel command/parameter format is used.

Table 15-19: LCD2 Parallel Command/Parameter Format 1

Pin Name	REG[0108h] bits 15-0 / REG[010Ch] bits 15-0		
	REG[018Ch] bits 5-4 = 00b	REG[018Ch] bits 5-4 = 01b	REG[018Ch] bits 5-4 = 10b
P2DAT23	Low	Low	Low
P2DAT22	Low	Low	Low
P2DAT21	Low	Low	Low
P2DAT20	Low	Low	Low
P2DAT19	Low	Low	Low
P2DAT18	Low	Low	Low
P2DAT17	Low	bit 15	bit 15
P2DAT16	Low	bit 14	bit 14
P2DAT15	bit 15	bit 13	bit 13
P2DAT14	bit 14	bit 12	bit 12
P2DAT13	bit 13	bit 11	bit 11
P2DAT12	bit 12	bit 10	Low/High (Note 2)
P2DAT11	bit 11	bit 9	bit 10
P2DAT10	bit 10	bit 8	bit 9
P2DAT9	bit 9	Low	bit 8
P2DAT8	bit 8	bit 7	bit 7
P2DAT7	bit 7	bit 6	bit 6
P2DAT6	bit 6	bit 5	bit 5
P2DAT5	bit 5	bit 4	bit 4
P2DAT4	bit 4	bit 3	bit 3
P2DAT3	bit 3	bit 2	bit 2
P2DAT2	bit 2	bit 1	bit 1
P2DAT1	bit 1	bit 0	bit 0
P2DAT0	bit 0	Low	Low/High (Note 1)

Note

1. The output is driven according to the logical AND of bits 4-0.
2. The output is driven according to the logical AND of bits 15-11.

15.6.2 LCD2 Parallel Command/Parameter Format 2

When panel interface Mode 3 (REG[0104h] bits 1-0 = 10b) and 8-bit transfer mode (REG[018Ch] bit 8 = 0b) is selected, the following parallel command/parameter format is used.

Table 15-20: LCD2 Parallel Command/Parameter Format 2

Pin Name	REG[0108h] bits 7-0 / REG[010Ch] bits 7-0
P2DAT7	bit 7
P2DAT6	bit 6
P2DAT5	bit 5
P2DAT4	bit 4
P2DAT3	bit 3
P2DAT2	bit 2
P2DAT1	bit 1
P2DAT0	bit 0

Note

REG[0108h] bits 15-8 and REG[010Ch] bits 15-8 are not used.

15.6.3 LCD2 Parallel Command/Parameter Format 3

When panel interface Mode 3 (REG[0104h] bits 1-0 = 10b) and 16-bit transfer mode (REG[018Ch] bit 8 = 1b) is selected, the following parallel command/parameter format is used.

Table 15-21: LCD2 Parallel Command/Parameter Format 3

Pin Name	REG[0108h] bits 15-0 / REG[010Ch] bits 15-0	
	Cycle 1	Cycle 2
P2DAT7	bit 7	bit 15
P2DAT6	bit 6	bit 14
P2DAT5	bit 5	bit 13
P2DAT4	bit 4	bit 12
P2DAT3	bit 3	bit 11
P2DAT2	bit 2	bit 10
P2DAT1	bit 1	bit 9
P2DAT0	bit 0	bit 8

15.7 TV-Out HSYNC & FIELD / ITU-R BT656 Interface Type Data Format

When the TV-Out interface type is configured for HSYNC & FIELD (REG[0200h] bits 1-0 = 01b) or ITU-R-BT656 (REG[0200h] bits 1-0 = 11b), the following data format is used.

Table 15-22: HSYNC and FIELD / ITU-R BT656 TV-Out Interface Type Data Format

Cycle Count	1	2	3	4	5	6	7	8	...
TVDT7	U_0^7	Y_0^7	V_0^7	Y_1^7	U_2^7	Y_2^7	V_2^7	Y_3^7	...
TVDT6	U_0^6	Y_0^6	V_0^6	Y_1^6	U_2^6	Y_2^6	V_2^6	Y_3^6	...
TVDT5	U_0^5	Y_0^5	V_0^5	Y_1^5	U_2^5	Y_2^5	V_2^5	Y_3^5	...
TVDT4	U_0^4	Y_0^4	V_0^4	Y_1^4	U_2^4	Y_2^4	V_2^4	Y_3^4	...
TVDT3	U_0^3	Y_0^3	V_0^3	Y_1^3	U_2^3	Y_2^3	V_2^3	Y_3^3	...
TVDT2	U_0^2	Y_0^2	V_0^2	Y_1^2	U_2^2	Y_2^2	V_2^2	Y_3^2	...
TVDT1	U_0^1	Y_0^1	V_0^1	Y_1^1	U_2^1	Y_2^1	V_2^1	Y_3^1	...
TVDT0	U_0^0	Y_0^0	V_0^0	Y_1^0	U_2^0	Y_2^0	V_2^0	Y_3^0	...

15.8 TV-Out Parallel Interface Type Data Formats

15.8.1 8-Bit Parallel (RGB 5:6:5) Data Format

When the TV-Out interface type is configured for Parallel (REG[0200h] bits 1-0 = 10b) and the RGB Output Data Type Select bit is set to 0b (REG[0200h] bit 7 = 0b), the following data format is used.

Table 15-23: 8-Bit Parallel (RGB 5:6:5) Data Format

Cycle Count	1	2	...	3n+1	3n+2
TVDT7	R_0^7	G_0^4	...	R_n^7	G_n^4
TVDT6	R_0^6	G_0^3	...	R_n^6	G_n^3
TVDT5	R_0^5	G_0^2	...	R_n^5	G_n^2
TVDT4	R_0^4	B_0^7	...	R_n^4	B_n^7
TVDT3	R_0^3	B_0^6	...	R_n^3	B_n^6
TVDT2	G_0^7	B_0^5	...	G_n^7	B_n^5
TVDT1	G_0^6	B_0^4	...	G_n^6	B_n^4
TVDT0	G_0^5	B_0^3	...	G_n^5	B_n^3

15.8.2 8-Bit Parallel (RGB 8:8:8) Data Format

When the TV-Out interface type is configured for Parallel (REG[0200h] bits 1-0 = 10b) and the RGB Output Data Type Select bit is set to 1b (REG[0200h] bit 7 = 1b), the following data format is used.

Table 15-24: 8-bit Parallel (RGB 8:8:8) Data Format

Cycle Count	1	2	2	...	3n+1	3n+2	3n+2
TVDT7	R_0^7	G_0^7	B_0^7	...	R_n^7	G_n^7	B_n^7
TVDT6	R_0^6	G_0^6	B_0^6	...	R_n^6	G_n^6	B_n^6
TVDT5	R_0^5	G_0^5	B_0^5	...	R_n^5	G_n^5	B_n^5
TVDT4	R_0^4	G_0^4	B_0^4	...	R_n^4	G_n^4	B_n^4
TVDT3	R_0^3	G_0^3	B_0^3	...	R_n^3	G_n^3	B_n^3
TVDT2	R_0^2	G_0^2	B_0^2	...	R_n^2	G_n^2	B_n^2
TVDT1	R_0^1	G_0^1	B_0^1	...	R_n^1	G_n^1	B_n^1
TVDT0	R_0^0	G_0^0	B_0^0	...	R_n^0	G_n^0	B_n^0

15.9 TV-Out Parallel Interface Type Command Format

When the TV-Out interface type is configured for Parallel (REG[0200h] bits 1-0 = 10b), the following command data format is used.

Table 15-25: TV-Out Parallel Interface Type Command/Data Format

Pin Name	REG[0228h] bits 7-0
TVDT7	bit 7
TVDT6	bit 6
TVDT5	bit 5
TVDT4	bit 4
TVDT3	bit 3
TVDT2	bit 2
TVDT1	bit 1
TVDT0	bit 0

15.10 LUT

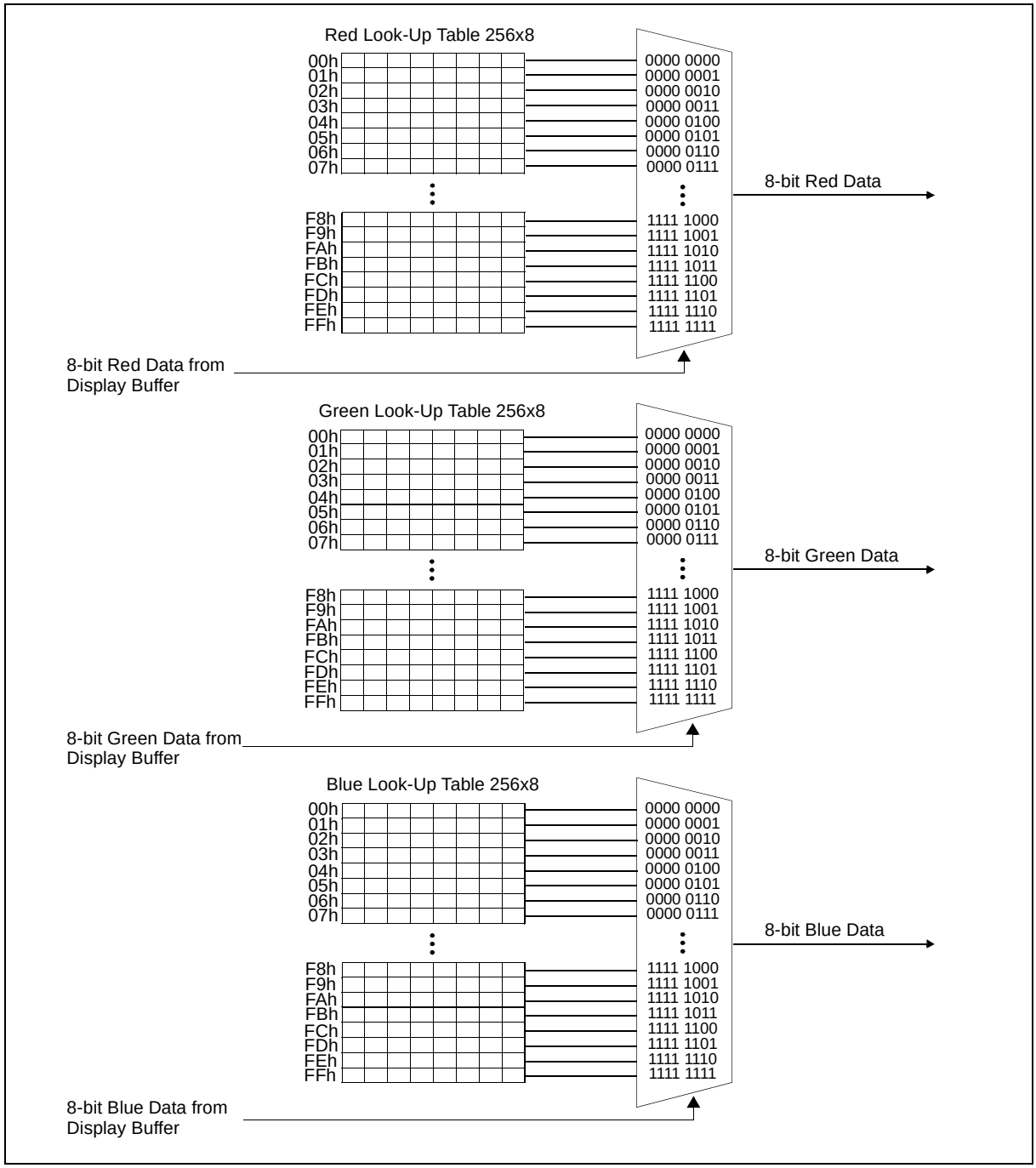


Figure 15-16: LUT Architecture

Note

When the Display Output Port is set for LCD1 (Main) + TV-Out (PIP1/PIP2) (REG[0604h] bits 11-8 = 1011b), the LUT function is applied only to the TV-Out display and has no effect on LCD1.

15.11 Pseudo Color Mode

The S1D13774 supports Pseudo Color Mode which is used to minimize the change in image color quality when the color depth of the image is lowered for output to a panel. This is useful for panels with a smaller data bus width than the display output size. For example, if the S1D13774 is configured for a 16-bit TFT panel, the internal display image data is RGB 8:8:8 (24-bit) and must be converted to RGB 5:6:5 (16-bit) for output to the panel.

When Pseudo Color Mode is disabled (REG[0648h] bits 2-0 = 000b), each color component (RGB) is rounded down to the data bus width selected by the Pseudo RGB Output Color Format bits (see REG[0648h] bits 5-4). When enabled, the following options are selectable.

- 2x2 Matrix Dither - REG[0648h] bits 2-0 = 001b
- FRM - REG[0648h] bits 2-0 = 010b
- Error Diffusion - REG[0648h] bits 2-0 = 011b

Note
For display using parallel/serial LCD interfaces or using the parallel TV-Out interface, these settings are not valid.

To determine the optimum Pseudo Color Mode, it may be necessary to perform a visual evaluation for each specific implementation.

16 Video Input Interface

The Video Input Interface allows the S1D13774 to receive image data from a streaming input source. The Video Input Interface can be configured as:

- 8-bit YUV interface
- 12-bit RGB interface

16.1 Video Input Interface Data Formats

16.1.1 RGB 8:8:8

Interface Type = RGB: REG[0484h] bits 5-4 = 00b or 01b
Format = RGB 8:8:8: REG[0484h] bits 14-12 = 000b

Table 16-1: RGB 8:8:8 Input Format

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	G_0^7	G_0^6	G_0^5	G_0^4
2	G_0^3	G_0^2	G_0^1	G_0^0	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
3	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_0^1	R_1^0	G_1^7	G_1^6	G_1^5	G_1^4
4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
	...											

16.1.2 RGB 6:6:6 Format 1

Interface Type = RGB: REG[0484h] bits 5-4 = 00b or 01b
Format = RGB 6:6:6 Format 1: REG[0484h] bits 14-12 = 001b

Table 16-2: RGB 6:6:6 Input Format 1

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	—	—	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	—	—	G_0^5	G_0^4
2	G_0^3	G_0^2	G_0^1	G_0^0	—	—	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
3	—	—	R_1^5	R_1^4	R_1^3	R_1^2	R_0^1	R_1^0	—	—	G_1^5	G_1^4
4	G_1^3	G_1^2	G_1^1	G_1^0	—	—	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
	...											

16.1.3 RGB 6:6:6 Format 2

Interface Type = RGB: REG[0484h] bits 5-4 = 00b or 01b
Format = RGB 6:6:6 Format 2: REG[0484h] bits 14-12 = 010b

Table 16-3: RGB 6:6:6 Input Format 2

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	—	—	G_0^5	G_0^4	G_0^3	G_0^2
2	G_0^1	G_0^0	—	—	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0	—	—
3	R_1^5	R_1^4	R_1^3	R_1^2	R_0^1	R_1^0	—	—	G_1^5	G_1^4	G_1^3	G_1^2
4	G_1^1	G_1^0	—	—	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0	—	—
	...											

16.1.4 Conversion RGB 6:6:6 to RGB 8:8:8

For RGB 6:6:6 formats (REG[0484h] bits 14-12 = 001b or 010b), the image data must be converted to RGB 8:8:8 before being written to memory. The conversion is done as follows.

Table 16-4: RGB 6:6:6 to RGB 8:8:8 Conversion

RGB 6:6:6 (Input)							RGB 8:8:8 (Memory)							
R5	R4	R3	R2	R1	R0	→	R5	R4	R3	R2	R1	R0	R5	R4
G5	G4	G3	G2	G1	G0	→	G5	G4	G3	G2	G1	G0	G5	G4
B5	B4	B3	B2	B1	B0	→	B5	B4	B3	B2	B1	B0	B5	B4

16.1.5 RGB 5:6:5 Format 1

Interface Type = RGB: REG[0484h] bits 5-4 = 00b or 01b
Format = RGB 5:6:5 Format 1: REG[0484h] bits 14-12 = 011b

Table 16-5: RGB 5:6:5 Input Format 1

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	—	—	—	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	—	—	G_0^5	G_0^4
2	G_0^3	G_0^2	G_0^1	G_0^0	—	—	—	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
3	—	—	—	R_1^4	R_1^3	R_1^2	R_0^1	R_1^0	—	—	G_1^5	G_1^4
4	G_1^3	G_1^2	G_1^1	G_1^0	—	—	—	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
	...											

16.1.6 RGB 5:6:5 Format 2

Interface Type = RGB: REG[0484h] bits 5-4 = 00b or 01b
Format = RGB 5:6:5 Format 2: REG[0484h] bits 14-12 = 100b

Table 16-6: RGB 5:6:5 Input Format 2

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	—	—	—	G_0^5	G_0^4	G_0^3	G_0^2
2	G_0^1	G_0^0	—	—	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0	—	—	—
3	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0	—	—	—	G_1^5	G_1^4	G_1^3	G_1^2
4	G_1^1	G_1^0	—	—	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0	—	—	—
	...											

16.1.7 YUV 4:2:2 Format 1

Interface Type = YUV: REG[0484h] bits 5-4 = 10b or 11b
YUV 4:2:2 Format 1: REG[0484h] bits 11-10 = 00b

Table 16-7: YUV 4:2:2 Input Format 1

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	—	—	—	—	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
2	—	—	—	—	Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0
3	—	—	—	—	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0
4	—	—	—	—	Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^0
	...											

16.1.8 YUV 4:2:2 Format 2

Interface Type = YUV: REG[0484h] bits 5-4 = 10b or 11b
YUV 4:2:2 Format 2: REG[0484h] bits 11-10 = 01b

Table 16-8: YUV 4:2:2 Input Format 2

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	—	—	—	—	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0
2	—	—	—	—	Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0
3	—	—	—	—	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
4	—	—	—	—	Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^0
	...											

16.1.9 YUV 4:2:2 Format 3

Interface Type = YUV: REG[0484h] bits 5-4 = 10b or 11b
YUV 4:2:2 Format 3: REG[0484h] bits 11-10 = 10b

Table 16-9: YUV 4:2:2 Input Format 3

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	—	—	—	—	Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0
2	—	—	—	—	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
3	—	—	—	—	Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^0
4	—	—	—	—	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0
	...											

16.1.10 YUV 4:2:2 Format 4

Interface Type = YUV: REG[0484h] bits 5-4 = 10b or 11b
YUV 4:2:2 Format 4: REG[0484h] bits 11-10 = 11b

Table 16-10: YUV 4:2:2 Input Format 4

	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	—	—	—	—	Y_0^7	Y_0^6	Y_0^5	Y_0^4	Y_0^3	Y_0^2	Y_0^1	Y_0^0
2	—	—	—	—	V_0^7	V_0^6	V_0^5	V_0^4	V_0^3	V_0^2	V_0^1	V_0^0
3	—	—	—	—	Y_1^7	Y_1^6	Y_1^5	Y_1^4	Y_1^3	Y_1^2	Y_1^1	Y_1^0
4	—	—	—	—	U_0^7	U_0^6	U_0^5	U_0^4	U_0^3	U_0^2	U_0^1	U_0^0
	...											

16.2 Video Input Interface Programming Flow

Programming for the Video Input Interface requires the contents of the Main or Sub Write Path registers are updated according to a specific sequence. An example programming flow which shows when the registers should be updated is available in Section 13.2, “Video Input Interface” on page 342.

17 GPIO Interface

The S1D13774 is designed with 39 general purpose IO pins (GPIOs). Many of these pins are associated with multiple functions. For detailed information on each GPIO pin, see Section 4.2.4, “GPIO” on page 22. For a pin mapping summary, see Section 4.7, “GPIO Pin Mapping” on page 38.

The GPIO pins are driven by either the PIOVDD IO voltage (GPIOP[14:0]) or HIOVDD IO voltage (GPIOH[23:0]). The GPIOP pins are primary used by the LCD1, LCD2, or TV-Out interfaces. The GPIOH pins are used by the Indirect Host interface, but are available for use by the LCD2 or TV-Out interfaces when the Indirect Host interface is not selected (CNF0=0).

The GPIO function is asynchronous allowing the GPIO pins and registers to be used in normal operation mode, and also when the S1D13774 is in a power saving mode (Standby Mode A, Standby Mode B, and Sleep Mode).

Interrupts can be output to the Host using either positive or negative edge triggers for each GPIO pin. Interrupts are possible while in all modes (Normal Operation Mode, Standby Mode A, Standby Mode B, and Sleep Mode).

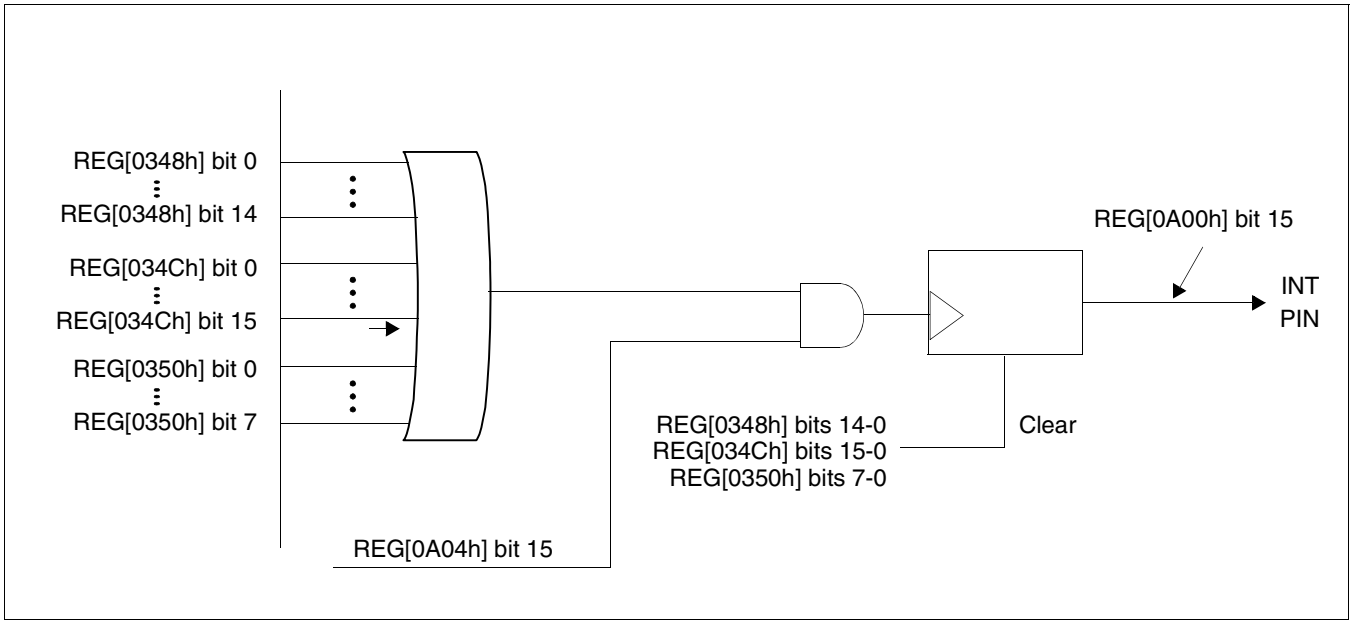


Figure 17-1: GPIO Interrupt

18 Crystal Oscillator Circuit

The S1D13774 supports a crystal oscillation circuit that can be used as the source clock. The circuit constant is a reference value.

Table 18-1: Crystal Oscillator Circuit Frequency Range

Description	Min	Typ	Max	Units
Oscillator Circuit Frequency Range	20	27	40	MHz

The oscillation characteristics depend on the components used in the circuit (X'tal, Rf, Rd, Cg, Cd, condition of board). An example circuit and example component values are shown below.

Table 18-2: Crystal Oscillation Circuit Component

Frequency	Rf	Rd	Cg	Cd	X'tal
27MHz	1MΩ	820Ω	5.6pF	5.6pF	EPSON TOYOCOM FA-128 CL=6.4pF

Note

For optimum results, the component values used in this circuit should be evaluated for each specific application.

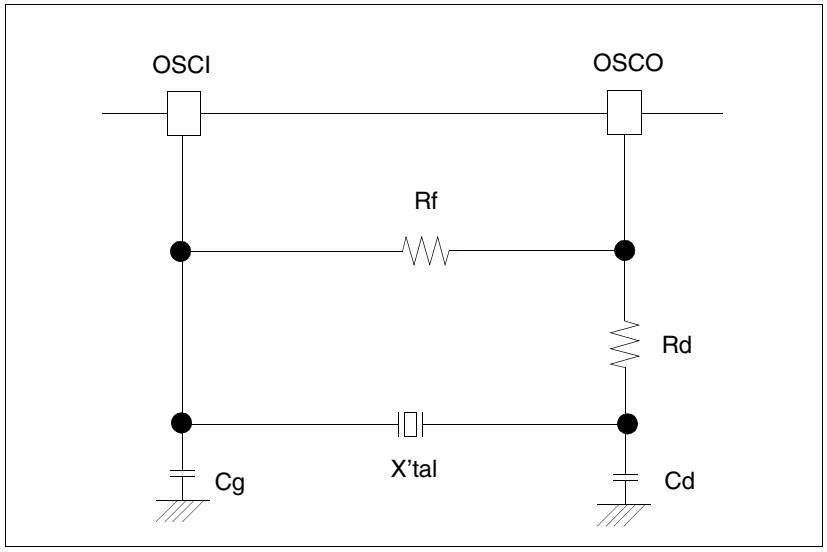


Figure 18-1: Recommended Crystal Oscillator Circuit

19 RESET# Glitch Rejection

The S1D13774 provides glitch rejection for RESET# as shown in the following figure.

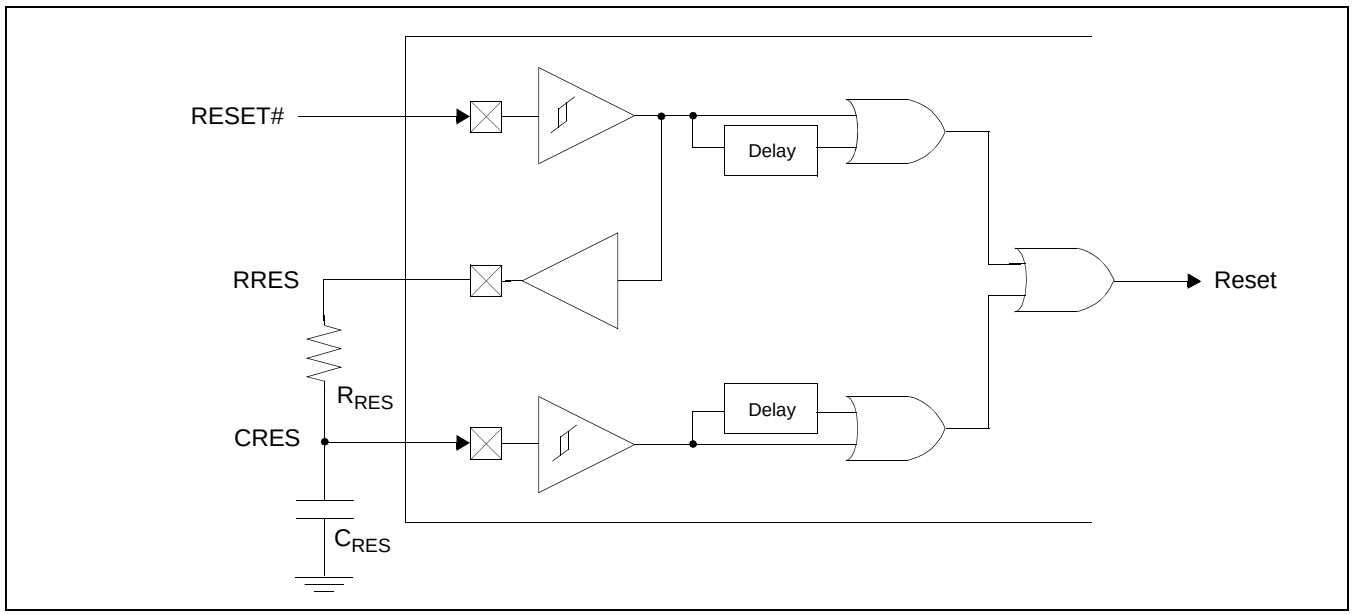


Figure 19-1: RESET# Glitch Rejection Circuit

To calculate the glitch rejection period for HIOVDD = 1.8V:

Glitch Rejection Period (µs) = 1.5 x (RRES + 200) x CRES

Where:

RRES is in Ω

CRES is in µF

To calculate the glitch rejection period for HIOVDD = 2.5V:

Glitch Rejection Period (µs) = 1.3 x (RRES + 200) x CRES

Where:

RRES is in Ω

CRES is in µF

Note

1. The above formulas are for typical conditions. The actual glitch rejection period varies based on board conditions and temperature.
2. If reset glitch rejection is not required, RRES should be left unconnected and CRES should be connected to VSS.

20 Analog Power Supply Considerations

The PLLVDD circuit is an analog circuit which is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of these circuits to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for these circuits to be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLLVDD circuit. This will result in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

20.1 Guidelines for Analog Power Layout

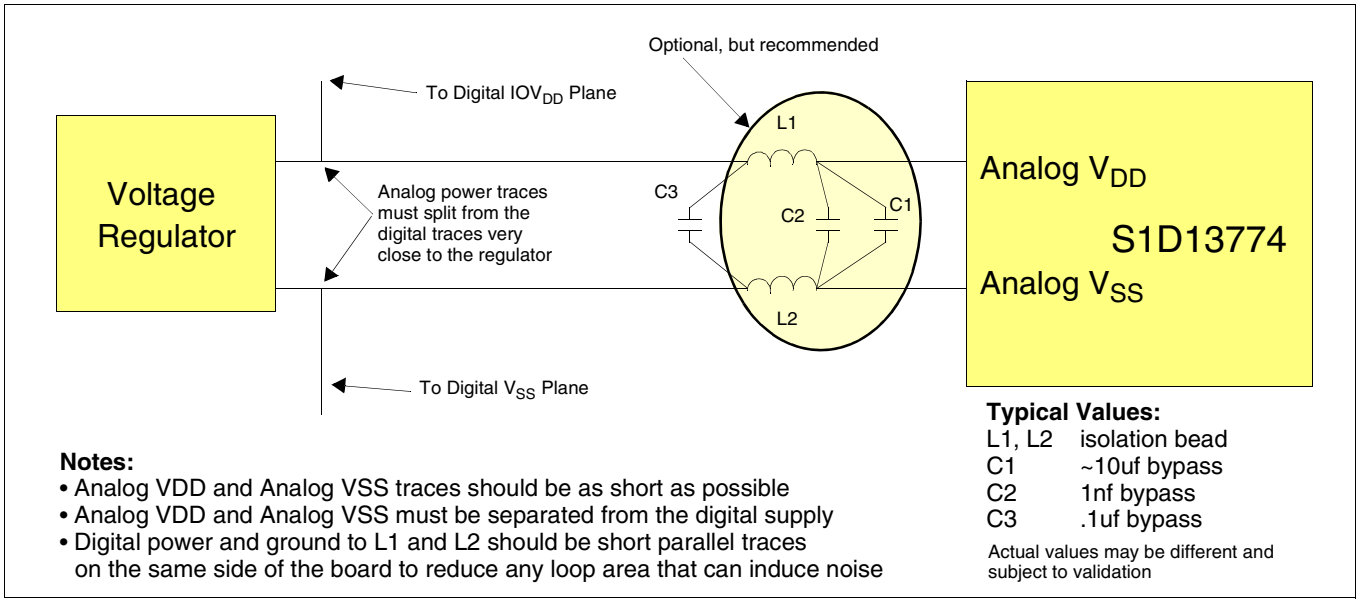


Figure 20-1: Analog Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).

- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the S1D13774 ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.
- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

21 Mechanical Data

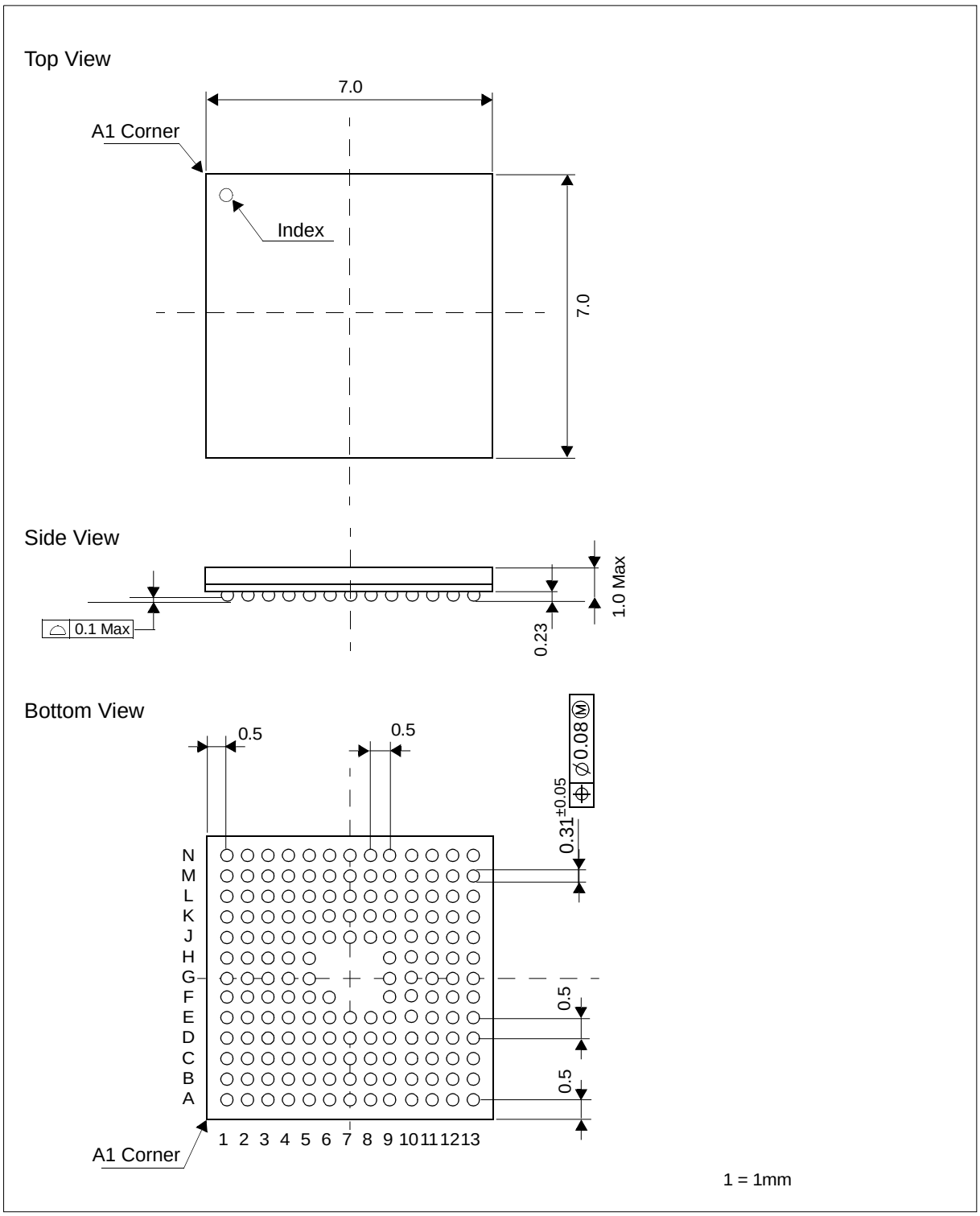


Figure 21-1: VFBGA7HX161 161-pin Package

22 References

The following documents contain additional information related to the S1D13774. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13774 Product Brief (X85A-C-001-xx)
- S5U13774A00C Evaluation Board User Manual (X85A-G-001-xx)

23 Sales and Technical Support

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23.1 Ordering Information

To order the S1D13774 LCD Controller, contact the Epson sales representative in your area.

Change Record

X85A-A-003-01 Revision 1.5 - Issued: July 2, 2008

- All changes from the previous Revision are Red
- section 6.3.1 Power-On Sequence - in table 6-5 Power-On Sequence, change the Parameters for t5 and t6
- section 6.3.2 Power-Off Sequence - in table 6-6 Power-Off Sequence, change the Parameters for t1 and t2
- section 9.3 Register Restrictions - change “All reserved bits must be set to 0b unless...” to “All reserved bits must be set to the default value unless...”
- REG[0100h] bits 4-0 - in note 1, change “<“ to “≤”
- REG[0104h] bit 7 - rewrite bit description
- REG[0188h] bits 7-5 - add note 3 “For normal operations of LCD2 frame transfer...”
- REG[059Ch] - rewrite note 1
- REG[0800h] bits 2-0 - in note 2, change “≤“ to “<”
- section 10.5 Power Save Mode Functions - in table for LCD1, LCD2 Serial Interface Pins, change FPA0 Reset State to “Forced Low”
- section 12.6.3 PIP2 Panorama Scaling Restrictions - in note 2 change “≤” to “<”
- section 12.7 Image Scrolling - add Noe 2 “When the Main1 window vertical pixel doubling...”
- section 15.2.2 Mode 2 - correct an error in figure 15-8

X85A-A-003-01 Revision 1.4 - Issued: March 26, 2008

- All changes from the previous Revision are Red
- section 3.1, for Example System Block Diagram 2 changed the FPCS2# signal from an input from SCS# to an output to SCS#
- section 3.1, for Example System Block Diagram 2 changed the LCD2 signal from “VOUT” to “VIN”
- section 3.2, removed “Direct Memory Read/Write” from the block diagram
- section 6.2.3, added PLL Output Clock Period Jitter parameter to the PLL Start-up table and added note 2
- section 7.3, reserved reference to REG[0410h]
- section 8.1, updated the CLKI frequency range in the clock diagram and clarified the clock source options for the clock tree

- REG[0190h] bits 7-0, updated the formula for the LCD2 VSYNC Position bits
- REG[0408h] ~ REG[0414h], reserved the Host Direct Memory Access registers
- REG[0520h], corrected reference to the Rotation Mode Select bits, should be bits 2-1 instead of bits 1-0
- REG[0524h], corrected reference to the Rotation Mode Select bits, should be bits 2-1 instead of bits 1-0
- REG[092Ch], replaced formula with recommended settings table
- REG[0930h], replaced formula with recommended settings table
- section 11.2.3, corrected references to the Rotation Mode Select bits, should be bits 2-1 instead of bits 1-0
- section 18, added the Oscillator frequency range

X85A-A-003-01 Revision 1.3 - Issued: March 25, 2008

- All changes from the previous Revision are Red
- administrative update - no technical changes

X85A-A-003-01 Revision 1.02 - Issued: December 11, 2007

- All changes from the previous Revision are Red
- created from X85A-A-001-01, Revision 1.02
- removed references to unavailable functions
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