

## Program Memory Lock Bits

The AT89C52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

## Lock Bit Protection Modes

| Program Lock Bits |     |     |   | Protection Type                                                                                                                                                                                                               |
|-------------------|-----|-----|---|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LB1               | LB2 | LB3 |   |                                                                                                                                                                                                                               |
| 1                 | U   | U   | U | No program lock features.                                                                                                                                                                                                     |
| 2                 | P   | U   | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled. |
| 3                 | P   | P   | U | Same as mode 2, but verify is also disabled.                                                                                                                                                                                  |
| 4                 | P   | P   | P | Same as mode 3, but external execution is also disabled.                                                                                                                                                                      |

When lock bit 1 is programmed, the logic level at the  $\overline{EA}$  pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of  $\overline{EA}$  must agree with the current logic level at that pin in order for the device to function properly.

## Programming the Flash

The AT89C52 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage ( $V_{CC}$ ) program enable signal. The Low-voltage programming mode provides a convenient way to program the AT89C52 inside the user's system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C52 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

|               | $V_{PP} = 12V$          | $V_{PP} = 5V$               |
|---------------|-------------------------|-----------------------------|
| Top-side Mark | AT89C52<br>xxxx<br>yyww | AT89C52<br>xxxx - 5<br>yyww |

|           | $V_{PP} = 12V$                               | $V_{PP} = 5V$                                |
|-----------|----------------------------------------------|----------------------------------------------|
| Signature | (030H) = 1EH<br>(031H) = 52H<br>(032H) = FFH | (030H) = 1EH<br>(031H) = 52H<br>(032H) = 05H |

The AT89C52 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

**Programming Algorithm** Before programming the AT89C52, the address, data and control signals should be set up according to the Flash programming mode table and Figure 9 and Figure 10. To program the AT89C52, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise  $\overline{EA}/V_{PP}$  to 12V for the high-voltage programming mode.
5. Pulse  $ALE/\overline{PROG}$  once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

**Data Polling** The AT89C52 features  $\overline{Data}$  Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin.  $\overline{Data}$  Polling may begin any time after a write cycle has been initiated.

**Ready/Busy** The progress of byte programming can also be monitored by the  $RDY/\overline{BSY}$  output signal. P3.4 is pulled low after  $ALE$  goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

**Program Verify** If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase** The entire Flash array is erased electrically by using the proper combination of control signals and by holding  $ALE/\overline{PROG}$  low for 10 ms. The code array is written with all 1s. The chip erase operation must be executed before the code memory can be reprogrammed.