

SANYO

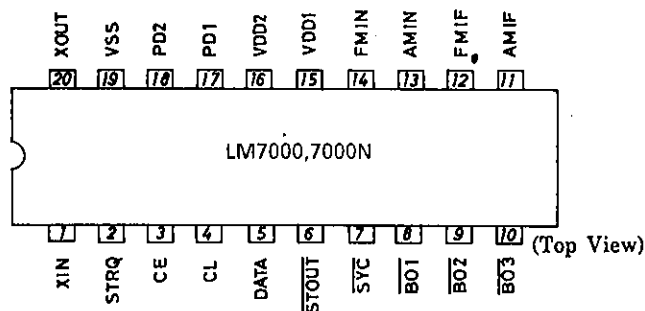
No.1434G

LM7000, 7000NDirect PLL Frequency Synthesizer
for Electronic Tuning**Features**

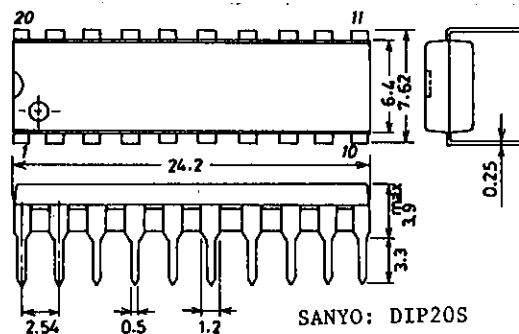
- The LM7000N is a modified version of the LM7000 whose phase comparator dead zone is changed.
- High-speed programmable divider capable of direct dividing FM band VCO frequency.
- Reference frequency (7 kinds) : 100,50,25,10,9,5,1kHz
- Output for band select (3 bits)
- Clock output for controller (400kHz)
- Time base output for clock (8Hz)
- Data input : Serial input (CE,CL,DATA pins)
- On-chip IF count circuit : FM : $\pm 10\text{kHz}$
MW, SW : $\pm 3\text{kHz}$
LW : $\pm 0.6\text{kHz}$

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

				unit
Maximum Supply Voltage	$V_{DD} \text{ max}$	V_{DD1}, V_{DD2}	-0.3 to +7.0	V
Maximum Input Voltage	$V_{IN1} \text{ max}$	CE, CL, DATA, STRQ	-0.3 to +7.0	V
	$V_{IN2} \text{ max}$	Input pins other than V_{IN1}	-0.3 to $V_{DD} + 0.3$	V
Maximum Output Voltage	$V_{OUT1} \text{ max}$	SYN, STOUT	-0.3 to +7.0	V
	$V_{OUT2} \text{ max}$	BO1, BO2, BO3	-0.3 to +13	V
	$V_{OUT3} \text{ max}$	Output pins other than $V_{OUT1,2}$	-0.3 to $V_{DD} + 0.3$	V
Allowable Power Dissipation	$P_d \text{ max}$	$T_a = 85^\circ\text{C}$	300	mW
Operating Temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

Pin Assignment**Package Dimensions 3021B**

(unit : mm)

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

D1593MO, O2693JN/6018TA/5155KI/3104/2244 /9303KI, TS No.1434-1/7

LM7000,7000N

Allowable Operating Conditions at Ta = -40 to +85°C, VSS = 0V

				unit
Supply Voltage	VDD1	VDD1, PLL operation	4.5 to 6.5	V
	VDD2	VDD2, Xtal OSC time base	3.5 to 6.5	V
Input 'H'-Level Voltage	VIH	CE, CL, DATA, STRQ	2.2 to 6.5	V
Input 'L'-Level Voltage	VIL	CE, CL, DATA, STRQ	0 to 0.7	V
Output Voltage	VOUT1	SYC, STOUT	0 to 6.5	V
	VOUT2	BO1, BO2, BO3	0 to 13	V
Output Current	IOUT	BO1, BO2, BO3, VDD = 4.5 to 6.5V	0 to 3.0	mA
Input Frequency	fin1	XIN, sine wave, capacitive coupling	1.0 to 7.2typ to 8.0	MHz
	fin2	FMIN, " (Note 1), *(S=1)	45 to 130	MHz
	fin3	FMIN, " (Note 2), *(S=1)	5 to 30	MHz
	fin4	AMIN, " *(S=0)	0.5 to 10	MHz
	fin5	FMIF, "	10.0 to 10.7typ to 11.5	MHz
	fin6	AMIF, "	400 to 450typ to 500	kHz
Oscillation-Guaranteed Crystal Resonator	Xtal	XIN-XOUT, CI ≤ 30Ω	5.0 to 7.2typ to 8.0	MHz
Input Amplitude	Vin1	XIN, sine wave, capacitive coupling	0.5 to 1.5	Vrms
	Vin2	FMIN, "	0.1 to 1.5	Vrms
	Vin3	AMIN, "	0.1 to 1.5	Vrms
	Vin4	FMIF, "	0.1 to 1.5	Vrms
	Vin5	AMIF, "	0.1 to 1.5	Vrms

*: 'S': Control bit in serial data

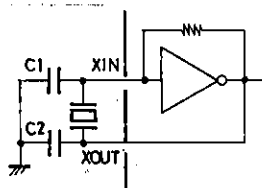
(Note 1): fref = 100, 50, 25kHz (Note 2): Reference frequency other than fref = (Note 1)

Electrical Characteristics / Under allowable operating conditions

			min	typ	max	unit
On-chip Feedback Resistance	Rf1	XIN		1.0		MΩ
	Rf2	FMIN		0.5		MΩ
	Rf3	AMIN		0.5		MΩ
	Rf4	FMIF		0.5		MΩ
	Rf5	AMIF		0.5		MΩ
Input 'H'-Level Current	IIH	CE, CL, DATA, STRQ			5.0	μA
Input 'L'-Level Current	IIL	CE, CL, DATA, STRQ			5.0	μA
Output 'L'-Level Voltage	VOL1	FMIF, AMIF, FMIN, AMIN			3.5	V
	VOL2	SYC			0.3	V
Output Off Leak Current	Ioff1	SYC			5.0	μA
Output 'L'-Level Voltage	VOL3	STOUT			1.0	V
Output Off Leak Current	Ioff2	STOUT			5.0	μA
Output 'L'-Level Voltage	VOL4	BO1 to 3			1.0	V
Output Off Leak Current	Ioff3	BO1 to 3			3.0	μA
Output 'H'-Level Voltage	VOH1	PD1,2			0.5VDD	V
Output 'L'-Level Voltage	VOL5	PD1,2			0.3	V
'H'-Level Tri-state Off Leak Current	IoffH	PD1,2			0.01	nA
'L'-Level Tri-state Off Leak Current	IoffL	PD1,2			0.01	nA
Supply Voltage	IDD1	VDD1 + VDD2			25	mA
	IDD2	VDD2			2.0	mA
Input Capacitance	cin	FMIN			1	pF

(Note 3) VDD = 3.5 to 6.5V

(Note 4) 7.2MHz Xtal connected across XIN and XOUT



fin2 = 130MHz
VIN2 = 100mVrms
Other input pins = VSS
Output pins = Open

Kinseki Co., Ltd

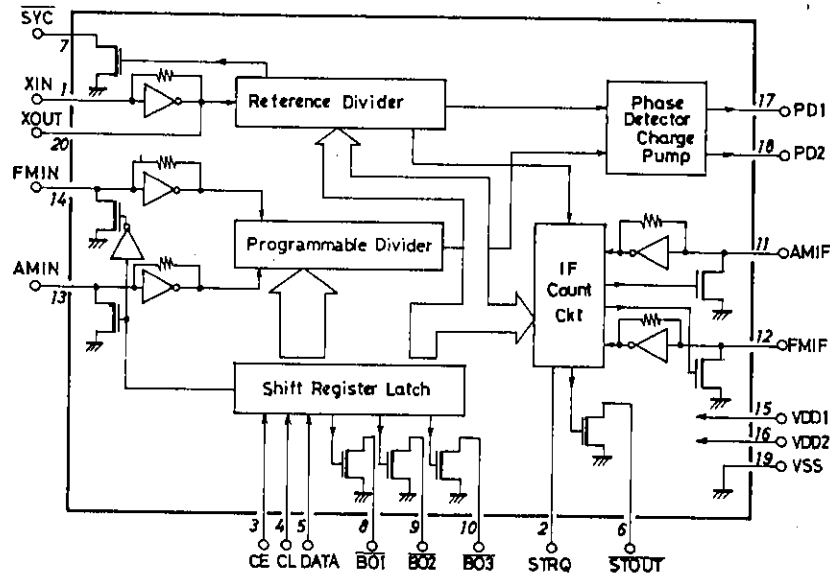
HC43/U: 2114-84521 (1) : CL=10pF C1=15 (10 to 22)pF C2=15pF

HC43/U: 2114-84521 (2) : CL=16pF C1=22 (15 to 33)pF C2=33pF

Nihon Denpa Kogyo Co., Ltd

NR-18: LM-X-0701 : CL=10pF C1=15pF C2=15pF

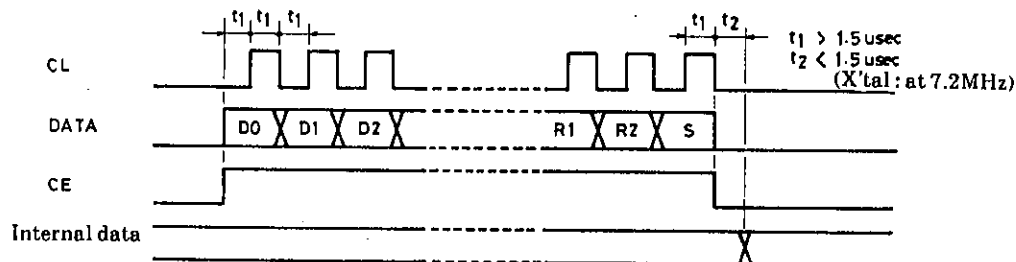
Equivalent Circuit Block Diagram



Pin Description

SYC	: Controller clock (400kHz)
XIN,XOUT	: Xtal OSC (7.2MHz), on-chip feedback resistor
FMIN,AMIN	: Local oscillation signal input
CE,CL,DATA	: Data input
BO1,BO2,BO3	: Band data output, $\overline{BO1}$ can be also used for time base output (8Hz)
STRQ	: IF count request input
STOUT	: Auto search stop signal output
VDD1,VDD2,VSS	: Power supply (V_{DD2} is for backup)
AMIF,FMIF	: IF signal input
PD1,PD2	: Charge pump output

Data Input



← Inputting starts at D0.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	T0	T1	B0	B1	B2	TB	R0	R1	R2	S
----	----	----	----	----	----	----	----	----	----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	---

(1) D0 (LSB) to D13 (MSB) : Division ratio data

For FMIN, use D0 to D13; for AMIN, use D4 to D13.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
----	----	----	----	----	----	----	----	----	----	-----	-----	-----	-----

1	1	1	1	0	1	1	1	1	1	0	0	0	0	MSB	→ FMIN division ratio = 1007
LSB	X	X	X	X	1	0	0	0	1	0	0	1	0	MSB	→ AMIN division ratio = 145
				LSB											

Continued on next page.

Continued from preceding page.

Example

① FM 100kHz Step ($f_{ref}=100\text{kHz}$)

FM VCO = 100.7MHz (FM RF = 90.0MHz, IF = +10.7MHz)

Division Ratio = 100.7MHz (FM VCO) $\div$ 100kHz(f_{ref}) = 1007 $\rightarrow$ 3EF_(HEX)② AM 10kHz Step ($f_{ref}=10\text{kHz}$)

AM VCO = 1450kHz (AM RF = 1000kHz, IF = +450kHz)

Division Ratio = 1450kHz (AM VCO) $\div$ 10kHz (f_{ref}) = 145 $\rightarrow$ 91_(HEX)

(2) T0, T1 : For LSI test (0, 0)

(3) B0 to B2, TB : Band data
: Time base data

Input				Output		
B0	B1	B2	TB	BO1	BO2	BO3
0	0	0	0	*	*	*
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	*	*
×	1	0	1	TB	1	0
×	0	1	1	TB	0	1
×	1	1	1	TB	1	1
1	0	0	1	TB	0	0

* : Determined by R0 to R2

× : Don't care

TB : 8Hz

(4) R0 to R2 : Reference frequency data

R0	R1	R2	fref	BO1	BO2	BO3	IF Count
0	0	0	100 kHz	1	1	0	10.7MHz $\pm$ 10kHz
0	0	1	50	1	1	0	
0	1	0	25	1	1	0	
0	1	1	5	0	0	1	450kHz $\pm$ 3 kHz
1	0	0	10	1	0	1	
1	0	1	9	1	0	1	
1	1	0	1	0	1	1	450kHz $\pm$ 0.6kHz
1	1	1	5	0	0	1	450kHz $\pm$ 3 kHz

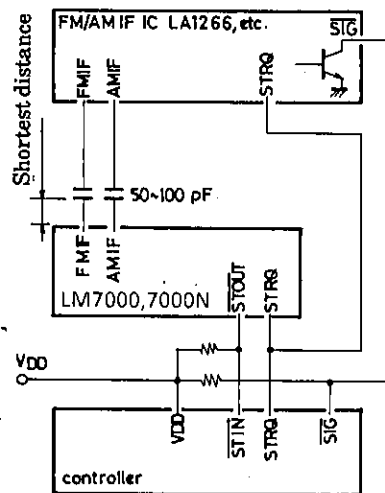
(Note) B0 to B2 = 0

(5) S : Divider select data

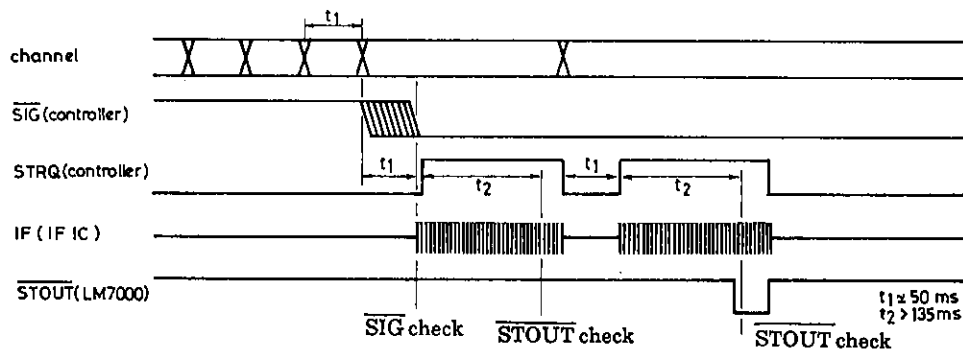
'1' : FMIN, '0' : AMIN

LM7000,7000N

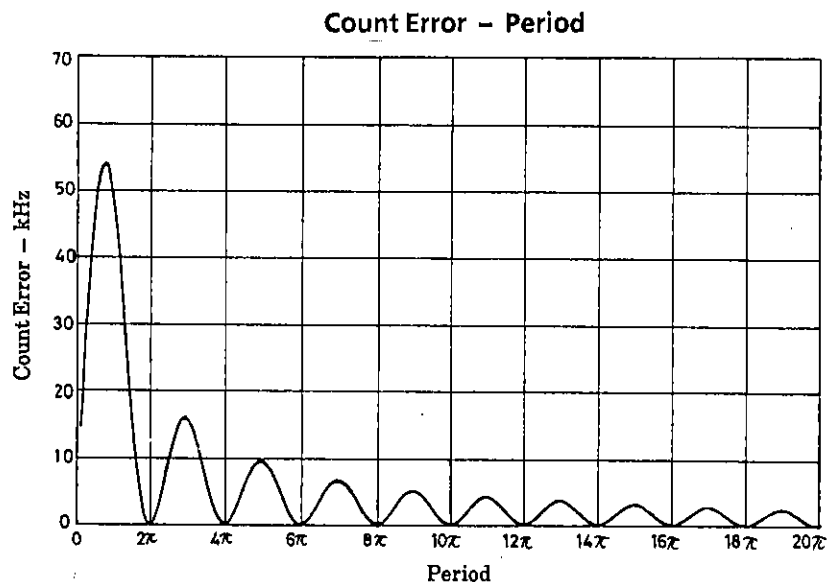
IF Count Circuit : Circuit to stop auto tuning



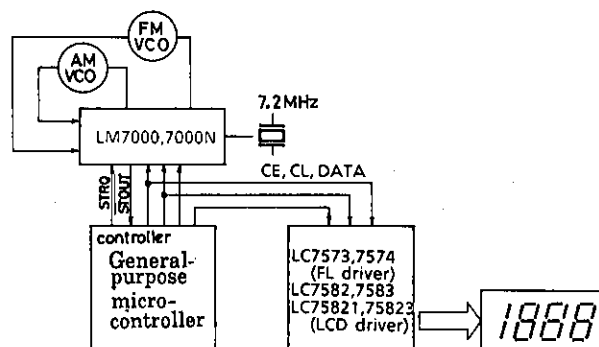
- When in the neighborhood of a broadcasting station, "SIG" signal is output, setting $\overline{\text{SIG}}$ of the controller to "0".
- "STRQ" signal is applied to the LM7000 and IF IC from the controller.
- IF signal is applied to the LM7000 from the IF IC and the LM7000 counts this signal.
- When a specified count value is reached, "STOUT" signal is applied to the controller from the LM7000, stopping auto tuning.



- Counting is performed only at "STRQ" = 1.
- The count time is 120msec.
- For FM, the count error is shown below.
(Example : For 50Hz-100% modulation, the maximum count error is 5kHz.)

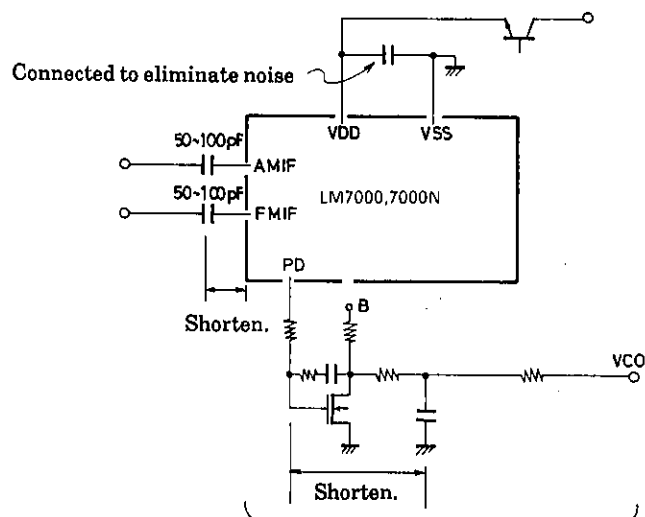


Sample Connection to Controller



Notes for Using PLL IC

(1) The layout nearby PLL-IC.



Surround this section with the ground pattern, because it is in a high impedance state and is very susceptible to noise.

(2) State of output ports ($\overline{BO1}$ to $\overline{BO3}$) at power-on.

The output ports are undefined until the control data is transmitted.

The $\overline{BO1}$ and $\overline{BO3}$ ports may output a internal clock of PLL-IC, and so don't forget to transmitte of control data after power-on.

The control data should be input only after X'tal OSC have become stable.

(3) VCO design.

At design of the VCO, try to do not stop oscillation no matter what Tuning Voltage(V_{tune}) is 0 Volt.

When the VCO oscillation stops, the PLL is possible to become a dead -lock condition.

Differences Between the LM7000 and LM7000N

The only difference between LM7000 and LM7000N is the phase detector dead zone. Otherwise, they are identical.

Continued on next page.

Continued from preceding page.

Dead Zone

The phase detector shown in figure 1 compares the reference frequency (f_r) with f_p . The characteristics of the phase detector are shown in figure 2. A phase detector ideally should output a voltage proportional to the phase difference (ϕ) as shown by curve (A), but in reality, delays in the internal circuitry mean that small phase differences cannot be detected. This causes the dead zone shown by curve (B). To realize a large signal-to-noise ratio, this dead zone should be made as small as possible.

Standard models, however, can have a rather wide dead zone. When there is a strong RF input signal, with these models, the VCO can be modulated to compensate for part of the RF signal being leak to the VCO from the MIX. In the case of dead zone is small, the VCO output is modulated and a beat between the RF and VCO is created.

Figure 1

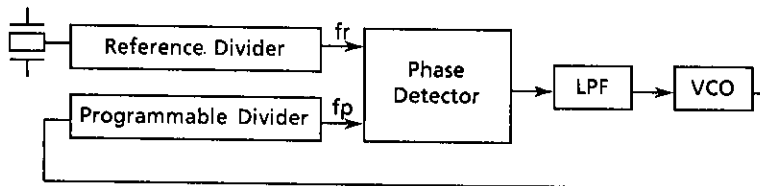
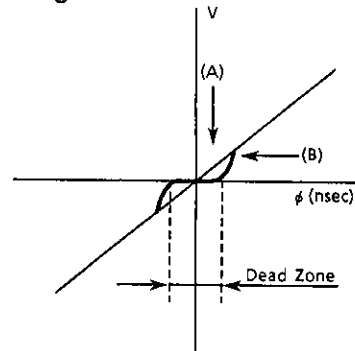


Figure 2



LM7000/LM7000N

Because of the above reasons, the LM7000 and LM7000N were developed with different dead zones.

LM7000 : Dead zone ≈ 0 ns, S/N is 90 to 100 dB or greater

LM7000N : Dead zone ≈ 5 to 10 ns, for standard models

Note

If the LM7000N is used in a circuit designed for the LM7000, the S/N ratio will decrease.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.