A BiCMOS Time-to-Digital Converter with Time Stretching Interpolators

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Abstract - A time-to-digital converter (TDC) capable to measure time intervals over a range of several microseconds with an accuracy of 100 - 200 ps has been designed. The TDC has been fabricated in a 1.2 um BiCMOS process and according to preliminary test results the single-shot resolution is better than 200 ps and the nonlinearity is less than 150 ps when input time intervals range from 2.5 to 2500 ns.

1. Introduction

Time-to-digital converters are used in applications such as laser range-finding, test equipment for electronic system characterization and instrumentation for particle physics experiments. The TDC presented here is designed for a portable laser range-finder and a measurement accuracy of 100 ps over a range of several microseconds is aimed at. To achieve this goal with low power consumption the method of Fig. 1 is used. The time interval to be measured is digitized in three parts. The main part T12 is synchronous with respect to the system clock and can therefore be digitized with the clock and a counter. The non-synchronous parts T1 and T2 are digitized separately with interpolators. Thus, the measurement range is set by the number of bits in the counter and limited only by the stability of the system clock. The LSB width of the TDC is determined by the properties of the interpolators at the specified clock frequency.

One practical interpolator structure is a delay line [1], [2]. Digital CMOS delay lines are simple to implement, have a low power consumption and can be easily stabilized over a large temperature range with a delay-locked loop. However, in long delay lines process gradients cause systematic

delay variation which increases the width of the distribution of single-shot results and thus limits the achievable precision. Also, in a CMOS time-to-digital converter the overall accuracy tends to suffer from jitter and supply and temperature sensitivity of CMOS logic as well as from crosstalk between the interpolators. Another approach is to use time-to-voltage converters, where a capacitor is discharged with a constant current during the time interval being measured [3] - [5]. Here we present an interpolating time-to-digital converter, where interpolators are based on time-to-voltage conversion and bipolar logic is used to reduce timing uncertainties in logic.

2. Circuit realization

In the control block of the TDC (Fig. 1) an erraneous measurement is possible due to excess delay in the flip-flop D2a (D2b) in case a start (stop) -pulse occurs near the rising clock edge. To reduce this possibility, the end mark of T1 (T2) is taken not from the first but from the second clock pulse following start (stop). Thus, if the flip-flop D2a (D2b) settles in less time than one clock period, the measurement is not affected. However, the linear measurement range required of the interpolators is doubled from Tclk to 2*Tclk, where Tclk is the period of the system clock. The control logic is implemented with ECL-type current steering structures to minimize jitter, crosstalk and temperature sensitivity.

The interpolator principle is based on the dual slope converter, where a capacitor is first discharged with a constant current (I) during the input time interval (tin) and then charged back with a smaller current (I/N). During the charging time (N*tin) clock pulses are counted, which gives a measurement resolution equal to the case where tin would be directly digitized with an N times higher clock frequency. However, a large stretch factor N requires a large current ratio which at some point becomes unfeasible. Here the stretch factor is implemented as a combination of a current ratio and a capacitor ratio (Fig. 2). At the beginning of the measurement the voltages of the capacitors C1 and C2 are reset and equal. During the interpolator input time interval the smaller capacitor C1 is discharged with a constant current I1. Next, the larger capacitor C2=M*C1 is discharged with a smaller current I2=I1/N until the voltages of the capacitors are again equal. At this point the comparator, which was enabled at the beginning of the second discharging, changes state and the counting of clock pulses stops. Thus, the time stretch factor is N*M. Compared with the dual slope converter a larger dynamic range might also be achievable since there is no need for the charging current source and, additionally, the nonlinearities of the two discharging events may to some extent cancel out. With the interpolator of Fig. 2 the LSB width of the TDC is Tclk/(M*N). In the prototype TDC Tclk=20ns, C1=5 pF, C2=40 pF and the currents are adjustable.

The comparator consists of three bipolar differential pairs buffered with emitter followers. The input of the comparator is buffered with MOS source followers, since the leakage of the capacitor charge due to bipolar base current is unacceptable. Interleaved layout of the MOS transistors is used to minimize the offset of the comparators. A difference between the comparators' offsets causes a constant difference between the interpolator results which can be compensated in the

calculation of the final result. The enable/disable operation is performed in the second stage.

In this prototype the counters are off-chip. The three clocks gated by T1, T2 and T12 are buffered with emitter followers and amplified outside the chip to CMOS levels.

3. Experimental results

The prototype chips were fabricated in a 1.2 um BiCMOS process. The size of the circuit is 3 mm * 3 mm.

The clock frequency in the test system is 50 MHz. With the nominal capacitor ratio of 40pF/5pF=8 and a current ratio of 32 an 8 bit resolution of 20ns/256=78ps is aimed at. In both interpolators the discharging current I1 was set to approximately 200 uA and the current I2 was adjusted until the stretch factor of 256 was achieved. An example of the distribution of digitized T1 is shown in Fig. 3a. The width of the distribution is equal to the stretch factor of 256. In an ideal case the starting point of the non-zero distribution is 256 but in practice it depends on several offset components including the offset of the comparator. These results were collected from asynchronous time measurements i.e. the distribution should be uniform, so deviations from the average value indicate differential nonlinearity of the respective interpolator.

The single-shot resolution of the TDC was measured as the σ–value of the distribution of single-shot measurements (Fig. 3b). The measured value was less than 150 ps for input time intervals up to 500 ns and less than 200 ps for input time intervals up to 2500 ns. The nonlinearity of the TDC was 150 ps for input time intervals from 2.5 ns to 2500 ns as shown in Fig. 4.

4. Discussion

The preliminary measurement results show that an accuracy of 100 ps is achievable in a range of several microseconds. With a single-shot resolution of 200 ps an average of 20 samples improves the σ to 50 ps. However, the input parameters used in the measurements are not yet optimized, e.g. the nominal dynamic range of the time-to-voltage conversion is now only 1.6V with 5V supply. A larger dynamic range improves the noise margins which might improve the single-shot resolution since the deterioration of the resolution with longer input time intervals seems to indicate some input-dependable interaction between the two interpolators and the main clock gated by T12.

References:

[1] Y. Arai, T. Matsumura, K. Endo, "A CMOS four-channel x 1K time memory LSI with 1-ns/b resolution", IEEE J. Solid-State Circuits, vol. sc-27, pp. 359-364, March 1992.

[2] E. Räisänen-Ruotsalainen, T. Rahkonen, J. Kostamovaara, "A Low-Power CMOS Time-to-Digital Converter", IEEE J. Solid-State Circuits, vol. sc-30, pp. 984-990, Sept. 1995.

[3] J. Kostamovaara, R. Myllylä, "Time-to-digital converter with an analog interpolation circuit", Rev. Sci. Instrum. vol. 57, pp. 2880-2885, Nov. 1986.

[4] A. Stevens, R. Van Berg, J. Van der Spiegel, H. Williams, "A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors", IEEE J. Solid-State Circuits, vol. sc-24, pp. 1748-1752, Dec. 1989.

[5] E. Gerds, J. Van der Spiegel, R. Van Berg, H. Williams, L. Callewaert, W. Eyckmans, W. Sansen, "A CMOS Time to Digital Converter IC with 2 Level Analog CAM", IEEE J. Solid-State Circuits, vol. sc-29, pp. 1068-1076, Sept. 1994.

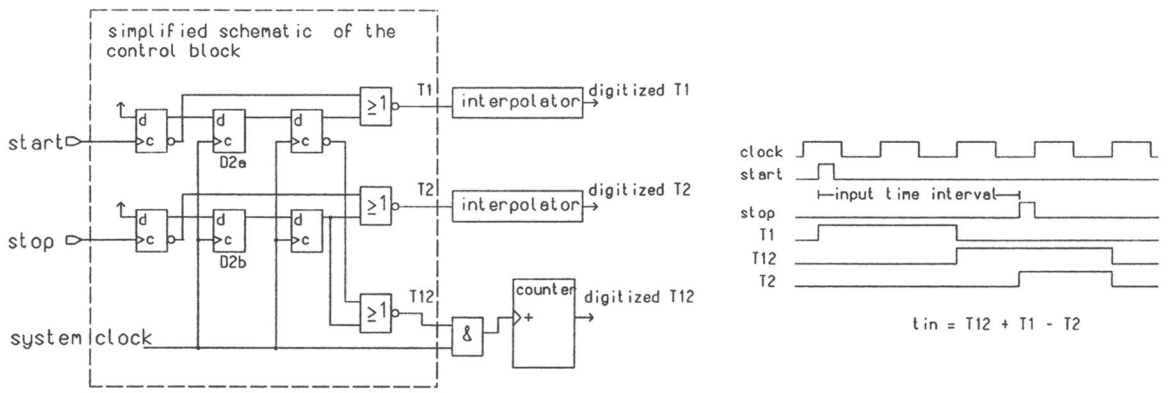

Fig. 1. Block diagram and operating principle of the TDC.

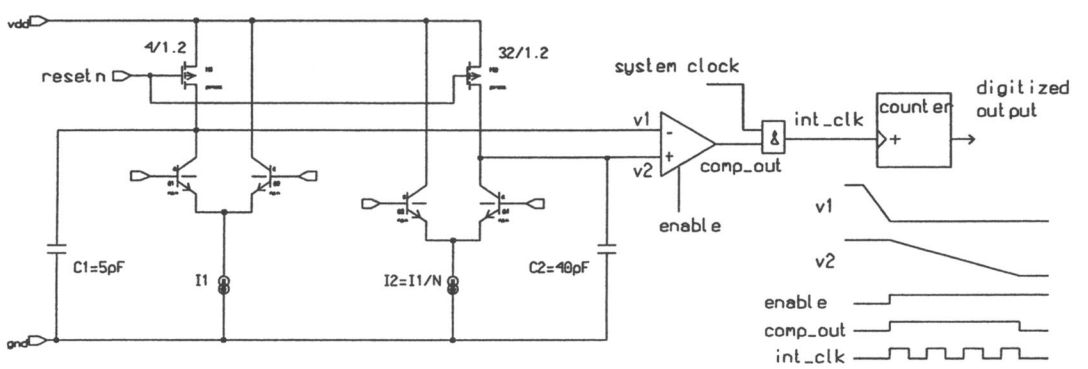

Fig. 2. Principle of the time stretching interpolator.

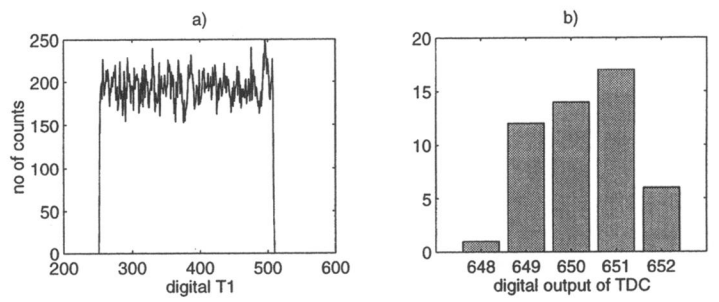

Fig. 3. a) Measured distribution of the results of one interpolator when the stretch factor is 256. b) Distribution of single-shot measurement results of the TDC with an input time interval 50 ns.

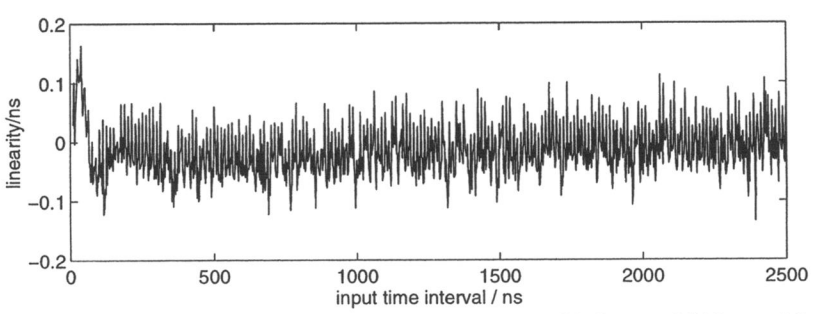

Fig. 4. Measured linearity of the TDC over an input time interval range of 2.5 ns to 2500 ns with an increment of 2.5 ns. Each point corresponds to an average of 50 single-shot measurements.