An Integrated Time-to-Digital Converter with 30-ps Single-Shot Precision

Elvi Räisänen-Ruotsalainen, Timo Rahkonen, and Juha Kostamovaara

***Abstract*—A time-to-digital converter (TDC) with 32-ps resolution and 2.5-μs measurement range has been integrated in a 0.8-μm BiCMOS process. The TDC is based on a counter with a 100-MHz clock. Two separate time digitizers improve the time resolution by interpolating within the clock period. These interpolators are based on analog dual-slope conversion. According to test results, the single-shot precision of the TDC is better than 30 ps (σ-value) and the nonlinearity is less than $\pm$5 ps when input time intervals range from 10 ns to 2.5 μs. The conversion time is $\leq$6.3 μs. Temperature drift, excluding the temperature dependence of the oscillator, is below $\pm$40 ps in the temperature range of -40 to 60 °C. The size of this chip, including pads, is 3.5×3.4 mm^2 and its power consumption is 350 mW.**

***Index Terms*—Laser radar, time measurement, time-of-flight, time-to-digital converter, time-to-voltage.**

I. Introduction

A time-to-digital converter (TDC) is one of the critical components of a pulsed time-of-flight laser radar in which the distance measurement is based on the measurement of the transit time of a short laser pulse to an optically visible target and back to the receiver. The goal of this work was to develop an integrated time-to-digital converter which would enable the realization of an integrated laser radar with millimeter-level distance measurement accuracy (1 mm corresponds to 6.7 ps in time measurement). A prototype integrated laser radar with centimeter-level accuracy has already been implemented [1].

Typical industrial applications for laser radars are, for example, the measurement of level height in silos, positioning of tools and vehicles, velocity measurement, anticollision radars, and proximity sensors [2]–[4]. Other application areas for TDCs are high-energy physics [5], [6], calibration of automatic test equipment systems [7], and telecommunications applications such as the FM demodulator described in [8].

II. Implementation of the Time-to-Digital Converter

The operating principle of the TDC is shown in Fig. 1 [9]. The time interval $T_{\rm in}$ from the rising edge of the start pulse to the rising edge of the stop pulse is digitized in three parts. The main part $T12$ is synchronous with respect to the system clock and can be digitized by counting clock pulses with period $T_{\rm clk}$. With a counter and a 100-MHz clock, a resolution of 10 ns is achieved. The resolution is improved by digitizing the fractional parts $T1$ and $T2$ separately with n-bit interpolators. The theoretical worst-case single-shot precision of the TDC in asynchronous measurement is $0.5T_{\rm clk}/2^n$. In practice, the single-shot precision is often limited by the gain error and the nonlinearity of the interpolators. These errors result in a periodic single-shot error which depends on the input interval [10].

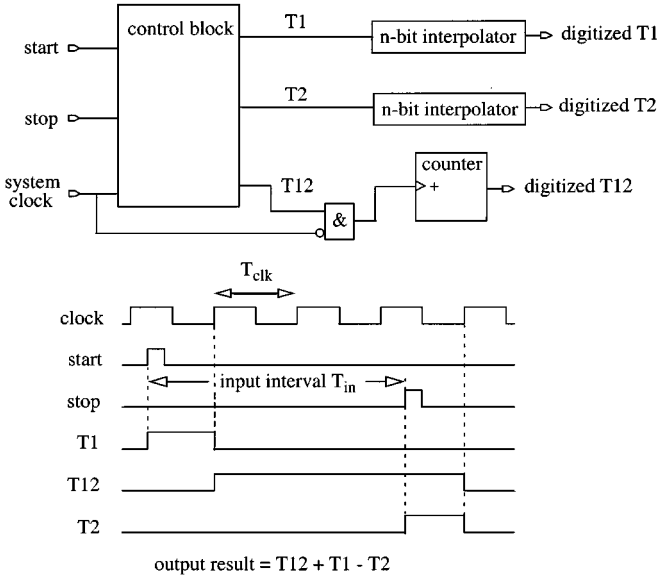

Fig. 1. Block diagram and operating principle of the TDC.

The linearity of this TDC is basically as good as that of the counting method. Although the gain error or nonlinearity of the interpolators decreases single-shot precision from the theoretical value, for averaged results their effect is merely a constant bias error independent of the time to be measured, and can be subtracted from the final result [10]. The stability error of the TDC can be divided into two components. The first is an offset drift component which is independent of the input time interval. It results, for example, from the temperature dependence of the random mismatch between start and stop signal paths in the control block or between the interpolators. The second error component is a gain error, which is dependent on the input interval and arises from the temperature or time dependence of the reference oscillator.

It can be concluded that the nonidealities of the interpolators to a large extent cancel out in averaged results. To minimize the errors, the start and stop signal paths in the control logic and interpolators need to be matched carefully.

A. Input Synchronization

In the actual implementation, the time intervals $T1$, $T2$, and $T12$ are generated as shown in Fig. 2. In this case, $T1$ and $T2$ are measured to the second, and not to the first clock pulse following the start/stop input. In asynchronous measurement the timing pulses arrive at a random phase with respect to the reference clock. Thus, when the setup time requirement of flip-flop $D2a$, for example, is not fulfilled, the propagation delay of that

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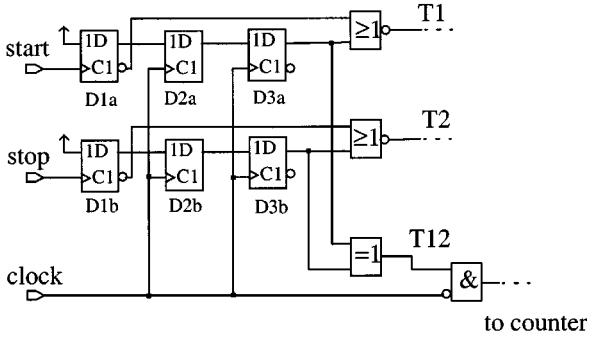

Fig. 2. Synchronization of start and stop inputs.

flip-flop will increase and in an extreme case the flip-flop will enter a metastable state. The probability of metastability is low, but even a small increase in the delay causes an error in $T1$ and thus in the final measurement result, as well. The probability of a synchronization error is effectively reduced by waiting before sampling the output of flip-flop $D2a$ with the flip-flop $D3a$ [11], [12]. As long as $D2a$ settles in one clock period, the measurement result will be correct since $T12$ is adapted according to the value of $T1$. The drawback of the three-flip-flop scheme is that the linear measurement range required of the interpolators increases as now the measured time intervals range from $T_{\rm clk}$ to $2T_{\rm clk}$. Ideally, the range from 0 to $T_{\rm clk}$ appears as a constant offset in the measurement results.

B. Analog Interpolator

The interpolators are based on dual-slope conversion, where the input interval $t_{\rm in}$ is stretched with a factor of $M \cdot N$ and clock pulses are counted during this time. This gives a measurement resolution equal to the case in which $t_{\rm in}$ is directly digitized with a clock frequency $M \cdot N$ times higher. The stretch factor is implemented as a product of a current ratio and a capacitor ratio. The principle of the interpolator is shown in Fig. 3. At the beginning of the measurement, the voltages of the capacitors $C1$ and $C2$ are reset and equal. During the interpolator input time interval, the smaller capacitor $C1$ is discharged with a constant current $I1$. Next, the larger capacitor $C2 = M \cdot C1$ is discharged with a smaller current $I2 = I1/N$ until the voltages of the capacitors are equal again. At this point, the comparator which was enabled at the beginning of the second discharging changes its state and the counting of clock pulses stops. The stretch factor is thus $M \cdot N$ and the LSB width of the TDC is $T_{\rm clk}/(M \cdot N)$. The output result of the TDC is now $t_{\rm in} = N_c T_{\rm clk} + (N_1 - N_2)T_{\rm clk}/(M \cdot N)$ where N_c, N_1, and N_2 are the outputs of the main counter, start interpolator counter, and stop interpolator counter, respectively.

The analog interpolators can be calibrated by two calibration pulses generated on-chip. The first one is equal to the minimum input interval of the interpolators, i.e., one clock period, and the second is equal to the maximum input interval of two clock periods. From the interpolator output values for these calibration pulses, the offset and gain of the interpolators can be determined and used when calculating measurement results. Another method to determine the offset and gain of the interpolators is to calculate them from the interpolator output result distributions collected from measurements. This procedure is much slower than the calibration with two pulses, since a large number of results need to be collected, but it is inherently accurate. Thus, the calibration with two pulses can be used for determining the interpolator parameters after start-up, and the calibration based on the distributions can be used, after the number of measurement results is adequate, to gain more accurate results.

III. Measured Performance

The prototype TDC was integrated in a 0.8-μm BiCMOS process. In addition to the main TDC and calibration functions the circuit includes some test logic to detect, for example, the functionality of the counters, digital logic for the interface to the laser radar system, and biasing circuitry. The only external component is a 100-MHz (P)ECL oscillator. All critical parts of the TDC were implemented with emitter-coupled logic/current-mode logic (ECL/CML)-type current steering structures, which reduces crosstalk between the start and stop channels but increases power consumption.

The size of the circuit is 3.5 $\times$ 3.4 mm^2 and it has a power consumption of 350 mW. With a 100-MHz clock, $C1 = 7$ pF, $C2 = 56$ pF, $I1 = 800$ μA, and $I2 = 20$ μA. The nominal stretch factor is 320 and the LSB of the TDC is 32 ps. The worst-case conversion time (from the arrival of the stop mark) is $320 \cdot 2T_{\rm clk} = 320 \cdot 20$ ns ≈ 6.4 μs. Since the measurement rate of the laser radar is limited to a few tens of kiloHertz, the conversion time of the TDC does not limit the performance of the system.

A. Single-Shot Precision

To measure the single-shot precision of the TDC, a single output pulse was taken from a pulse generator and split into two pulses with a power splitter. One pulse was fed directly into the start input of the TDC while the other pulse was first delayed in a coaxial cable and then fed into the stop input. Thus, a constant and nearly jitter-free input time interval was created. The single-shot precision of the TDC for this input time interval was calculated as the standard deviation σ of the distribution of 1000 measurement results. Since the precision depends on the input time interval, the input time was swept over the clock period with a 2-ns increment. The measured single-shot precision of the TDC is shown in Fig. 4. In Fig. 4(a), an average stretch factor of $K_{\rm av} = 310$ was used when calculating the results, while the real stretch factors varied from chip to chip in the range of 306–316 ($\pm$1.5%). The effect of interpolator gain error (which can be considered a special case of nonlinearity) on the precision of the TDC can clearly be seen. When the real stretch factors (K_1 and K_2) were used to calculate the measurement results, as would be the case in a real measurement situation, the single-shot precision was better than 30 ps [Fig. 4(b)].

B. Linearity

The linearity of the available pulse generators was not adequate to measure the linearity of the prototype TDC. This is why a reference TDC was used in parallel with the prototype TDC and the results of the two TDCs were then compared to compensate the errors from the pulse generator. The reference TDC

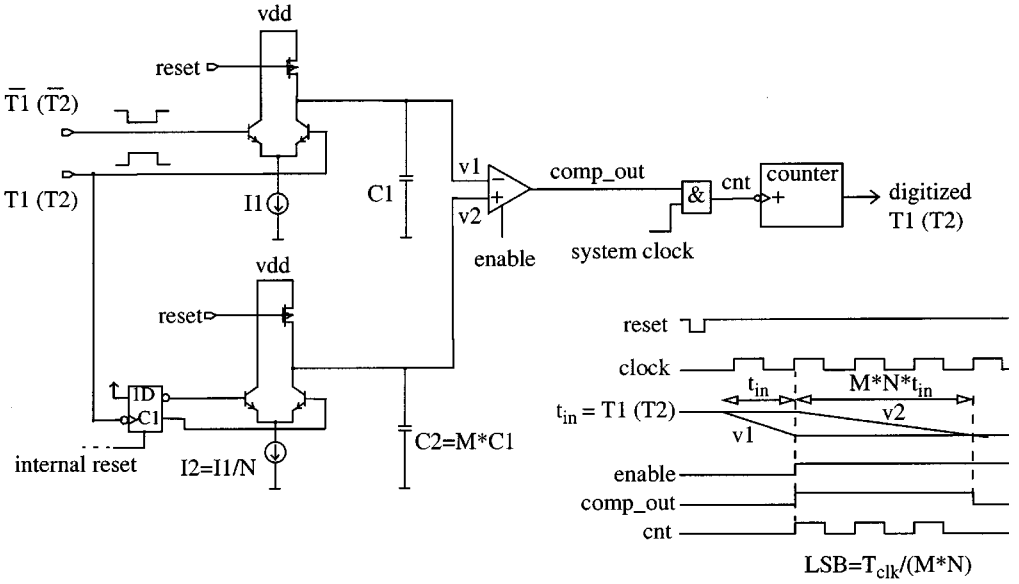

Fig. 3. Principle of the interpolator based on time-to-voltage conversion.

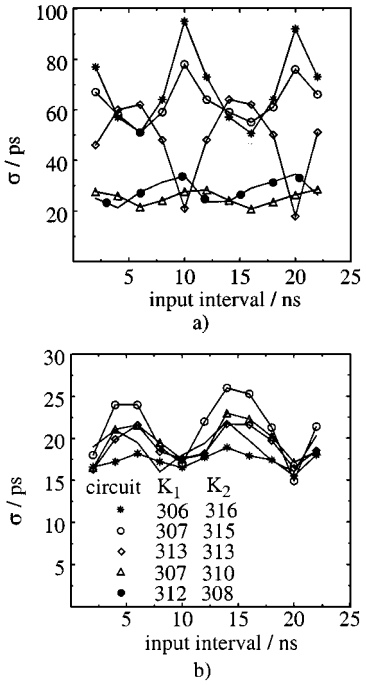

Fig. 4. Single-shot precision of TDC for five circuits. (a) Results calculated with the average stretch factor. (b) Results calculated with the real stretch factors K_1 and K_2 specific to the circuit.

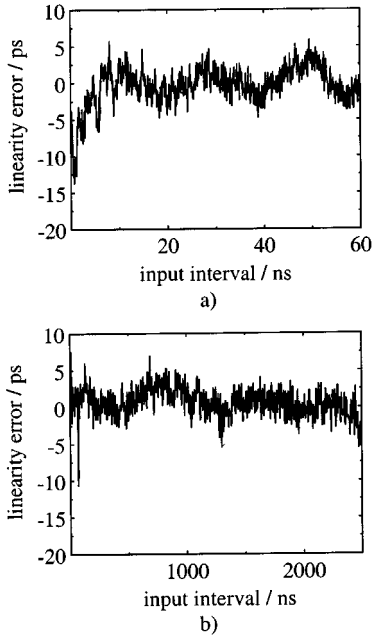

Fig. 5. Measured linearity of the TDC. (a) Input increment 65 ps. (b) Input increment 1.6 ns.

has been implemented with discrete ECL components and calibrated in a real laser radar environment. The results indicate that the linearity of the reference TDC is better than ± 10 ps for input intervals of 40–340 ns and the single-shot precision is <35 ps (σ-value). To measure the linearity of the prototype TDC, both the start and the stop pulses taken from the pulse generator were split into two pulses with a power splitter and fed simultaneously to the prototype TDC and to the reference TDC. The linearity of the prototype TDC was then calculated by comparing the measurement results of the two TDCs. For each output result, an average of 1000 samples was taken. The measured nonlinearity of the prototype TDC was less than ± 5 ps for input time intervals from 10 ns to 2.5 μs, as shown in Fig. 5.

C. Stability

Two examples of the temperature drift measurements are shown in Fig. 6. The temperature drift at each temperature was calculated as a difference relative to the room-temperature results. The offset-type error resulting from random mismatch between start and stop channels is shown in Fig. 6(a), while in Fig. 6(b) the gain error arises from the temperature dependence of the reference oscillator. For short input intervals [Fig. 6(a)] the offset error dominates since temperature dependence of the reference oscillator causes notable error only for longer

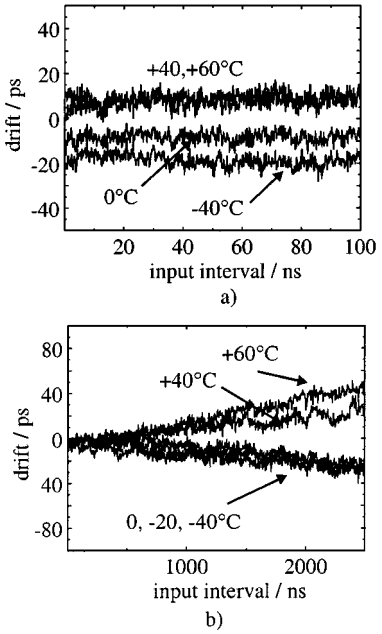

Fig. 6. Measured output error of the TDC compared to room temperature. (a) Drift due to the TDC itself. (b) Temperature dependence due to the reference oscillator.

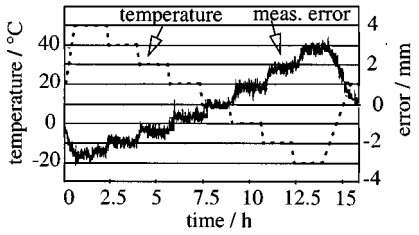

Fig. 7. Effect of the temperature on the offset of one TDC chip when a constant input interval of 50 ns (corresponding to a distance of 7.5 m) is measured.

intervals. The results in Fig. 6(b) are from a different chip which has a negligible offset error, i.e., the matching between start and stop channels is good. Without compensation and excluding the temperature dependence of the oscillator, the measured temperature drift of the TDC is below ± 40 ps in a temperature range of -40 to 60 °C.

In Fig. 7 is shown the effect of the temperature on the offset of one TDC chip when a constant input interval of 50 ns (corresponding to a distance of 7.5 m) is measured. Temperature is varied between -20 and 50 °C. The error is $< \pm 4$ mm in distance measurement, i.e., $< \pm 27$ ps in time measurement. The measurement results are summarized in Table I.

IV. Summary

An integrated time-to-digital converter has been implemented for a laser radar with millimeter-level distance measurement accuracy. The TDC is based on a main counter with a 100-MHz clock and two separate time digitizers for interpolation within the clock period to improve single-shot resolution. The interpolators are based on dual-slope conversion. In distance measurement, the measured single-shot time precision of the TDC ($\sigma < 30$ ps) corresponds to 4.5 mm and the time measurement linearity of <5 ps in the range of 10 ns to 2.5 μs corresponds to an accuracy of ± 1 mm in the range of 1.5 m to 370 m. The size of the TDC chip is 3.5×3.4 mm^2 and the only external component required is a 100-MHz oscillator.

TABLE I
Measured Performance of the TDC

Parameter	Value
lsb width	32 ps
input range	2.5 μs
clock frequency	100 MHz
time precision	σ = 30 ps (worst case)
integral linearity error	≤ ± 5 ps
temperature sensitivity	≤ ± 40 ps (-40... +60 °C)
conversion time	≤ 6.4 μs
supply voltage	5 V
power consumption	350 mW
chip size	3.5 mm * 3.4mm

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