AFE4900 Ultra-Low Power, Integrated AFE for Wearable Optical, Electrical Bio-Sensing With FIFO

1 Features

- Synchronized PPG, ECG Signal Acquisition at Data Rates Up to 1 kHz
- ECG Signal Chain:
  - Standalone ECG Acquisition Up to 4 kHz
  - Input Bias: 1-Lead ECG With RLD Bias
  - Programmable INA Gain: 2 to 12
  - Input Noise (1 Hz to 150 Hz): 2.5 µVrms at 1 kHz, 1.25 µVrms at 4-kHz Data Rate
  - AC, DC Lead-Off Detect: 12.5-nA to 100-nA
- PPG Receiver:
  - Supports Three Time-Multiplexed PD Inputs
  - 24-Bit Representation of Current From PD
  - DC Offset Subtraction DAC (Up to ±126-µA) at TIA Input for Each LED, Ambient
  - Digital Ambient Subtraction at ADC Output
  - Noise Filtering With Programmable Bandwidth
  - Transimpedance Gain: 10 kΩ to 2 MΩ
  - Dynamic Range Up to 100 dB
  - Receiver Operates in PPG-Only mode at Approximately 1-µA/Hz Sampling Rate
  - Power-Down Mode: Approximately 0 µA
- PPG Transmitter:
  - Four LEDs in Common Anode Configuration
  - 8-Bit LED Current Up to 200 mA
  - Mode to Fire Two LEDs in Parallel
  - Programmable LED On-Time
  - Simultaneous Support of Three LEDs for SpO_2, or Multiwavelength HRM
  - Average Current of 30 µA Adequate for a Typical Heart-Rate Monitoring Scenario:
    - 20-mA Setting, 60-µs Pulse Duration, 25-Hz Sampling Rate
- Clocking Using an External or Internal Clock
- FIFO With 128-Sample Depth for ECG and PPG
- I^2C, SPI™ Interfaces: Selectable by Pin
- Operating Temperature Range: –20°C to +70°C
- 2.6-mm × 2.1-mm, 0.4-mm Pitch DSBGA Package
- Supplies:
  - Rx: 1.8 V to 1.9 V (LDO Bypass), 2.0 V to 3.6 V (LDO Enabled)
  - Tx: 3 V to 5.25 V
  - IO: 1.7 V to Rx_SUP

2 Applications

- Synchronized PPG, ECG for Blood Pressure Estimation
- HRM for Wearables, Hearables
- Heart-Rate Variability (HRV)
- Pulse Oximetry (SpO_2) Measurements

3 Description

The AFE4900 device is an analog front-end (AFE) for synchronized electrocardiogram (ECG), photoplethysmogram (PPG) signal acquisition. The device can also be used for optical bio-sensing applications, such as heart-rate monitoring (HRM) and saturation of peripheral capillary oxygen (SpO_2). The PPG signal chain supports up to four switching light-emitting diodes (LEDs) and up to three photodiodes (PDs). The LEDs can be switched on using a fully integrated LED driver. The current from the photodiode is converted into voltage by the transimpedance amplifier (TIA) and digitized using an analog-to-digital converter (ADC). The ECG signal chain has an instrumentation amplifier (INA) with a programmable gain that interfaces to the same ADC. A right-leg drive (RLD) amplifier set can be used to the bias for the ECG input pins. AC and dc lead-off detect schemes are supported. The ADC codes from the PPG and ECG phases can be stored in a 128-sample first in, first out (FIFO) block and read out using either an I^2C or a serial programming interface (SPI) interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE4900	DSBGA (30)	2.60 mm × 2.10 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Block Diagram

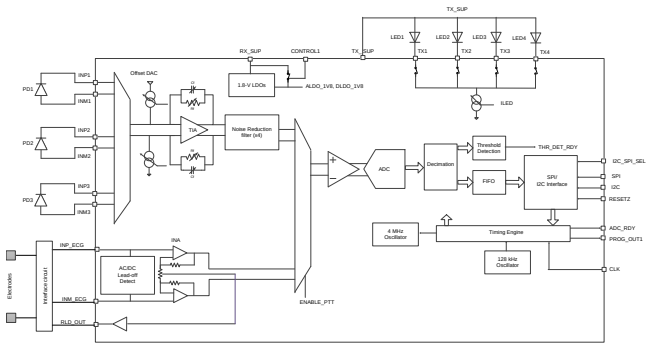


Table of Contents

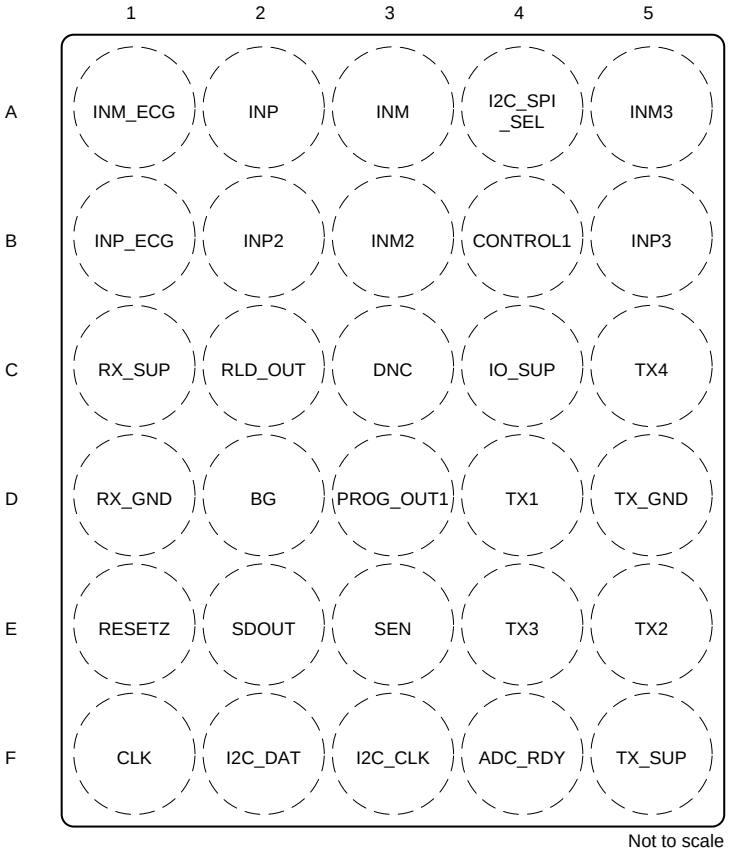
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2017	*	Initial release.

5 Pin Configuration and Functions

YZ Package
30-Ball DSBGA
Top View



Not to scale

Pin Functions

NO.	NAME	I/O	DESCRIPTION
A1	INM_ECG	Analog	ECG channel input (negative)
A2	INP	Analog	Connect to the photodiode cathode only
A3	INM	Analog	Connect to the photodiode anode only
A4	I2C_SPI_SEL	Digital	This pin enables selection between the I^2C and SPI interfaces. 0 = I^2C interface enabled 1 = SPI interface enabled Levels = 0 V to RX_SUP. If RX_SUP and IO_SUP differ by more than 0.3 V, a level shifter is required for the connection if driven from an MCU I/O pin.
A5	INM3	Analog	Connect to the third photodiode anode only
B1	INP_ECG	Analog	ECG channel input (positive)
B2	INP2	Analog	Connect to the second photodiode cathode only
B3	INM2	Analog	Connect to the second photodiode anode only
B4	CONTROL1	Digital	When RX_SUP is 2.0 V or higher, connect CONTROL1 to ground (0 V) to operate with the internal low-dropout (LDO) regulators enabled. When RX_SUP is 1.8 V–1.9 V, connect CONTROL1 to an MCU I/O pin. Pull this pin to 1 to operate with the LDO bypassed. Levels = 0 V to RX_SUP.
B5	INP3	Analog	Connect to the third photodiode cathode only

Pin Functions (continued)

NO.	NAME	I/O	DESCRIPTION
C1	RX_SUP	Supply	Receiver supply; 1-µF decapacitor to GND. With the internal LDO enabled (with CONTROL1 = 0), the allowed receiver supply range is 2.0 V to 3.6 V with the maximum value set to lower than or equal to TX_SUP. An external buck converter can be used to drive RX_SUP. With the internal LDO bypassed (CONTROL1 = 1), the receiver supply is 1.8 V to 1.9 V. If the internal LDO is bypassed, then drive RX_SUP with a clean external supply (for example, from the output of an external LDO).
C2	RLD_OUT	Analog	Output common-mode bias voltage for ECG input pins. Connect a 100-pF decoupling capacitor to ground. Typical voltage = 0.9 V.
C3	DNC	—	Do not connect (leave floating)
C4	IO_SUP	Supply	This pin provides a separate supply for the digital I/O from 1.7 V to a maximum value equal to RX_SUP. This pin can also be set to be the same as RX_SUP.
C5	TX4	Analog	Transmit output, LED4
D1	RX_GND	Ground	Receiver ground. Level = 0 V.
D2	BG	Analog	Band-gap voltage output. An optional 0.1-µF decoupling capacitor can be used.(1)
D3	PROG_OUT1	Digital	Programmable interrupt (output).(2) Levels = 0 V to IO_SUP. Connect to an MCU input pin.
D4	TX1	Analog	Transmit output, LED1
D5	TX_GND	Ground	Transmitter ground. Level = 0 V.
E1	RESETZ	Digital	This pin is either RESETZ or PWDN. Functionality is based on the (active low) duration of RESETZ. A low-going pulse duration between 25 µs and 50 µs resets the device. When pulled down for a duration longer than 200 µs, the device enters a hardware power-down mode (PWDN). Levels = 0 V to IO_SUP. Do not leave floating.
E2	SDOUT	Digital	In I^2C mode, this pin is a programmable interrupt (output). In SPI mode, this pin is a serial data output for the SPI. Levels = 0 V to IO_SUP.
E3	SEN	Digital	In I^2C mode, this pin inverts the LSB of the I^2C slave address. In SPI mode, this pin is the chip-select pin for the SPI (active low). Levels = 0 V to IO_SUP.
E4	TX3	Analog	Transmit output, LED3
E5	TX2	Analog	Transmit output, LED2
F1	CLK	Digital	Clock input pin. Levels = 0 V to IO_SUP. The lowest frequency clock that the device can function with is 32 kHz. Using a higher clock frequency enables finer timing control resolution for the timing signals (for example, SAMP, LED_ON, and so forth) in the active phase.
F2	I2C_DAT	Digital	In I^2C mode, this pin is an I^2C data pin. An external pullup resistor (for example, 10 kΩ) to IO_SUP is required. In SPI mode, this pin is a serial data input. Levels = 0 V to IO_SUP.
F3	I2C_CLK	Digital	In I^2C mode, this pin is an I^2C clock pin. An external pullup resistor (for example, 10 kΩ) to IO_SUP is required. In SPI mode, this pin is a serial clock input. Levels = 0 V to IO_SUP.
F4	ADC_RDY	Digital	Programmable interrupt (output). Levels = 0 V to IO_SUP. Connect to an MCU input pin.
F5	TX_SUP	Supply	Transmitter supply; 1-µF to 10-µF decapacitor to GND. Levels = 3.0 V to 5.25 V.

(1) Using a 0.1-µF capacitor on BG improves device noise but results in a higher recovery time from a software or hardware power-down.
(2) To enable the PROG_OUT1 pin as an output pin, set the EN_PROG_OUT1 bit to 1.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage range	RX_SUP to GND; LDO bypassed	–0.3	2.1	V
	RX_SUP to GND; LDO enabled(3)	–0.3	4	
	IO_SUP to GND	–0.3	Min [4,(RX_SUP+0.3)]	
	TX_SUP to GND	–0.3	6	
Voltage applied to analog inputs		Max [–0.3, (GND – 0.3)]	Min [4.0, (RX_SUP + 0.3)]	V
Voltage applied to digital inputs		Max [–0.3, (GND – 0.3)]	Min [4.0, (IO_SUP + 0.3)]	V
Maximum duty cycle (cumulative): sum of all LED phase durations as a function of the total period	50-mA LED current		10%	
	100-mA LED current		3%	
	200-mA LED current		1%	
Junction temperature, T_J			105	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If subjected to additional processing steps (for example during PCB assembly or product manufacturing), avoid exposure of the device to UV radiation and exposure to high temperatures (350°C and higher).
(3) Voltages higher than 2.1 V can be applied on RX_SUP only when CONTROL1 pin is at 0.

6.2 ESD Ratings(1)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±250	

(1) External ESD protection devices may be required if higher system-level ESD requirements must be satisfied.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
RX_SUP	Receiver supply	LDO bypassed	1.8	1.9	V
		LDO enabled	2.0	Minimum (3.6, TX_SUP)	
IO_SUP	I/O supply		1.7	RX_SUP	V
TX_SUP	Transmitter supply	When operating at the maximum current setting	3.0 or $(0.3 + V_{HR} + V_{LED})$(1), whichever is greater	5.25	V
	Digital inputs		0	IO_SUP	V
	Analog inputs		0	RX_SUP	V
T_A	Operating temperature range		–20	70	°C

(1) V_{LED} refers to the maximum voltage drop across the external LED (at maximum LED current). This value is usually governed by the forward drop voltage (V_{FB}) of the LED. V_{HR} refers to the headroom voltage of the LED driver as listed in Table 18 for various LED current settings. The extra 0.3 V is the suggested margin.

6.4 Thermal Information

THERMAL METRIC[1]		AFE4900 WCSP (DSBGA) 30 BALLS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

typical specifications are at T_A = 25°C; TX_SUP = 5 V, RX_SUP = 1.8 V (with CONTROL1 = 1.8 V to bypass internal LDOs), IO_SUP = 1.8 V, external clock mode with 32-kHz clock on CLK pin (period = t_{TE} = 31.25 µs), the AFE operates with ULP mode enabled (ENABLE_ULP = 1); **PPG:** 1-kHz sampling rate, SAMP width of 3 × t_{TE}, LED ON width of 4 × t_{TE}, C_F chosen such that there are 7-8 TIA time constants within the SAMP width, NUMAV = 1 (2 ADC averages), noise-reduction filter bandwidth set to 2.5 kHz, C_{IN} = 100 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD); **ECG:** 1-kHz sampling rate, INA gain of 12, chopper mode enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE REPETITION FREQUENCY						
PRF[1]	Pulse repetition frequency	PPG-only and synchronized PPG, ECG signal acquisitions		20 to 1000		SPS
PRF_ECG	Maximum ECG acquisition rate	In ECG-only mode with PPG phases set as dummy phases		4000		SPS
RECEIVER						
	Offset cancellation DAC current range	Default range		–15.75 to 15.75		µA
		2x range		–31.5 to 31.5		
		4x range		–63 to 63		
		8x range		–126 to 126		
	Offset cancellation DAC current step	Default (–15.75 µA to 15.75 µA) range		0.125		µA
	TIA gain setting			10k to 2M		Ω
	C_F setting			2.5 to 25		pF
	Switched RC filter bandwidth[2]			2.5, 5, 10		kHz
	ADC averages		1		16	
	Detector capacitance	Differential capacitance between INP, INN	10		200	pF
PPG TRANSMITTER						
	LED current range	50-mA mode		0 to 50		mA
		100-mA mode		0 to 100		
		200-mA mode		0 to 200		
	LED current resolution			8		Bits
PPG PERFORMANCE						
	Receiver-only noise	Receiver inputs open, R_F = 500 kΩ, C_F = 7.5 pF		40		µV[3]
	Transmitter + receiver noise	50-mA LED current looped back electrically to the receiver inputs through an external op amp to create an output voltage of 0.4 V (R_F = 500 kΩ, C_F = 7.5 pF)		60		µV[3]

(1) PRF refers to the rate at which samples from each of the four phases are output from the AFE.
(2) Lower filter bandwidth setting gives lower effective bandwidth for both signal and noise.
(3) Output noise over the full Nyquist bandwidth calculated from the standard deviation of the output code.

Electrical Characteristics (continued)

typical specifications are at T_A = 25°C; TX_SUP = 5 V, RX_SUP = 1.8 V (with CONTROL1 = 1.8 V to bypass internal LDOs), IO_SUP = 1.8 V, external clock mode with 32-kHz clock on CLK pin (period = t_{TE} = 31.25 µs), the AFE operates with ULP mode enabled (ENABLE_ULP = 1); **PPG:** 1-kHz sampling rate, SAMP width of 3 × t_{TE}, LED ON width of 4 × t_{TE}, C_F chosen such that there are 7-8 TIA time constants within the SAMP width, NUMAV = 1 (2 ADC averages), noise-reduction filter bandwidth set to 2.5 kHz, C_{IN} = 100 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD); **ECG:** 1-kHz sampling rate, INA gain of 12, chopper mode enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ECG PERFORMANCE						
	INA gain range			2–12		Range
	Input common-mode voltage	Biased using RLD_OUT		0.9		V
	AC input impedance	Estimated with a 10-mV_{pp}, 10-Hz sine-wave input to the AFE through a series impedance of 620 kΩ in parallel with 4.7 nF; lead-off detect enabled		> 10		MΩ
	Noise(4)	ECG sampling rate = 1 kHz, lead-off detect disabled		2.5		µVrms
		ECG sampling rate = 4 kHz, lead-off detect disabled		1.25		
		ECG sampling rate = 1 kHz, lead-off detect enabled with 25-nA current		3.5		
CMRR	Common-mode rejection ratio	50-Hz common-mode tone		110		dB
RLD OUTPUT						
	Output voltage			0.9		V
	Output impedance			25		kΩ
ECG LEAD OFF						
	DC lead-off current settings			12.5–100		nA
	AC lead-off current settings			12.5–100		nA
	AC lead-off frequency settings	Relative to ECG sample rate, f_{ECG}		f_{ECG} / 4, f_{ECG} / 2		Hz
EXTERNAL CLOCK (When Using External Clock Mode)						
	Frequency of external clock		32		4000	KHz
	Input clock high level			IO_SUP		V
	Input clock low level			0		V
	Input capacitance of CLK pin	Capacitance to ground		< 4		pF
INTERNAL OSCILLATOR FOR TIMING ENGINE (When Using Internal Oscillator Mode)						
	Frequency			128		KHz
	Accuracy	Room temperature		±1%		
	Frequency drift with temperature	Full temperature range		±1%		
	Jitter (RMS)			12		ns
FIFO						
	FIFO depth				128	Samples
I^2C INTERFACE						
	Maximum clock speed			400		kHz
	I^2C slave address	SEN = 1		5A		Hex
		SEN = 0		5B		
SPI INTERFACE						
	Maximum clock speed			4		MHz

(4) Input-referred noise integrated over 1-Hz to 150-Hz bandwidth with INA gain = 12, ECG chopping mode enabled, NUMAV = 1.

Electrical Characteristics (continued)

typical specifications are at T_A = 25°C; TX_SUP = 5 V, RX_SUP = 1.8 V (with CONTROL1 = 1.8 V to bypass internal LDOs), IO_SUP = 1.8 V, external clock mode with 32-kHz clock on CLK pin (period = t_{TE} = 31.25 µs), the AFE operates with ULP mode enabled (ENABLE_ULP = 1); **PPG:** 1-kHz sampling rate, SAMP width of 3 × t_{TE}, LED ON width of 4 × t_{TE}, C_F chosen such that there are 7-8 TIA time constants within the SAMP width, NUMAV = 1 (2 ADC averages), noise-reduction filter bandwidth set to 2.5 kHz, C_{IN} = 100 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD); **ECG:** 1-kHz sampling rate, INA gain of 12, chopper mode enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
	RX_SUP current excluding switching current from I²C or SPI readout(5)	Low PRF PPG signal acquisition(6)		50		µA
		High PRF ECG, PPG signal acquisition(7)		600		
		Hardware power-down (PWDN) mode(8)		< 1		
		Software power-down (PDNAFE) mode(8)		15		
	RX_SUP current resulting from switching current at I²C readout	At PRF of 50 Hz, readout with FIFO enabled with FIFO_PERIOD = 60, FIFO_NPHASE = 4(9)		6		µA
		Power-down mode		0		
	IO_SUP current	Low PRF, PPG signal acquisition(6)		1		µA
		High PRF, ECG, PPG signal acquisition(6)		1		
		Hardware power-down (PWDN) mode(8)		< 1		
		Software power-down (PDNAFE) mode(8)		< 1		
	TX_SUP current	Low PRF, PPG signal acquisition(6)		4		µA
		High PRF, ECG, PPG signal acquisition(7)		20		
		Hardware power-down (PWDN) mode(8)(10)		< 1		
		Software power-down (PDNAFE) mode(8)(10)		< 1		
DIGITAL INPUTS						
V_{IH}	High-level input voltage	Digital inputs except CONTROL1, I2C_SPI_SEL	0.9 × IO_SUP	IO_SUP		V
		CONTROL1 and I2C_SPI_SEL(11)	0.85 × RX_SUP	RX_SUP		
V_{IL}	Low-level input voltage	Digital inputs except CONTROL1, I2C_SPI_SEL		0	0.1 × IO_SUP	V
		CONTROL1 and I2C_SPI_SEL(11)		0	0.1 × RX_SUP	
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage			IO_SUP		V
V_{OL}	Low-level output voltage			0		V

(5) The additional current for FIFO readout is negligible when operating in the SPI mode.
(6) Acquisition of four phases of signal in PPG mode at 50-Hz PRF.
(7) PTT mode at 1-kHz sampling rate for both ECG and PPG
(8) External clock switched off.
(9) This current depends on the percentage of time for which the I2C_CLK is low; and scales with FIFO_NPHASE and PRF. This extra component of current is negligible when operating in the SPI interface mode.
(10) With LED currents set to 0 mA
(11) CONTROL1 and I2C_SPI_SEL can also be driven directly by the MCU (with IO_SUP levels) if the V_{IH}, V_{IL} levels are satisfied.

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
INTERRUPTS					
$t_{DATA\_RDY\_RISE}$	DATA_RDY rise time (10% to 90%) with a 15-pF capacitive load to ground (1)		12		ns
$t_{DATA\_RDY\_FALL}$	DATA_RDY fall time (90% to 10%) with a 15-pF capacitive load to ground (1)		12		ns
I²C INTERFACE					
t_{I2C_RISE} (2)	I²C data rise time with a 10-kΩ pullup resistor with a 20-pF load from I²C data to GND		1200		ns
t_{I2C_FALL}	I²C data fall time (when the data line is pulled down by the AFE) with a 20-pF load from I²C data to GND		28		ns
SPI (3)					
t_{SPICLK}	Serial shift clock period	125			ns
t_{STECLK}	Serial data enable low to serial clock rising edge, setup time	15			ns
$t_{CLKSTEH,L}$	Serial clock transition to serial data enable high or low	15			ns
t_{SIMOSU}	Serial data input to serial clock rising edge, setup time	15			ns
t_{SIMOHD}	Valid serial data input after SCLK rising edge, hold time	15			ns
t_{SOMIPD}	Serial clock falling edge to valid serial data output			15	ns
t_{SOMIHD}	Serial clock rising edge to invalid serial data output		0.5		t_{SPICLK}

(1) Same timing applies to other interrupts also.
(2) Maximum achievable speed of the I²C interface could be limited by this parameter if the load on the I² C lines are high.
(3) The values in this table refer to the timings of these logic signals internal to the AFE. Additional timing margins may need to be accounted for based on the external delays and rise and fall times of these signals.

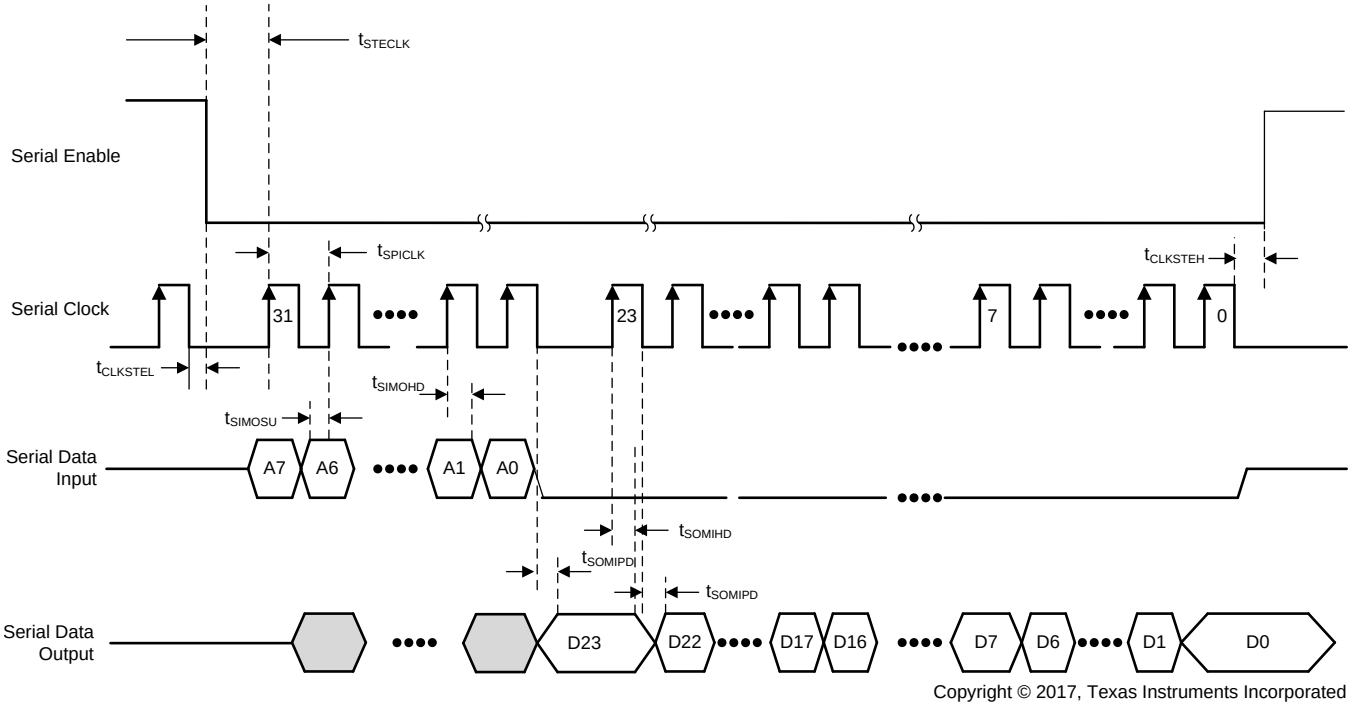


Figure 1. Serial Interface Timing Diagram: Read Operation

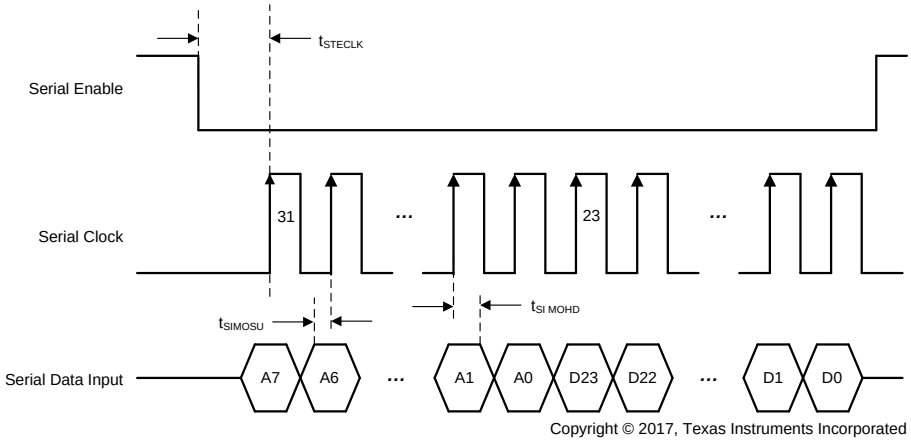


Figure 2. Serial Interface Timing Diagram: Write Operation

6.7 Typical Characteristics: PPG-Only Mode

at T_A = 25°C; TX_SUP = 5 V, LDO enable mode (with RX_SUP = 2V, IO_SUP = 1.8 V), 25-Hz PRF as set by a 32.768-kHz external clock on the CLK pin, SAMP width of 1 × t_{TE}, LED_ON width of 2 × t_{TE}, R_F = 500 kΩ, C_F chosen such that there are at least five TIA time constants within the SAMP width, NUMAV = 3 (4 ADC averages), noise-reduction filter bandwidth set to 5 kHz, 1 µF on the BG pin, C_{IN} = 50 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD pin), and the AFE is operated with the ULP mode enabled (ENABLE_ULP = 1) and in PPG-only mode (ENABLE_PTT = 0) (unless otherwise noted)

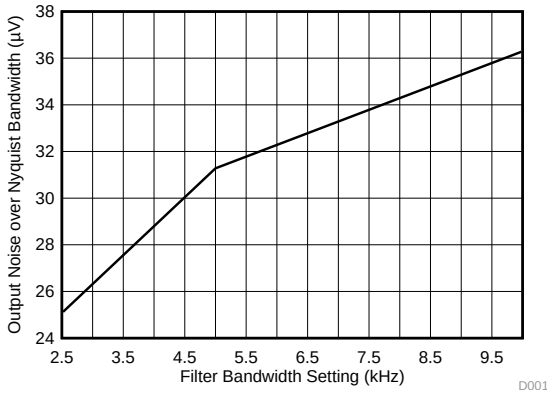


Figure 3. Output Noise vs Filter Bandwidth Setting

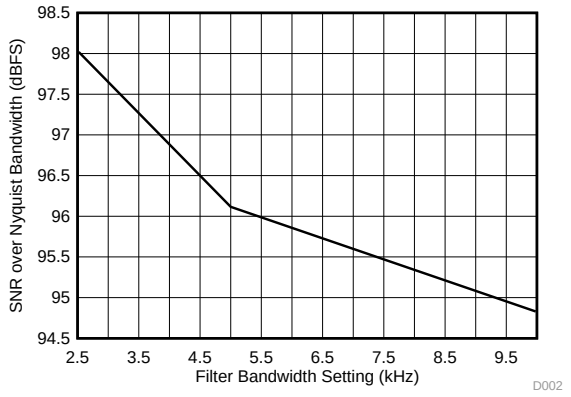


Figure 4. Signal-to-Noise Ratio vs Filter Bandwidth Setting

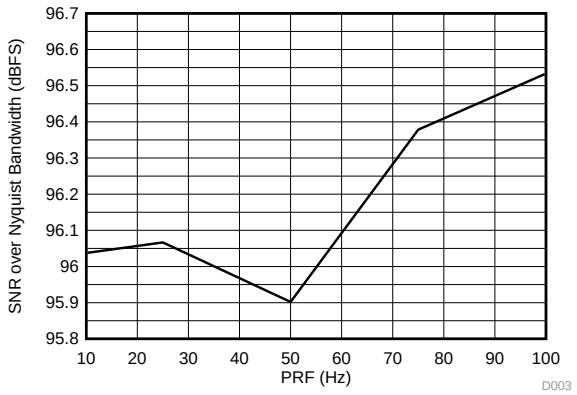


Figure 5. Signal-to-Noise Ratio vs Pulse Repetition Frequency

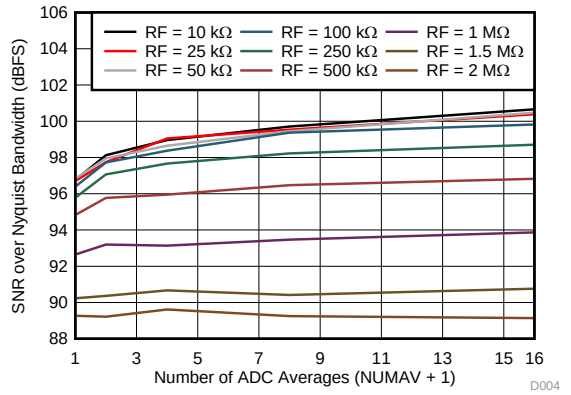


Figure 6. Signal-to-Noise Ratio vs ADC Averaging Across TIA Gains

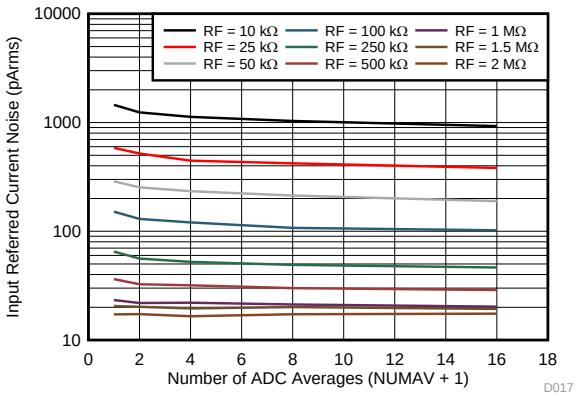


Figure 7. Input-Referred Noise Current vs ADC Averaging Across TIA Gains

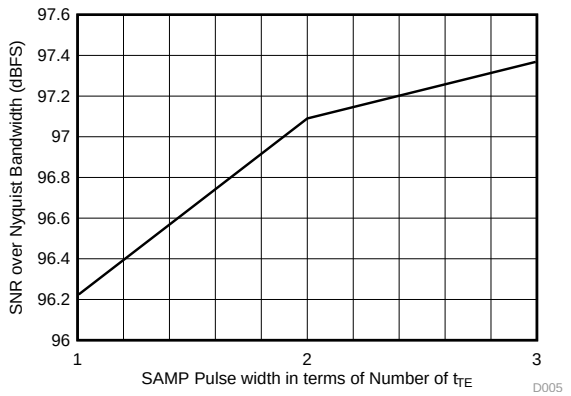


Figure 8. Signal-to-Noise Ratio vs Sampling Pulse Duration

Typical Characteristics: PPG-Only Mode (continued)

at T_A = 25°C; TX_SUP = 5 V, LDO enable mode (with RX_SUP = 2V, IO_SUP = 1.8 V), 25-Hz PRF as set by a 32.768-kHz external clock on the CLK pin, SAMP width of 1 × t_{TE}, LED_ON width of 2 × t_{TE}, R_F = 500 kΩ, C_F chosen such that there are at least five TIA time constants within the SAMP width, NUMAV = 3 (4 ADC averages), noise-reduction filter bandwidth set to 5 kHz, 1 µF on the BG pin, C_{IN} = 50 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD pin), and the AFE is operated with the ULP mode enabled (ENABLE_ULP = 1) and in PPG-only mode (ENABLE_PTT = 0) (unless otherwise noted)

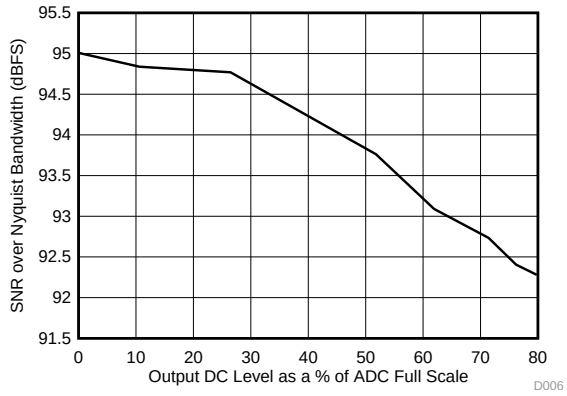


Figure 9. Signal-to-Noise Ratio vs Output DC Level

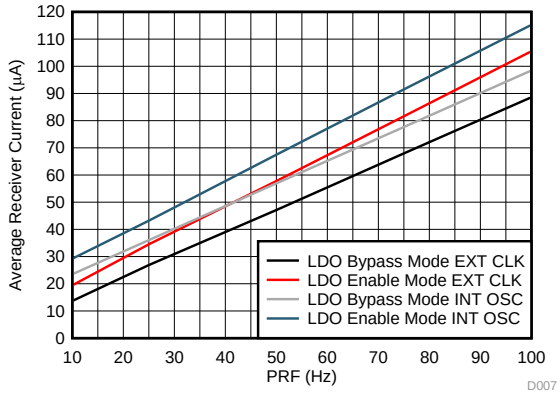


Figure 10. RX_SUP Current vs Pulse Repetition Frequency (Excluding FIFO Readout Current)

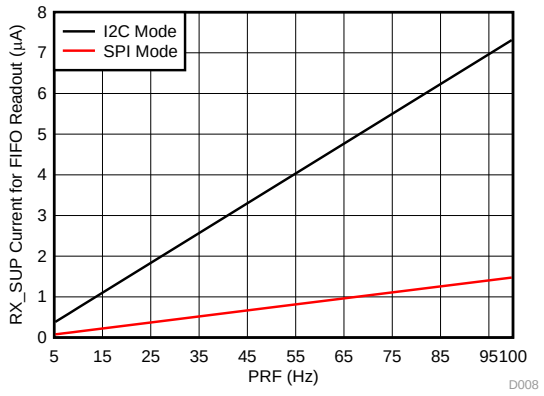


Figure 11. RX_SUP Current for FIFO Readout

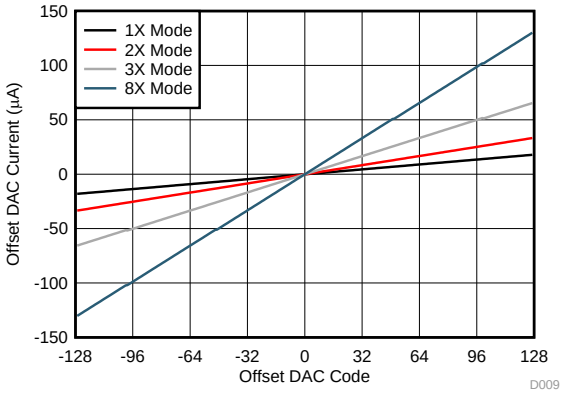


Figure 12. Offset DAC Current vs Code

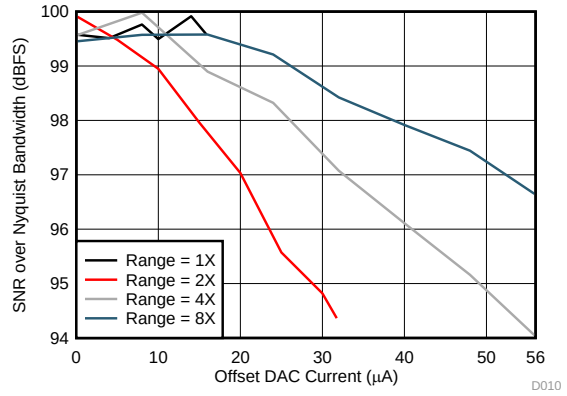
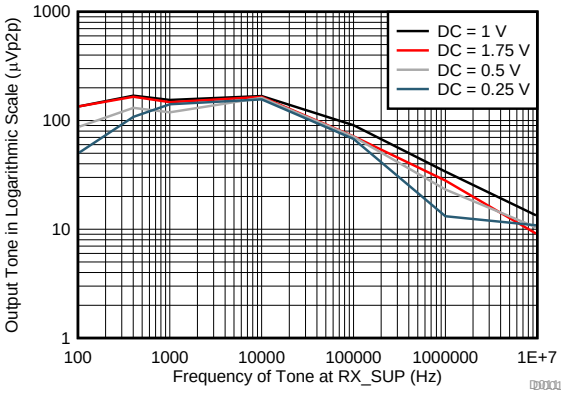


Figure 13. Noise With Offset DAC Enabled

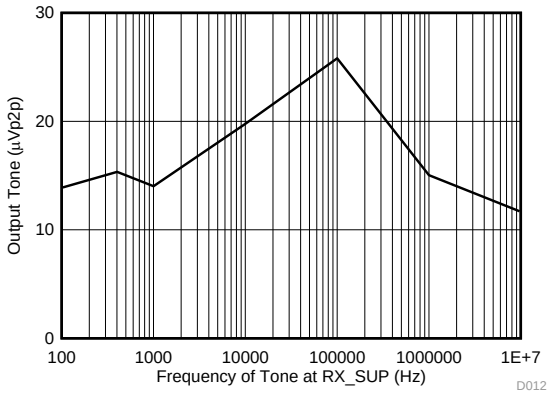


1-µF capacitor on the BG pin (across various output dc levels)

Figure 14. Output Tone Resulting From a 50-mV_{PP} Tone on RX_SUP in LDO Bypass Mode

Typical Characteristics: PPG-Only Mode (continued)

at T_A = 25°C; TX_SUP = 5 V, LDO enable mode (with RX_SUP = 2V, IO_SUP = 1.8 V), 25-Hz PRF as set by a 32.768-kHz external clock on the CLK pin, SAMP width of 1 × t_{TE}, LED_ON width of 2 × t_{TE}, R_F = 500 kΩ, C_F chosen such that there are at least five TIA time constants within the SAMP width, NUMAV = 3 (4 ADC averages), noise-reduction filter bandwidth set to 5 kHz, 1 µF on the BG pin, C_{IN} = 50 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD pin), and the AFE is operated with the ULP mode enabled (ENABLE_ULP = 1) and in PPG-only mode (ENABLE_PTT = 0) (unless otherwise noted)



1-µF capacitor on BG pin with a 1-V output dc signal

Figure 15. Output Tone Resulting From a 50-mV_{PP} Tone on RX_SUP in LDO Enable Mode

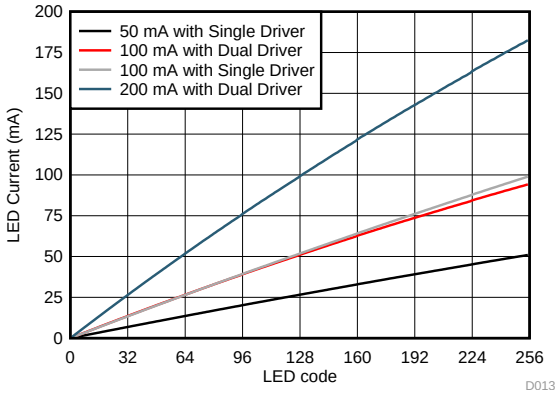


Figure 16. LED Current vs LED Code

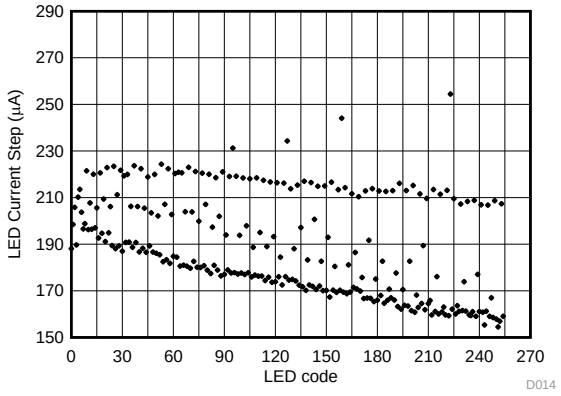


Figure 17. LED Current Step vs Code

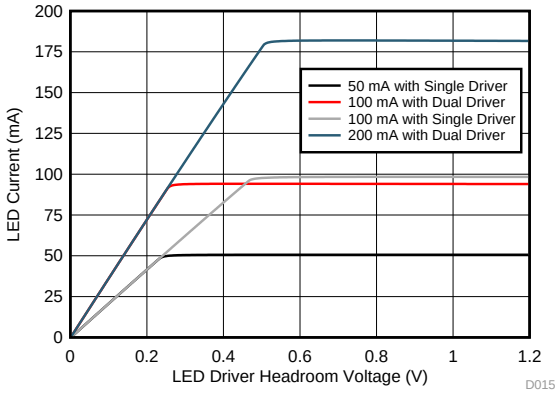
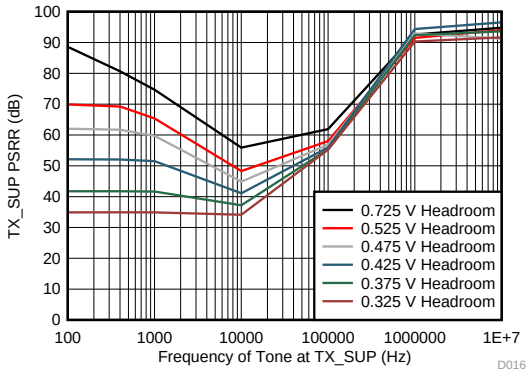


Figure 18. Full-Scale LED Driver Current vs Headroom Voltage



50-mV_{PP} tone on TX_SUP (across various LED headroom voltages)

Figure 19. Tone in LED Current

6.8 Typical Characteristics: PPG+ECG Mode

typical characteristics are at T_A = 25°C, TX_SUP = 5 V, PTT mode (ENABLE_PTT = 1), LDO enable mode (with RX_SUP = 2 V, IO_SUP = 1.8 V), PRF as set by a 32.768 kHz external clock on CLK pin, and 1 µF on the BG pin; **PPG signal acquisition:** SAMP width of 3 × t_{TE}, LED ON width of 4 × t_{TE}, R_F = 500 kΩ, C_F chosen such that there are at least 5 TIA time constants within the SAMP width, NUMAV = 1 (2 ADC averages), noise-reduction filter bandwidth set to 5 kHz, and C_{IN} = 50 pF (capacitor across the input pins to model the zero bias differential capacitance of the PD); **ECG signal acquisition:** INA gain = 6, chopping mode enabled, NUMAV = 1, and lead-off detect disabled (unless otherwise noted)

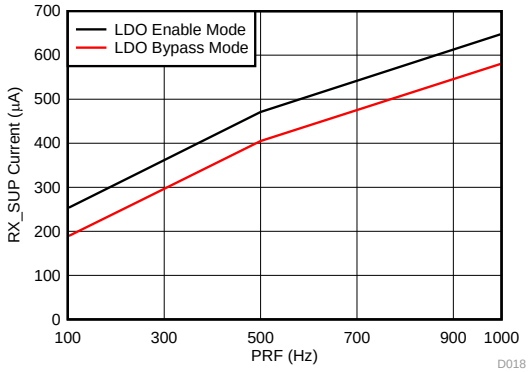


Figure 20. RX_SUP Current vs PRF (Excluding FIFO Readout Current) in PTT Mode (3 PPG Phases + 1 ECG Phase)

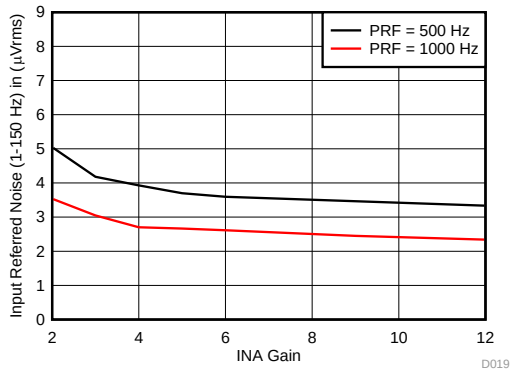


Figure 21. Input-Referred Noise of the ECG Signal Chain vs INA Gain

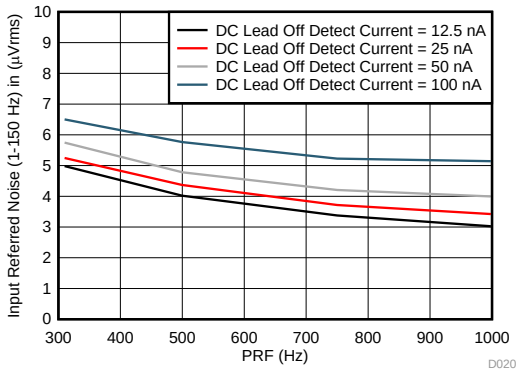


Figure 22. Input-Referred Noise of the ECG Signal vs PRF With DC Lead-Off Detect Enabled

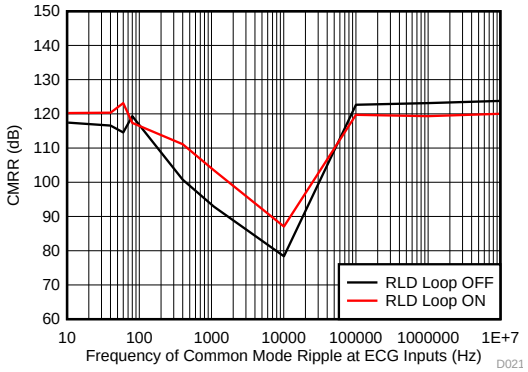


Figure 23. CMRR of ECG Signal Chain vs Frequency (INA Gain = 3)

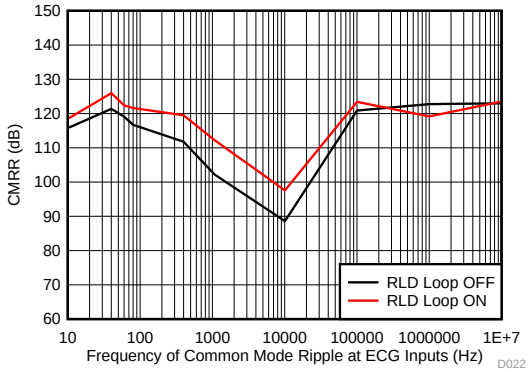


Figure 24. CMRR of ECG Signal Chain vs Frequency (INA Gain = 12)

6.9 Typical Characteristics: ECG-Only Mode

typical characteristics are at T_A = 25°C, ECG-only mode (ENABLE_PTT = 1, the three PPG phases set as dummy phases), LDO enable mode (with RX_SUP = 2 V, IO_SUP = 1.8 V), PRF as set by a 1-MHz external clock on the CLK pin, and 1 µF on the BG pin; **ECG signal acquisition:** INA gain = 6, chopping mode enabled, NUMAV = 1, and lead-off detect disabled (unless otherwise noted)

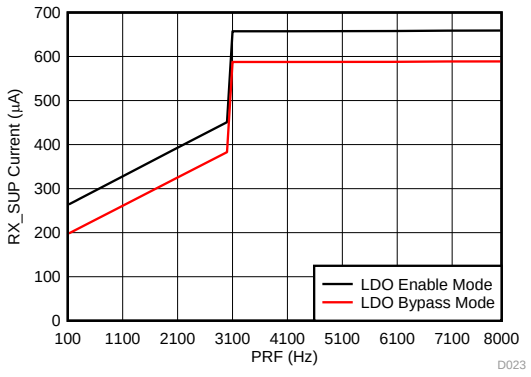


Figure 25. RX_SUP Current vs PRF in ECG-Only Mode

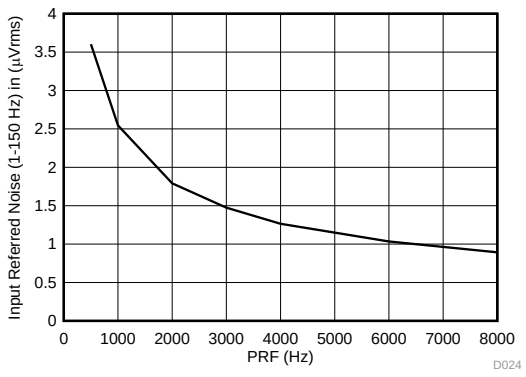


Figure 26. Input-Referred Noise of the ECG Signal Chain vs PRF in ECG-Only Mode (With INA Gain = 12)

7 Parameter Measurement Information

NOTE

Throughout this document, * is used to denote multiple variables. For instance, I_OFFDAC* refers to all of the following I_OFFDAC variations:

- I_OFFDAC_LED2_MID
- I_OFFDAC_AMB1_MID
- I_OFFDAC_LED1_MID
- I_OFFDAC_AMB2_MID\I_OFFDAC_LED3_MID, and so forth.

Figure 3 illustrates the output noise of the receiver as a function of the bandwidth setting of the noise-reduction filter. Receiver-only noise is measured by keeping the receiver inputs open and reading the output codes (LED minus Ambient). The noise is calculated in µVrms from the standard deviation of the output code multiplied by the voltage level corresponding to 1 LSB (0.57 µV). The pulse repetition frequency (PRF) is set to 25 Hz and the noise corresponds to the total integrated noise over the full Nyquist band (0 Hz to 12.5 Hz). The R_F setting is 500 kΩ; thus, the input-referred noise current can be deduced by dividing the output noise by 1 MΩ (equal to 2 × R_F).

Figure 4 corresponds to the same data as in Figure 3 but plots the SNR instead of the output noise. The SNR in dBFS is calculated by referring the standard deviation of the output noise to an output full-scale value of 2 V_{PP} (although the full-scale differential input to the ADC is 2.4 V_{PP}, the operating range is considered to be 2 V_{PP}, which is the valid operating range of the TIA, and hence the valid range of the signal swing).

Figure 5 plots the SNR versus PRF. SNR is fairly constant across the PRF because SNR is measured from the standard deviation of the output (and hence represents the noise over the full Nyquist band), SNR is fairly constant across the PRF. However, when the PRF increases, the noise floor lowers and the same noise gets spread over a larger Nyquist bandwidth. Thus, if the signal bandwidth of interest is lower than the Nyquist bandwidth, and the MCU low-pass filters the signal and noise to a lower bandwidth (such as 10 Hz), then the SNR in the bandwidth of interest keeps improving when the PRF increases.

Figure 6 plots the SNR versus number of ADC averages (set as NUMAV+1). The multiple curves correspond to different TIA gain settings. As expected, SNR improves with a higher number of ADC averages. The improvement is more pronounced at lower TIA gain settings. This improvement is because the contribution of the ADC noise to the total noise becomes more significant at lower TIA gain settings. The trend of the SNR reducing with increasing TIA gain is explained by the fact that the full-scale input current keeps inversely reducing when the TIA gain increases. However, the input-referred noise current does not reduce at the same rate.

Figure 7 plots the input-referred noise current corresponding to the data in Figure 6. As illustrated in this figure, operating with higher TIA gain settings results in a lower input-referred noise. The motivation for using the offset cancellation DAC to subtract some or all of the dc current allowing operation with a higher TIA gain is clear from the trend provided in this plot.

Figure 8 plots the SNR versus the duration of the sampling pulse (SAMP). The duration is specified in terms of the number of clocks of the external 32.768 kHz clock. For example, a duration of 3 × t_{TE} corresponds to 91.55 µs. For each setting of the SAMP width, the C_F value is changed so that the TIA time constant (R_F × C_F) is maintained close to 1/5th of the SAMP width. When the SAMP width increases, the SNR keeps improving. The primary reason for this improvement is the reduction in the noise bandwidth of the TIA because C_F is set to a higher value.

Figure 9 plots the SNR as a function of the output dc level. For this plot, the transmitter is turned on and the LED driver current is made to flow through a 20-Ω resistor. The voltage across the resistor is fed as an input current to the receiver through an electrical loopback circuit using an external operational amplifier (op amp). The dc output voltage of the receiver is swept by changing the LED current setting from 0 mA to 40 mA. The curve shows a slight reduction in SNR at higher output dc levels. The noise contribution from the ADC is lowest at a dc level close to 0 V. Additional sources of noise at higher dc levels come from the LED driver noise as well as a slight contribution from the loopback amplifier.

Figure 10 plots the RX_SUP current versus PRF. Across this plot, the active width remains the same across the PRF (accommodating four sampling phases), resulting in the device spending more time in the deep sleep phase at lower PRFs. The curves correspond to the four combinations of LDO bypass, LDO enabled and external clock, internal oscillator.

Figure 11 plots the extra (average) switching current on RX_SUP resulting from periodic FIFO readout for both the I^2C and SPI modes when operated at their maximum rated read-out rates. Four phases of data are stored and read out from the FIFO. This current depends on the duty cycle of the read-out phase.

Figure 12 illustrates the offset cancellation digital-to-analog converter (DAC) current across the decimal equivalent of the code as set by the I_OFFDAC* register control. The negative codes correspond to POL_OFFDAC = 1. The different plots correspond to the different full-scale ranges of 1x (default), 2x, 4x, and 8x as set by the IFS_OFFDAC control.

Figure 13 plots the SNR versus the offset DAC current across the four IFS_OFFDAC settings (1x, 2x, 4x, and 8x ranges). For the same range of offset DAC current, the 2x range setting gives the worst noise. Therefore, using the 2x setting is recommended to be avoided.

Figure 14 illustrates the effect of a tone on the RX_SUP pin when operating in LDO bypass mode. The amplitude of the tone is set to 50 mV_{PP} and the frequency is swept. The TIA gain is set to 100 kΩ and the input current for the four different curves is set to 1.25 µA, 2.5 µA, 3.75 µA, and 5 µA, resulting in output dc levels of 0.25 V, 0.5 V, 0.75 V, and 1 V, respectively.

Figure 15 illustrates the improvement in PSRR when the device is operated with the LDO enabled. The input current is set so that the output dc is 1 V.

Figure 16 illustrates the LED current across the decimal equivalent of the LED code as set by the ILED* register control. The currents are plotted for the four modes of operation described below:

- 50 mA with a single driver: corresponds to one LED driver on and a 50-mA current range (ILED_FS set to 0)
- 100 mA with a single driver: corresponds to one LED driver on and a 100-mA current range (ILED_FS set to 1)
- 100 mA with dual drivers: corresponds to both LED drivers on and a 50-mA current range (ILED_FS set to 0)
- 200 mA with dual drivers: corresponds to both LED drivers on and a 100-mA current range (ILED_FS set to 1)

The dual-driver case has increased nonlinearity towards the full-scale currents as compared with the single driver case.

Figure 17 illustrates the LED current step plotted against the LED code for the 50-mA LED current mode for the unit used to generate Figure 16.

Figure 18 illustrates the full-scale LED current (for the 50-mA and 100-mA current modes) as a function of the voltage at the TX pin. For this measurement, the voltage at the TX pin is swept by connecting a load resistor from the TX pin to TX_SUP and changing the voltage of TX_SUP. The four curves correspond to the four cases detailed for Figure 16.

Figure 19 illustrates the effect of a tone on the TX_SUP pin when the LED driver current is set to 50 mA (and a single driver is turned on). The amplitude of the tone on TX_SUP is set to 50 mV_{PP} and the frequency is swept. The PSRR is defined as the equivalent tone on the LED driver current (deduced from the tone at the receiver output) referred to the current setting of 50 mA. The PSRR curve is plotted for different values of LED driver headroom, which is measured as the lowest voltage at the TX pin during the transient wave form resulting from the tone on TX_SUP.

Figure 20 plots the RX_SUP current (excluding the FIFO readout current) vs PRF with the PTT mode enabled. In this mode, the signal chain acquires three samples of the PPG signal and one sample of the ECG signal.

Figure 21 plots the input-referred noise of the ECG signal chain versus INA gain for PRF settings of 500 Hz and 1 kHz. The output noise is integrated over a 1-Hz to 150-Hz bandwidth and divided by the INA gain to derive the input-referred noise.

Figure 22 illustrates the input-referred noise of the ECG signal chain over a 1-Hz to 150-Hz bandwidth versus PRF with the dc lead-off detect circuit enabled. The different curves correspond to different settings of the lead-off detect currents. The extra noise at the higher settings of the lead-off current comes from the noise introduced by the lead-off current sources.

Figure 23 and Figure 24 illustrate the common-mode rejection ratio (CMRR) of the ECG signal chain versus frequency for INA gains of 3 and 12, respectively. A 200-mV_{PP} ac signal (approximately a 0.9-V dc level) is applied commonly to both the INP_ECG and INM_ECG input pins through a 100-kΩ series resistor. The input pins are additionally connected to the RLD_OUT pin through a separate 100-kΩ resistor. With the RLD loop disabled, a 100-mV_{PP} common-mode tone appears at the input pins and encounters a rejection resulting from the differential nature of the ECG signal chain. The CMRR is calculated by measuring the output tone, dividing the tone amplitude by the INA gain to refer the amplitude to an input of 100 mV_{PP}. With the RLD enabled, the method of computing the CMRR as well as the calculation remains the same. The RLD loop gives enhanced common-mode rejection especially at the lower frequencies. In these measurements, the PRF is set to 1 kHz.

Figure 25 illustrates the RX_SUP current versus PRF with the PTT mode enabled and dummy CONV phases defined for the three PPG signals such that only the ECG signal is acquired. This scheme allows the extension of the ECG signal acquisition up to 4 kHz. At the higher range of PRF, there is insufficient time to go into and come out of deep sleep mode. The RX_SUP current versus PRF flattens out at the higher PRF settings because the AFE is in active mode throughout the PRF cycle.

Figure 26 plots the input-referred noise of the ECG signal chain (for an INA gain of 12) integrated over a 1-Hz to 150-Hz bandwidth versus PRF during ECG-only acquisition. As the PRF increases, the noise gets spread over a wider Nyquist bandwidth, thereby causing the noise in the 1-Hz to 150-Hz band to reduce.

8 Detailed Description

8.1 Overview

The *Functional Block Diagram* section provides a signal chain diagram of the AFE. The AFE has three modes of operation:

1. PPG-only mode
2. PTT mode for synchronized PPG + ECG signal acquisition
3. ECG-only mode

Both the PTT mode and ECG-only modes require the ENABLE_PTT register bit to be set to 1.

In PPG-only mode, the AFE converts four phases of the PPG signal (for example, three LED phases, one ambient phase). In PTT mode, the AFE uses three phases for PPG and one phase for the ECG signal.

By defining the three PPG phases as dummy phases in the PTT mode, the ECG signals can be acquired at rates higher than what is supported by the synchronized PPG+ECG signal acquisition in the PTT mode. This mode is referred to as ECG-only mode.

The PPG signal chain has an integrated transmitter and receiver. The system is characterized by a parameter termed the *pulse repetition frequency* (PRF) that determines the repetition periodicity of a sequence of operations. Every cycle of a PRF results in four 24-bit digital samples at the output of the AFE, each stored in a register. A FIFO with a programmable depth can be used to store samples across multiple periods. When the FIFO is enabled, the ADC_RDY pin can be configured as a FIFO_RDY interrupt, the periodicity of which changes with the programmed FIFO depth.

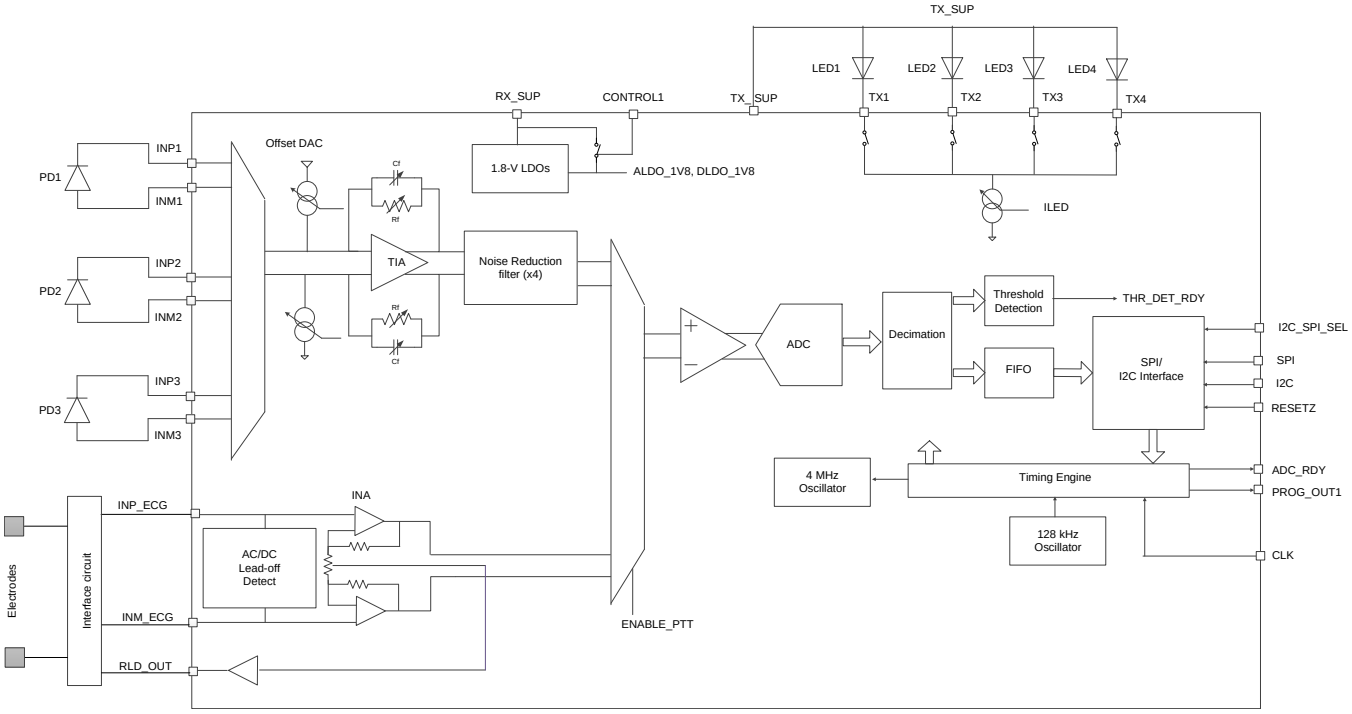
The PPG receiver input pins (INP, INM) are meant to be connected differentially to a photodiode. The signal current from the photodiode is converted to a differential voltage using a transimpedance amplifier (TIA). The TIA gain is set by the feedback resistor (R_F) and can be programmed from 10 kΩ to 2 MΩ. The transimpedance gain between the input current and output differential voltage of the TIA is equal to 2 × R_F. At the output of the TIA is a programmable switched RC filter that serves as a noise-bandwidth reduction filter. There are four parallel RC filters that are each connected to the TIA output signal during one of the four sampling phases. The output of each filter at the end of the sampling phase is stored on a capacitor, buffered, and converted by an ADC. The ADC output in each phase can be stored in the FIFO and read out using the SPI or I^2C interface. An offset cancellation DAC (ODAC) at the input of the receiver can be programmed to subtract a dc current from the incident current signal from the photodiode. By removing some or all of the dc current, a higher TIA gain can be applied to maximize the signal-to-noise ratio at the output of the AFE. The signal chain is kept fully differential throughout the receiver channel in order to enable excellent rejection of common-mode noise as well as noise on the power supplies. The PPG transmitter comprises of an LED current driver which can be routed to a different LED in different phases. The current setting of the LED driver can be independently programmed in each phase. The operation of the LEDs turning on is fully synchronized with the sampling of the signal from the photodiode by the receiver. The synchronization is made possible using a programmable timing engine.

Overview (continued)

In the PTT mode, the AFE can be configured to acquire an ECG signal in a synchronized manner with the PPG signal. The ECG signal acquisition takes the place of the fourth conversion in the PRF cycle. The sample rate for the ECG is equal to PRF and the sample rate for the PPG signal can be set to a programmable fraction of PRF. The ECG signal chain has an INA with a programmable gain, which interfaces with the shared ADC. An RLD output can be used to set the bias for the ECG input pins. Programmable dc and ac current sources at the input pins enable lead-off detection.

The AFE has two internal LDOs (ALDO and DLDO) that can be used for driving the analog and digital sections of the receiver. When CONTROL1 is connected to RX_SUP, the LDOs are powered down with their outputs in tri-state, and the internal nodes ALDO_1V8 and DLDO_1V8 are connected through switches to RX_SUP. When CONTROL1 is 0 V, two Internal LDOs are enabled and drive ALDO_1V8 and DLDO_1V8 to 1.8 V. When operating in internal LDO mode, the LDOs can be made to enter a low-power state during the deep sleep phase to prevent the LDOs from turning on. The internal LDOs provide additional rejection for noise on the RX_SUP. So when operating with the LDOs bypassed, care must be taken to ensure that a clean RX_SUP is provided.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Sequence of Receiver Operations

The AFE has four sets of sampling and convert phases within the active phase of each PRF cycle. The four sampling phases listed in Table 1 can be configured to acquire different signal combinations in different modes of operation.

Table 1. Signal Acquisition in Different Modes of Operation

MODE	MANNER OF SETTING MODE	MAX ACQUISITION RATE	SIGNAL ACQUIRED IN EACH PHASE			
			PHASE 1	PHASE 2	PHASE 3	PHASE 4
PPG only	ENABLE_PTT = 0	1 kHz	PPG(1)	PPG(1)	PPG(1)	PPG
PTT mode (PPG and ECG)	ENABLE_PTT = 1	1 kHz	PPG(1)	PPG(1)	PPG(1)	ECG
ECG only	ENABLE_PTT = 1	4 kHz	Dummy(2)	Dummy	Dummy	ECG

(1) The phases marked PPG correspond either to an LED phase (if the LED is on) or an Ambient phase (if the LED is off).
(2) The dummy phase corresponds to a dummy convert signal.

Figure 27 illustrates the sequence of the signals within the active phase of the pulse repetition cycle.

In the 2-LED mode, LED1 and LED2 are pulsed around the corresponding sampling phases. In the 3-LED mode, LED1, LED2, and LED3 are pulsed around the corresponding sampling phases. The TIA gain (R_F) and feedback capacitor (C_F) can be programmed differently between the four phases. If R_F and C_F must be independently programmed for the first and second phases, then the LED3 ON signal must be programmed even if LED3 is not used. If independent programmability of R_F and C_F is required for the third and fourth phases, an LED4 ON signal (for the physically non-existent LED) must be programmed.

A fourth LED can be optionally connected on the TX4 pin and can be turned on in ambient phase 1. However, operation with all four LEDs turned on in the same PRF cycle is not recommended because such operation does not allow acquisition of the ambient signal (which requires the LEDs to be off). When LED4 is turned on, then use one of the other three phases as the ambient phase.

An interrupt termed *DATA_RDY* can be programmed by setting a start and end count and can be output on the ADC_RDY pin. This signal can serve as an interrupt to the MCU to read data from the AFE every PRF cycle. This interrupt is applicable when the FIFO is not used. When the FIFO is used, this interrupt can be replaced by the FIFO_RDY interrupt.

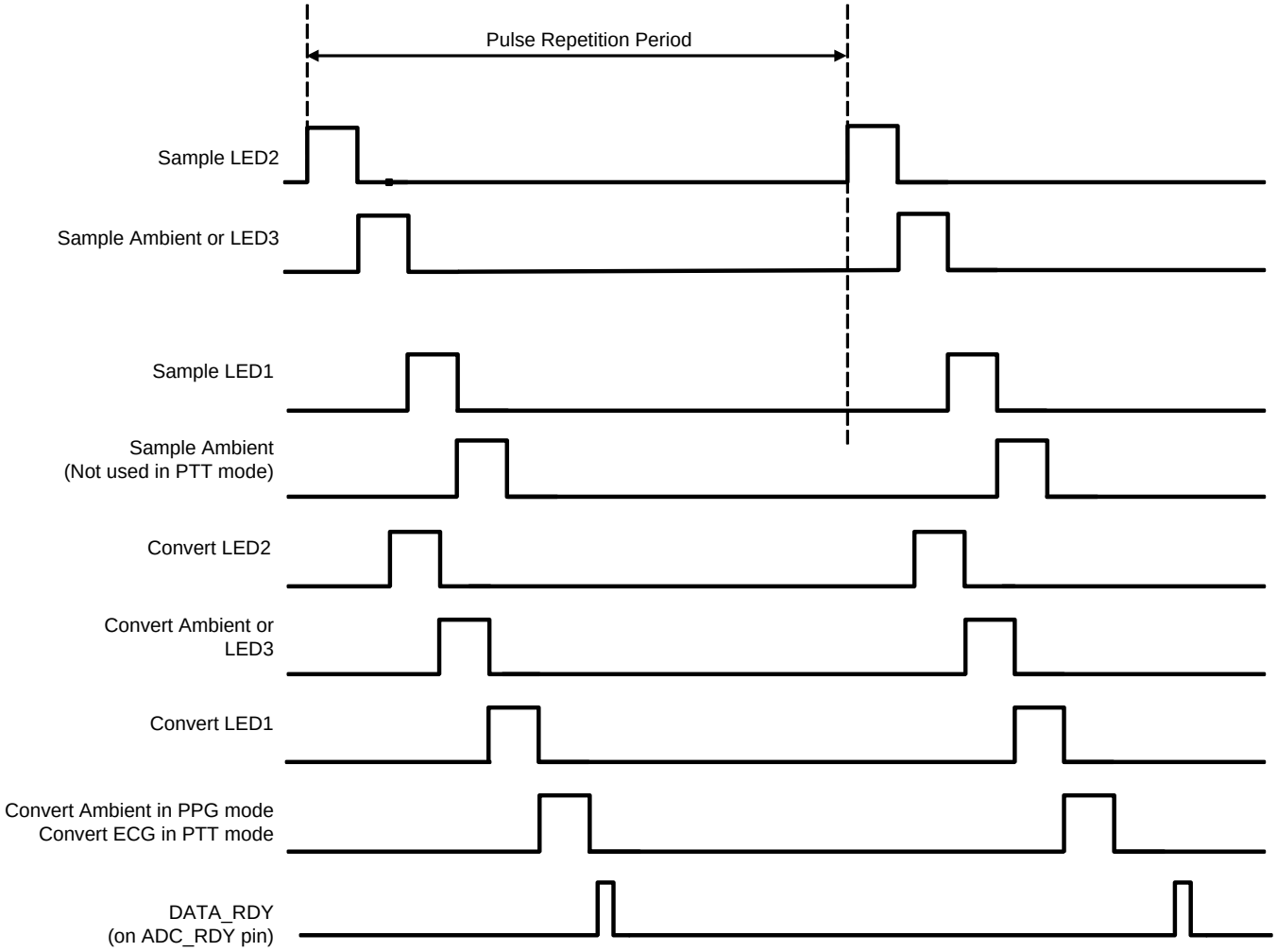


Figure 27. Sequence of Four Sampling and Conversion Phases

8.3.2 TIA Gain and Bandwidth Controls (PPG Signal Chain)

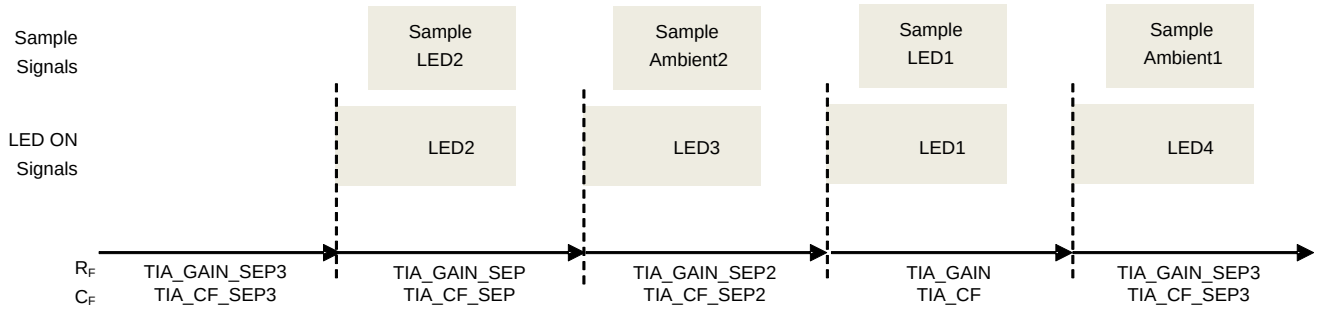
The TIA gain is set by programming the value of R_F (the feedback resistor of the TIA). The R_F setting is controlled using the TIA_GAIN* and TIA_GAIN_SEP* register controls. The TIA feedback capacitance is set by programming the value of C_F. The product of R_F and C_F determines the time constant of the TIA and must be set to approximately 1/5th (or less) of the sampling pulse durations. This choice of time constant allows the TIA to pass the incoming pulses from the photodiode, and for the output to settle close to the steady-state value.

By default, the TIA_GAIN and TIA_CF register controls determine the R_F and C_F applied for all four phases of the receiver. Table 2 lists separate values that can be set for the phases by setting either the ENSEPGAIN or ENSEPGAIN4 bits.

Table 2. Mapping of Register Controls to the R_F and C_F Controls in Various Phases

PHASE	DEFAULT		ENSEPGAIN = 1		ENSEPGAIN4 = 1	
	R_F	C_F	R_F	C_F	R_F	C_F
LED2	TIA_GAIN	TIA_CF	TIA_GAIN_SEP	TIA_CF_SEP	TIA_GAIN_SEP	TIA_CF_SEP
LED3, Ambient2	TIA_GAIN	TIA_CF	TIA_GAIN_SEP	TIA_CF_SEP	TIA_GAIN_SEP2	TIA_CF_SEP2
LED1	TIA_GAIN	TIA_CF	TIA_GAIN	TIA_CF	TIA_GAIN	TIA_CF
Ambient1	TIA_GAIN	TIA_CF	TIA_GAIN	TIA_CF	TIA_GAIN_SEP3	TIA_CF_SEP3

As Figure 28 shows, when ENSEPGAIN4 = 1, the transition points of the four R_F and C_F settings are defined by the start of the corresponding LED phase. Thus, when using separate gains in the four phases, program the LED3 start and end counts even if LED3 is not used and program the LED4 start and end counts even if LED4 is not used. Using four different TIA settings across the four phases may not be a realistic or useful case because TI recommends having the same TIA settings for both the LED and ambient phases.



NOTE: If the order of the LED_ON phases is altered with respect to what is shown in Figure 28, then alter the sequence of the associated SAMP phases correspondingly as well. The mapping of R_F and C_F to the LED_ON, SAMP phases continues to remain as given in Table 2.

Figure 28. TIA R_F, C_F Transitions Within a Period for ENSEPGAIN4 = 1

Table 3 shows the register bits that create the 4-bit controls for the TIA gain. Table 4 and Table 5 list the settings for R_F and C_F, respectively.

Table 3. Mapping of Register Controls to the 4-Bit TIA Gain Control

4-BIT CONTROL	MAPPING OF REGISTER CONTROLS TO CONTROL BITS			
	3	2	1	0
TIA_GAIN	TIA_GAIN_MSB	TIA_GAIN_LSB		
TIA_GAIN_SEP	TIA_GAIN_SEP_MSB	TIA_GAIN_SEP_LSB		
TIA_GAIN_SEP2	TIA_GAIN_SEP2_MSB	TIA_GAIN_SEP2_LSB		
TIA_GAIN_SEP3	TIA_GAIN_SEP3_MSB	TIA_GAIN_SEP3_LSB		

Table 4. TIA_GAIN Register Settings

TIA_GAIN, TIA_GAIN_SEP* REGISTER VALUE	R_F
0	500 kΩ
1	250 kΩ
2	100 kΩ
3	50 kΩ
4	25 kΩ
5	10 kΩ
6	1 MΩ
7	2 MΩ
8	1.5 MΩ
Other settings	Do not use

Table 5. TIA_CF Register Settings

TIA_CF, TIA_CF_SEP* REGISTER VALUE	C_F
0	5 pF
1	2.5 pF
2	10 pF
3	7.5 pF
4	20 pF
5	17.5 pF
6	25 pF
7	22.5 pF

8.3.3 Offset Cancellation DAC (PPG Signal Chain)

A typical optical heart-rate signal has a dc component and an ac component. Although a higher TIA gain maximizes the ac signal at the AFE output, the magnitude of the dc component limits the maximum gain possible in the TIA. In order to decouple the effect of the dc level from the TIA gain setting, a current DAC is placed at the input of the device. By setting a programmable cancellation current (based on the dc current signal level), the effective dc current signal that gets gained up by the TIA can be reduced. This reduction in the effective signal current into the TIA results in the ability to set a higher TIA gain than what is otherwise possible without enabling the offset correction. In each of the four phases of operation, a separate programmable current value can be set by programming four different sets of register bits. These cancellation currents are automatically presented to the input of the TIA in the appropriate sampling phase. The ability to set a different cancellation current in each of the four phases can be used to cancel out the ambient current in the ambient phase. In the LED phase, this ability can be used to cancel out the sum of the ambient current and the dc current component of the heart-rate signal. Figure 29 illustrates the polarities of the signal current and offset cancellation current. The polarity of the offset cancellation current can be reversed by programming the POL_OFFDAC bits.

With zero input current and zero current in the offset cancellation DAC, the output of the AFE is close to zero. Based on the channel offset, the output voltage for zero input current can be a small positive or negative value, usually in the range of several millivolts. With the photodiode connected as depicted in Figure 29 and a signal current coming from the photodiode, the output code of the device is expected to be positive with the offset cancellation DAC set to zero (I_{OFFSET} = 0). With I_{OFFSET} set as a negative (POL_OFFFAC = 1), a dc offset can be subtracted from the signal and the ac signal can be amplified with a higher gain than what is otherwise possible.

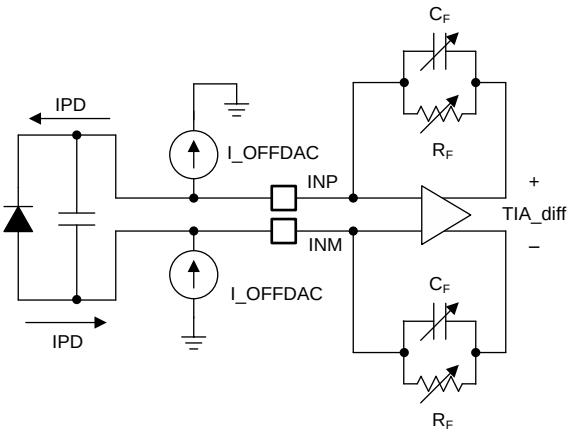


Figure 29. Offset Cancellation Current Polarity Diagram

A breakdown of the signal current and voltage levels is provided in Table 6 for a variety of signal levels. In Table 6, the current transfer ratio (CTR) is used to describe the relationship between the set LED current and the resulting photodiode current (IPD). CTR is defined as the ratio of the photodiode current for a given LED current and is a function of the optical and mechanical parameters as well as human physiology.

Table 6. Signal Current and Voltage Levels for a Hypothetical Use Case(1)

PHASE	ILED (mA)	CTR (µA / mA)	I_{sig} (µA)	I_{amb} (µA)	IPD (µA)	I_OFFDAC (µA)	I_{eff} (µA)	R_F (MΩ)	TIA_diff (V)
LED2	25	0.025	0.625	1	1.625	–1.5	0.125	1	0.25
LED3	50	0.025	1.25	1	2.25	–2	0.25	0.5	0.25
LED1	12.5	0.025	0.3125	1	1.3125	–1	0.3125	0.5	0.3125
Ambient1	0	0.025	0	1	1	–1	0	2	0

(1) ILED is the set LED current; CTR is the current transfer ratio (in µA per mA); I_{sig} is the photodiode signal current resulting from the LED pulsing (I_{sig} = ILED × CTR); I_{amb} is the current in the photodiode resulting from ambient light (that is present in all phases and adds to I_{sig}); IPD is the total input current (I_{sig} + I_{amb}); I_OFFDAC is the current setting of the offset cancellation DAC; I_{eff} is the effective current after offset cancellation (I_{sig} + I_OFFDAC); R_F is the TIA gain setting; and TIA_diff is the output differential signal of the TIA (this signal must be within the range of ±1 V).

The I_OFFDAC* bits control the magnitude of the current subtracted (or added) at the TIA input. The POL_OFFDAC bits determine whether the current is subtracted from or added to the input. Table 7 lists the mapping of the register controls to the 7-bit control for I_OFFDAC. By default, the full-scale current range of the offset cancellation DAC is ±15.75 µA. As shown in Table 8, this range can be extended by using the IFS_OFFDAC register control. Table 9 lists the offset DAC value as a function of the I_OFFDAC*.

Table 7. Mapping of Register Controls to the 7-Bit Control of I_OFFDAC*

7-BIT CONTROL	MAPPING OF REGISTER CONTROLS TO CONTROL BITS						
	6	5	4	3	2	1	0
I_OFFDAC_LED1	I_OFFDAC_LED1_MSB	I_OFFDAC_LED1_MID				I_OFFDAC_LED1_LSB	I_OFFDAC_LED1_LSB_EXT
I_OFFDAC_LED2	I_OFFDAC_LED2_MSB	I_OFFDAC_LED2_MID				I_OFFDAC_LED2_LSB	I_OFFDAC_LED2_LSB_EXT
I_OFFDAC_LED3	I_OFFDAC_LED3_MSB	I_OFFDAC_LED3_MID				I_OFFDAC_LED3_LSB	I_OFFDAC_LED3_LSB_EXT
I_OFFDAC_AMB1	I_OFFDAC_AMB1_MSB	I_OFFDAC_AMB1_MID				I_OFFDAC_AMB1_LSB	I_OFFDAC_AMB1_LSB_EXT

Table 8. Full-Scale Current Control of the Offset Cancellation DAC Using IFS_OFFDAC Control

IFS_OFFDAC VALUE (Binary)	FULL-SCALE CURRENT
000	±15.75 µA
011	±31.5 µA
101	±63 µA
111	. ±126 µA
Other settings	Do not use

Table 9. Mapping of the Offset DAC Setting to the 7-Bit I_OFFDAC* Control(1)(2)(3)

DECIMAL EQUIVALENT OF 7-BIT I_OFFDAC*	OFFSET CANCELLATION DAC CURRENT (µA) FOR DIFFERENT IFS_OFFDAC (Binary Setting)			
	IFS_OFFDAC = 000	IFS_OFFDAC = 011	IFS_OFFDAC = 101	IFS_OFFDAC = 111
0	0	0	0	0
1	0.125	0.25	0.5	1
2	0.25	0.5	1	2
…	…	…	…	…
127	15.75	31.5	63	126

(1) I_OFFDAC* corresponds to one of the four phases.
(2) The offset cancellation DAC is not trimmed at production; therefore, the value of the full-scale current can vary across units by ±20%.
(3) This table corresponds to POL_OFFDAC* = 0. If POL_OFFDAC* = 1, then the previous currents become negative.

The relative accuracy of the current control from the I_OFFDAC*_LSB_EXT bit is worse than the accuracy of the other bits. Additionally, the absolute accuracy of the offset DAC current setting becomes worse at higher settings of IFS_OFFDAC. As illustrated in Figure 13, the noise contribution from the offset DAC also increases for higher current settings. As a result, using the higher offset cancellation currents can result in diminishing returns of SNR.

Figure 30 shows how the offset cancellation DAC transitions by default. The offset DAC transitions to the value set for a given phase at the start of the SAMP phase and returns to the value set for the Ambient1 phase (I_OFFDAC_AMB1) between SAMP phases.

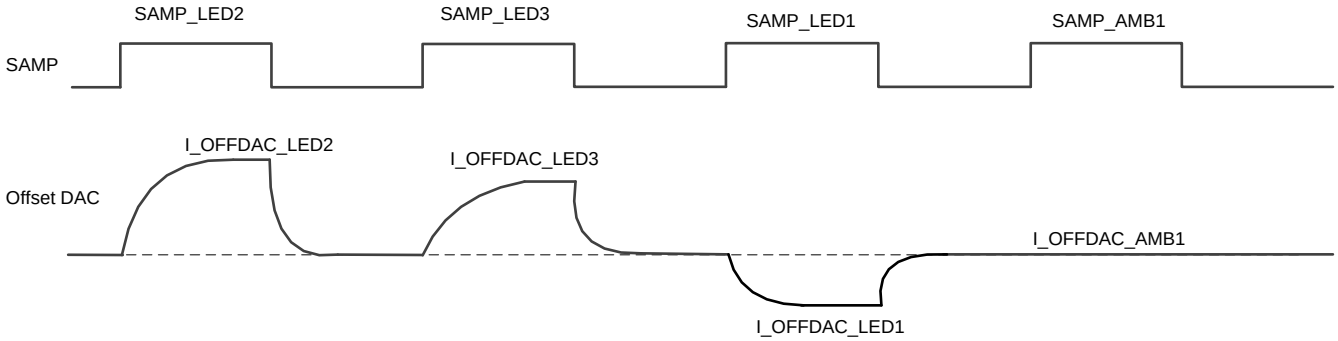


Figure 30. Transitions of the Offset DAC at the SAMP Phases

The transition of the offset DAC can be advanced to happen at the start of the LED_ON signal (as shown in Figure 31) by programming the EARLY_OFFSET_DAC register control; see the *Sampling Width Considerations for PPG Signal Acquisition* section for more details. Using the EARLY_OFFSET_DAC mode allows more time for the TIA output to settle to the current step from the offset DAC because the LED_ON phase is recommended to start earlier than the SAMP phase. Also when using this mode, all four LED_ON phases must be defined.

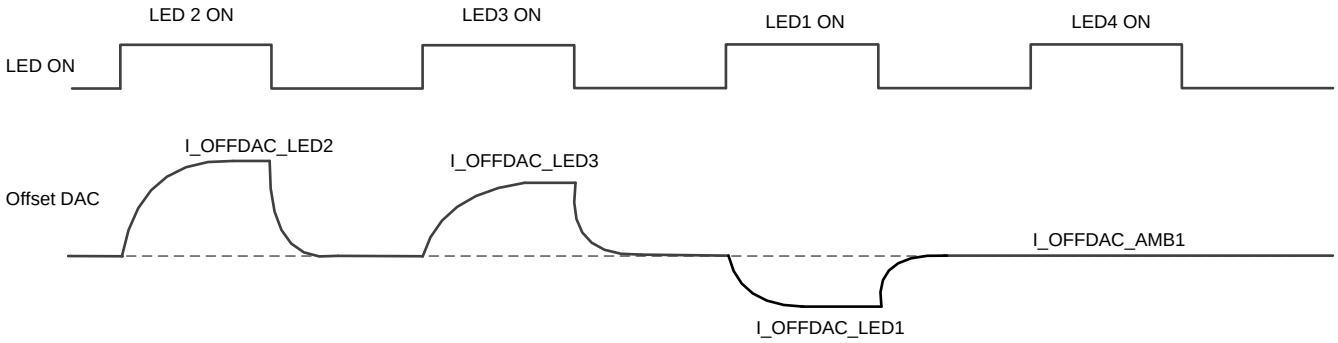


Figure 31. Transitions of the Offset DAC When EARLY_OFFSET_DAC is Set to 1

8.3.4 Noise-Reduction Filter (PPG Signal Chain)

The AFE4900 has a programmable noise bandwidth filter that is connected to the output of the TIA during the SAMP phase. There are four filters, one dedicated for each phase. Each filter is meant to be input with the settled voltage of the TIA output corresponding to that phase, which corresponds to the steady-state envelope of the signal for that phase. For simplicity, the scheme with the four parallel filters is illustrated in Figure 32 for a single-ended representation of the signal chain. The effective bandwidth for both the signal and the noise is determined by the RC time constant of the switched RC filter and the sampling pulse duty cycle. The RC time constant of the filter is programmable. The filter provides noise bandwidth reduction. However, the effective signal bandwidth is also limited at low sampling duty cycles to a value roughly equal to (sampling duty cycle) × f_{RC} kHz, where f_{RC} is the physical 3-dB bandwidth of the filter as determined by the R-C product.

An ADCRST signal is generated automatically by the AFE4900 at the start of the CONV phases, and is used to reset the input capacitance of the ADC buffer prior to each ADC conversion phase. This resetting of the input capacitance of the buffer helps erase the memory from previous conversions. After the ADCRST phase and over the rest of the conversion phase, the output of the corresponding phase filter is connected to the input of the ADC buffer and is converted by the ADC.

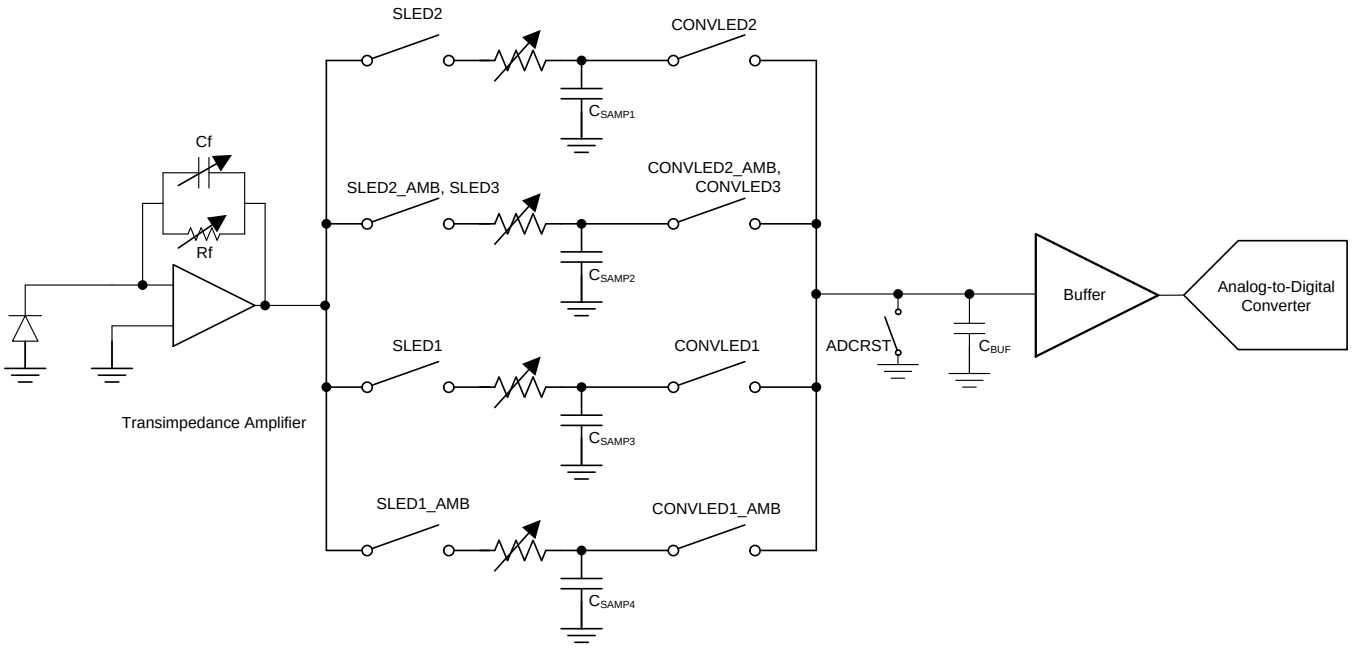


Figure 32. Noise-Reduction Filter Diagram

The filter bandwidth has a default typical value of 2.5 kHz. As shown in Table 10, the bandwidth for the four filters can also be programmed between a typical value of 2.5 kHz (default), 5 kHz, or 10 kHz using the FILTER_BW<1> and FILTER_BW<0> register controls.

Table 10. Filter Bandwidth Set by the FILTER_BW<1:0> Control

FILTER_BW<1>	FILTER_BW<0>	TYPICAL f_{RC} (kHz)(1)
0	0	2.5
0	1	5
1	0	10
1	1	Do not use

(1) The physical bandwidth of the filter is not trimmed and can vary between 65% and 160% of the typical value.

8.3.5 Analog-to-Digital Converter (PPG and ECG Signal Chain)

The AFE has an ADC that is common to both the PPG and ECG signal chains. The ADC provides a 24-bit representation of either the current from the photodiode (in the PPG signal chain) or the voltage from the electrodes (in the ECG signal chain). The ADC codes corresponding to the various sampling phases can be read out from 24-bit registers in two's complement format. The ADC full-scale input range (±FS) is nominally ±1.2 V and spans bits 21 to 0. Table 11 shows the mapping of the ADC input voltage to the ADC code.

Table 11. Mapping the ADC Input Voltage to the ADC Code

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT	24-BIT ADC OUTPUT CODE
–FS	111000000000000000000000
(–FS / 2^{21})	111111111111111111111111
0	000000000000000000000000
(FS / 2^{21})	000000000000000000000001
FS	000111111111111111111111

When the input exceeds the full-scale levels, the output code saturates. The exact saturation value depends on the NUMAV setting. For different NUMAV settings, the saturation value on the positive side is between 1FFF19h and 1FFFFFh and the saturation value on the negative side is between E080E7h and E00000h. This kind of saturation behavior is applicable to the register data corresponding to an individual conversion phase (for example, data in the LED2 phase register). The behavior of the (LED–ambient) register data are different from the one outlined above. Table 12 shows that for the (LED minus ambient) register data, the two MSBs of the 24-bit word serve as sign-extension bits to the 22-bit ADC code, and are equal to the MSB of the 22-bit ADC code when the input to the ADC is within the full-scale range.

Table 12. Using Sign-Extension Bits to Determine the Input Operating Voltage

BITS 23-21	INPUT STATUS
000	Positive and lower than positive full-scale (within full-scale range)
111	Negative and higher than negative full-scale (within full-scale range)
001	Positive and higher than positive full-scale (outside full-scale range)
110	Negative and lower than negative full-scale (outside full-scale range)

Figure 33 shows the TIA has an operating range of ±1 V even though the ADC input full-scale range is ±1.2 V. When setting the TIA gain, make sure that the signal at the TIA output does not exceed ±1 V.

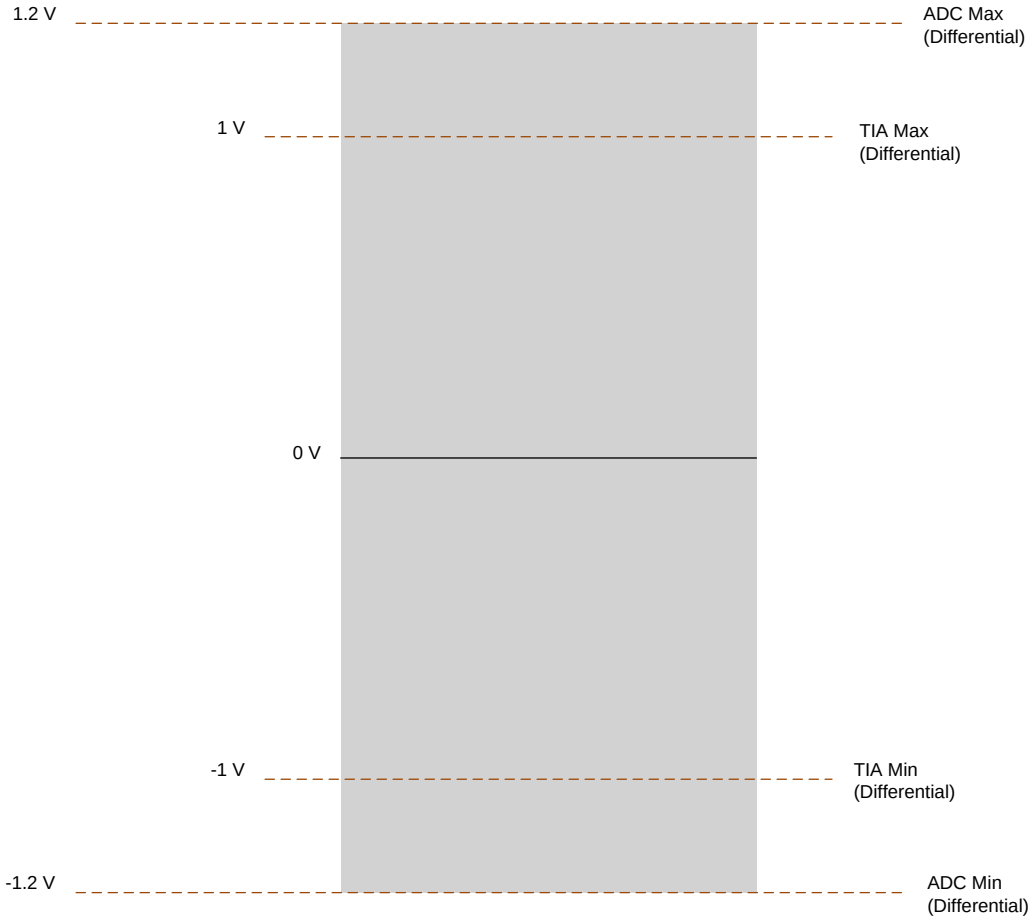


Figure 33. TIA and ADC Dynamic Ranges

To reduce the noise, the input to the ADC (sampled on the C_{SAMPx} capacitors) can be converted by the ADC multiple times and averaged. The number of averages is set using the NUMAV register control as:

$$\text{Number of Averages} = (\text{NUMAV} + 1) \quad (1)$$

By default, NUMAV = 0. Therefore, the default mode corresponds to when the ADC converts the input one time in each of the four phases and stores the content in the register corresponding to that phase.

When NUMAV is programmed (for example, if NUMAV = 3), the ADC converts the input four times in each phase, averages the four conversions, and stores the averaged value in the register corresponding to that phase. Averaging only helps in reducing ADC noise and not the front-end noise because the input to the ADC is the same sampled voltage across all ADC conversions used to generate the average (this voltage corresponds to the voltage sampled on the C_{SAMPx} capacitors). The number of samples that can be averaged ranges from 1 to 16 (when NUMAV is programmed from 0 to 15). A higher number of averages results in larger conversion times.

Averaging is implemented as shown in Equation 2; the number of ADC samples corresponding to the number of averages (NUMAV + 1) are accumulated:

$$\text{SUMADC} = \sum_{i=1}^{(NUMAV+1)} (\text{ADCi}) \quad (2)$$

where

- ADCi = the i^{th} sample converted by the ADC

The accumulator output (SUMADC) is then divided by a factor D that is obtained by D = 128 / X , with X being an integer. The averaged output is calculated as:

$$\text{ADCOUT} = \text{SUMADC} / D \quad (3)$$

where

- D = 128 / X, with X being an integer

Table 13 shows that this implementation gives an averaging function that is exact when the number of averages is a power of 2 but deviates from ideal values for other settings.

Table 13. Average Mode Settings

NUMAV	NUMBER OF AVERAGES	INTEGER (X)	DIVISION FACTOR (D)
0	1	128	1.0
1	2	64	2.0
2	3	43	2.97
3	4	32	4.0
4	5	26	4.92
5	6	21	6.10
6	7	18	7.11
7	8	16	8.0
8	9	14	9.14
9	10	13	9.85
10	11	12	10.67
11	12	11	11.64
12	13	10	12.8
13	14	9	14.22
14	15	9	14.22
15	16	8	16.0

When using PTT mode, the NUMAV register control gets applied to the fourth phase (ECG signal acquisition phase) in the following manner:

- When chopping mode is disabled (ENABLE_ECG_CHOP = 0): Table 13 lists the averaging factors that the ADC operates with.
- When chopping mode is enabled (ENABLE_ECG_CHOP = 1): the ADC preforms two conversions as though NUMAV is set to 1. This case is independent of the setting of the NUMAV register control. To ensure that the CONV width is sufficient for the two conversions, set NUMAV to a value of 1 or higher.

8.3.6 LED Current Driver (PPG Signal Chain)

The AFE generates the drive current for the LEDs using an internally generated reference voltage termed *TX_REF*. A voltage-to-current conversion circuit is used to convert the TX_REF voltage to the programmed LED current range, and an 8-bit current DAC is used to set the current of the LED driver to the programmed value. Figure 34 shows the switches that are controlled by the LED_ON signals and that are used to route the LED driver current to the appropriate TX pin. The AFE has two identical LED drivers. Both drivers can be made to operate over a current range of 0-50 mA or 0-100 mA. By default, only LED driver 1 is active.

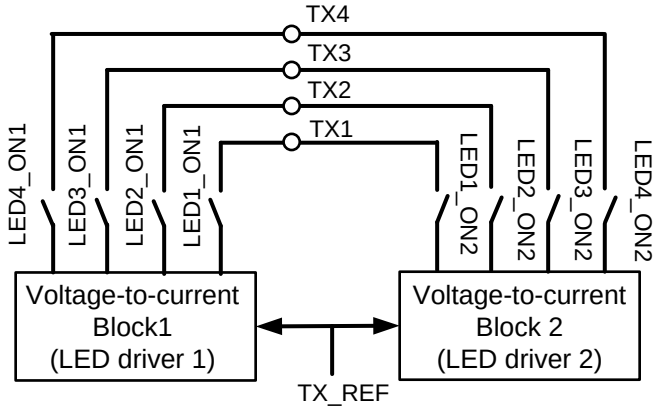


Figure 34. Support of Parallel LED Drivers

The default LED current range is from 0 mA to 50 mA. The individual currents of each of the three LEDs can be controlled independently with separate 8-bit controls. Table 14 shows that the 8-bit LED control is split into two sets of register controls.

Table 14. Mapping of Register Controls to the 8-Bit LED Current Control

8-BIT CONTROL	MAPPING OF REGISTER CONTROLS TO CONTROL BITS							
	7	6	5	4	3	2	1	0
ILED1	ILED1_MSB						ILED1_LSB	
ILED2	ILED2_MSB						ILED2_LSB	
ILED3	ILED3_MSB						ILED3_LSB	
ILED4	ILED4_MSB						ILED4_LSB	

Taken as a decimal number, the 8-bit setting provides 255 steps between 0 mA and 50 mA. Each increment of the ILED 8-bit code causes the LED current setting to increment by approximately 0.2 mA. The LED current range can be programmed using the ILED_FS register control. This register control, as shown in Table 15, changes the full-scale LED driver current by changing the voltage on TX_REF.

Table 15. Registers for the Full-Scale LED Current Control

ILED_FS REGISTER CONTROL	FULL-SCALE LED DRIVER CURRENT	TX_REF VOLTAGE
0	50 mA	0.15 V
1	100 mA	0.3 V

Table 16 shows the register control mapping of the 50-mA and 100-mA current modes to the LED current.

Table 16. LED Current Setting versus ILED Values as Set by the Registers (each driver)

ILED1, ILED2, ILED3 REGISTER VALUES (Decimal Equivalent of 8-Bit Code)	NOMINAL LED CURRENT SETTING (mA) IN 50-mA MODE	NOMINAL LED CURRENT SETTING (mA) IN 100-mA MODE
0	0	0
1	0.196	0.392
2	0.392	0.784
…	…	…
255	50	100

The control signals for the switches connected to each driver are derived from the LED*_ON signals generated by the timing engine as defined by the start and end counts. The control signals connected to each driver can be masked in a programmable manner. By default, only LED driver 1 is active and the control signals for the switches connected to LED driver 1 (LED*_ON1) are set using the LED_ON signals. Table 17 shows how the control signals for LED driver 1 and LED driver 2 can be modified using the DIS_DRV1_LEDx and EN_DRV2_LEDx register controls, respectively.

Table 17. Registers for Controlling the LED Driver 1 and LED Driver 2 Control Signals

REGISTER CONTROL(1)	LED DRIVER CONTROL SIGNALS MAPPING TO LED_ON SIGNALS(1)
DIS_DRV1_LEDx (Default = 0)	LEDx_ON1 = LEDx_ON, $\overline{\text{DIS\_DRV1\_LEDx}}$ (Default = Active)
EN_DRV2_LEDx (Default = 0)	LEDx_ON2 = LEDx_ON, EN_DRV2_LEDx (Default = Inactive)

(1) x refers to the LED number (LED1, LED2, LED3, or LED4).

The DIS_DRV1_LEDx and EN_DRV2_LEDx controls can be used to turn on two LEDs simultaneously. For example, to turn on LED1 and LED2 simultaneously, the following settings can be used:

- Program LED1_ON and LED2_ON to be identical (coincident) signals
- Program the LED current settings ILED1 and ILED2 to be the same value
- Route the current of only LED driver 1 to TX1 during LED1_ON active by setting DIS_DRV1_LED1 = 0, EN_DRV2_LED1 = 0
- Route the current of only LED driver 2 to TX2 during LED2_ON active by setting DIS_DRV1_LED2 = 1, EN_DRV2_LED2 = 1

The DIS_DRV1_LEDx and EN_DRV2_LEDx controls can also be used to route the current from both the LED drivers to the same LED. When operating in this mode, where two LEDx_ON signals are made active at the same time, operate the receiver with a common gain set for all four phases (with ENSEPGAIN = 0 and ENSEPGAIN4 = 0). The two parallel LEDs are also recommended to be connected to (TX2, TX3) or (TX1, TX4). Table 18 lists various use cases for the full-scale LED current and headroom voltages.

Table 18. Full-Scale LED Current and Headroom Voltages

ILED_FS REGISTER CONTROL	1 LED DRIVER ON		2 LED DRIVERS ON, THROUGH 1 LED		2 LED DRIVERS ON, THROUGH 2 LEDS	
	FULL-SCALE CURRENT(1)	V_{HR}(2)	FULL-SCALE CURRENT(1)	V_{HR}(2)	FULL-SCALE CURRENT(1)	V_{HR}(2)
0	50 mA	320 mV	100 mA	370 mV	50 mA	345 mV
1	100 mA	600 mV	200 mA	650 mV	100 mA	625 mV

(1) Full-scale current per LED.
(2) Typical voltage headroom required for the LED driver.

The parameter V_{HR} mentioned in Table 18 refers to the typical voltage headroom required for the LED driver when operating at a LED code corresponding to the full-scale current for the ILED_FS setting. If the battery is directly used to drive TX_SUP, then the V_{HR} can be interpreted as the voltage that, when added to the forward voltage of the LED and any other resistor voltage drops in the current path, signifies the lowest voltage that the battery can discharge to before the LED driver current starts to fall. If using a boost converter to drive TX_SUP, the boost converter output voltage can be chosen as the sum of V_{HR} and the maximum forward voltage of the LED and any other resistive drops, with an additional approximate 300 mV added for extra margin.

8.3.7 ECG Signal chain

This section describes the blocks used in the ECG signal acquisition. The ECG signal chain can be enabled by setting the ENABLE_PTT register control. This control enables synchronized ECG and PPG signal acquisition. The ADC is common between both the PPG and ECG signal chains.

8.3.7.1 Instrumentation Amplifier (INA) and RLD Amplifier

The front-end of the ECG signal chain is an INA with the programmable gain between 2 to 12. Table 19 lists which GAIN_ECG register control value is used to program the INA gain.

Table 19. Register Control for the ECG Gain Setting

GAIN_ECG REGISTER VALUE	INA GAIN SETTING
0	3
1	2
2	4
3	5
4	6
5	9
6	12

The INA has low-frequency noise that can affect the ECG signal chain acquisition. By setting the ENABLE_ECG_CHOP bit, the low-frequency noise from the ECG signal chain can be shifted to a higher frequency. This chopping is done by having the ADC convert the ECG signal chain twice each PRF cycle with the chopping switches changing state between the two conversions.

When the ENABLE_ECG_CHOP is set to 1 (chop function enabled), the NUMAV control is ignored for the ECG conversion and the ADC converts the ECG signal twice every PRF cycle. In this case, set the width of the CONV signal for the ECG corresponding to a NUMAV of 1 (ADC averages = 2) or higher (if more averaging is needed for the PPG signal acquisition) to ensure sufficient conversion time.

The ECG input pins are meant to operate with a common-mode voltage of 0.9 V. This setting of input common-mode voltage is to ensure that the INA output common-mode voltage is also at 0.9 V. A feedback circuit using an RLD amplifier between the INA outputs and the inputs can be used to maintain the input bias. The RLD output amplifier can be enabled using the ENABLE_RLD bit. The SHORT_ECG_TO_RLD register control can be used to short the ECG input pins (INP_ECG, INM_ECG) internally to RLD_OUT. The SHORT_ECG_TO_RLD is a diagnostic feature and not meant to be used in normal operation.

Figure 35 shows the RLD_OUT generation scheme.

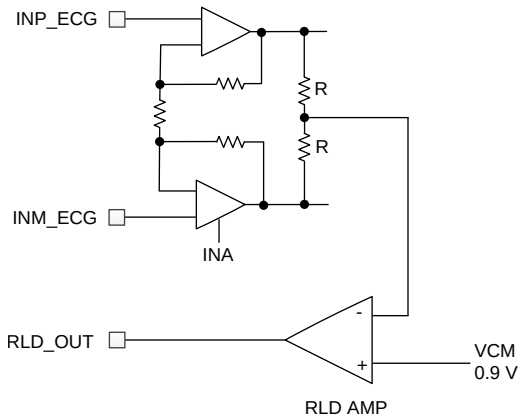


Figure 35. Generation of RLD_OUT

RLD_OUT can be used to bias the input common-mode of the ECG input pins; see the *Reference Circuits for ECG Signal Acquisition* section.

8.3.7.2 ECG Lead-Off Detect

To detect the presence or absence of ECG electrodes on the ECG input pins, the AFE has two types of lead-off detect scheme: dc lead-off detect and ac lead-off detect. The selection between the two schemes is done using the CHOOSE_AC_LEADOFF register control.

8.3.7.2.1 DC Lead-Off Detect Scheme

The dc lead-off detect scheme is chosen when the CHOOSE_AC_LEADOFF register bit is 0. In the dc lead-off scheme, programmable dc current sources on the INP_ECG and INM_ECG pins can be independently configured to source or sink current into the ECG input pins. The current sources are connected to the input pins by setting the EN_ILEADOFF register bit. By enabling the EN_LEADOFF_COMP register bit, the voltages at INP_ECG and INM_ECG are compared against a low threshold and a high threshold. The comparison results can be read out from a register to determine if the ECG leads are connected or not. Figure 36 shows the dc lead-off detect scheme.

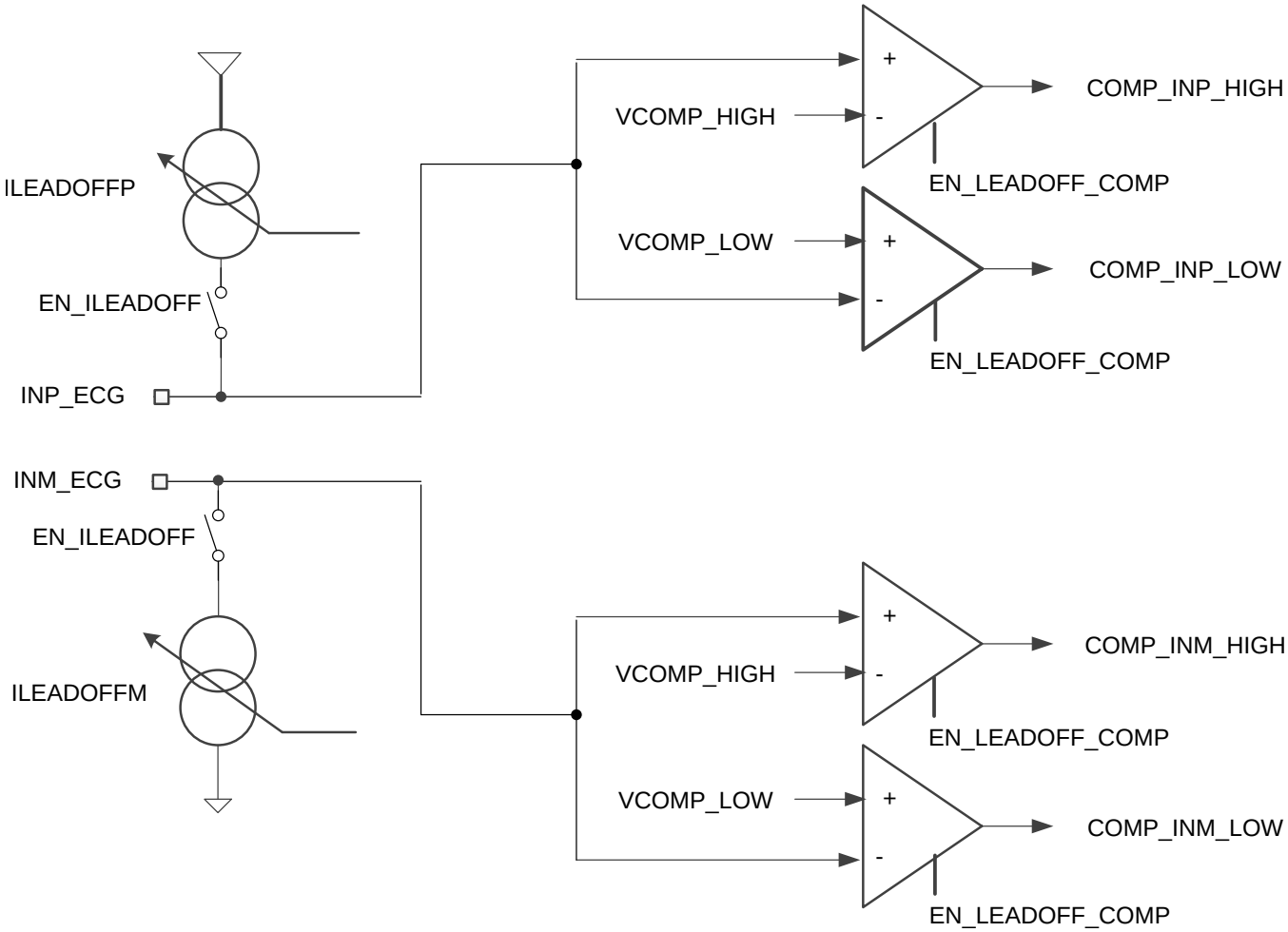


Figure 36. Circuit for the DC Lead-Off Detect Scheme

As illustrated in Table 20, the magnitude of ILEADOFFP, ILEADOFFM can be programmed using the MAG_ILEADOFF register control.

Table 20. Register Setting for Programming Magnitude of Lead-Off Current

MAG_ILEADOFF REGISTER VALUE	MAGNITUDE OF LEAD-OFF CURRENTS ILEADOFFP, ILEADOFFM
0	12.5 nA
1	25 nA
2	50 nA
3	100 nA

As shown in Table 21, the polarity of ILEADOFFP and ILEADOFFM can be independently programmed as source or sink using the POL_ILEADOFFP and POL_ILEADOFFM register controls. For example, when POL_ILEADOFFP is 0 and POL_ILEADOFFM is 1, then the current source ILEADOFFP flows (sources) into INP_ECG and the current source ILEADOFFM flows (sinks) out of INM_ECG (both current sources having the magnitude of current as programmed using the MAG_ILEADOFF control). In this case, the voltage on INP_ECG going high and the voltage on INM_ECG going low can be used to detect the absence of lead connection. The current sources on INP_ECG and INM_ECG must be set to opposite polarities.

Table 21. Register Setting for Programming Polarity of ILEADOFFP, ILEADOFFM

POL_LEADOFFP(M) REGISTER SETTING(1)	DIRECTION OF ILEADOFFP, ILEADOFFM INTO ECG_INP, ECG_INM
0	Source
1	Sink

(1) Set POL_OFFDACP and POL_OFFDACM to opposite values.

As shown in Table 22 and Table 23, the reference voltages VCOMP_HIGH and VCOMP_LOW are programmable using the PROG_VCOMP_HIGH and PROG_VCOMP_LOW register controls. Although VCOMP_HIGH and VCOMP_LOW are independently programmable, TI recommends that these reference voltages be set such that the average (common-mode) voltage of VCOM_HIGH and VCOMP_LOW is maintained as 0.9 V. For example, if VCOMP_HIGH is set to 1.1 V, then set VCOMP_LOW to 0.7 V.

Table 22. Register Setting for Programming VCOMP_HIGH

PROG_VCOMP_HIGH REGISTER VALUE	VCOMP_HIGH VOLTAGE
0	1.15 V
1	1.1 V
2	1.05 V
3	1.0 V
4	1.35 V
5	1.3 V
6	1.25 V
7	1.2 V

Table 23. Register Setting for Programming VCOMP_LOW

PROG_VCOMP_LOW REGISTER VALUE(1)	VCOMP_LOW VOLTAGE
0	0.65 V
1	0.7 V
2	0.75 V
3	0.8 V
4	0.45 V
5	0.5 V
6	0.55 V
7	0.6 V

(1) Set the PROG_VCOMP_LOW setting to be same value as the PROG_VCOMP_HIGH setting to ensure that the average value is maintained as 0.9 V.

The comparator decisions COMP_INP_HIGH, COMP_INP_LOW, COMP_INM_HIGH, and COMP_INM_LOW can be read out through the RCOMP_INP_HIGH, RCOMP_INP_LOW, RCOMP_INM_HIGH, and RCOMP_INM_LOW register bits, respectively.

8.3.7.2.2 AC Lead-Off Detect Scheme

The ac lead-off detect scheme is enabled by programming the CHOOSE_AC_LEADOFF register bit to 1. Figure 37 shows the ac detect scheme. Set the EN_ILEADOFF bit to 1 to enable the current sources; the magnitude of the ILEADOFFP and ILEADOFFM current sources are programmed using the MAG_ILEADOFF register control. Also, set POL_LEADOFFP and POL_LEADOFFM to opposite settings (for example, POL_OFFDACP = 0 and POL_OFFDACM = 1, or vice versa). The polarity of the current sources is then automatically switched across PRF cycles at a rate programmable to PRF / 2 or PRF / 4. The strength of the switching frequency component in the ECG output of the AFE can be used to determine the lead-off state.

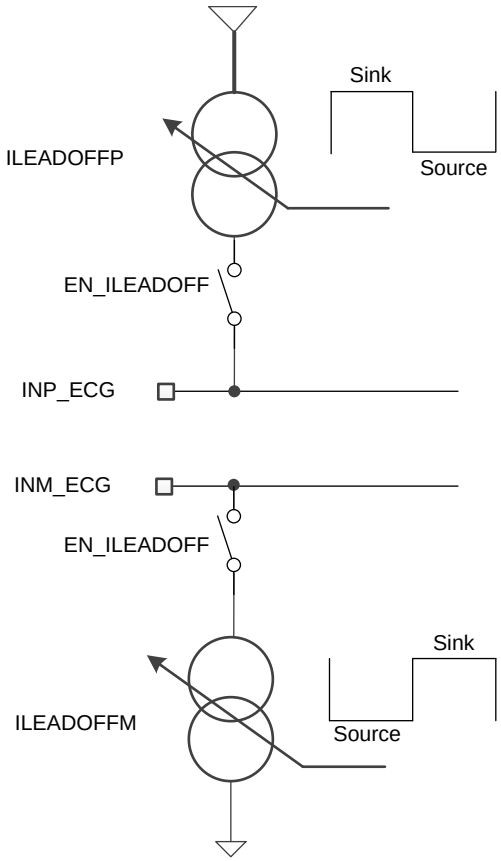


Figure 37. Circuit for the AC Lead-Off Detect Scheme

The ac lead-off switching frequency can be set using the AC_LEADOFF_FREQ register control. Table 24 shows the scheme for setting the ac lead-off switching frequency.

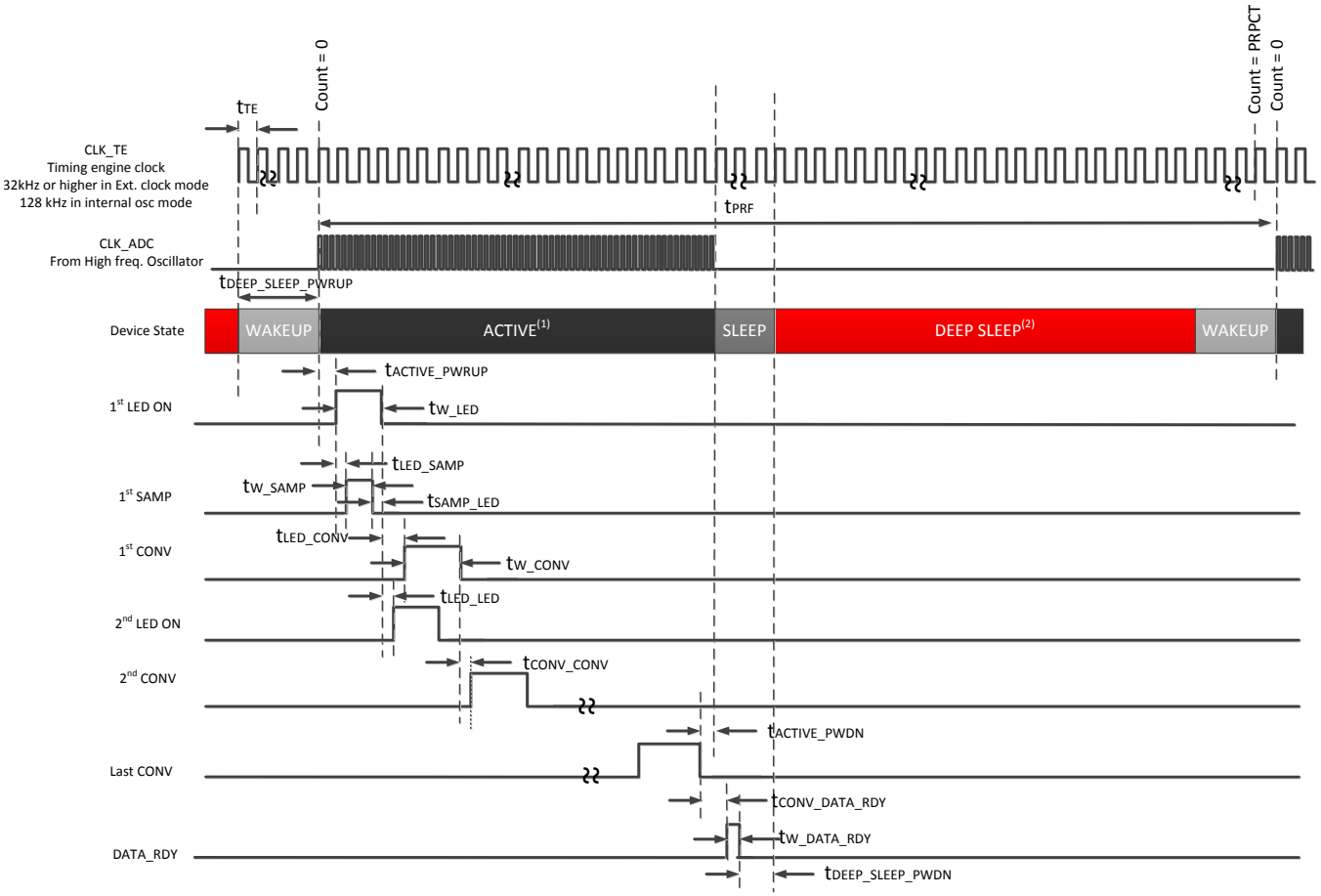
Table 24. Scheme for Setting the AC Lead-Off Switching Frequency

AC_LEADOFF_FREQ	SWITCHING FREQUENCY OF ILEADOFF	REPETITIVE PATTERN ON POLARITY OF ILEAOFF(1)			
		PRF CYCLE 1	PRF CYCLE 2	PRF CYCLE 3	PRF CYCLE 4
0	PRF / 4(2)	INP – SOURCE INM – SINK	INP – SOURCE INM - SINK	INP – SINK INM – SOURCE	INP – SINK INM – SOURCE
1	PRF / 2(2)	INP – SOURCE INM – SINK	INP – SINK INM – SOURCE	INP – SOURCE INM – SINK	INP – SINK INM – SOURCE

(1) Ensure that POL_OFFDACP and POL_OFFDACM are programmed to complementary values.
(2) PRF also corresponds to the ECG sampling rate, f_{ECG}.

8.3.8 Timing Engine

The AFE has an internal programmable timing engine that generates a repetitive pattern of signals at a rate referred to as the *pulse repetition frequency* (PRF). Operating the device in a mode called the ultra-low power (ULP) mode (ENABLE_ULP = 1), provides complete flexibility in dynamically power cycling the various blocks by programming the associated signals using the timing engine. This results in a highly power efficient operation. The timing engine can be configured to either run off an external clock provided on the CLK pin, or use an internally generated clock from a 128-kHz oscillator. The PRF is determined by the PRPCT register control. The high-frequency (4 MHz) oscillator required by the ADC for conversion can be turned on during the active phase. Figure 38 shows how various clocking signals can be used.



Set CONTROL_DYN_TIA = 1 and CONTROL_DYN_ADC = 1 to power up the TIA and ADC in active phase. Set the timing counts for DYN_CLK, DYN_TIA, and DYN_ADC to coincide with the active phase.

Set CONTROL_DYN_BIAS = 1, CONTROL_DYN_TX(1) = 1, CONTROL_DYN_TX(0) = 1, CONTROL_DYN_BG = 1, CONTROL_DYN_VCM = 1, to power down the TX, Band-gap references, and VCM buffer in the Deep sleep phase. In LDO Enable mode: Additionally set CONTROL_DYN_ALDO = 1, CONTROL_DYN_DLDO = 1, and SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP = 1.

Figure 38. Timing Scheme Governing a PRF Cycle

The AFE4900 has two main phases of operation: active and deep sleep. The active and deep sleep phases can be programmed by setting the start and end counts using the timing registers. In the deep sleep phase, the entire AFE4900 is put into an extremely low-power state. In the active phase, all blocks in the transmitter and receiver are active. The active phase contains all the LED_ON, sampling, and CONV signals.

Figure 39 shows the clocking scheme. The device can be operated either using an external clock (in external clock mode) or via the internal 128-kHz oscillator (in internal oscillator mode set by OSC_ENABLE = 1). The internal oscillator has some frequency inaccuracy and, for this reason, the external clock mode may be preferred. Alternatively, the frequency error of the internal oscillator can be estimated by the MCU by using a more accurate clock to measure the periodicity of the interrupts from the AFE. This frequency error can then be digitally compensated when calculating the heart rate. When operating in external clock mode, the frequency of the external clock determines the timing resolution of the timing counts. Using a clock frequency of 32 kHz results in a timing resolution of 31.25 µs. Operating at a lower clock frequency than this frequency is not recommended because the timing resolution may be insufficient at even lower clock frequencies.

The timing engine generates the timing signals for the active phase (LED_ON, SAMP, and CONV) as well as the dynamic controls to power-down the various blocks when in deep sleep phase. Figure 39 shows the clocking scheme and the clock domains.

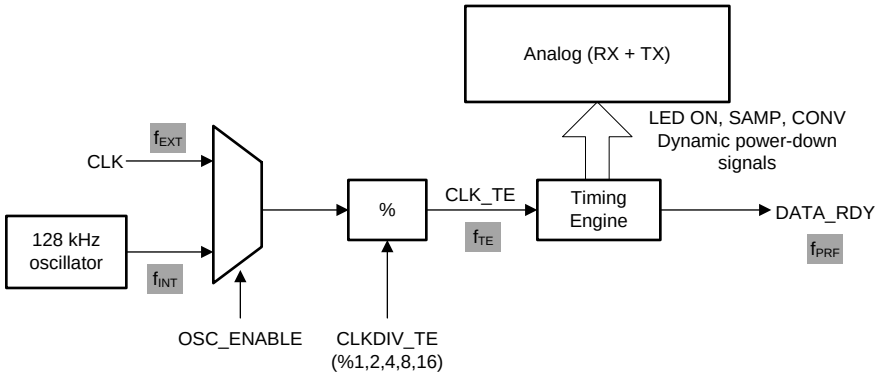


Figure 39. Clocking Scheme

Table 25 lists the clock domains.

Table 25. Clock Domains

SIGNAL	FREQUENCY	COMMENT
CLK	32 kHz to 4 MHz (f_{EXT})	External clock input for use in external clock mode.
CLK_INT	128 kHz (f_{INT})	Output clock of the 128-kHz oscillator for use in internal oscillator mode.
CLK_TE	f_{INT} or f_{EXT}	For example, all timing signal counts have a step size of 31.25 µs (when in external clock mode with a CLK frequency of 32 kHz and CLKDIV_TE is set to the default of divide-by-1).
DATA_RDY	50 Hz (f_{PRF})	Interrupt signal when PRPCT is set to a decimal value corresponding to 640 counts.

Table 26 shows how the timing engine can be divided using the CLKDIV_TE register setting. Dividing the clock to the timing engine results in a lower timing resolution for the timing counts.

Table 26. Division of the Clock to the Timing Engine

CLKDIV_TE REGISTER VALUE	DIVISION RATIO
0	1
4	2
5	4
6	8
7	16
Other settings	Do not use

Table 27 lists the specifications for the timing parameters illustrated in Figure 38. All these timings correspond to the physical timing instants. To map the physical time instants to the counts programmed in the timing registers, see Table 28.

Table 27. Timing Parameters Associated With the PRF Cycle

		MIN	TYP	MAX	UNIT
f_{EXT} ($1/t_{EXT}$)	Frequency of the external clock on the CLK pin	32		4000	kHz
f_{PRF} ($1/t_{PRF}$)	Pulse repetition frequency as set by the PRPCT register	20		1000	Hz
$t_{DEEP\_SLEEP\_PWRUP}$	End of deep sleep phase to start of active phase (as determined by DYN_TIA_STC, DYN_ADC_STC, DYN_CLK_STC)	200 (1)			µs
t_{ACTIVE_PWRUP}	Start of active phase to the start of the first LED_ON signal	300 (1)			µs
t_{W_LED}	LED_ON width	55	$3 \times t_{TE}$ (2) (3)		µs
t_{LED_SAMP}	LED_ON start to SAMP start	25	$1 \times t_{TE}$ (3) (4)		µs
t_{W_SAMP}	SAMP phase duration	30	$2 \times t_{TE}$ (3)		µs
t_{SAMP_LED}	SAMP end to LED_ON end	0			µs
t_{LED_LED}	LED_ON end to next LED_ON start	$1 \times t_{TE}$ (5)			µs
t_{LED_CONV}	LED_ON end to corresponding CONV phase start	$1 \times t_{TE}$			µs
t_{W_CONV}	CONV phase duration: external clock mode	52.3 × NUMAV + 67 (6)			µs
	CONV phase duration: internal oscillator mode	56.5 × NUMAV + 72 (7)			µs
t_{CONV_CONV}	End of CONV phase to start of next CONV phase	$1 \times t_{TE}$			µs
t_{ACTIVE_PWDN}	End of last CONV to end of active phase (determined by DYN_TIA_ENDC, DYN_ADC_ENDC, DYN_CLK_ENDC)	15	$2 \times t_{TE}$		µs
$t_{CONV\_DATA\_RDY}$	End of last CONV to start of DATA_RDY pulse	$6 \times t_{TE}$			µs
$t_{W\_DATA\_RDY}$	DATA_RDY pulse duration	$1 \times t_{TE}$			µs
$t_{DEEP\_SLEEP\_PWDN}$	DATA_RDY fall to start of deep sleep phase (determined by DEEP_SLEEP_STC)	$5 \times t_{TE}$			µs

(1) If the PRF setting is high, then there may not be sufficient time to put the device in deep sleep and recover in time for the next active phase. In that case, define the deep sleep phase to have zero duration (this setting can be done by setting the start and end counts to a value greater than PRPCT). The active phase must be defined to span the full PRF cycle. In this case, the t_{ACTIVE_PWRUP} and t_{ACTIVE_PWDN} parameters are not applicable and can be considered as having a value of 0.
(2) Throughout this table, t_{TE} refers to one clock period of the 32-kHz clock.
(3) See the *Sampling Width Considerations for PPG Signal Acquisition* section.
(4) See the *Reducing Sensitivity to Ambient Light Modulation* section.
(5) Assuming that TIA does not saturate in any of the phases. If the TIA saturates in an LED_ON phase, then a longer separation may be required to allow the TIA output to settle before entering the next LED_ON phase.
(6) To convert to timing counts, divide by t_{TE} and round off to the next highest integer. For example, If NUMAV = 1 (two ADC averages), then t_{W_CONV} = 119.3 µs. With an external clock of 32 kHz, this time duration corresponds to $4 \times t_{TE}$. To achieve this CONV width, the register setting must have the relation *CONVEND = *CONVST + 3.
(7) When using the 128-kHz internal clock, use t_{TE} = 7.8125 µs. For example, if NUMAV = 1 (two ADC averages), then t_{W_CONV} = 128.5 µs. This time duration corresponds to $17 \times t_{TE}$. To achieve this CONV width, the register setting must have the relation *CONVEND = *CONVST + 16.

Figure 40 shows the timing diagram associated with the various programmable phases.

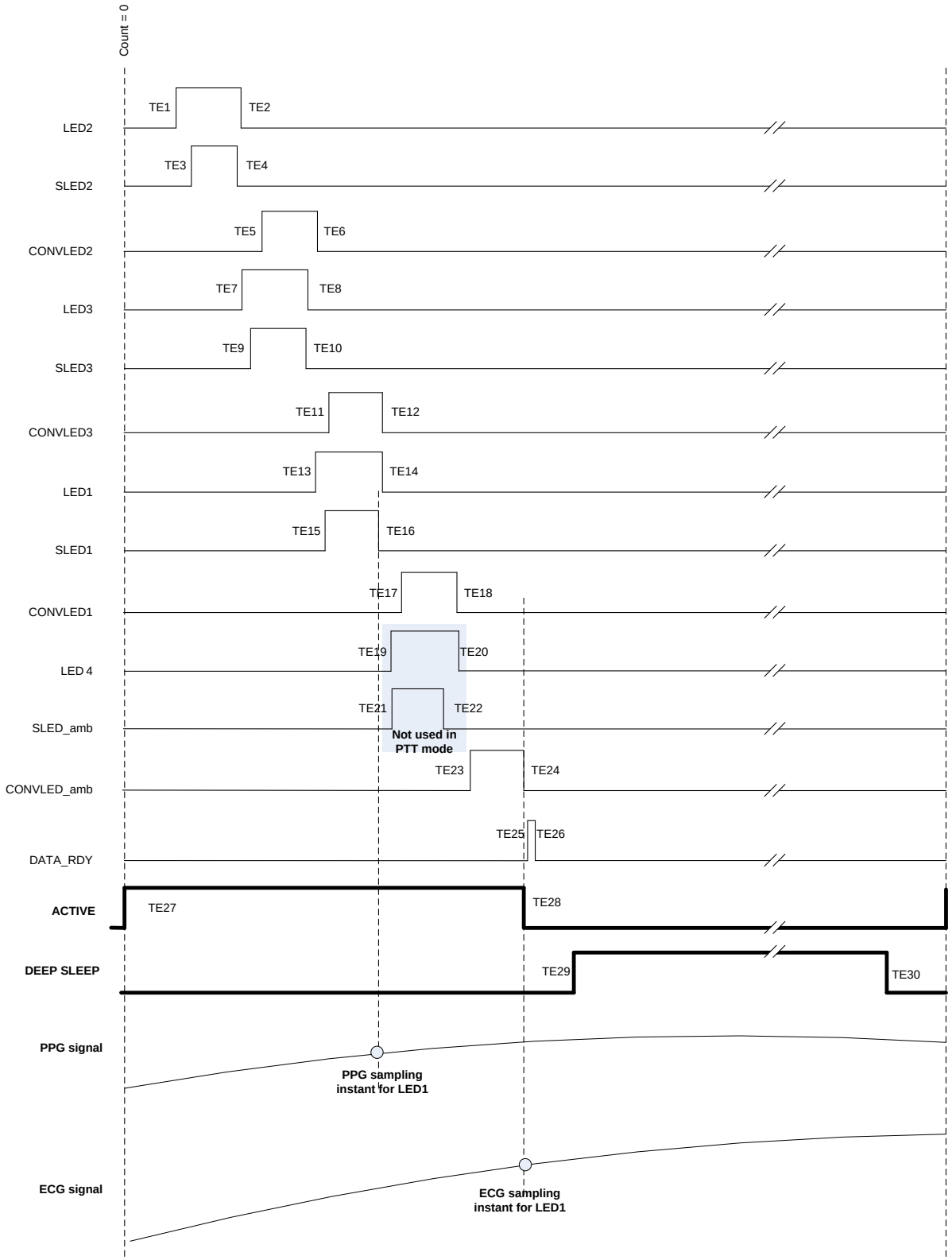


Figure 40. Timing Diagram of Various Programmable Signal Phases

Table 28 lists the register controls for the signals specified by the timing engine.

Table 28. Timing Register and Edge Details

TIMING SIGNAL	DESCRIPTION	ADDRESS (Hex) OF CONTROLLING REGISTER	ASSOCIATED TIMING EDGE	TIME INSTANT RELATION OF ACTUAL EVENT TO REGISTER VALUE IN DECIMAL (REGVAL)
LED2STC	Sample LED2 start	1h	TE3	REGVAL × t_{TE}
LED2ENDC	Sample LED2 end	2h	TE4	(REGVAL+1) × t_{TE}
LED1LEDSTC	LED1 start	3h	TE13	REGVAL × t_{TE}
LED1LEDENDC	LED1 end	4h	TE14	(REGVAL+1) × t_{TE}
LED3STC	Sample Ambient2 (or sample LED3) start	5h	TE9	REGVAL × t_{TE}
LED3ENDC	Sample Ambient2 (or sample LED3) end	6h	TE10	(REGVAL+1) × t_{TE}
LED1STC	Sample LED1 start	7h	TE15	REGVAL × t_{TE}
LED1ENDC	Sample LED1 end	8h	TE16	(REGVAL+1) × t_{TE}
LED2LEDSTC	LED2 start	9h	TE1	REGVAL × t_{TE}
LED2LEDENDC	LED2 end	Ah	TE2	(REGVAL+1) × t_{TE}
ALED1STC	Sample Ambient1 start(1)	Bh	TE21	REGVAL × t_{TE}
ALED1ENDC	Sample Ambient1 end(1)	Ch	TE22	(REGVAL+1) × t_{TE}
LED2CONVST	LED2 convert phase start	Dh	TE5	REGVAL × t_{TE}
LED2CONVEND	LED2 convert phase end	Eh	TE6	(REGVAL+1) × t_{TE}
LED3CONVST	Ambient2 (or LED3) convert phase start	Fh	TE11	REGVAL*t_{TE}
LED3CONVEND	Ambient2 (or LED3) convert phase end	10h	TE12	(REGVAL+1) × t_{TE}
LED1CONVST	LED1 convert phase start	11h	TE17	REGVAL × t_{TE}
LED1CONVEND	LED1 convert phase end	12h	TE18	(REGVAL+1) × t_{TE}
ALED1CONVST	Ambient1 convert phase start(2)	13h	TE23	REGVAL × t_{TE}
ALED1CONVEND	Ambient1 convert phase end(2)	14h	TE24	(REGVAL+1) × t_{TE}
DATA_RDY_STC	DATA_RDY start	52h	TE25	(REGVAL+N) × t_{TE}(3)
DATA_RDY_ENDC	DATA_RDY end	53h	TE26	(REGVAL+N+1) × t_{TE}(3)
LED3LEDSTC	LED3 start	36h	TE7	REGVAL × t_{TE}
LED3LEDENDC	LED3 end	37h	TE8	(REGVAL+1) × t_{TE}
LED4LEDSTC	LED4 start(1)	43h	TE19	REGVAL × t_{TE}
LED4LEDENDC	LED4 end(1)	44h	TE20	(REGVAL+1) × t_{TE}
ACTIVE_STC	Active phase start	64h, 66h, 68h(4)(5)	TE27	REGVAL × t_{TE}
ACTIVE_ENDC	Active phase end	65h, 67h, 69h(4)	TE28	(REGVAL+1) × t_{TE}
DEEP_SLEEP_STC	Deep sleep start	6Ah	TE29	REGVAL × t_{TE}
DEEP_SLEEP_ENDC	Deep sleep end	6Bh	TE30	(REGVAL+1) × t_{TE}

(1) Not used when operating in PTT mode.
(2) Used as ECG conversion phase when operating in PTT mode.
(3) See Table 43 for the value of N for various interrupts.
(4) Write the three registers to the same value.
(5) Set these three counts to zero so that the active phase starts at a count of 0.

Table 29 summarizes the cases that require the LED3 and LED4 signals.

Table 29. Cases Requiring the LED3_ON and LED4_ON Signals to be Programmed

USE CASE	SIGNALS REQUIRED TO BE DEFINED	ADDITIONAL REQUIREMENT
LED3 is used	LED3_ON	ILED3 must be set to the desired value
LED4 is used	LED4_ON	ILED4 must be set to the desired value
Separate R_F and C_F must be programmed in the LED2 and Ambient2 phases	LED3_ON(1)	ENSEPGAIN4 = 1
Separate R_F and C_F must be programmed in the LED1 and Ambient1 phases	LED4_ON(1)	ENSEPGAIN4 = 1
Independent offset DAC setting in the four phases with the offset DAC set to transition at LED_ON start (EARLY_OFFSET_DAC = 1)	LED3_ON, LED4_ON(1)	EARLY_OFFSET_DAC = 1

(1) If a particular LED is not used, set its current to 0.

8.3.8.1 Differences in Power Cycling Scheme Between LDO Enabled Mode and LDO Bypass Mode

When operating with the LDOs bypassed (CONTROL1 = 1), the analog and digital portions of the receiver are directly driven by the external RX_SUP. When operating with the LDO enabled (CONTROL1 = 0), the internal LDOs (ALDO and DLDO) are enabled when the DEEP SLEEP signal is low. The following register controls can be used to reduce the power impact from the LDOs while continuing to ensure that the device maintains the programmed operating state when the AFE4900 comes out of deep sleep phase and enters the next active phase:

- CONTROL_DYN_ALDO: powers down the analog LDO in deep sleep phase
- CONTROL_DYN_DLDO: puts the digital LDO to a low-power state in deep sleep phase
- SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP: shorts ALDO_1V8 to DLDO_1V8 so that both LDO outputs are commonly driven by the digital LDO

8.3.9 First-In, First-Out Block (FIFO)

8.3.9.1 FIFO Depth and Partitioning

The AFE4900 has a 128-sample FIFO that is used to store data from the phases of interest. Each sample corresponds to a 3-byte ADC word.

Enable the FIFO by setting the FIFO_EN bit to 1. The FIFO can be partitioned to store data from the phases of interest. The FIFO is partitioned with the FIFO_PARTITION register controls. The REG_FIFO_PERIOD register control sets the number of periods over which the FIFO is filled (FIFO_PERIOD) to be (REG_FIFO_PERIOD + 1). Table 30 lists the different ways to partition the FIFO using the FIFO_PARTITION register controls.

Table 30. FIFO Partitioning Across Multiple Phases(1)(2)(3)

FIFO_ PARTITION	FIFO_ NPHASE	PHASE 1	PHASE 2	PHASE 3	PHASE 4	PHASE 5	PHASE 6
0000	4	LED2	Ambient2	LED1	Ambient1	—	—
0001	1	(LED1–Ambient1)	—	—	—	—	—
0010	2	LED1	Ambient1	—	—	—	—
0011	1	(LED2–Ambient2)	—	—	—	—	—
0100	2	LED2	Ambient2	—	—	—	—
0101	2	(LED2–Ambient2)	(LED1–Ambient1)	—	—	—	—
0110	3	(LED1–Ambient1)	(LED2–Ambient1)	(Ambient2–Ambient1)	—	—	—
0111	6	LED2	Ambient2	(LED2–Ambient2)	LED1	Ambient1	(LED1–Ambient1)
1000	1	(LED2 + Ambient2 + LED1 + Ambient1) / 4	—	—	—	—	—
Other settings	Do not use						

(1) Data marked as Ambient2 are replaced by LED3 when the third LED is enabled. Data marked as Ambient1 are replaced by LED4 when the fourth LED is enabled.
(2) When decimation mode data are stored in the FIFO, the phases correspond to the corresponding decimation mode outputs.
(3) When in PTT mode, the ECG signal is available in the phase marked as Ambient1.

The FIFO depth that is used depends on the number of phases of data that are selected to be stored in the FIFO (FIFO_NPHASE). FIFO_DEPTH is equal to FIFO_PERIOD × FIFO_NPHASE. For example, if only one phase of data is selected to be stored (FIFO_NPHASE = 1), then the FIFO_DEPTH is equal to FIFO_PERIOD. However, if four phases of data are selected to be stored, then the FIFO_DEPTH is equal to FIFO_PERIOD × 4.

Figure 41 shows the manner in which the FIFO is filled when four phases of data are selected to be stored.

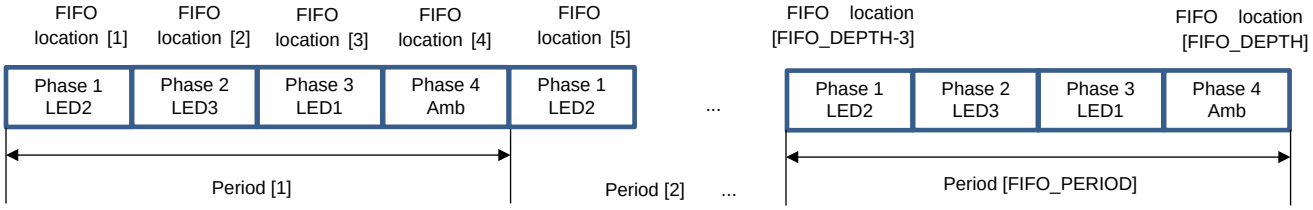


Figure 41. Scheme for a FIFO Write Where Four Phases of Data are Selected to be Stored

8.3.9.2 FIFO_RDY Interrupt Generation

The FIFO_RDY interrupt is an indicator of when the FIFO is filled to a depth equal to FIFO_DEPTH and ready for readout by the MCU. The FIFO_RDY interrupt comes with a periodicity (frequency) equal to (PRF / FIFO_PERIOD). For example, if the PRF is 120 Hz and FIFO_PERIOD is 60 periods, then the periodicity of FIFO_RDY is equal to 2 Hz.

The FIFO_RDY pulse is periodic over FIFO_PERIOD periods. The duration between two consecutive FIFO_RDY pulses constitutes a FIFO write cycle. By default, the pulse duration of the FIFO_RDY pulse is the same as the pulse duration of DATA_RDY (as set by the DATA_RDY_STC and DATA_RDY_ENDC registers). However, by programming a number using the FIFO_EARLY register control, the start of FIFO_RDY can be advanced by a number of periods equal to FIFO_EARLY. FIFO_EARLY can be set based on the estimate of how long the MCU takes to wake up before FIFO data are able to be read. For example, the MCU can be set to wake up on the FIFO_RDY rising edge. The FIFO_RDY falling edge can be used as an indicator that the FIFO data are ready for readout. Figure 42 shows the scheme of FIFO_RDY generation for two different values of FIFO_EARLY.

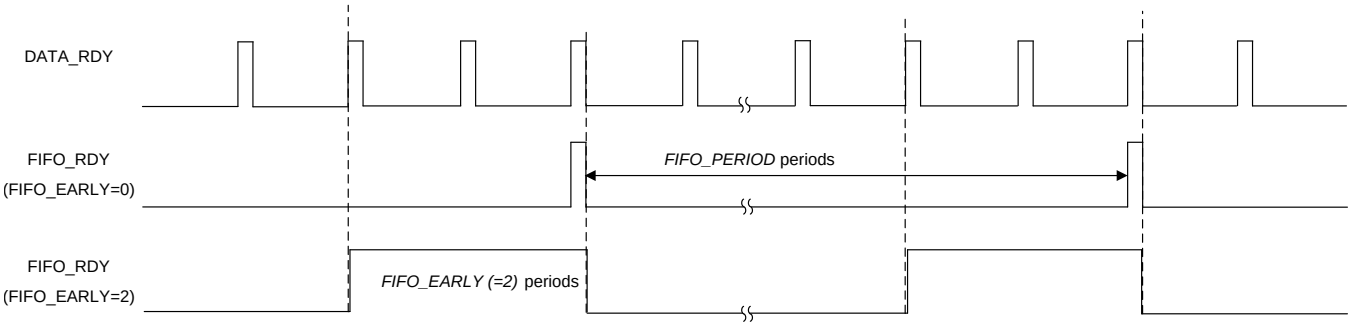


Figure 42. Scheme for FIFO_RDY Generation for FIFO_EARLY = 0 and FIFO_EARLY = 2

FIFO_RDY can be output on any of the interrupt pins; see the *Interrupts* section for more details.

When the FIFO_RDY interrupt is brought out on the ADC_RDY pin, a FIFO_RDY interrupt event can be registered by reading out the FIFO_TOGGLE register bit. This register bit toggles between 0 and 1 every time a FIFO_RDY interrupt is issued on the ADC_RDY pin. Reading the FIFO_TOGGLE bit at every FIFO_RDY interrupt can serve as an added check to help ascertain that the MCU has not missed a FIFO_RDY interrupt. Figure 43 shows an update of the FIFO_TOGGLE bit.

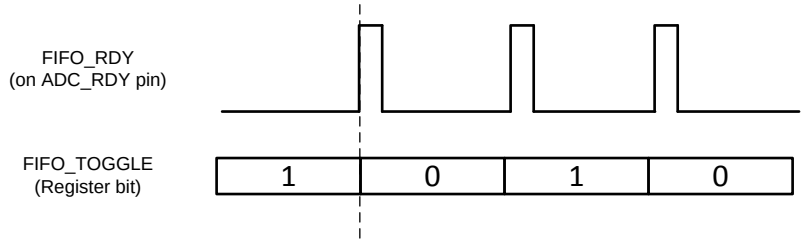


Figure 43. FIFO_TOGGLE Register Bit Update

8.3.9.3 Progression of the FIFO Read and Write Pointers

The FIFO write pointer moves automatically in a circular manner when new data are written to the FIFO. After the ADC conversions are completed in every new PRF cycle, the FIFO write pointer advances by a count equal to FIFO_NPHASE. The FIFO read pointer is a sum of two fields: the read start address and the read offset address. At every FIFO_RDY interrupt, the read start address automatically increments by a number of counts equal to FIFO_DEPTH. There is no mechanism to reverse this increment or to force the read start address. Thus, the data corresponding to a FIFO cycle must be completely read out before the next FIFO_RDY interrupt. The read offset address is reset to 0 when the device gets a software or hardware reset and subsequently increments by 1 every time a FIFO word (3-byte) is read out. Under normal circumstances, the read offset address is 0 when the first data corresponding to a FIFO read cycle is read out. When subsequent FIFO words are read out, the read offset address increments by 1. When the final FIFO word for the cycle is read out, the read offset address has a value equal to (FIFO_DEPTH – 1). Thus, at the next FIFO_RDY, the read start address increments by FIFO_DEPTH and, at the first read after FIFO_RDY, the read offset address wraps back to 0. As a result, the FIFO read pointer moves without a break to the first location corresponding to the new FIFO read cycle. To make sure that the read offset pointer starts at 0 at the start of every FIFO read cycle, an exact number of words equal to FIFO_DEPTH must be read out in every FIFO read cycle. An example of a proper and a faulty readout are illustrated in Figure 44.

The read offset pointer can also be reset to 0 or forced to a programmable count at any time using the FORCE_FIFO_OFFSET and FIFO_OFFSET_TO_FORCE register controls. For example, programming FORCE_FIFO_OFFSET to 1 and FIFO_OFFSET_TO_FORCE to 0 at the start of the FIFO read cycle explicitly forces the read offset address to 0 at the start of the FIFO read cycle. Subsequent FIFO reads result in the read offset pointer being auto-incremented. The out-of-sequence FIFO word corresponding to the read pointer (3 × FIFO_DEPTH – 1) in the faulty case illustrated in Figure 44 can be avoided if the read offset address is reset to 0 using the register controls prior to the start of the read. However, there is no way to go back and read the FIFO word corresponding to the read pointer (2 × FIFO_DEPTH – 1) that was missed in the previous cycle because the readout was incomplete.

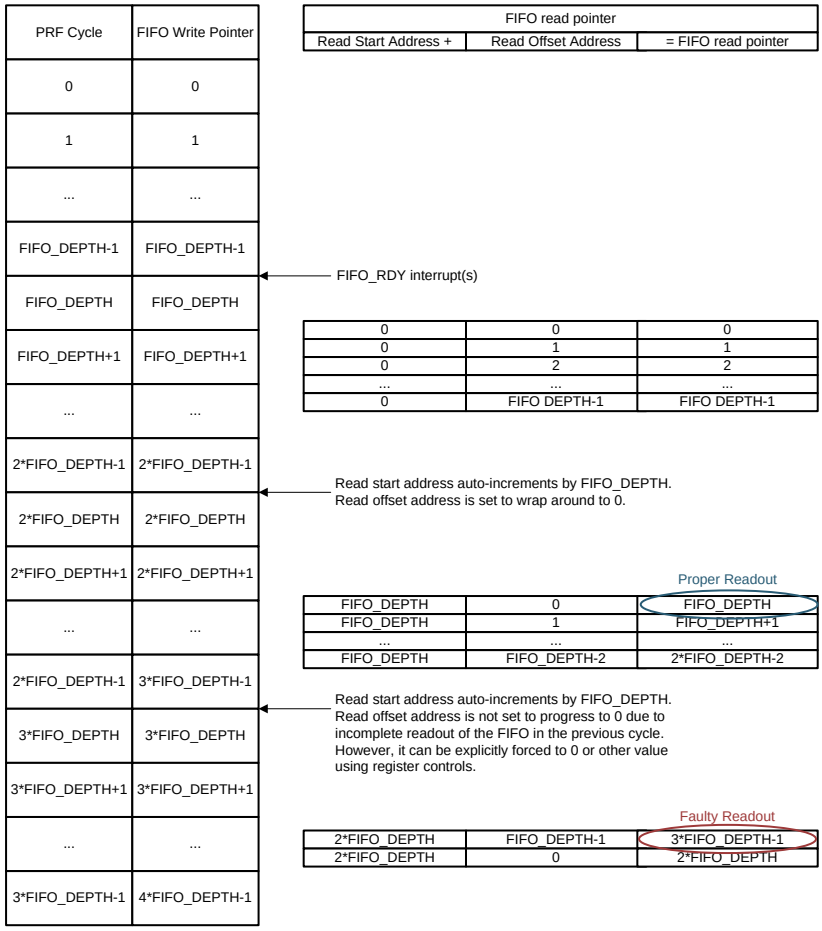


Figure 44. Progression of FIFO Read and Write Pointers

Checking the status of the FIFO_TOGGLE bit and explicitly forcing the FIFO read offset address to 0 at the start of every FIFO read cycle can serve as a mechanism to detect and correct for faults arising from an incorrect FIFO readout.

8.3.9.4 Considerations When Forcing the FIFO Read Offset

The FIFO read offset address forced through FORCE_FIFO_OFFSET and FIFO_OFFSET_TO_FORCE forces the FIFO offset address at the start of every fresh burst of continuous FIFO readouts. As shown in Figure 45, duplicate or incorrect data can be read out if the FIFO offset force is not removed in a timely manner.

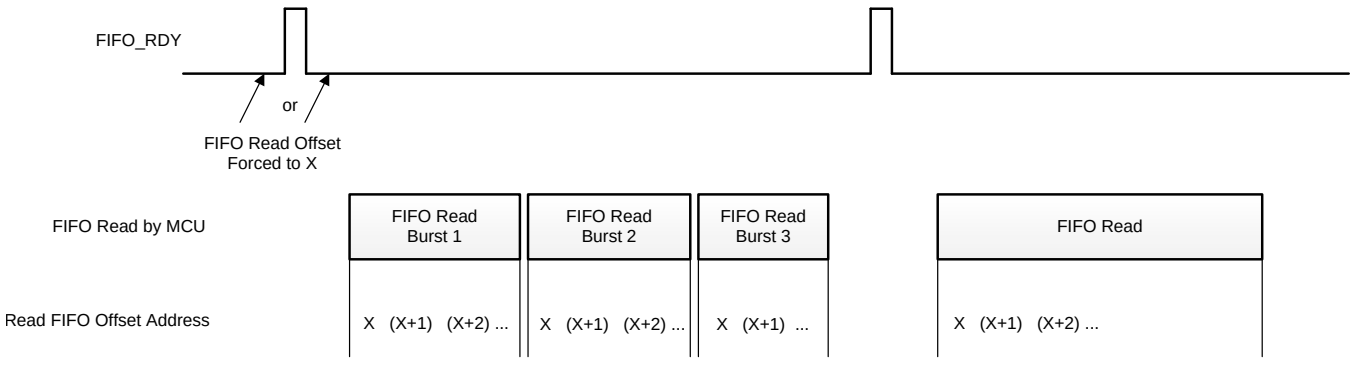


Figure 45. Read Offset Address of the FIFO When FORCE_FIFO_OFFSET is Enabled

The recommended method for proper assertion and deassertion of the FORCE_FIFO_OFFSET feature is shown in Figure 46 (for when the entire depth of the FIFO is completed in a single burst) and in Figure 47 (for when the read is broken up into multiple bursts).

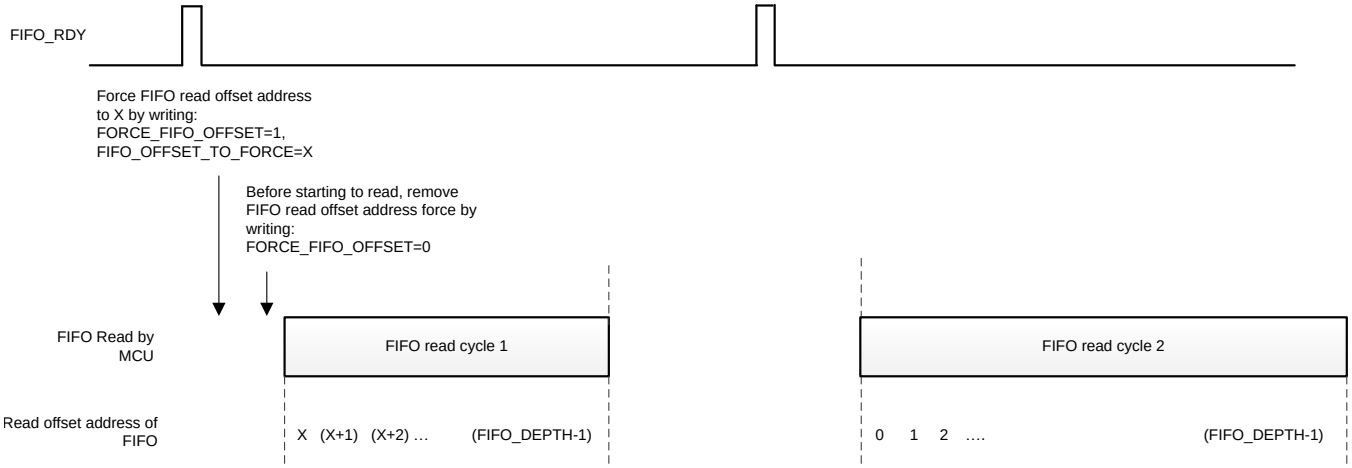


Figure 46. Recommended Method to Deassert FORCE_FIFO_OFFSET When Using a Single Read Burst to Read the FIFO

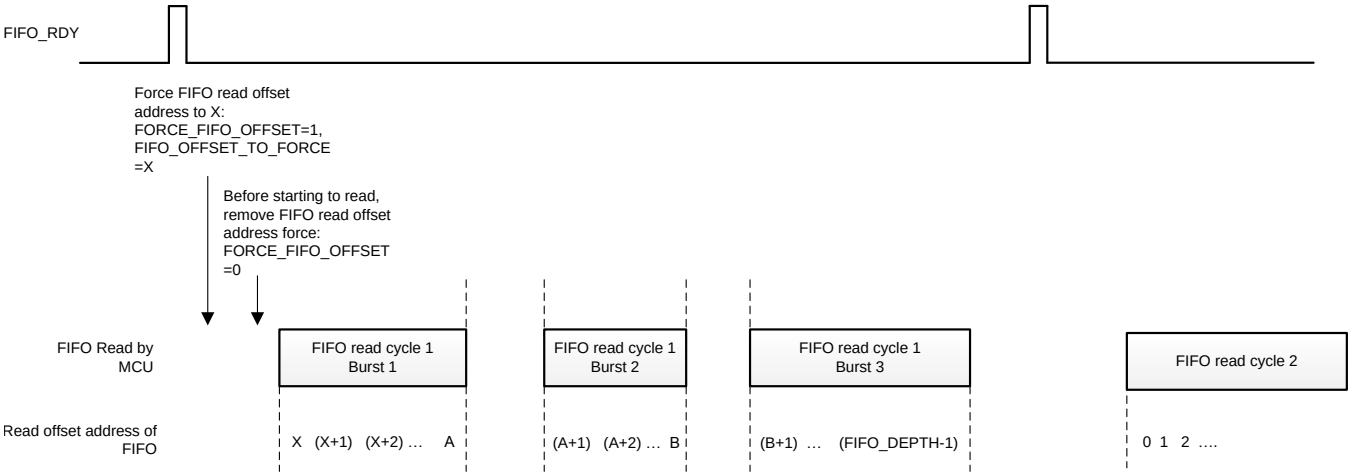


Figure 47. Recommended Method to Deassert FORCE_FIFO_OFFSET When Using Multiple Read Bursts to Read the FIFO

8.3.9.5 Achieving Deterministic Operation When Enabling and Reading From the FIFO

The FIFO read and write pointers are reset to 0 whenever a hardware or software reset is applied. The FIFO write pointer progresses every period when the timing engine is enabled. This progression is irrespective of whether the FIFO is enabled or not (FIFO_EN is 0 or 1). The read start address also progresses irrespective of whether the FIFO is enabled or not. On the other hand, the read offset address increments every time the MCU attempts to read from the FIFO if the FIFO is enabled. With these factors in consideration, the guidelines described in this section are recommended to be followed in order to obtain deterministic operation from the FIFO.

To enable the FIFO for the first time after powering up the device, follow the below sequence:

1. After powering up the device, apply a reset (either a software reset or using the RESETZ pin) to reset the FIFO read and write pointers to 0
2. Configure all device settings including the timing registers and FIFO settings. Enable the FIFO by setting FIFO_EN = 1. Do not attempt to read any data from the FIFO because doing so disturbs the read offset address.
3. When ready to start operation, set TIMEREN to 1
4. On receiving the first FIFO_RDY (and every subsequent FIFO_RDY), read the full depth of the FIFO before the next FIFO_RDY

Figure 48 shows an associated timing diagram with this sequence.

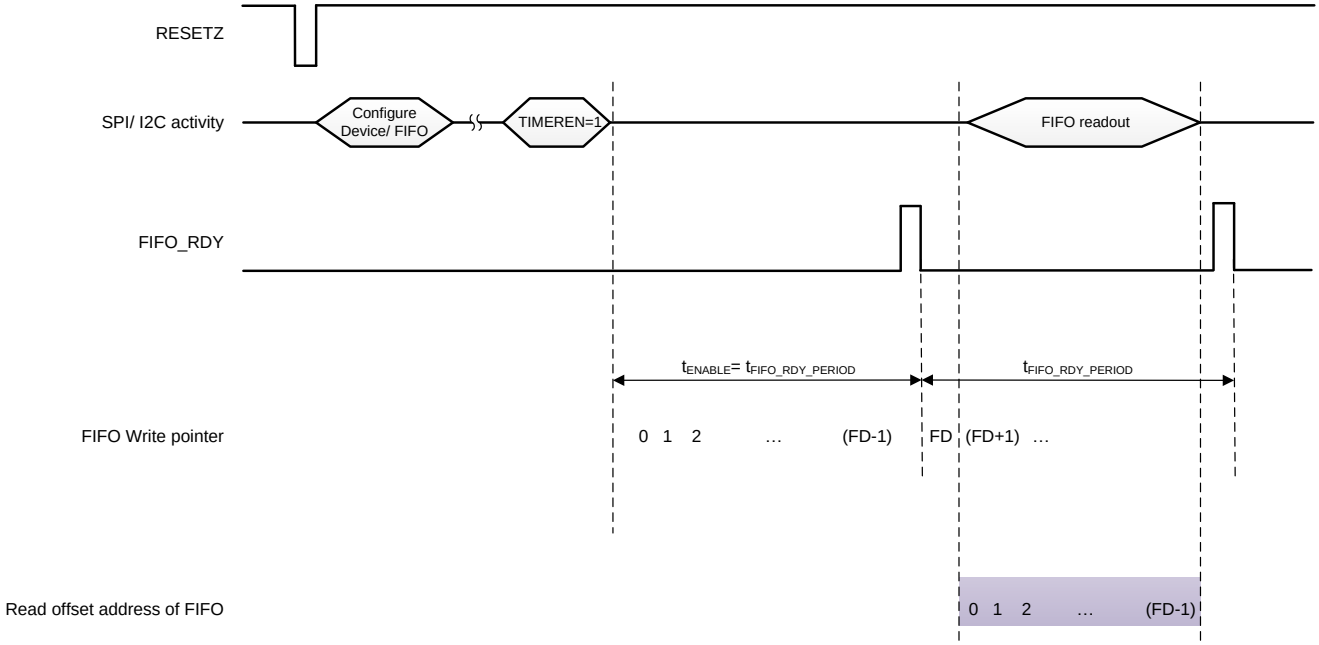


Figure 48. Recommended Scheme to Enable the FIFO for the First Time After a Reset

The FIFO can be disabled in the middle of operation by setting FIFO_EN = 0 and then re-enabled by setting FIFO_EN = 1.

8.3.9.6 FIFO Readout Timing Constraints

Figure 49 describes the time window in which the MCU can read the data from the FIFO.

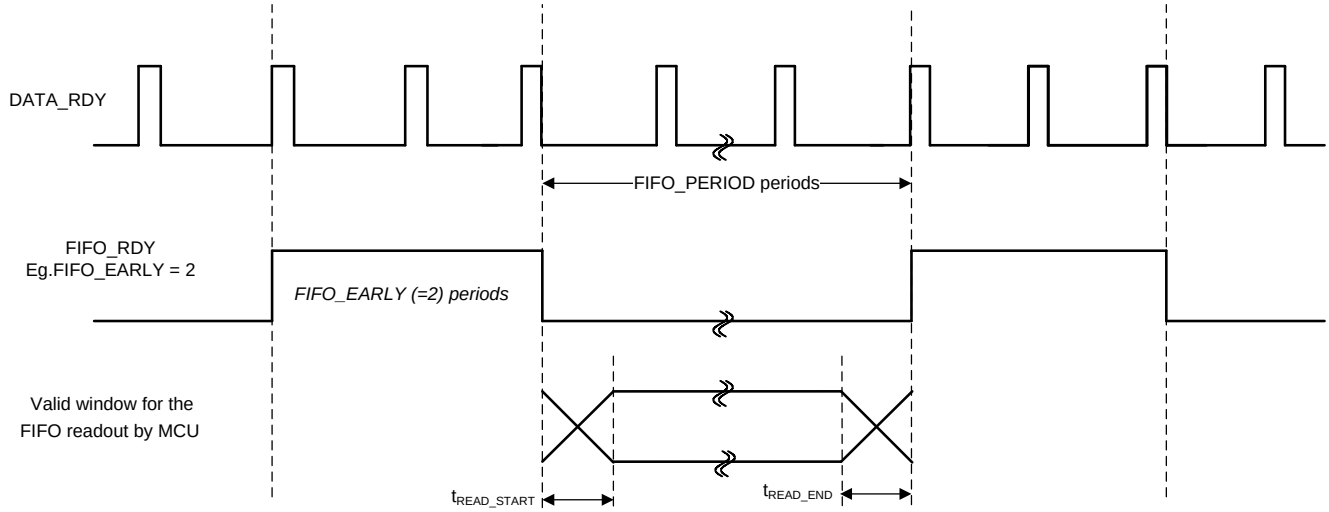


Figure 49. Time Window for the MCU to Read the FIFO

Table 31 lists the timing parameters associated with the start and end of the allowed FIFO read window.

Table 31. Timing Parameters Associated With the Readout Window of the FIFO

		MIN	TYP	MAX	UNIT
t_{READ_START}	FIFO_RDY falling edge to the start of valid FIFO read window	0			µs
t_{READ_END}	Time that the valid FIFO read window ends before the FIFO_RDY rising edge	10 × t_{TE} (1)			µs

(1) t_{TE} refers to one clock period of CLK_TE.

The FIFO can be read out in continuous readout mode from either the I^2C interface or the SPI interface. When receiving a FIFO_RDY interrupt, the MCU must set the readout register address to FFh and continuously read out the data. Starting from the first data of the previous write cycle, the FIFO outputs each 3-byte data on to the I^2C or SPI interface. The MCU must read out the entire depth of the FIFO (FIFO_DEPTH) before the next FIFO_RDY and then stop reading.

8.3.9.7 Performance Considerations Related to the FIFO Readout

The FIFO readout through the I^2C interface is a bursty and periodic event with a periodicity of multiple (FIFO_PERIOD) pulse repetition periods. To minimize noise coupling into the analog portion of the receiver from the readout activity, do not read out FIFO data during the active part of the pulse repetition period. The first way to address this noise-coupling issue (as shown in Figure 50) is by reading out the entire FIFO during the deep sleep phase signal (denoted in Figure 50 and Figure 51 as PDNCYCLE) immediately following the FIFO_RDY pulse.

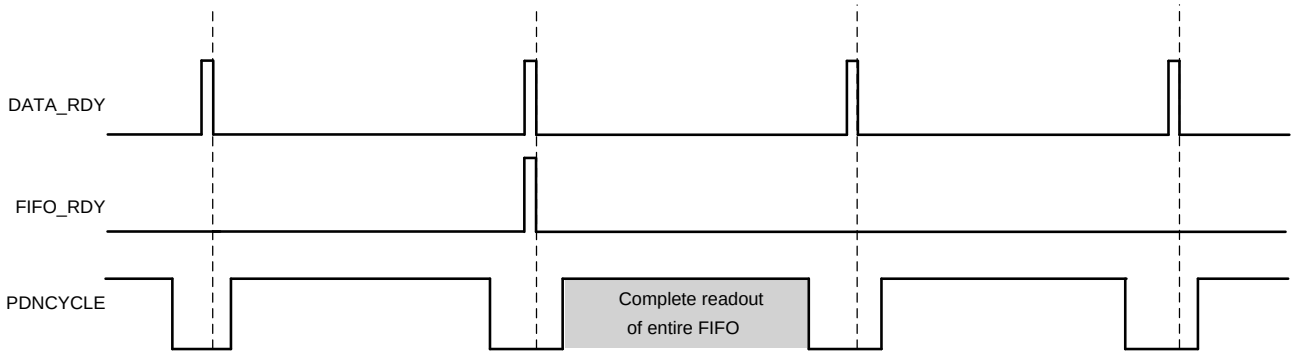


Figure 50. FIFO Readout During the First Deep Sleep Phase After FIFO_RDY

If the FIFO depth is high or if the PRF is high, a scheme as shown in Figure 50 may not be feasible. In that case, the scheme shown in Figure 51 can be used to read out the FIFO. The PDNCYCLE phase can be identified by the MCU by programming the same timing on one of the spare interrupts (INT_OUT1 or INT_OUT2) and making this spare interrupt output on one of the interrupt outputs (for example, on PROG_OUT1).

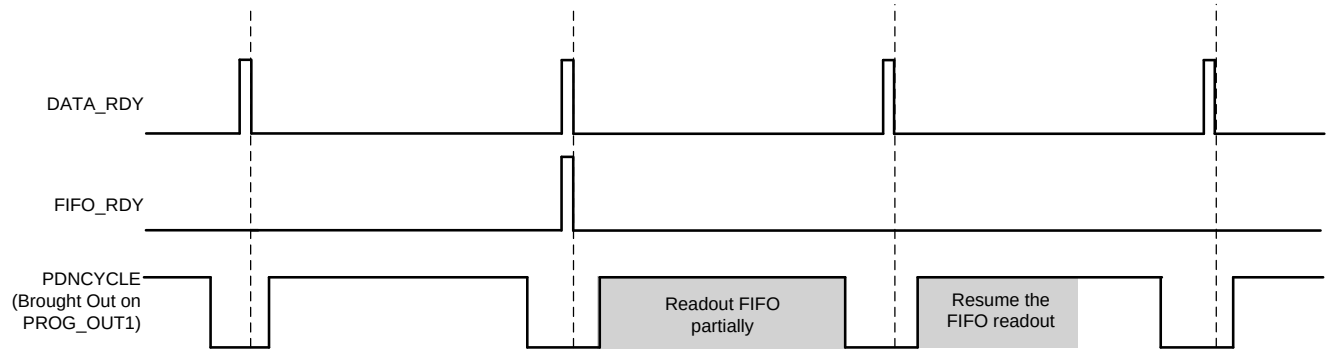


Figure 51. FIFO Readout Over Multiple Deep Sleep Phases

8.3.9.8 Watermark FIFO Mode

The FIFO mode of operation described thus far is referred to as the *normal FIFO mode*. The normal FIFO mode is a mode where FIFO_RDY is generated periodically based on the programmed value of FIFO_PERIOD. The AFE4900 has another FIFO mode where the FIFO_RDY is generated based on a programmed difference between the current locations of the write and read pointers which is referred to as the *watermark level*.

This FIFO mode, referred to as the *watermark FIFO mode* can be programmed using the WM_MODE register control. In this mode, FIFO_RDY is generated when the difference between the write and read pointers exceeds a programmed watermark (WM) level termed *WM_FIFO*. The REG_FIFO_PERIOD register control bits used to set FIFO_PERIOD in normal FIFO mode are repurposed as the REG_WM_FIFO register control in watermark FIFO mode and are used for setting WM_FIFO. The REG_WM_FIFO register control sets the watermark level (WM_FIFO) to be equal to (REG_WM_FIFO + 1). With WM_FIFO thus set, the FIFO_RDY interrupt is now an indication to the MCU that a number of samples equal to WM_FIFO are ready to be read out. The REG_WM_FIFO register control in watermark FIFO mode directly references the number of FIFO samples,

whereas the REG_FIFO_PERIOD register control used in normal FIFO mode references the number of periods (with the relation between the number of periods and number of FIFO samples determined by the FIFO_PARTITION setting). Therefore, select WM_FIFO to be a multiple of FIFO_NPHASE. If the MCU fails to start reading before the completion of the first cycle after FIFO_RDY, then the FIFO_RDY interrupt comes again in the next cycle; this interrupt is now an indication that (WM_FIFO+FIFO_NPHASE) samples must be read out.

The instantaneous difference between the write and read pointers can be read out through an 8-bit register, REG_POINTER_DIFF. The difference between the write and read pointers (POINTER_DIFF) is equal to (REG_POINTER_DIFF + 1). When FIFO_RDY is received, the MCU can read out this register (prior to reading out the FIFO) to confirm that POINTER_DIFF is indeed equal to WM_FIFO. Figure 52 shows the case of how the FIFO_RDY interrupt is generated in watermark FIFO mode for a case where WM_FIFO is set to 32. The MCU is shown as reading only eight samples after receipt of the first FIFO_RDY.

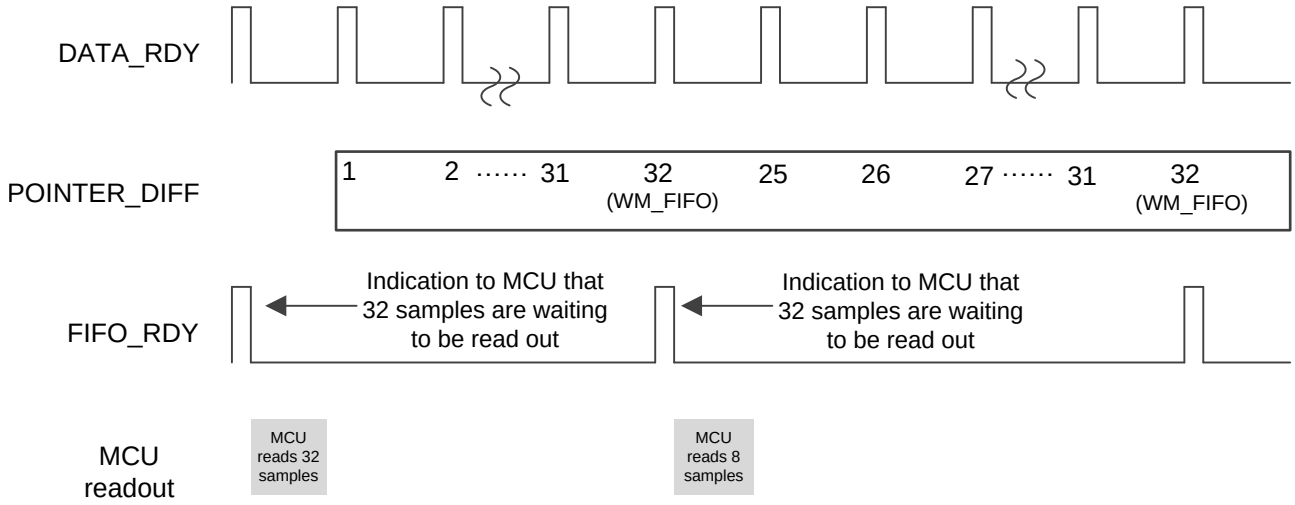


Figure 52. FIFO Mode Based on the Programmable Watermark Level

In addition to the automatic progression of the read pointer (which increments with every read), the read pointer can also be forced relative to the write pointer by setting FORCE_FIFO_OFFSET to 1 and then programming FIFO_OFFSET_TO_FORCE to set the location of the read pointer relative to the current location of the write pointer. The generation of the FIFO_RDY interrupt can be masked using the MASK_FIFO_RDY register control. Such masking can be useful in cases where the MCU does not need to read data from the AFE4900 for a period of time but needs to retrieve prior data stored in the FIFO when the read operation resumes. Figure 53 shows the recommended method of achieving this masking.

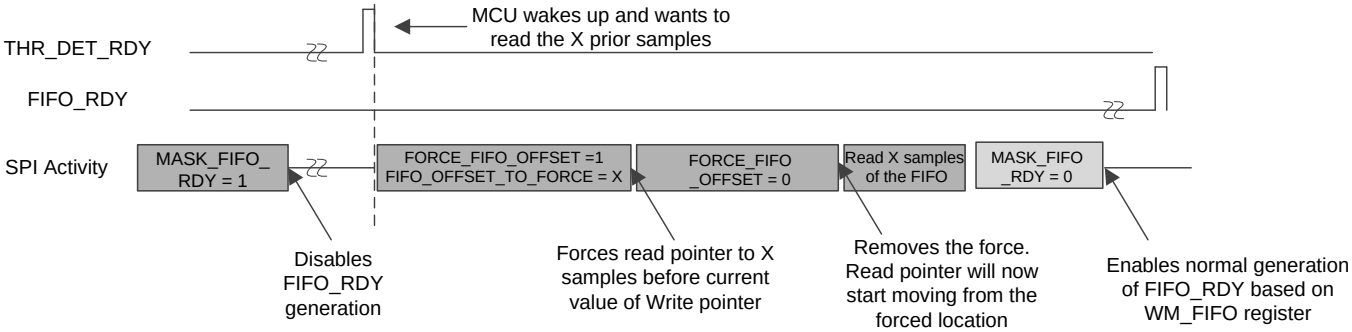


Figure 53. Method of Resuming a FIFO Read Following a FIFO_RDY Masking Phase

8.3.9.9 Arrangement of FIFO Data in PTT Mode

When operating in PTT mode, set FIFO_PARTITION either to 0000 or to 0010 depending on whether the PPG signal data must be stored in the FIFO or not. Figure 54 shows how the FIFO gets filled, when FIFO_PARTITION is set to 0000.

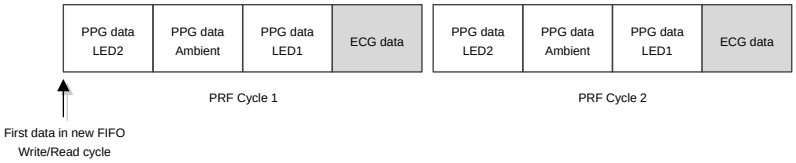


Figure 54. FIFO Data Order in PTT Mode With FIFO_PARTITION = 0

By default, the signal acquisition rate of the PPG and ECG signals is equal to the programmed PRF. However, (as shown in Table 32) the PPG acquisition rate can be set to a programmable fraction (1 / N where N = 1, 2, 4, 8, 16, and 32) of the PRF using the MASK_PPG register control.

Table 32. PPG Sampling Rate as Set by the MASK_PPG Register

MASK_PPG REGISTER SETTING (1)	VALUE OF N (2)(3)	SAMPLE RATE FOR PPG	SAMPLE RATE FOR ECG
0	1	PRF	PRF
1	2	PRF / 2	PRF
2	4	PRF / 4	PRF
3	8	PRF / 8	PRF
4	16	PRF / 16	PRF
5	32	PRF / 32	PRF

(1) Set the MASK1_PPG, MASK2_PPG, and MASK3_PPG registers to the same setting as MASK_PPG.
(2) N is the factor by which the PPG sampling rate is lower than the PRF.
(3) Choose FIFO_PERIOD to be a multiple of N.

In the first (N-1) PRF cycles, the PPG signal phases are masked and only ECG signal acquisition is done. In the Nth PRF cycle, signal acquisition of the three PPG samples is done followed by the signal acquisition of one ECG sample. The FIFO is filled up only by the samples that are acquired. Figure 55 shows how the FIFO is filled for the case, where N is equal to 4. For this case, TI recommends that FIFO_PERIOD be set to a multiple of 4. The FIFO_DEPTH is equal to 7 × (FIFO_PERIOD / 4).

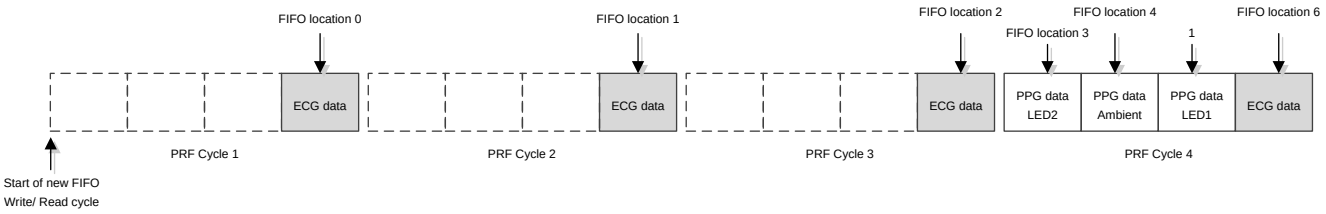


Figure 55. Repetitive Pattern of FIFO Data in PTT Mode When PPG Sampling Rate is Programmed to a Rate Equal to 1 / N of PRF (for N = 4) With FIFO_PARTITION = 0

8.4 Device Functional Modes

8.4.1 Power Modes

The AFE4900 has the following power modes:

1. Normal operation mode. In this mode, the device is in active mode for at least a fraction of the PRF and may or may not be in a deep sleep state for the rest of the PRF cycle. The transition from active mode to deep sleep mode is automatically controlled by the internal timing engine.
2. Hardware power-down mode (PWDN). This mode is set using the RESETZ pin. If the RESETZ pin is pulled low for more than 200 µs, the device enters hardware power-down mode where power consumption is very low. In hardware power-down mode, the contents of the registers are erased.
3. Software power-down mode (PDNAFE). This mode is enabled by using a register bit.

The external clock is recommended to be shut off during the power-down modes.

8.4.2 RESET Modes

The AFE4900 has internal registers that must be reset after powering up the supplies and before valid operation. There are two ways to reset the device:

1. Either through the RESETZ pin (a reset signal can be issued by pulsing the RESETZ pin low for a duration of time between 25 to 50 µs) or
2. A software reset using the SW_RESET register bit. This bit is self-clearing.

Only perform the reset operation after all three supplies (RX_SUP, TX_SUP, and IO_SUP) have powered on and are stabilized.

8.4.3 LDO Modes

The AFE4900 has the following LDO modes:

1. LDO enable mode is set when CONTROL1 = 0 V
2. LDO bypass mode is set by connecting CONTROL1 to RX_SUP

The heart-rate monitoring application requires that the level of spurious tones appearing at the output of the AFE4900 to be small compared to the heart rate tone. High-frequency tones on the supply appearing at the output after aliasing to low frequencies are one such source of spurious tone that can potentially degrade the accuracy of the system.

The fully differential architecture of the AFE4900 receiver provides excellent rejection to tones on RX_SUP.

In LDO enable mode, the internal LDOs provide additional rejection of tones on RX_SUP. Such rejection is very useful in rejecting tones at the switching frequency if a buck converter is used to drive RX_SUP.

The rejection of supply tones is to a lower extent in the LDO bypass mode. An external LDO is recommended to drive RX_SUP when operating in LDO bypass mode.

Device Functional Modes (continued)

8.4.4 Signal Acquisition Modes

The device can be used for three types of signal acquisition:

- **PPG only**: this mode is the default mode (ENABLE_PTT = 0). Up to four phases of PPG signals (including a combination of LED and Ambient phases) can be acquired. The maximum signal acquisition rate for each of the four phases is 1 kHz.
- **Synchronized PPG + ECG**: in this mode (set by ENABLE_PTT = 1), up to three phases of PPG signals and one phase of ECG signal can be acquired every PRF cycle. The maximum signal acquisition rate for each of the three PPG phases and one ECG phase is 1 kHz.
- **ECG-only**: when the acquisition of only the ECG signal is required at a rate higher than 1 kHz and up to 4 kHz, the synchronized PPG + ECG mode can be used in the manner mentioned below:
  - Set ENABLE_PTT = 1
  - Define the dummy CONV phases to be at least one clock wide for the three unused PPG phases: LED ON and SAMP phases for the PPG phases do not have to be defined
  - Dummy FIFO data get stored even in the dummy PPG phases: for example, with FIFO_PARTITION = 0010, the FIFO stores LED1 (third PPG phase – dummy data) and Ambient 1 (ECG phase) into the FIFO. The dummy PPG phase data can be read out and ignored. To reduce the occurrence of this dummy data in the FIFO readout, use the MASK_PPG control to reduce the data rate of this dummy PPG phase.

8.4.5 Decimation Mode

The device has a decimation mode that can be enabled using the DEC_EN register control. In this mode, as shown in Table 33, the device averages the LED output code (after subtracting the corresponding ambient phase) and stores the code in the AVG_LED2_ALED2VAL and AVG_LED1_ALED1VAL registers. Additionally, by setting the FIFO_EN_DEC register bit, any of the phases of LED or ambient data from the decimation mode output can be stored in the FIFO using a mapping similar to the one provided in Table 34. With the FIFO enabled in the decimation mode, the periodicity (time) of the FIFO_RDY interrupt is divided by the decimation factor.

Table 33. Contents of AVG_LED2_ALED2VAL and AVG_LED1_ALED1VAL in Decimation Mode

REGISTER	REGISTER CONTENTS
AVG_LED2_ALED2VAL	Averaged output of LED2 phase code minus Ambient2 phase code
AVG_LED1_ALED1VAL	Averaged output of LED1 phase code minus Ambient1 phase code

Averaging is done over multiple PRF cycles. Table 34 shows the number of PRF cycles over which averaging is done can be programmed through the DEC_FACTOR register control.

Table 34. Number of Averaging Cycles (Decimation Factor) as a Function of DEC_FACTOR

DEC_FACTOR	NUMBER OF SAMPLES AVERAGED (Decimation Factor)
0	1
1	2
2	4
3	8
4	16
5, 6, 7, 8	Do not use

When decimation mode is enabled, the periodicity (frequency) of the DATA_RDY interrupt automatically scales down by a factor equal to the decimation factor. For example, when the decimation factor is set to 4, the periodicity of DATA_RDY becomes PRF / 4. Figure 56 shows the timing of the decimation mode for a decimation factor of 4. Also, when the FIFO is used to store decimation mode data, the periodicity (frequency) of the FIFO_RDY interrupt is divided by the decimation factor.

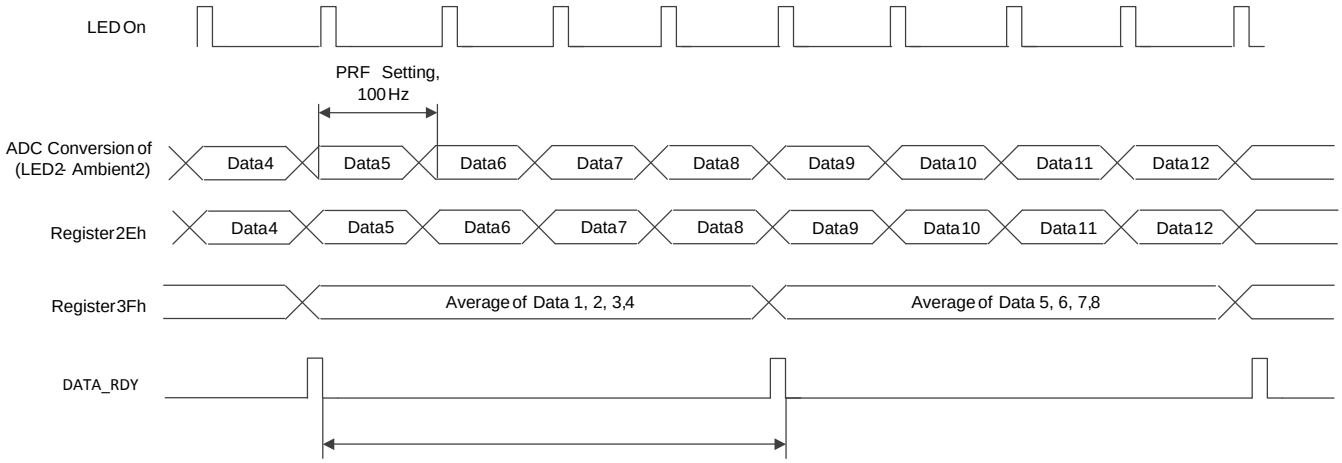


Figure 56. Decimation Mode Timing Diagram (Decimation Factor = 4, PRF = 100 Hz)

Table 35 shows that the decimation mode retains the SNR advantage of sampling at a high PRF while relaxing the output data rate to a lower rate.

Table 35. Different Modes of Operation

MODE	RATE OF DEVICE SAMPLES AND CONVERSIONS	RATE OF MCU DATA READS	RELATIVE PERFORMANCE
No decimation, 100-Hz PRF	100 Hz	100 Hz	Reference level
No decimation, 25-Hz PRF	25 Hz	25 Hz	SNR is 6 dB lower than the reference
4x decimation mode, 100-Hz PRF	100 Hz	25 Hz	SNR is not lower than the reference

8.4.6 Threshold Detect Mode

The device has a threshold detect mode that can be enabled using the THR_DET_EN register control. In this mode, the device detects if the averaged output code of a particular phase is within the programmed lower and upper limits. If the output code is within the limits, the THR_DET_RDY interrupt goes high during the corresponding window of the DATA_RDY pulse. The 24-bit ADC code is compared against lower and upper limits that are set using the 24-bit codes THR_DET_LOW_CODE and THR_DET_HIGH_CODE. Table 36 lists the mapping of these codes to the register controls.

Table 36. Mapping of Register Controls to the Low and High Threshold Code

24-BIT CODE USED FOR THRESHOLD COMPARISON	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THR_DET_LOW_CODE	THR_DET_LOW_CODE3								THR_DET_LOW_CODE2								THR_DET_LOW_CODE1							
THR_DET_HIGH_CODE	THR_DET_HIGH_CODE3								THR_DET_HIGH_CODE2								THR_DET_HIGH_CODE1							

Table 37 lists which THR_DET_PHASE_SEL register control determines which phase of the output data is compared against the low and high thresholds.

Table 37. Output Phase Used for Threshold Detect Based on the THR_DET_PHASE_SEL Value(1)

THR_DET_PHASE_SEL<8:0> (Binary)	OUTPUT PHASE CODE USED FOR THRESHOLD DETECT
XXXXXXXX1	LED2-AMB2
XXXXXXX10	LED2
XXXXXX100	AMB2
XXXXX1000	LED1
XXXX10000	AMB1
XXX100000	LED2-AMB1
XX1000000	AMB2-AMB1
X10000000	LED1-AMB2
100000000	LED1-AMB1

(1) AMB2 corresponds to LED3 and SAMP3; AMB1 corresponds to LED4 and SAMP4.

The CHANGE_SEL_LOGIC register control determines whether the THR_DET_RDY interrupt is generated by the output code going in-range or out-of-range for the range programmed through the THE_DET_HIGH and THR_DET_LOW codes. Table 38 shows the control of CHANGE_SEL_LOGIC.

Table 38. Generation of THR_DET_RDY Interrupt Based on the CHANGE_SEL_LOGIC Control

CHANGE_SEL_LOGIC (Binary)	LOGIC FOR GENERATION OF THR_DET_RDY
00	Generated when the output code comes in-range for the range set by the high and low thresholds
01	Generated when the output code goes out-of-range for the range set by the high and low thresholds
Other settings	Do not use

Table 39 lists the number of averages of the output code taken to compare against the thresholds depends on the DEC_FACTOR register control.

Table 39. Number of Samples Averaged in Threshold Detect Mode Before Comparison With Thresholds

DEC_FACTOR	NUMBER OF SAMPLES AVERAGED BEFORE COMPARISON WITH HIGH AND LOW THRESHOLDS
0	1
1	2
2	4
3	8
4	16
5, 6, 7, 8	Do not use

The THR_DET_RDY interrupt has the same timing as the DATA_RDY interrupt (start and end counts as set by DATA_RDY_STC and DATA_RDY_ENDC) and a periodicity (frequency) equal to PRF / (number of samples averaged).

The timing of the THR_DET_RDY interrupt generation is shown in Figure 57 when the number of averages is set to 4.

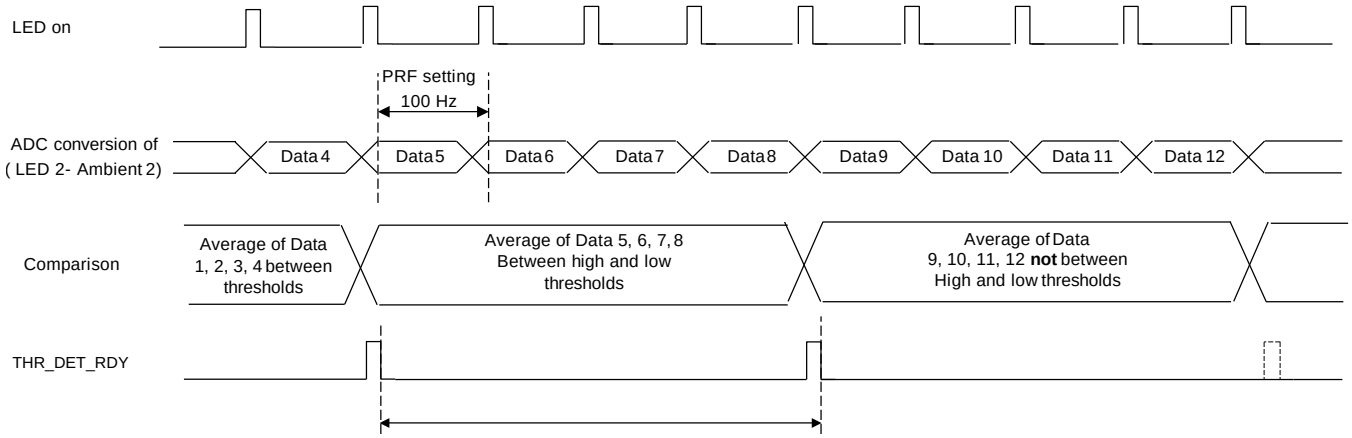


Figure 57. THR_DET_RDY Interrupt Generation Timing Diagram

8.4.7 Dual-Photodiode (PD) Mode

8.4.7.1 Overview of Dual-PD Mode

The AFE4900 supports operation with two photodiodes that can be time-multiplexed to the TIA input by using fully programmable timing engine signals. By default, PD1 (connected to INM and INP) is connected to the TIA input. To enable PD2 (externally connected to INM2 and INP2), a DUAL_PD_ENABLE bit must be set. The selection control between the two photodiodes is generated based on two independent timing signals (TG_PD1 and TG_PD2, as shown in Table 40) that are defined by the start and end counts. Figure 58 shows the multiplexing scheme.

Table 40. Register Controls for Defining TG_PD1 and TG_PD2

TIMING EDGE	REGISTER CONTROL	TIMING EDGE
TG_PD1 start	TG_PD1STC	TE31
TG_PD1 end	TG_PD1ENDC	TE32
TG_PD2 start	TG_PD2STC	TE33
TG_PD2 end	TG_PD2ENDC	TE34

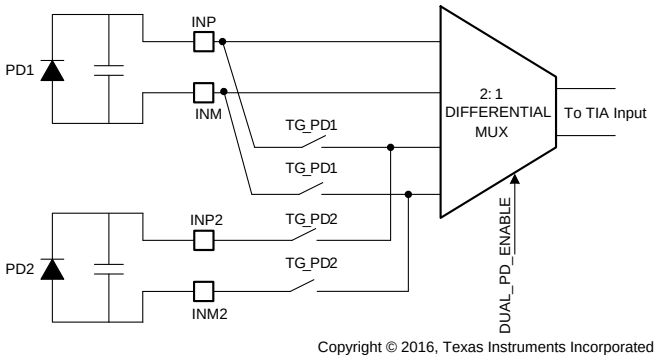


Figure 58. Photodiode Multiplexing Scheme

Figure 59 shows the complete circuit scheme.

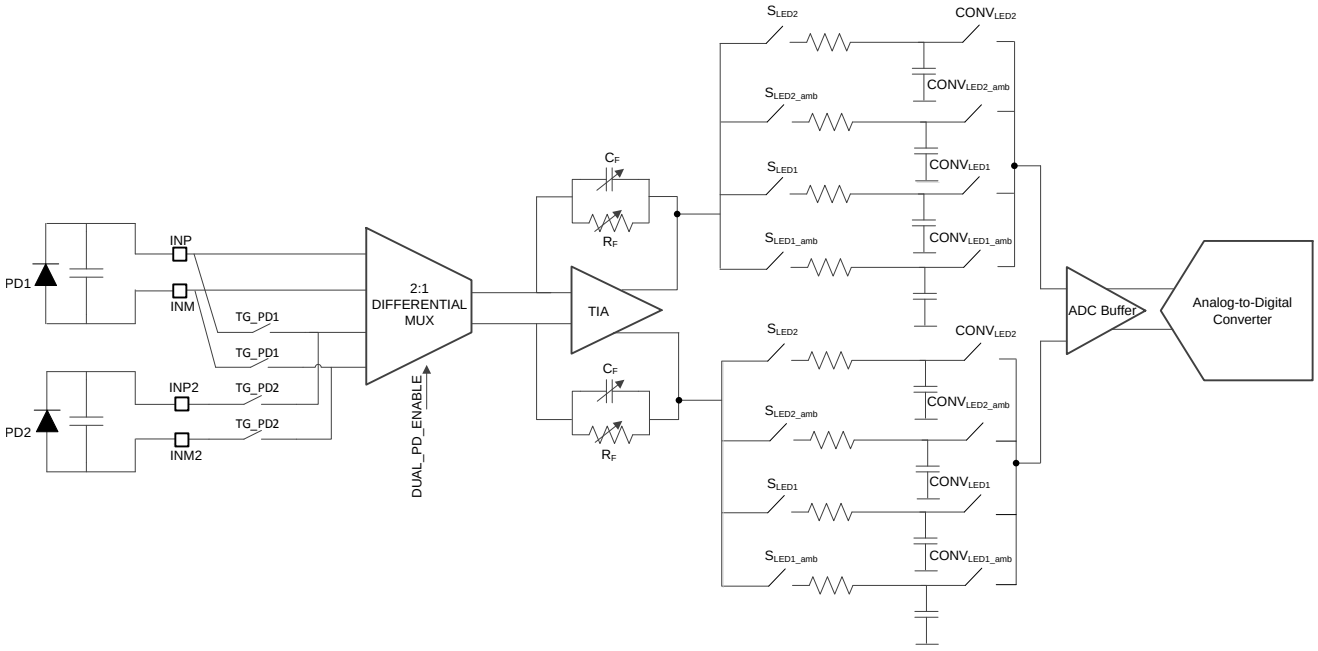


Figure 59. Dual-PD Multiplexer Connection to the TIA

8.4.7.2 PD Selection in Dual-PD Mode

Dual-PD mode can be used to either select the PD in a static manner or used to dynamically switch between two PDs in the middle of a PRF cycle. Table 41 shows the static selection.

Table 41. Static Selection of PDs Using Dual-PD Mode

DESIRED OPERATION	DUAL_PD_ENABLE	TG1	TG2
Receiver only converts PD1	0	X	X
Receiver only converts PD2	1	Off	On for the full PRF count

Figure 60 shows the dynamic switching between the two PDs mode. In this figure, the signal from PD1 is sampled in the first two sampling phases and the signal from PD2 is sampled in the last two sampling phases.

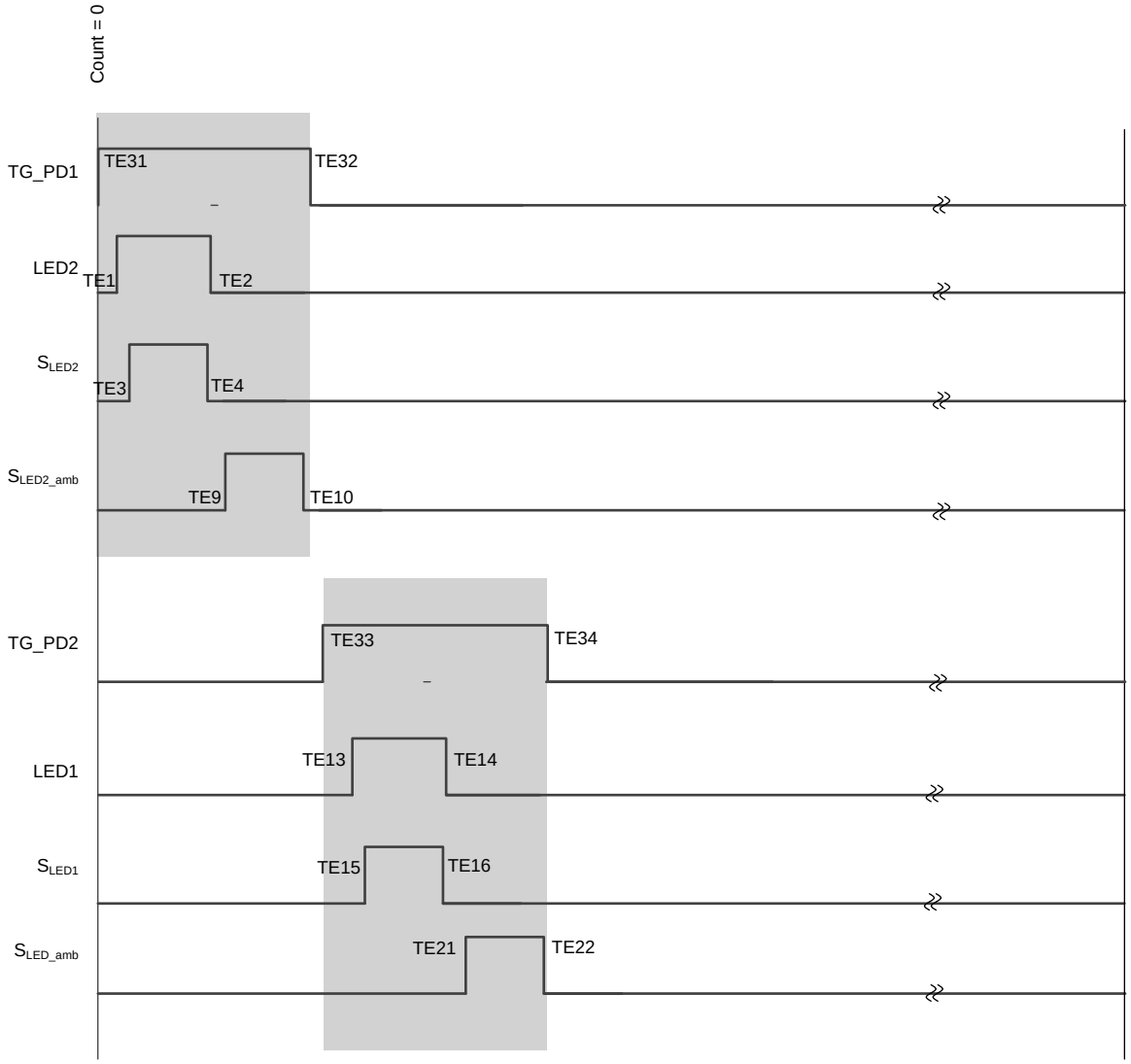


Figure 60. Timing Scheme for Dynamic Selection of the Dual PD Within the PRF Cycle

8.4.7.3 PD Bias Settling Time Considerations

When the TIA is in a powered-up state, the bias on the photodiode that gets connected to the TIA are set. When the TIA is powered down, the input pairs (INP, INM and INP2, INM2) can be differentially shorted by enabling the ENABLE_INPUT_SHORT register bit. This setting ensures that the bias of the PDs do not drift during this phase. Figure 61 and Table 42 show the various mechanisms setting the PD bias.

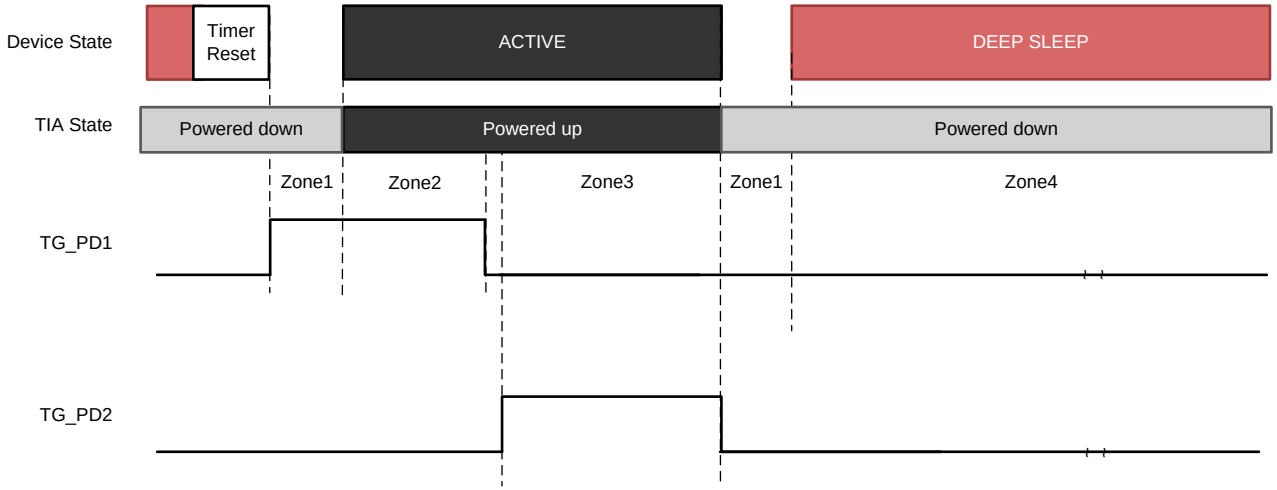


Figure 61. PD Bias Setting in Different Zones of Operation

Table 42. Mechanism of PD Bias Setting in Different Zones of Operation

ZONE	WHAT SETS THE PD BIAS	COMMENTS
Zone 2	TIA sets the PD1 bias through negative feedback. Switches short the PD2 inputs to common-mode voltage (V_{CM}).	Set ENABLE_PD2_SHORT = 1 to short the PD2 inputs to V_{CM} and thereby prevent the PD2 bias from drifting.(1)
Zone 3	TIA sets the PD2 bias through negative feedback PD1 bias drifts.	—
Zone 1	Switches at the input pins short the input pins of both PDs to VCM, which is the nominal common-mode bias at INP and INM.	The switches at the input pins are automatically switched on during the TIA power-down phase (invert of active phase) by setting the ENABLE_INPUT_SHORT bit.
Zone 4	Switches at the input pins short both PDs differentially to zero. However, the V_{CM} at the input pins can drift during this time.	

(1) In a similar manner, the ENABLE_PD1_SHORT bit can be used to short the PD1 inputs to V_{CM} when PD1 is disconnected from the TIA inputs.

In addition to the above considerations, the PD bias can become unsettled if the TIA amplifier output is saturated. Therefore, a gain calibration algorithm is recommended to monitor and adjust the LED current and TIA gain settings such that the TIA output does not saturate in any of the four phases.

8.4.7.4 Triple PD Mode

A triple PD mode can be enabled by programming the TRIPLE_PD_ENABLE register bit. In this mode, the PD1, PD2 inputs can be multiplexed in a manner similar to the dual PD mode using the TG_PD1* and TG_PD2* controls. The timing signals to multiplex the PD3 inputs are set using TG_PD3_STC and TG_PD3_ENDC. The ENABLE_PD2_SHORT register control is also used to short the PD3 inputs to V_{CM} and to maintain the PD3 bias in the phase where the active TIA does not connect to them.

8.5 Programming

8.5.1 I²C Interface

8.5.1.1 I²C Protocol

The AFE has an I²C interface for communication. The I2C_CLK and I2C_DAT lines require external pullup resistors to IO_SUP; see the I²C protocol standards documents for details of the I²C interface. This section only describes certain key features of the interface. Figure 62 shows that the data on I2C_DAT must be stable during the high level of I2C_CLK and can transition during the low level of I2C_CLK.

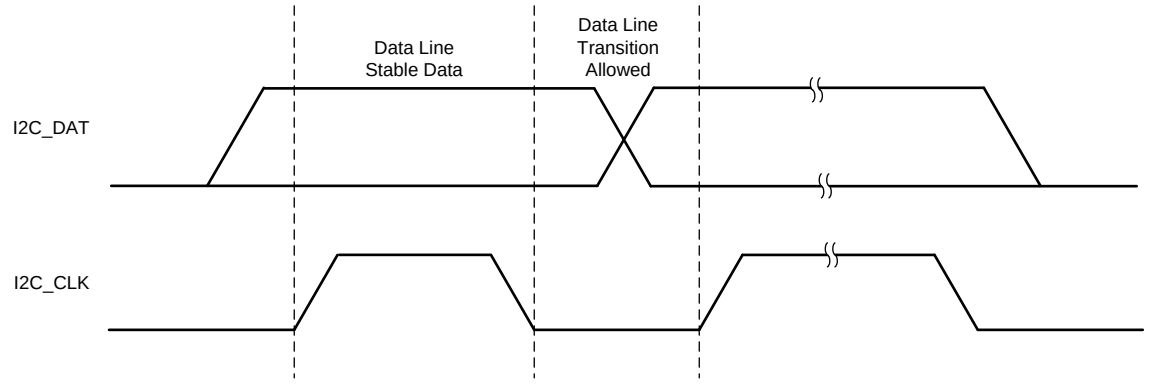


Figure 62. Allowed Transition of I2C_DAT During Data Bit Transmission

The start condition is indicated by a high-to-low transition of the I2C_DAT line when I2C_CLK is high. A stop condition is indicated by a low-to-high transition of the I2C_DAT line when I2C_CLK is high. Figure 63 shows the I2C_DAT start and stop conditions.

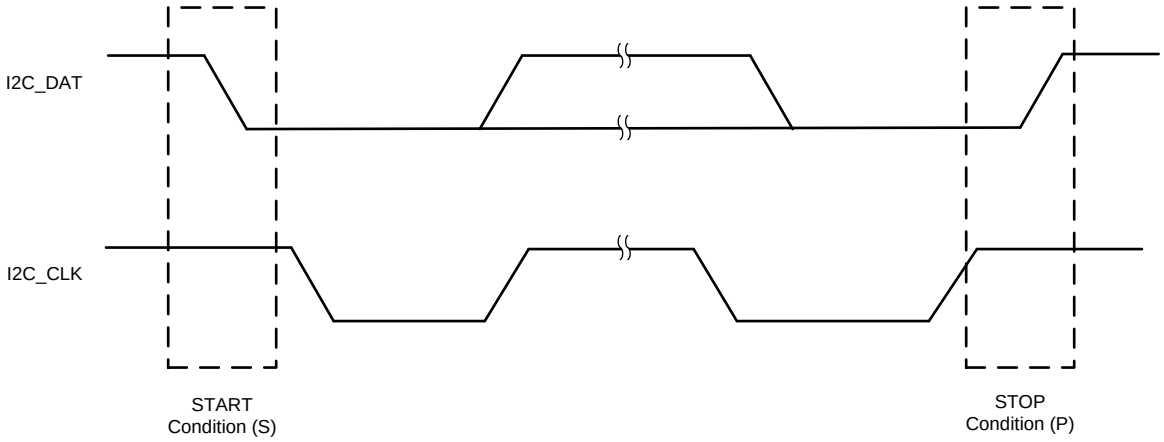
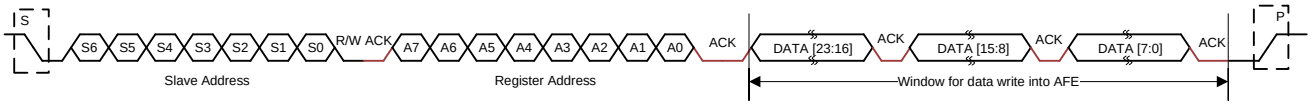


Figure 63. Transition of I2C_DAT During Start and Stop Conditions

Programming (continued)

8.5.1.2 I²C Read and Write Operations

Figure 64 and Figure 65 show the write and read operations, respectively, with the previously mentioned protocols for data, start, and stop conditions. The slave address for the AFE (indicated as SA6 to SA0) is a 7-bit representation of either address 5Ah (when the SEN pin is high) or 5Bh (when the SEN pin is low). The R/W bit is the read/write bit and is set to 1 for reads and 0 for writes. In Figure 64 and Figure 65, the activity performed by the host is shown in black whereas the activity from the AFE is shown in red. Thus, after the host sends the slave address during a write operation, the AFE pulls the I2C_DAT line low (shown as ACK) if the slave address matches 5Ah (when SEN is high) or 5Bh (when SEN is low). Similarly, the host pulls the I2C_DAT line high (shown as NACK) as an acknowledgment of a successfully completed read operation involving three bytes of data.



Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

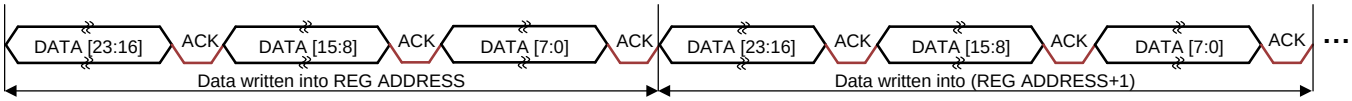
Figure 64. I²C Write Option Timing Diagram

Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 65. I²C Read Option Timing Diagram

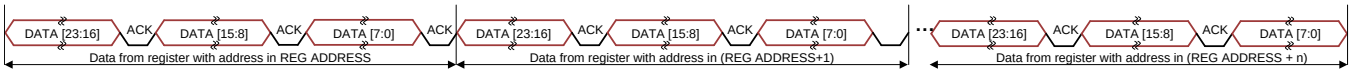
8.5.1.3 Continuous I²C Read and Write Mode

Continuous read/write mode is supported by enabling the RW_CONT bit. The FIFO, however, can be read out continuously without setting this bit. Figure 66 and Figure 67 show the protocol for the continuous write and read modes, respectively.



Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 66. Window for Data Writes to the AFE in Continuous I²C Write Mode (RW_CONT = 1)



Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 67. Transmission Window for Readout From the AFE in Continuous I²C Read Mode (RW_CONT = 1)

Programming (continued)

8.5.1.4 Data Readout From the FIFO Using a Single Continuous Read Operation

When the MCU receives the FIFO_RDY interrupt, Figure 68 shows that the FIFO can be read out through the I²C interface in continuous readout mode. The register address for reading out the FIFO is FFh. The MCU must read out the full depth of the FIFO before the next FIFO_RDY. Additional restrictions on the FIFO readout timing are discussed in the *FIFO Readout Timing Constraints* section.

Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 68. I²C Readout From the FIFO

8.5.1.5 Data Readout From the FIFO Over Multiple Read Operations

The data from the FIFO can also be read out over multiple read operations with a break in between the operations. Figure 69 shows a readout over two such read operations. The restrictions on the FIFO readout timing mentioned in the *FIFO Readout Timing Constraints* section continue to apply for this kind of FIFO readout.

Activity performed by the host is shown in black whereas activity from the AFE is shown in red.

Figure 69. I²C Readout From the FIFO Over Two Read Operations

8.5.2 Serial Peripheral Interface (SPI) Protocol

The SPI consists of four signals: SCLK (serial clock), SDOUT (serial interface data output), SDIN (serial interface data input), and SEN (serial interface enable).

The SPI is enabled by setting the I2C_SPI_SEL pin high. The logic high level of I2C_SPI _SEL corresponds to the RX_SUP voltage level. shows how the pins are reconfigured when operating in SPI mode.

SPI Mode Pin Functions

PIN		PIN FUNCTION IN SPI MODE
NAME	NO.	
I2C_CLK	F3	SCLK: serial clock input
I2C_DAT	F2	SDIN: serial clock data
SEN	E3	SEN: chip select (active low)
SDOUT	E2	SDOUT: serial data output

The serial clock (SCLK) is the SPI serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on SDOUT. Data are clocked in on SDIN. Even though the input has hysteresis, SCLK is recommended to be kept as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low. The serial interface enable (SEN) enables the serial interface to clock data from SDIN into the device.

8.5.2.1 Writing Data

The SPI_REG_READ register bit must be set to 0 before writing to a register. When SEN is low:

- Serially shifting bits into the device is enabled.
- Serial data (on SDIN) are latched at every SCLK rising edge.
- Serial data are loaded into the register at every 32nd SCLK rising edge.

The first eight bits form the register address and the remaining 24 bits form the register data. Figure 70 shows an SPI timing diagram for a single write operation.

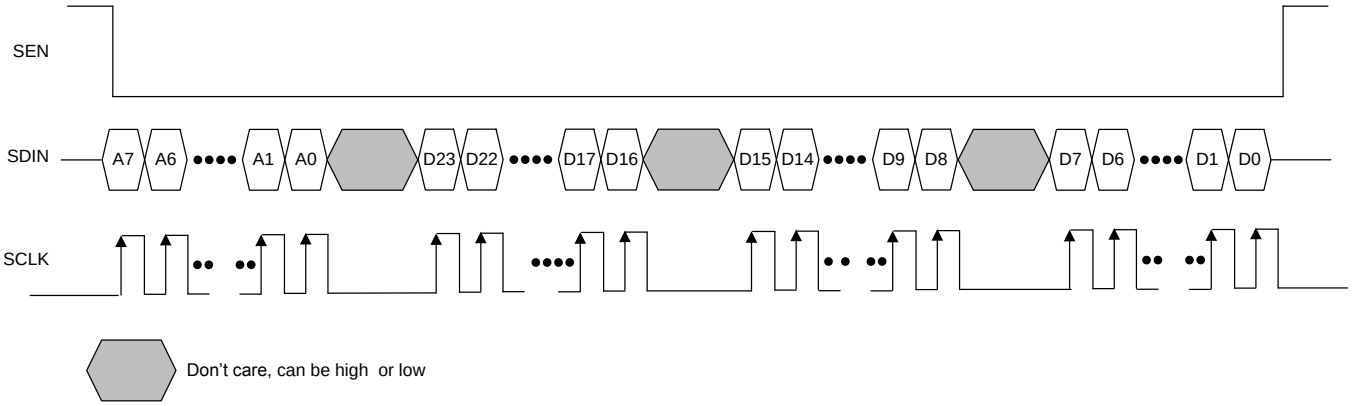
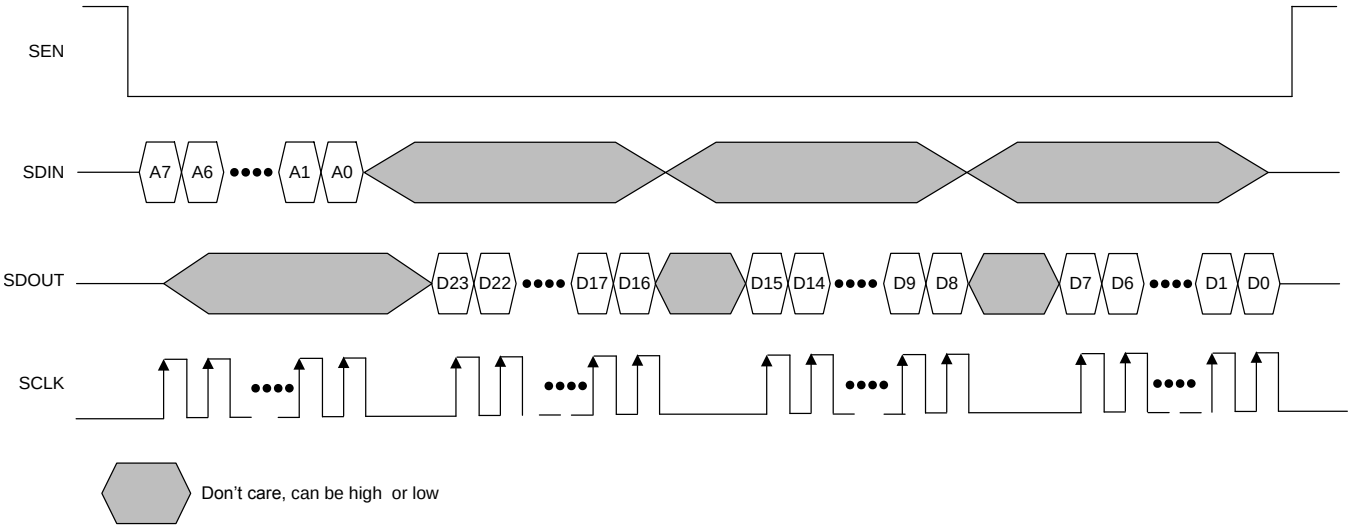


Figure 70. AFE SPI Write Timing Diagram

8.5.2.2 Reading Data

The AFE includes a mode where the contents of the internal registers can be read back on SDOUT. This mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_REG_READ register bit using the SPI write command. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SDOUT pin. Figure 71 shows an SPI timing diagram for a single read operation. The SDOUT pin can be put in tri-state mode by setting SDOUT_TRISTATE bit to 1.



The SPI_REG_READ register bit must be enabled before attempting a serial readout from the AFE.

Specify the register address of the content that must be read back on bits A[7:0].

The AFE outputs the contents of the specified register on the SDOUT pin.

Figure 71. AFE SPI Read Timing Diagram

8.5.2.3 Continuous Read and Write Mode With SPI

The SPI interface can be operated in a continuous read or write mode by writing 1 to the RW_CONT bit. In this mode, the address is specified at the start of the read or write cycle. Subsequently, the address of the register being read or written auto-increments until SEN is pulled high. Figure 72 and Figure 73 show the continuous write and read modes, respectively.

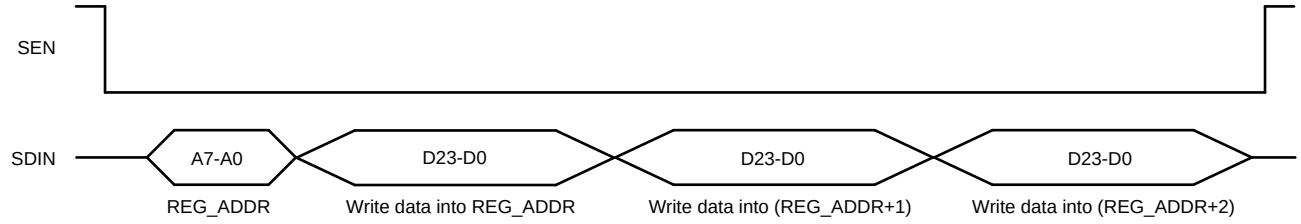


Figure 72. Continuous SPI Write (RW_CONT = 1)

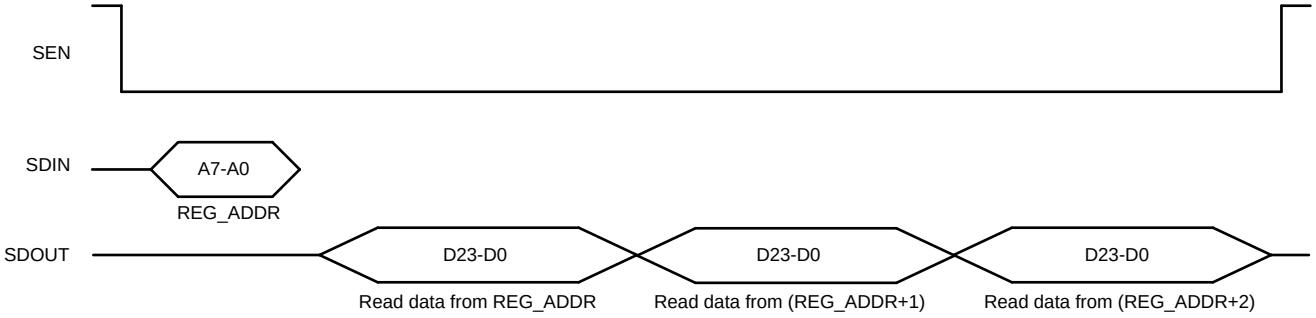


Figure 73. Continuous SPI Read (RW_CONT = 1, SPI_REG_READ = 1)

8.5.2.4 FIFO Readout Through the SPI Over a Single Continuous Read Operation

The contents of the FIFO can be readout in a continuous manner using the SPI interface. The RW_CONT bit is not required to be set to 1 to continuously read out the FIFO. The SPI_REG_READ bit is also not required to be set to 1 when reading out the FIFO. The REG_ADDR used for reading out the FIFO must be set to FFh. Figure 74 shows the readout method.

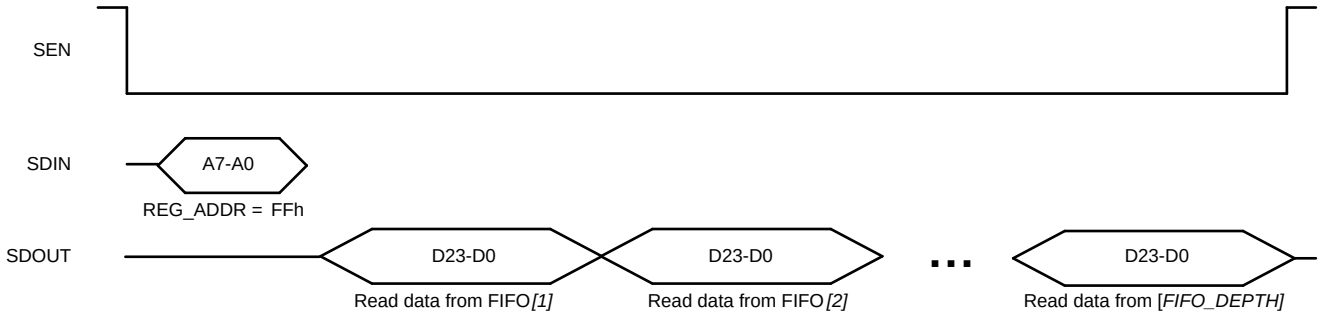


Figure 74. Continuous FIFO Readout Through the SPI

8.5.2.5 FIFO Readout Through the SPI Over Multiple Read Operations

The FIFO can also be read out over multiple read operations. Figure 75 shows the FIFO being read out over two read operations.

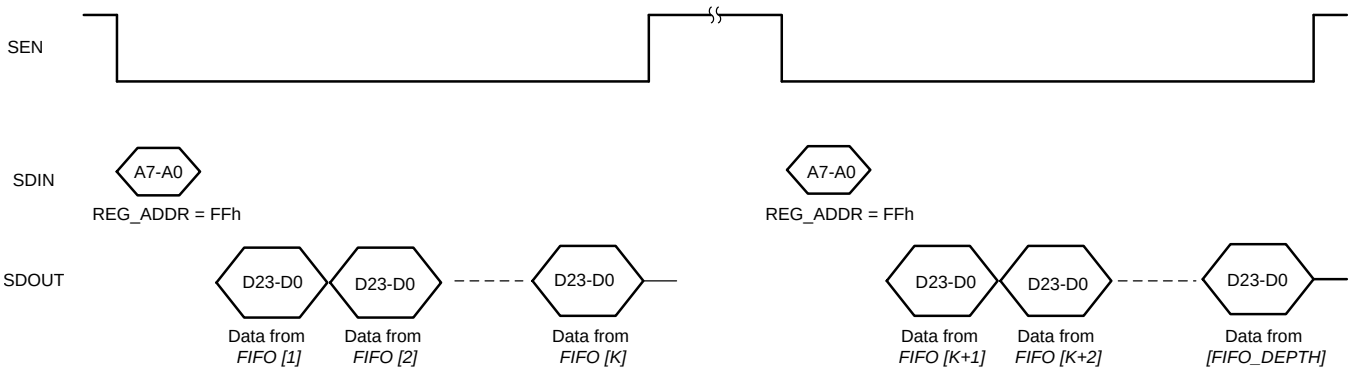


Figure 75. FIFO Readout Over Two Read Operations

8.5.3 Interrupts

The device has three output pins, ADC_RDY, PROG_OUT1, and SDOUT, where a variety of interrupts can be output on. SDOUT is available as an interrupt only in the I^2C interface mode. The PROG_OUT1 pin is disabled by default and can be enabled by setting the EN_PROG_OUT1 bit to 1. A variety of interrupts can be multiplexed on the ADC_RDY, PROG_OUT1, and SDOUT pins by using the INT_MUX1, INT_MUX2, and INT_MUX3 controls. Table 43 describes the interrupts.

Table 43. Description of Various Interrupts

INTERRUPT	DESCRIPTION	EFFECTIVE START COUNT	EFFECTIVE END COUNT
DATA_RDY	Interrupt that comes out at the same rate as the output data rate. Rate is equal to the PRF when decimation is not enabled and (PRF / DEC_FACTOR) when decimation is enabled (DEC_EN = 1).	DATA_RDY_STC + 1	DATA_RDY_ENDC + 2
FIFO_RDY	Interrupt that comes one time every FIFO write cycle with a periodicity (in terms of pulse repetition periods) equal to FIFO_PERIOD. The rate is further reduced by DEC_FACTOR when decimation mode is enabled and the decimated data is stored in the FIFO.	DATA_RDY_STC + 2	DATA_RDY_ENDC + 3 The end count occurs when the programmed FIFO depth is filled up. The start count is advanced by a number of periods as set by FIFO_EARLY.
THR_DET_RDY	Threshold detect flag applicable when the device is in threshold detect mode; goes high during the corresponding DATA_RDY window in the periods where the averaged ADC output is between the programmed thresholds.	DATA_RDY_STC + 2	DATA_RDY_ENDC + 3
INT_OUT1	Spare interrupt 1 that is generated as a pulse every period.	PROG_INT1_STC	PROG_INT1_ENDC + 1
INT_OUT2	Spare interrupt 2 that is generated as a pulse every period.	PROG_INT2_STC	PROG_INT2_ENDC + 1

The INT_MUX1, INT_MUX2, and INT_MUX3 register controls determine the selection of the interrupts described in Table 43 on the output pins. Table 44, Table 45, and Table 46 show this selection.

Table 44. Selection of Interrupts Output on the ADC_RDY Pin

INT_MUX1	INTERRUPT OUTPUT ON ADC_RDY PIN	ADDITIONAL CONTROLS REQUIRED
00	DATA_RDY	—
01	THR_DET_RDY	Set THR_DET_EN = 1
10	FIFO_RDY	Set FIFO_EN = 1
11	Do not use	Do not use

Table 45. Selection of Interrupts Output on the PROG_OUT1 Pin

INT_MUX2	INTERRUPT OUTPUT ON PROG_OUT1 PIN	ADDITIONAL CONTROLS REQUIRED
00	INT_OUT1	EN_PROG_OUT1 = 1
01	DATA_RDY	EN_PROG_OUT1 = 1
10	THR_DET_RDY	EN_PROG_OUT1 = 1, THR_DET_EN = 1
11	FIFO_RDY	EN_PROG_OUT1 = 1, FIFO_EN = 1

Table 46. Selection of Interrupts Output on the SDOUT Pin (Only in I^2C Interface Mode)

INT_MUX3	INTERRUPT OUTPUT ON SDOUT PIN	ADDITIONAL CONTROLS REQUIRED
00	INT_OUT2	Set EN_SDOUT_INT = 1
01	DATA_RDY	Set EN_SDOUT_INT = 1
10	THR_DET_RDY	Set THR_DET_EN = 1, EN_SDOUT_INT = 1
11	FIFO_RDY	Set FIFO_EN = 1, EN_SDOUT_INT = 1

8.6 Register Map

Table 47. Register Map(1)

ADDRESS (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FIFO_EN	ENABLE_ULP	RW_COUNT	SW_RESET	0	TM_COUNT_RST	SPI_REG_READ
01h	0	0	0	0	0	0	0	0	LED2STC															
02h	0	0	0	0	0	0	0	0	LED2ENDC															
03h	0	0	0	0	0	0	0	0	LED1LEDSTC															
04h	0	0	0	0	0	0	0	0	LED1LEDENDC															
05h	0	0	0	0	0	0	0	0	ALED2STC\LED3STC															
06h	0	0	0	0	0	0	0	0	ALED2ENDC\LED3ENDC															
07h	0	0	0	0	0	0	0	0	LED1STC															
08h	0	0	0	0	0	0	0	0	LED1ENDC															
09h	0	0	0	0	0	0	0	0	LED2LEDSTC															
0Ah	0	0	0	0	0	0	0	0	LED2LEDENDC															
0Bh	0	0	0	0	0	0	0	0	ALED1STC															
0Ch	0	0	0	0	0	0	0	0	ALED1ENDC															
0Dh	0	0	0	0	0	0	0	0	LED2CONVST															
0Eh	0	0	0	0	0	0	0	0	LED2CONVEND															
0Fh	0	0	0	0	0	0	0	0	ALED2CONVST\LED3CONVST															
10h	0	0	0	0	0	0	0	0	ALED2CONVEND\LED3CONVEND															
11h	0	0	0	0	0	0	0	0	LED1CONVST															
12h	0	0	0	0	0	0	0	0	LED1CONVEND															
13h	0	0	0	0	0	0	0	0	ALED1CONVST															
14h	0	0	0	0	0	0	0	0	ALED1CONVEND															
1Dh	0	0	0	0	0	0	0	0	PRPCT															
1Eh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TIMEREN	0	0	0	0	NUMAV			
1Fh	0	0	0	0	0	0	0	0	0	TIA_GAIN_SEP3_MSB	TIA_CF_SEP3			TIA_GAIN_SEP3_LSB			0	TIA_GAIN_SEP2_MSB	TIA_CF_SEP2				TIA_GAIN_SEP2_LSB	

(1) After reset, all register bits are reset to 0.

Register Map (continued)

Table 47. Register Map[1] (continued)

ADDRESS (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20h	0	0	0	0	0	0	0	0	ENSEPGAIN	0	0	0	0	0	0	0	0	TIA_GAIN_SEP_MSB	TIA_CF_SEP			TIA_GAIN_SEP_LSB		
21h	0	0	0	0	0	0	0	0	0	IFS_OFFDAC			0	0	FILTER_BW(0)	0	0	TIA_GAIN_MSB	TIA_CF			TIA_GAIN_LSB		
22h	ILED3_ LSB		ILED2_ LSB		ILED1_ LSB		ILED3_MSB						ILED2_MSB						ILED1_MSB					
23h	0	0	0	CONTROL_DYN_TX(0)	0	0	ILED_FS	0	ENSEPGAIN4	CONTROL_DYN_BIAS	0	0	0	0	OSC_ENABLE	0	0	0	0	CONTROL_DYN_TIA	CONTROL_DYN_ADC	0	PDNRX	PDNAFE
24h	0	0	0	0	0	0	0	ILED4_MSB						ILED4_LSB		0	0	0	0	0	0	0	0	0
28h	x[2]	FIFO_TOGGLE	x	x	DESIGN_ID													x	x	x	x	x	x	x
29h	0	0	0	0	0	0	0	0	0	0	0	0	0	SDOUT_TRISTATE	0	0	0	0	0	0	0	0	0	EN_SDOUT_INT
2Ah	LED2VAL																							
2Bh	ALED2VAL\LED3VAL																							
2Ch	LED1VAL																							
2Dh	ALED1VAL																							
2Eh	LED2-ALED2VAL																							
2Fh	LED1-ALED1VAL																							

(2) x = don't care.

Register Map (continued)

Table 47. Register Map[1] (continued)

ADDRESS (Hex)	REGISTER DATA																						
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31h	FILTER_BW<1>	0	0	0	0	0	0	0	0	0	0	0	0	PD_DISCONNECT	0	0	0	0	ENABLE_INPUT_SHORT	0	0	0	0	0
34h	0	0	0	0	0	0	0	0	PROG_INT2_STC															
35h	0	0	0	0	0	0	0	0	PROG_INT2_ENDC															
36h	0	0	0	0	0	0	0	0	LED3LEDSTC															
37h	0	0	0	0	0	0	0	0	LED3LEDENDC															
39h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKDIV_TE		
3Ah	0	0	0	EARLY_OFFSET_DAC	POL_OFFDAC_LED2	I_OFFDAC_LED2_MID				POL_OFFDAC_AMB1	I_OFFDAC_AMB1_MID				POL_OFFDAC_LED1	I_OFFDAC_LED1_MID				POL_OFFDAC_AMB2\POL_OFFDAC_LED3	I_OFFDAC_AMB2_MID\ I_OFFDAC_LED3_MID			
3Bh	THR_DET_LOW_CODE																							
3Ch	THR_DET_HIGH_CODE																							
3Dh	0	0	0	0	0	WM_MODE	0	0	0	THR_DET_PHASE_SEL<7>	THR_DET_PHASE_SEL<6>	THR_DET_PHASE_SEL<5>	THR_DET_PHASE_SEL<4>	THR_DET_PHASE_SEL<3>	THR_DET_PHASE_SEL<2>	THR_DET_PHASE_SEL<1>	THR_DET_PHASE_SEL<8>	FIFO_EN_DEC	DEC_EN	THR_DET_EN	DEC_FACTOR			THR_DET_PHASE_SEL<0>

Register Map (continued)

Table 47. Register Map[1] (continued)

ADDRESS (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3Eh	0	0	0	0	0	0	0	0	0	0	0	0	I_OFFDAC_LED2_LSB_EXT	I_OFFDAC_AMB1_LSB_EXT	I_OFFDAC_LED1_LSB_EXT	I_OFFDAC_LED3_LSB_EXT	I_OFFDAC_LED2_MSB	I_OFFDAC_LED2_LSB	I_OFFDAC_AMB1_MSB	I_OFFDAC_AMB1_LSB	I_OFFDAC_LED1_MSB	I_OFFDAC_LED1_LSB	I_OFFDAC_LED3_MSB	I_OFFDAC_LED3_LSB
3Fh	AVG_LED2-ALED2VAL																							
40h	AVG_LED1-ALED1VAL																							
42h	INT_MUX3		INT_MUX2		0	FIFO_EARLY					REG_FIFO_PERIOD / REG_WM_FIFO								INT_MUX1		FIFO_PARTITION			
43h	0	0	0	0	0	0	0	0	LED4LEDSTC															
44h	0	0	0	0	0	0	0	0	LED4LEDENDC															
45h	0	0	0	0	0	0	0	0	TG_PD1STC															
46h	0	0	0	0	0	0	0	0	TG_PD1ENDC															
47h	0	0	0	0	0	0	0	0	TG_PD2STC															
48h	0	0	0	0	0	0	0	0	TG_PD2ENDC															
49h	0	0	0	0	0	0	0	0	TG_PD3STC															
4Ah	0	0	0	0	0	0	0	0	TG_PD3ENDC															
4Bh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_PROG_OUT1	0	0	0	0	CONTROL_DYN_VCM	CONTROL_DYN_DLDO	CONTROL_DYN_ALDO	CONTROL_DYN_BG
4Eh	AC_LEADOFF_FREQ	PROG_VCOMP_HIGH			PROG_VCOMP_LOW			POL_ILEADOFFP	POL_ILEADOFFM	MAG_ILEADOFF		CHOOSE_ AC_LEADOFF	0	0	0	0	0	0	0	TRIPLE_PD_ ENABLE	DUAL_PD_ ENABLE	ENABLE_PTT	0	0

Register Map (continued)

Table 47. Register Map[1] (continued)

ADDRESS (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
50h	SHORT_ECG_TO_RLD		0	GAIN_ECG			0	0	0	0	0	0	0	0	0	0	0	0	SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP	ENABLE_PD2_SHORT	CONTROL_DYN_TX(1)	0	0	0
51h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MASK_FIFO_RDY	FORCE_FIFO_ OFFSET	FIFO_OFFSET_TO_FORCE							
52h	0	0	0	0	0	0	0	0	DATA_RDY_STC															
53h	0	0	0	0	0	0	0	0	DATA_RDY_ENDC															
54h	0	0	0	0	0	0	0	0	0	MASK_PPG			0	0	0	MASK1_PPG			MASK2_PPG			MASK3_PPG		
57h	0	0	0	0	0	0	0	0	PROG_INT1_STC															
58h	0	0	0	0	0	0	0	0	PROG_INT1_ENDC															
61h	0	0	0	0	ENABLE_ECG_CHOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
62h	ENABLE_RLD	EN_ILEAOFF	EN_LEADOFF_COMP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Map (continued)

Table 47. Register Map[1] (continued)

ADDRESS (Hex)	REGISTER DATA																							
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
63h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RCOMP_INP_HIGH	RCOMP_INP_LOW	RCOMP_INM_HIGH	RCOMP_INM_LOW
64h	0	0	0	0	0	0	0	0	DYN_TIA_STC															
65h	0	0	0	0	0	0	0	0	DYN_TIA_ENDC															
66h	0	0	0	0	0	0	0	0	DYN_ADC_STC															
67h	0	0	0	0	0	0	0	0	DYN_ADC_ENDC															
68h	0	0	0	0	0	0	0	0	DYN_CLK_STC															
69h	0	0	0	0	0	0	0	0	DYN_CLK_ENDC															
6Ah	0	0	0	0	0	0	0	0	DEEP_SLEEP_STC															
6Bh	0	0	0	0	0	0	0	0	DEEP_SLEEP_ENDC															
6Ch	0	0	0	0	0	0	0	0	0	0	0	0	ENABLE_PD1_SHORT	0	0	0	0	0	0	0	0	0	0	0
6Dh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	REG_POINTER_DIFF							
72h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_DRV2_LED4	EN_DRV2_LED3	EN_DRV2_LED2	EN_DRV2_LED1	DIS_DRV1_LED4	DIS_DRV1_LED3	DIS_DRV1_LED2	DIS_DRV1_LED1
73h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CHANGE_SEL_LOGIC

8.6.1 Example Register Settings

This section shows example register settings for different PRFs. The clock for the timing engine is assumed to be a 32-kHz external clock corresponding to t_{TE} = 31.25 µs. The SAMP width is set to 3 × t_{TE} and the LED_ON time is 4 × t_{TE}. NUMAV is set to 1 (two ADC averages).

Table 48 shows the sample timing registers at a 1-kHz PRF. At this high PRF, there is insufficient time to operate the device in deep sleep mode. Notice how the active phase spans the entire PRF period and the first LED starts at a count of 0. The register settings shown in Table 48 are applicable to both PPG-only mode and PPG+ECG mode.

Table 48. Sample Timing Register Settings: 1-kHz PRF

REGISTER ADDRESS (Hex)	TIMING REGISTER NAME	VALUE (Hex)
1	LED2STC	1
2	LED2ENDC	3
3	LED1LEDSTC	A
4	LED1LEDENDC	D
5	LED3STC	6
6	LED3ENDC	8
7	LED1STC	B
8	LED1ENDC	D
9	LED2LEDSTC	0
A	LED2LEDENDC	3
B	ALED1STC	10
C	ALED1ENDC	12
D	LED2CONVST	5
E	LED2CONVEND	8
F	ALED2CONVST	A
10	ALED2CONVEND	D
11	LED1CONVST	F
12	LED1CONVEND	12
13	ALED1CONVST	14
14	ALED1CONVEND	17
1D	PRPCOUNT	1F
36	LED3LEDSTC	5
37	LED3LEDENDC	8
43	LED4LEDSTC	F
44	LED4LEDENDC	12
52	DATA_RDY_STC	1D
53	DATA_RDY_END	1D
64	DYN_TIA_STC	0
65	DYN_TIA_ENDC	20
66	DYN_ADC_STC	0
67	DYN_ADC_ENDC	20
68	DYN_CLK_STC	0
69	DYN_CLK_ENDC	20
6A	DEEP_SLEEP_STC	21
6B	DEEP_SLEEP_ENDC	18

Table 49 shows the sample timing registers at a 500-Hz PRF. The device is put in deep sleep mode for a fraction of the PRF cycle. The active phase (as defined by the time counts of DYN_TIA_STC, DYN_ADC_STC, and DYN_CLK_STC) start at 0. The first LED_ON signal is offset by a time determined by t_{ACTIVE_PWRUP}.

Table 49. Sample Timing Register Settings: 500-Hz PRF

REGISTER ADDRESS (Hex)	TIMING REGISTER NAME	VALUE (Hex)
1	LED2STC	B
2	LED2ENDC	D
3	LED1LEDSTC	14
4	LED1LEDENDC	17
5	LED3STC	10
6	LED3ENDC	12
7	LED1STC	15
8	LED1ENDC	17
9	LED2LEDSTC	A
A	LED2LEDENDC	D
B	ALED1STC	1A
C	ALED1ENDC	1C
D	LED2CONVST	F
E	LED2CONVEND	12
F	ALED2CONVST	14
10	ALED2CONVEND	17
11	LED1CONVST	19
12	LED1CONVEND	1C
13	ALED1CONVST	1E
14	ALED1CONVEND	21
1D	PRPCT	3F
36	LED3LEDSTC	F
37	LED3LEDENDC	12
43	LED4LEDSTC	19
44	LED4LEDENDC	1C
52	DATA_RDY_STC	27
53	DATA_RDY_END	27
64	DYN_TIA_STC	0
65	DYN_TIA_ENDC	23
66	DYN_ADC_STC	0
67	DYN_ADC_ENDC	23
68	DYN_CLK_STC	0
69	DYN_CLK_ENDC	23
6A	DEEP_SLEEP_STC	2E
6B	DEEP_SLEEP_ENDC	38

To adapt the same conditions to a different PRF, only the PRPCT and DEEP_SLEEP_ENDC registers must be modified with respect to Table 49. For example, at a 100-Hz PRF, change PRPCT to 13Fh and DEEP_SLEEP_ENDC to 138h.

Table 50 lists the sample timing registers at a 4-kHz PRF in the ECG-only signal acquisition. A 1-MHz clock is used for the timing engine. Notice how the dummy CONV phases associated with the three unused PPG phases are defined to be one clock wide by setting the start and end count to the same value. The SAMP and LED_ON signals associated with the PPG phases are blanked out by setting their start and end counts to be higher than the PRPCT. Additionally, because the TIA is not required to be active for ECG-only signal acquisition, the TIA active phase is also disabled by setting DYN_TIA_STC to be higher than PRPCT. Also, by setting the DEEP_SLEEP_STC timer to be higher than PRPCT, the device never enters deep sleep mode.

Table 50. Sample Timing Register Settings (ECG Only): 4-kHz PRF

REGISTER ADDRESS (Hex)	TIMING REGISTER NAME	VALUE (Hex)
1	LED2STC	103
2	LED2ENDC	103
3	LED1LEDSTC	103
4	LED1LEDENDC	103
5	LED3STC	103
6	LED3ENDC	103
7	LED1STC	103
8	LED1ENDC	103
9	LED2LEDSTC	103
A	LED2LEDENDC	103
B	ALED1STC	103
C	ALED1ENDC	103
D	LED2CONVST	0
E	LED2CONVEND	0
F	ALED2CONVST	1
10	ALED2CONVEND	1
11	LED1CONVST	2
12	LED1CONVEND	2
13	ALED1CONVST	4
14	ALED1CONVEND	81
1D	PRPCT	F9
36	LED3LEDSTC	103
37	LED3LEDENDC	103
43	LED4LEDSTC	103
44	LED4LEDENDC	103
52	DATA_RDY_STC	87
53	DATA_RDY_END	87
64	DYN_TIA_STC	103
65	DYN_TIA_ENDC	103
66	DYN_ADC_STC	0
67	DYN_ADC_ENDC	103
68	DYN_CLK_STC	0
69	DYN_CLK_ENDC	103
6A	DEEP_SLEEP_STC	103

8.6.2 Register Descriptions

Table 51. Register Address Access Type Codes

Access Type	Code	Description
Read-only	R	Read
Read-write	R/W	Read, write, or both
Write-only	W	Write
-n		Value after reset or the default value

8.6.2.1 Register 00h (address = 00h) [reset = 0h]

Figure 76. Register 00h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	FIFO_EN	ENABLE_ULP	RW_CONT	SW_RESET	0	TM_COUNT_RST	SPI_REG_READ
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 52. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
23-7	0	W	0h	Must write 0
6	FIFO_EN	W	0h	0 = FIFO disabled 1 = FIFO enabled
5	ENABLE_ULP	W	0h	Enables ultra-low power (ULP) mode; must write 1. Program this bit before programming registers with address 23h or higher.
4	RW_CONT	W	0h	0 = Read or write only one register at a time 1 = Read or write continuously in both I^2C and SPI modes
3	SW_RESET	W	0h	Self-clearing reset bit. For a software reset, write 1.
2	0	W	0h	Must write 0
1	TM_COUNT_RST	W	0h	This bit is used to suspend the count and keep the counter in a reset state.
0	SPI_REG_READ	W	0h	Register readout enable for write registers in SPI mode (not needed in I^2C mode or for reading ADC output registers or FIFO in SPI mode). 0 = Register write mode in SPI interface mode 1 = Enables the readout of write registers in SPI interface mode Not required for readout of read-only registers with these addresses: 2Ah, 2Bh, 2Ch, 2Dh, 2Eh, 2Fh, and FFh.

8.6.2.2 Register 01h (address = 01h) [reset = 0h]

Figure 77. Register 01h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2STC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2STC							
R/W-0h							

Table 53. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2STC	R/W	0h	Determines sample LED2 start

8.6.2.3 Register 02h (address = 02h) [reset = 0h]

Figure 78. Register 02h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2ENDC							
R/W-0h							

Table 54. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2ENDC	R/W	0h	Determines sample LED2 end

8.6.2.4 Register 03h (address = 03h) [reset = 0h]

Figure 79. Register 03h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1LEDSTC							
R/W-0h							

Table 55. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1LEDSTC	R/W	0h	Determines LED1 start

8.6.2.5 Register 04h (address = 04h) [reset = 0h]

Figure 80. Register 04h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1LEDENDC							
R/W-0h							

Table 56. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1LEDENDC	R/W	0h	Determines LED1 end

8.6.2.6 Register 05h (address = 05h) [reset = 0h]

Figure 81. Register 05h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2STC\LED3STC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2STC\LED3STC							
R/W-0h							

Table 57. Register 05h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2STC\LED3STC	R/W	0h	Determines sample Ambient2 (or determines sample LED3) start

8.6.2.7 Register 06h (address = 06h) [reset = 0h]

Figure 82. Register 06h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2ENDC\LED3ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2ENDC\LED3ENDC							
R/W-0h							

Table 58. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2ENDC\LED3ENDC	R/W	0h	Determines sample Ambient2 (or determines sample LED3) end

8.6.2.8 Register 07h (address = 07h) [reset = 0h]

Figure 83. Register 07h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1STC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1STC							
R/W-0h							

Table 59. Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1STC	R/W	0h	Determines sample LED1 start

8.6.2.9 Register 08h (address = 08h) [reset = 0h]

Figure 84. Register 08h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED1ENDC							
R/W-0h							

Table 60. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1ENDC	R/W	0h	Determines sample LED1 end

8.6.2.10 Register 09h (address = 09h) [reset = 0h]

Figure 85. Register 09h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2LEDSTC							
R/W-0h							

Table 61. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2LEDSTC	R/W	0h	Determines LED2 start

8.6.2.11 Register 0Ah (address = 0Ah) [reset = 0h]

Figure 86. Register 0Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED2LEDENDC							
R/W-0h							

Table 62. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2LEDENDC	R/W	0h	Determines LED2 end

8.6.2.12 Register 0Bh (address = 0Bh) [reset = 0h]

Figure 87. Register 0Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1STC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1STC							
R/W-0h							

Table 63. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1STC	R/W	0h	Determines sample Ambient1 start

8.6.2.13 Register 0Ch (address = 0Ch) [reset = 0h]

Figure 88. Register 0Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1ENDC							
R/W-0h							

Table 64. Register 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1ENDC	R/W	0h	Determines sample Ambient1 end

8.6.2.14 Register 0Dh (address = 0Dh) [reset = 0h]

Figure 89. Register 0Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
LED2CONVST							
R/W-0h							

Table 65. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2CONVST	R/W	0h	Determines LED2 convert phase start

8.6.2.15 Register 0Eh (address = 0Eh) [reset = 0h]

Figure 90. Register 0Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED2CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
LED2CONVEND							
R/W-0h							

Table 66. Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED2CONVEND	R/W	0h	Determines LED2 convert phase end

8.6.2.16 Register 0Fh (address = 0Fh) [reset = 0h]

Figure 91. Register 0Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2CONVST\LED3CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2CONVST\LED3CONVST							
R/W-0h							

Table 67. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2CONVST\LED3CONVST	R/W	0h	Determines Ambient2 (or LED3) convert phase start

8.6.2.17 Register 10h (address = 10h) [reset = 0h]

Figure 92. Register 10h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED2CONVEND\LED3CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
ALED2CONVEND\LED3CONVEND							
R/W-0h							

Table 68. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED2CONVEND\LED3CONVEND	R/W	0h	Determines Ambient2 (or LED3) convert phase end

8.6.2.18 Register 11h (address = 11h) [reset = 0h]

Figure 93. Register 11h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
LED1CONVST							
R/W-0h							

Table 69. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1CONVST	R/W	0h	Determines LED1 convert phase start

8.6.2.19 Register 12h (address = 12h) [reset = 0h]

Figure 94. Register 12h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED1CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
LED1CONVEND							
R/W-0h							

Table 70. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED1CONVEND	R/W	0h	Determines LED1 convert phase end

8.6.2.20 Register 13h (address = 13h) [reset = 0h]

Figure 95. Register 13h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1CONVST							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1CONVST							
R/W-0h							

Table 71. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1CONVST	R/W	0h	Determines Ambient1 convert phase start

8.6.2.21 Register 14h (address = 14h) [reset = 0h]

Figure 96. Register 14h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ALED1CONVEND							
R/W-0h							
7	6	5	4	3	2	1	0
ALED1CONVEND							
R/W-0h							

Table 72. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	ALED1CONVEND	R/W	0h	Determines Ambient1 convert phase end

8.6.2.22 Register 1Dh (address = 1Dh) [reset = 0h]

Figure 97. Register 1Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PRPCT							
R/W-0h							
7	6	5	4	3	2	1	0
PRPCT							
R/W-0h							

Table 73. Register 1Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PRPCT	R/W	0h	These bits are the count value for the counter that sets the PRF. The counter automatically counts until PRPCT and then returns back to 0 to start the count for the next PRF cycle.

8.6.2.23 Register 1Eh (address = 1Eh) [reset = 0h]

Figure 98. Register 1Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	TIMEREN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	NUMAV			
W-0h	W-0h	W-0h	W-0h	R/W-0h			

Table 74. Register 1Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0
8	TIMEREN	R/W	0h	This bit enables the timing engine that can be programmed to generate all clock phases for the synchronized transmit drive, receive sampling, and data conversion. 0 = Timer module disabled 1 = Enables timer module
7-4	0	W	0h	Must write 0
3-0	NUMAV	R/W	0h	These bits determine the number of ADC averages. By programming a higher ADC conversion time, the ADC can be set to do multiple conversions and average these multiple conversions to achieve lower noise. This programmability is set with the NUMAV bit control. The number of samples that are averaged is represented by the decimal equivalent of NUMAV + 1. For example, NUMAV = 0 represents no averaging, NUMAV = 2 represents averaging of three samples, and NUMAV = 15 represents averaging of 16 samples. When operating in PTT mode (ENABLE_PTT = 1), NUMAV must be set to a value of 1 or higher if chopping mode is enabled (ENABLE_ECG_CHOP = 1).

8.6.2.24 Register 1Fh (address = 1Fh) [reset = 0h]

Figure 99. Register 1Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	TIA_GAIN_SEP3_MSB	TIA_CF_SEP3			TIA_GAIN_SEP3_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		
7	6	5	4	3	2	1	0
0	TIA_GAIN_SEP2_MSB	TIA_CF_SEP2			TIA_GAIN_SEP2_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		

Table 75. Register 1Fh Field Descriptions(1)

Bit	Field	Type	Reset	Description
23-15	0	W	0h	Must write 0
14	TIA_GAIN_SEP3_MSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP3_MSB is the MSB of the R_F control in the Ambient1 phase.
13-11	TIA_CF_SEP3	R/W	0h	When ENSEPGAIN4 = 1, TIA_CF_SEP3 is the C_F control in the Ambient1 phase.
10-8	TIA_GAIN_SEP3_LSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP3_LSB is the three LSBs of the R_F control in the Ambient1 phase.
7	0	W	0h	Must write 0
6	TIA_GAIN_SEP2_MSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP2_MSB is the MSB of the R_F control in the LED3, Ambient2 phase.
5-3	TIA_CF_SEP2	R/W	0h	When ENSEPGAIN4 = 1, TIA_CF_SEP2 is the C_F control in the LED3, Ambient2 phase.
2-0	TIA_GAIN_SEP2_LSB	R/W	0h	When ENSEPGAIN4 = 1, TIA_GAIN_SEP2_LSB is the three LSBs of the R_F control in the LED3, Ambient2 phase.

(1) See Table 2, Table 3, Table 4, and Table 5.

8.6.2.25 Register 20h (address = 20h) [reset = 0h]

Figure 100. Register 20h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ENSEPGAIN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	TIA_GAIN_ SEP_MSB	TIA_CF_SEP			TIA_GAIN_SEP_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		

Table 76. Register 20h Field Descriptions(1)

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15	ENSEPGAIN	R/W	0h	Mode to enable independently programmable R_F and C_F values for each of two sets of phases (each set having two phases).
14-7	0	W	0h	Must write 0
6	TIA_GAIN_ SEP_MSB	R/W	0h	When ENSEPGAIN = 1, TIA_GAIN_SEP_MSB is the MSB of the R_F control in the LED2 and LED3, Ambient2 phases. When ENSEPGAIN4 = 1, TIA_GAIN_SEP_MSB is the MSB of the R_F control in the LED2 phase.
5-3	TIA_CF_SEP	R/W	0h	When ENSEPGAIN = 1, TIA_CF_SEP is the C_F control in the LED2 and LED3, Ambient2 phases. When ENSEPGAIN4 = 1, TIA_CF_SEP is the C_F control in the LED2 phase.
2-0	TIA_GAIN_SEP_LSB	R/W	0h	When ENSEPGAIN = 1, TIA_GAIN_SEP_LSB is the three LSBs of the R_F control in the LED2 and LED3, Ambient2 phases. When ENSEPGAIN4 = 1, TIA_GAIN_SEP_LSB is the three LSBs of the R_F control in the LED2 phase.

(1) See Table 2, Table 3, Table 4, and Table 5.

8.6.2.26 Register 21h (address = 21h) [reset = 0h]

Figure 101. Register 21h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	IFS_OFFDAC			0	0	FILTER_BW<0>	0
W-0h	R/W-0h			W-0h	W-0h	R/W-0h	W-0h
7	6	5	4	3	2	1	0
0	TIA_GAIN_MSB	TIA_CF			TIA_GAIN_LSB		
W-0h	R/W-0h	R/W-0h			R/W-0h		

Table 77. Register 21h Field Descriptions(1)

Bit	Field	Type	Reset	Description
23-15	0	W	0h	Must write 0
14-12	IFS_OFFDAC	R/W	0h	Programs the full-scale current range of the offset cancellation DAC.
11-10	0	W	0h	Must write 0
9	FILTER_BW<0>	R/W	0h	Bit D0 that controls the bandwidth setting of the noise-reduction filter.
8-7	0	W	0h	Must write 0
6	TIA_GAIN_MSB	R/W	0h	When both ENSEPGAIN and ENSEPGAIN4 are 0, TIA_GAIN_MSB is the MSB of the R_F control in all four phases. When ENSEPGAIN = 1, TIA_GAIN_MSB is the MSB of the R_F control in the LED1, Ambient1 phases. When ENSEPGAIN4 = 1, TIA_GAIN_MSB is the MSB of the R_F control in the LED1 phase.
5-3	TIA_CF	R/W	0h	When both ENSEPGAIN and ENSEPGAIN4 are 0, TIA_CF is the C_F control in all four phases. When ENSEPGAIN = 1, TIA_CF is the C_F control in the LED1, Ambient1 phases. When ENSEPGAIN4 = 1, TIA_CF is the C_F control in the LED1 phase.
2-0	TIA_GAIN_LSB	R/W	0h	When both ENSEPGAIN and ENSEPGAIN4 are 0, TIA_GAIN_LSB is the three LSBs of the R_F control in all four phases. When ENSEPGAIN = 1, TIA_GAIN_LSB is the three LSBs of the R_F control in the LED1, Ambient1 phases. When ENSEPGAIN4 = 1, TIA_GAIN_LSB is the three LSBs of the R_F control in the LED1 phase.

(1) See Table 2, Table 3, Table 4, and Table 5.

8.6.2.27 Register 22h (address = 22h) [reset = 0h]

Figure 102. Register 22h

23	22	21	20	19	18	17	16
ILED3_LSB		ILED2_LSB		ILED1_LSB		ILED3_MSB	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
ILED3_MSB				ILED2_MSB			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ILED2_MSB		ILED1_MSB					
R/W-0h		R/W-0h					

Table 78. Register 22h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	ILED3_LSB	R/W	0h	Lower two bits (LSBs) of ILED3 (the LED3 current control)
21-20	ILED2_LSB	R/W	0h	Lower two bits (LSBs) of ILED2 (the LED2 current control)
19-18	ILED1_LSB	R/W	0h	Lower two bits (LSBs) of ILED1 (the LED1 current control)
17-12	ILED3_MSB	R/W	0h	Upper six bits (MSBs) of ILED3 (the LED3 current control)
11-6	ILED2_MSB	R/W	0h	Upper six bits (MSBs) of ILED2 (the LED2 current control)
5-0	ILED1_MSB	R/W	0h	Upper six bits (MSBs) of ILED1 (the LED1 current control)

8.6.2.28 Register 23h (address = 23h) [reset = 0h]

Figure 103. Register 23h

23	22	21	20	19	18	17	16
0	0	0	CONTROL_ DYN_TX<0>	0	0	ILED_FS	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	R/W-0h	W-0h
15	14	13	12	11	10	9	8
ENSEPGAIN4	CONTROL_ DYN_BIAS	0	0	0	0	OSC_ENABLE	0
R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	CONTROL_ DYN_TIA	CONTROL_ DYN_ADC	0	PDNRX	PDNAFE
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h

Table 79. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0
20	CONTROL_DYN_TX<0>	R/W	0h	Always write 1. This bit is one of the bits that powers down the LED current bias when the device is in deep sleep phase.
19-18	0	W	0h	Must write 0
17	ILED_FS	R/W	0h	Programs the full-scale current range of the LED driver.
16	0	W	0h	Must write 0
15	ENSEPGAIN4	R/W	0h	Mode to enable independently programmable R_F and C_F values in each of the four phases.
14	CONTROL_DYN_BIAS	R/W	0h	Powers down the bias for the offset cancellation DAC and ADC when the device is in deep sleep phase. Always write 1.
13-10	0	W	0h	Must write 0
9	OSC_ENABLE	R/W	0h	0 = External clock mode (default). In this mode, the CLK pin functions as an input pin where the external clock can be input. 1 = Enables oscillator mode. In this mode, the 128-kHz internal oscillator is enabled and used by the timing engine.
8-5	0	W	0h	Must write 0
4	CONTROL_DYN_TIA	R/W	0h	Always write 1. Powers down the TIA when the device comes out of active mode.
3	CONTROL_DYN_ADC	R/W	0h	Always write 1. Powers down the ADC when the device comes out of active mode.
2	0	W	0h	Must write 0
1	PDNRX	R/W	0h	0 = Normal mode 1 = RX portion of the AFE is powered down
0	PDNAFE	R/W	0h	0 = Normal mode 1 = Entire AFE is powered down

8.6.2.29 Register 24h (address = 24h) [reset = 0h]

Figure 104. Register 24h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	ILED4_MSB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
15	14	13	12	11	10	9	8
ILED4_MSB					ILED4_LSB		0
R/W-0h					R/W-0h		W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 80. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
23-17	0	W	0h	Must write 0
16-11	ILED4_MSB	R/W	0h	Upper six bits (MSBs) of ILED4 (the LED4 current control)
10-9	ILED4_LSB	R/W	0h	Lower two bits (LSBs) of ILED4 (the LED4 current control)
8-0	0	W	0h	Must write 0

8.6.2.30 Register 28h (address = 28h)

Figure 105. Register 28h

23	22	21	20	19	18	17	16
x	FIFO_TOGGLE	x	x	DESIGN_ID			
R-x	R-x	R-x	R-x	R-x			
15	14	13	12	11	10	9	8
DESIGN_ID							
R-x							
7	6	5	4	3	2	1	0
DESIGN_ID	x	x	x	x	x	x	x
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

Table 81. Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
23	x	R	n/a	Read-only (don't care)
22	FIFO_TOGGLE	R	n/a	Toggles between 0 and 1 at every FIFO_RDY The FIFO_TOGGLE register bit can also be brought out on the ADC_RDY pin.
21 -20	x	R	n/a	Read-only (don't care)
19-7	DESIGN_ID	R	n/a	Silicon revision ID: contact factory for details.
6-0	x	R	n/a	Read-only (don't care)

8.6.2.31 Register 29h (address = 29h) [reset = 0h]

Figure 106. Register 29h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	SDOUT_TRISTATE	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN_SDOUT_INT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 82. Register 29h Field Descriptions

Bit	Field	Type	Reset	Description
23-11	0	W	0h	Must write 0
10	SDOUT_TRISTATE	R/W	0h	Tri-states the SDOUT buffer.
9-1	0	W	0h	Must write 0
0	EN_SDOUT_INT	R/W	0h	Set to 1 to get a programmed interrupt on SDOUT when operating in I^2C mode.

8.6.2.32 Register 2Ah (address = 2Ah)

Figure 107. Register 2Ah

23	22	21	20	19	18	17	16
LED2VAL							
R-0h							
15	14	13	12	11	10	9	8
LED2VAL							
R-0h							
7	6	5	4	3	2	1	0
LED2VAL							
R-0h							

Table 83. Register 2Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED2VAL	R	0h	These bits are the LED2 output code in 24-bit, two's complement format.

8.6.2.33 Register 2Bh (address = 2Bh)

Figure 108. Register 2Bh

23	22	21	20	19	18	17	16
ALED2VAL\LED3VAL							
R-0h							
15	14	13	12	11	10	9	8
ALED2VAL\LED3VAL							
R-0h							
7	6	5	4	3	2	1	0
ALED2VAL\LED3VAL							
R-0h							

Table 84. Register 2Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	ALED2VAL\LED3VAL	R	0h	These bits are the Ambient2 or LED3 output code in 24-bit, two's complement format.

8.6.2.34 Register 2Ch (address = 2Ch)

Figure 109. Register 2Ch

23	22	21	20	19	18	17	16
LED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1VAL							
R-0h							

Table 85. Register 2Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1VAL	R	0h	These bits are the LED1 output code in 24-bit, two's complement format.

8.6.2.35 Register 2Dh (address = 2Dh)

Figure 110. Register 2Dh

23	22	21	20	19	18	17	16
ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
ALED1VAL							
R-0h							

Table 86. Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	ALED1VAL	R	0h	These bits are the Ambient1 output code in 24-bit, two's complement format. When the ECG signal chain is enabled (ENABLE_PTT = 1), ALED1VAL denotes the output code corresponding to the ECG signal.

8.6.2.36 Register 2Eh (address = 2Eh)

Figure 111. Register 2Eh

23	22	21	20	19	18	17	16
LED2-ALED2VAL							
R-0h							
15	14	13	12	11	10	9	8
LED2-ALED2VAL							
R-0h							
7	6	5	4	3	2	1	0
LED2-ALED2VAL							
R-0h							

Table 87. Register 2Eh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED2-ALED2VAL	R	0h	These bits are the (LED2–Ambient2) output code in 24-bit, two's complement format.

8.6.2.37 Register 2Fh (address = 2Fh)

Figure 112. Register 2Fh

23	22	21	20	19	18	17	16
LED1-ALED1VAL							
R-0h							
15	14	13	12	11	10	9	8
LED1-ALED1VAL							
R-0h							
7	6	5	4	3	2	1	0
LED1-ALED1VAL							
R-0h							

Table 88. Register 2Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	LED1-ALED1VAL	R	0h	These bits are the (LED1–Ambient1) output code in 24-bit, two's complement format.

8.6.2.38 Register 31h (address = 31h) [reset = 0h]

Figure 113. Register 31h

23	22	21	20	19	18	17	16
FILTER_BW<1>	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	PD_ DISCONNECT	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	ENABLE_ INPUT_ SHORT	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 89. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
23	FILTER_BW<1>	R/W	0h	Bit D1 that controls the bandwidth setting of the noise-reduction filter.
22-11	0	W	0h	Must write 0
10	PD_DISCONNECT	W	0h	This bit disconnects the PD signals (INP, INM) from the TIA inputs. When enabled, the current input to the TIA is determined completely by the offset cancellation DAC current (I_OFFDAC). In this mode, the AFE no longer sets the bias for the PD.
9-6	0	W	0h	Must write 0
5	ENABLE_INPUT_SHORT	R/W	0h	INP, INN are shorted to V_{CM} whenever the TIA is in power-down.
4-0	0	W	0h	Must write 0

8.6.2.39 Register 34h (address = 34h) [reset = 0h]

Figure 114. Register 34h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT2_STC							
W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_STC							
W-0h							

Table 90. Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT2_STC	W	0h	Determines spare interrupt 2 start

8.6.2.40 Register 35h (address = 35h) [reset = 0h]

Figure 115. Register 35h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT2_ENDC							
W-0h							
7	6	5	4	3	2	1	0
PROG_INT2_ENDC							
W-0h							

Table 91. Register 35h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT2_ENDC	W	0h	Determines spare interrupt 2 end

8.6.2.41 Register 36h (address = 36h) [reset = 0h]

Figure 116. Register 36h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED3LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED3LEDSTC							
R/W-0h							

Table 92. Register 36h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED3LEDSTC	R/W	0h	Determines LED3 start

8.6.2.42 Register 37h (address = 37h) [reset = 0h]

Figure 117. Register 37h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED3LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED3LEDENDC							
R/W-0h							

Table 93. Register 37h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED3LEDENDC	R/W	0h	Determines LED3 end

8.6.2.43 Register 39h (address = 39h) [reset = 0h]

Figure 118. Register 39h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	CLKDIV_TE		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

Table 94. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
23-3	0	W	0h	Must write 0
2-0	CLKDIV_TE	R/W	0h	Clock division ratio for the clock divider in the path of the input clock (external clock or clock from 128-kHz internal oscillator) input to the timing engine.

8.6.2.44 Register 3Ah (address = 3Ah) [reset = 0h]

Figure 119. Register 3Ah

23	22	21	20	19	18	17	16
0	0	0	EARLY_OFFSET_DAC	POL_OFFDAC_LED2	I_OFFDAC_LED2_MID		
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
I_OFFDAC_LED2_MID	POL_OFFDAC_AMB1	I_OFFDAC_AMB1_MID				POL_OFFDAC_LED1	I_OFFDAC_LED1_MID
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
I_OFFDAC_LED1_MID			POL_OFFDAC_AMB2\POL_OFFDAC_LED3	I_OFFDAC_AMB2_MID\I_OFFDAC_LED3_MID			
R/W-0h			R/W-0h	R/W-0h			

Table 95. Register 3Ah Field Descriptions(1)

Bit	Field	Type	Reset	Description
23-21	0	W	0h	Must write 0
20	EARLY_OFFSET_DAC	R/W	0h	0 = Offset DAC phase transitions at start of SAMP 1 = Offset DAC phase transitions at start of LED_ON
19	POL_OFFDAC_LED2	R/W	0h	Offset cancellation DAC polarity for LED2
18-15	I_OFFDAC_LED2_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for LED2
14	POL_OFFDAC_AMB1	R/W	0h	Offset cancellation DAC polarity for Ambient1
13-10	I_OFFDAC_AMB1_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for Ambient1
9	POL_OFFDAC_LED1	R/W	0h	Offset cancellation DAC polarity for LED1
8-5	I_OFFDAC_LED1_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for LED1
4	POL_OFFDAC_AMB2\POL_OFFDAC_LED3	R/W	0h	Offset cancellation DAC polarity for Ambient2 (or LED3)
3-0	I_OFFDAC_AMB2_MID\I_OFFDAC_LED3_MID	R/W	0h	Middle four bits of the offset cancellation DAC setting for Ambient2 (or LED3)

(1) See Table 7 and Table 9.

8.6.2.45 Register 3Bh (address = 3Bh) [reset = 0h]

Figure 120. Register 3Bh

23	22	21	20	19	18	17	16
THR_DET_LOW_CODE							
R/W-0h							
15	14	13	12	11	10	9	8
THR_DET_LOW_CODE							
R/W-0h							
7	6	5	4	3	2	1	0
THR_DET_LOW_CODE							
R/W-0h							

Table 96. Register 3Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THR_DET_LOW_CODE	R/W	0h	24-bit code in two's complement format used for setting the low threshold when checking the output code in threshold detect mode.

8.6.2.46 Register 3Ch (address = 3Ch) [reset = 0h]

Figure 121. Register 3Ch

23	22	21	20	19	18	17	16
THR_DET_HIGH_CODE							
R/W-0h							
15	14	13	12	11	10	9	8
THR_DET_HIGH_CODE							
R/W-0h							
7	6	5	4	3	2	1	0
THR_DET_HIGH_CODE							
R/W-0h							

Table 97. Register 3Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-0	THR_DET_HIGH_CODE	R/W	0h	24-bit code in two's complement format used for setting the high threshold when checking the output code in threshold detect mode.

8.6.2.47 Register 3Dh (address = 3Dh) [reset = 0h]

Figure 122. Register 3Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	WM_MODE	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	THR_DET_PHASE_SEL<7>	THR_DET_PHASE_SEL<6>	THR_DET_PHASE_SEL<5>	THR_DET_PHASE_SEL<4>	THR_DET_PHASE_SEL<3>	THR_DET_PHASE_SEL<2>	THR_DET_PHASE_SEL<1>
W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
THR_DET_PHASE_SEL<8>	FIFO_EN_DEC	DEC_EN	THR_DET_EN	DEC_FACTOR			THR_DET_PHASE_SEL<0>
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h

Table 98. Register 3Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-19	0	W	0h	Must write 0
18	WM_MODE	R/W	0h	Enables watermark FIFO mode where the FIFO interrupt is generated based on a programmable watermark level.
17-15	0	W	0h	Must write 0
14	THR_DET_PHASE_SEL<7>	R/W	0h	Controls priority for the (LED1–AMB2) phase in threshold detect mode.
13	THR_DET_PHASE_SEL<6>	R/W	0h	Controls priority for the (AMB2–AMB1) phase in threshold detect mode.
12	THR_DET_PHASE_SEL<5>	R/W	0h	Controls priority for the (LED2–AMB1) phase in threshold detect mode.
11	THR_DET_PHASE_SEL<4>	R/W	0h	Controls priority for the (AMB1) phase in threshold detect mode.
10	THR_DET_PHASE_SEL<3>	R/W	0h	Controls priority for the (LED1) phase in threshold detect mode.
9	THR_DET_PHASE_SEL<2>	R/W	0h	Controls priority for the (AMB2) phase in threshold detect mode.
8	THR_DET_PHASE_SEL<1>	R/W	0h	Controls priority for the (LED2) phase in threshold detect mode.
7	THR_DET_PHASE_SEL<8>	R/W	0h	Controls priority for the (LED1–AMB1) phase in threshold detect mode.
6	FIFO_EN_DEC	R/W	0h	Enables the FIFO in decimation mode.
5	DEC_EN	R/W	0h	0 = Decimation mode disabled 1 = Decimation mode enabled
4	THR_DET_EN	R/W	0h	Enables threshold detect mode
3-1	DEC_FACTOR	R/W	0h	Decimation factor (how many samples are to be averaged)
0	THR_DET_PHASE_SEL<0>	R/W	0h	Controls priority for the (LED2–AMB2) phase in threshold detect mode.

8.6.2.48 Register 3Eh (address = 3Eh) [reset = 0h]

Figure 123. Register 3Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	I_OFFDAC_LED2_LSB_EXT	I_OFFDAC_AMB1_LSB_EXT	I_OFFDAC_LED1_LSB_EXT	I_OFFDAC_LED3_LSB_EXT
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
I_OFFDAC_LED2_MSB	I_OFFDAC_LED2_LSB	I_OFFDAC_AMB1_MSB	I_OFFDAC_AMB1_LSB	I_OFFDAC_LED1_MSB	I_OFFDAC_LED1_LSB	I_OFFDAC_LED3_MSB	I_OFFDAC_LED3_LSB
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 99. Register 3Eh Field Descriptions(1)

Bit	Field	Type	Reset	Description
23-8	0	W	0h	Must write 0
11	I_OFFDAC_LED2_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for LED2.
10	I_OFFDAC_AMB1_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for AMB1.
9	I_OFFDAC_LED1_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for LED1.
8	I_OFFDAC_LED3_LSB_EXT	R/W	0h	Extended LSB of the offset cancellation DAC setting for LED3.
7	I_OFFDAC_LED2_MSB	R/W	0h	MSB of the offset cancellation DAC setting for LED2.
6	I_OFFDAC_LED2_LSB	R/W	0h	LSB of the offset cancellation DAC setting for LED2.
5	I_OFFDAC_AMB1_MSB	R/W	0h	MSB of the offset cancellation DAC setting for Ambient1.
4	I_OFFDAC_AMB1_LSB	R/W	0h	LSB of the offset cancellation DAC setting for Ambient1.
3	I_OFFDAC_LED1_MSB	R/W	0h	MSB of the offset cancellation DAC setting for LED1.
2	I_OFFDAC_LED1_LSB	R/W	0h	LSB of the offset cancellation DAC setting for LED1.
1	I_OFFDAC_LED3_MSB	R/W	0h	MSB of the offset cancellation DAC setting for LED3.
0	I_OFFDAC_LED3_LSB	R/W	0h	LSB of the offset cancellation DAC setting for LED3.

(1) See Table 7 and Table 9.

8.6.2.49 Register 3Fh (address = 3Fh)

Figure 124. Register 3Fh

23	22	21	20	19	18	17	16
AVG_LED2-ALED2VAL							
R/W-0h							
15	14	13	12	11	10	9	8
AVG_LED2-ALED2VAL							
R/W-0h							
7	6	5	4	3	2	1	0
AVG_LED2-ALED2VAL							
R/W-0h							

Table 100. Register 3Fh Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AVG_LED2-ALED2VAL	R/W	0h	These bits are the 24-bit averaged output code for (LED2–Ambient2) when decimation mode is enabled. The averaging is done over the number of samples specified by the decimation factor.

8.6.2.50 Register 40h (address = 40h)

Figure 125. Register 40h

23	22	21	20	19	18	17	16
AVG_LED1-ALED1VAL							
R/W-0h							
15	14	13	12	11	10	9	8
AVG_LED1-ALED1VAL							
R/W-0h							
7	6	5	4	3	2	1	0
AVG_LED1-ALED1VAL							
R/W-0h							

Table 101. Register 40h Field Descriptions

Bit	Field	Type	Reset	Description
23-0	AVG_LED1-ALED1VAL	R/W	0h	These bits are the 24-bit averaged output code for (LED1–Ambient1) when decimation mode is enabled. The averaging is done over the number of samples specified by the decimation factor.

8.6.2.51 Register 42h (address = 42h) [reset = 0h]

Figure 126. Register 42h

23	22	21	20	19	18	17	16
INT_MUX3		INT_MUX2		0	FIFO_EARLY		
R/W-0h		R/W-0h		W-0h	R/W-0h		
15	14	13	12	11	10	9	8
FIFO_EARLY		REG_FIFO_PERIOD / REG_WM_FIFO					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
REG_FIFO_PERIOD/ REG_WM_FIFO		INT_MUX1		FIFO_PARTITION			
R/W-0h		R/W-0h		R/W-0h			

Table 102. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	INT_MUX3	R/W	0h	Selection for interrupt multiplexing on the SDOUT pin (only available in I^2C interface mode); see Table 46.
21-20	INT_MUX2	R/W	0h	Selection for interrupt multiplexing on the PROG_OUT1 pin (available in both I^2C and SPI interface modes); see Table 45.
19	0	W	0h	Must write 0
18-14	FIFO_EARLY	R/W	0h	Advances the generation of the FIFO_RDY interrupt start by a number of periods equal to the decimal equivalent of FIFO_EARLY; see Figure 42.
13-6	REG_FIFO_PERIOD/ REG_WM_FIFO	R/W	0h	Normal FIFO mode: the value of FIFO_PERIOD (periodicity of the FIFO write cycle) is set by the decimal value of REG_FIFO_PERIOD + 1. Watermark FIFO mode: the watermark level is set by the decimal value of REG_WM_FIFO + 1. The watermark level determines the difference between the write and read pointer at which a FIFO_RDY interrupt is generated. The interrupt is an indication to the MCU that (REG_WM_FIFO + 1) are waiting to be read out.
5-4	INT_MUX1	R/W	0h	Selection for interrupt multiplexing on the ADC_RDY pin; see Table 44.
3-0	FIFO_PARTITION	R/W	0h	Partitioning of the FIFO depth across the different phases of data; see Table 30 for details.

8.6.2.52 Register 43h (address = 43h) [reset = 0h]

Figure 127. Register 43h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED4LEDSTC							
R/W-0h							
7	6	5	4	3	2	1	0
LED4LEDSTC							
R/W-0h							

Table 103. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED4LEDSTC	R/W	0h	Determines LED4 start.

8.6.2.53 Register 44h (address = 44h) [reset = 0h]

Figure 128. Register 44h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
LED4LEDENDC							
R/W-0h							
7	6	5	4	3	2	1	0
LED4LEDENDC							
R/W-0h							

Table 104. Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	LED4LEDENDC	R/W	0h	Determines LED4 end.

8.6.2.54 Register 45h (address = 45h) [reset = 0h]

Figure 129. Register 45h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD1STC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD1STC							
R/W-0h							

Table 105. Register 45h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD1STC	R/W	0h	Determines the TG_PD1 start count. Must be defined if DUAL_PD_ENABLE is set to 1.

8.6.2.55 Register 46h (address = 46h) [reset = 0h]

Figure 130. Register 46h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD1ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD1ENDC							
R/W-0h							

Table 106. Register 46h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD1ENDC	R/W	0h	Determines the TG_PD1 end count. Must be defined if DUAL_PD_ENABLE is set to 1.

8.6.2.56 Register 47h (address = 47h) [reset = 0h]

Figure 131. Register 47h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD2STC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD2STC							
R/W-0h							

Table 107. Register 47h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD2STC	R/W	0h	Determines the TG_PD2 start count. Must be defined if DUAL_PD_ENABLE is set to 1.

8.6.2.57 Register 48h (address = 48h) [reset = 0h]

Figure 132. Register 48h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD2ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD2ENDC							
R/W-0h							

Table 108. Register 48h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD2ENDC	R/W	0h	Determines the TG_PD2 end count. Must be defined if DUAL_PD_ENABLE is set to 1.

8.6.2.58 Register 49h (address = 49h) [reset = 0h]

Figure 133. Register 49h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD3STC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD3STC							
R/W-0h							

Table 109. Register 49h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD3STC	R/W	0h	Determines the TG_PD3 start count. Must be defined if PD3 is used.

8.6.2.59 Register 4Ah (address = 4Ah) [reset = 0h]

Figure 134. Register 4Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
TG_PD3ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
TG_PD3ENDC							
R/W-0h							

Table 110. Register 4Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	TG_PD3ENDC	R/W	0h	Determines the TG_PD3 end count. Must be defined if PD3 is used.

8.6.2.60 Register 4Bh (address = 4Bh) [reset = 0h]

Figure 135. Register 4Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	EN_PROG_OUT1
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	CONTROL_DYN_VCM	CONTROL_DYN_DLDO	CONTROL_DYN_ALDO	CONTROL_DYN_BG
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 111. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-9	0	W	0h	Must write 0
8	EN_PROG_OUT1	R/W	0h	This bit enables PROG_OUT1 to become an output pin where interrupts can be made to come out on.
7-4	0	W	0h	Must write 0
3	CONTROL_DYN_VCM	R/W	0h	Powers down the V_{CM} buffer used to set the dc bias at the input pins and inside the ADC when the device is in deep sleep phase. Always write to 1.
2	CONTROL_DYN_DLD	R/W	0h	When operating with the internal LDOs enabled, this bit puts the digital LDO in a low power state when the device is in deep sleep phase.
1	CONTROL_DYN_ALDO	R/W	0h	When operating with the internal LDOs enabled, this bit powers down the analog LDO (and tri-states the output) when the device is in deep sleep phase. If this bit is set to 1, then short the output of the analog LDO in deep sleep phase to the output of the digital LDO using the SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP register control.
0	CONTROL_DYN_BG	R/W	0h	Powers down the band-gap and reference circuits when the device is in deep sleep phase. Always write to 1.

8.6.2.61 Register 4Eh (address = 4Eh) [reset = 0h]

Figure 136. Register 4Eh

23	22	21	20	19	18	17	16
AC_LEADOFF_FREQ	PROG_VCOMP_HIGH			PROG_VCOMP_LOW			POL_ILEADOFFP
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
POL_ILEADOFFM	MAG_ILEADOFF		CHOOSE_AC_LEADOFF	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	TRIPLE_PD_ENABLE	DUAL_PD_ENABLE	ENABLE_PTT	0	0
W-0h	W-0h	W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 112. Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
23	AC_LEADOFF_FREQ	R/W	0h	This bit sets the switching frequency of the input current sources in the ac lead-off detect scheme. 0 = Switching frequency of current sources is PRF / 4 1 = Switching frequency of current sources is PRF / 2
22-20	PROG_VCOMP_HIGH	R/W	0h	Programs the comparison voltage for the high-side comparator in the dc lead-off scheme
19-17	PROG_VCOMP_LOW	R/W	0h	Programs the comparison voltage for the low-side comparator in the dc lead-off scheme
16	POL_ILEADOFFP	R/W	0h	Programs the polarity (as source or sink) for the current source connected to INP_ECG in the dc lead-off detect scheme or the starting value of the polarity of the current source connected to INP_ECG in the ac lead-off detect scheme. Set to the invert of POL_ILEADOFFM.
15	POL_ILEADOFFM	R/W	0h	Programs the polarity (as source or sink) for the current source connected to INM_ECG in the dc lead-off detect scheme or the starting value of the polarity of the current source connected to INM_ECG in the ac lead-off detect scheme. Set to the invert of POL_ILEADOFFP.
14-13	MAG_ILEADOFF	R/W	0h	Programs the magnitude of the lead-off detect currents in both the dc and ac lead-off detect schemes
12	CHOOSE_AC_LEADOFF	R/W	0h	Sets the lead-off detect scheme as dc or ac lead-off. 0 = DC lead-off scheme 1 = AC lead-off scheme
11-5	0	W	0h	Must write 0
4	TRIPLE_PD_ENABLE	R/W	0h	This bit enables triple PD mode.
3	DUAL_PD_ENABLE	R/W	0h	This bit enables dual PD mode.
2	ENABLE_PTT	R/W	0h	This bit enables PTT mode for synchronized ECG and PPG signal acquisition. The ECG signal chain is enabled through this bit.
1-0	0	W	0h	Must write 0

8.6.2.62 Register 50h (address = 50h) [reset = 0h]

Figure 137. Register 50h

23	22	21	20	19	18	17	16
SHORT_ECG_TO_RLD		0	GAIN_ECG			0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP	ENABLE_PD2_SHORT	CONTROL_DYN_TX(1)	0	0	0
W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 113. Register 50h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	SHORT_ECG_TO_RLD	R/W	0h	Control for shorting the ECG input pins to RLD_OUT 00 = INP_ECG, INM_ECG not shorted to RLD_OUT 11 = INP_ECG, INM_ECG internally shorted to RLD_OUT
21	0	W	0h	Must write 0
20-18	GAIN_ECG	R/W	0h	Sets the gain of the INA in the ECG signal chain
17-6	0	W	0h	Must write 0
5	SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP	R/W	0h	Shorts the output of the analog LDO to the output of the digital LDO when in deep sleep mode.
4	ENABLE_PD2_SHORT	W	0h	Short PD2 input pins to VCM (internal common-mode voltage) when PD2 is disconnected from the active TIA in dual PD mode. Similarly shorts PD2 and PD3 input pins to VCM when in triple PD mode.
3	CONTROL_DYN_TX(1)	R/W	0h	Second bit that powers down LED current bias when the device is in deep sleep mode. Always write 1.
2-1	0	W	0h	Must write 0

8.6.2.63 Register 51h (address = 51h) [reset = 0h]

Figure 138. Register 51h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	MASK_FIFO_RDY	FORCE_FIFO_OFFSET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
FIFO_OFFSET_TO_FORCE							
R/W-0h							

Table 114. Register 51h Field Descriptions

Bit	Field	Type	Reset	Description
23-10	0	W	0h	Must write 0
9	MASK_FIFO_RDY	R/W	0h	Masks the FIFO_RDY interrupt generation when operating in watermark FIFO mode.
8	FORCE_FIFO_OFFSET	R/W	0h	Force the read offset address part of the FIFO read pointer. The read offset address to force is set by FIFO_OFFSET_TO_FORCE.
7-0	FIFO_OFFSET_TO_FORCE	R/W	0h	8-bit number of which decimal equivalent determines the read offset address part of the FIFO read pointer. Use in conjunction with FORCE_FIFO_OFFSET set to 1.

8.6.2.64 Register 52h (address = 52h) [reset = 0h]

Figure 139. Register 52h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DATA_RDY_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DATA_RDY_STC							
R/W-0h							

Table 115. Register 52h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DATA_RDY_STC	R/W	0h	Determines the start count for DATA_RDY, FIFO_RDY, and THR_DET_EN.

8.6.2.65 Register 53h (address = 53h) [reset = 0h]

Figure 140. Register 53h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DATA_RDY_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DATA_RDY_ENDC							
R/W-0h							

Table 116. Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DATA_RDY_ENDC	R/W	0h	Determines the end count for DATA_RDY, FIFO_RDY, and THR_DET_EN.

8.6.2.66 Register 54h (address = 54h) [reset = 0h]

Figure 141. Register 54h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	MASK_PPG			0	0	0	MASK1_PPG
W-0h	R/W-0h			W-0h	W-0h	W-0h	R/W-0h
7	6	5	4	3	2	1	0
MASK1_PPG		MASK2_PPG			MASK3_PPG		
R/W-0h							

Table 117. Register 54h Field Descriptions

Bit	Field	Type	Reset	Description
23-15	0	W	0h	Must write 0
14-12	MASK_PPG	R/W	0h	Determines the sampling rate (relative to the PRF) for the PPG signal acquisition
11-9	0	W	0h	Must write 0
8-6	MASK1_PPG	R/W	0h	Write same value as the value for MASK_PPG
5-3	MASK2_PPG	R/W	0h	Write same value as the value for MASK_PPG
2-0	MASK3_PPG	R/W	0h	Write same value as the value for MASK_PPG

8.6.2.67 Register 57h (address = 57h) [reset = 0h]

Figure 142. Register 57h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT1_STC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT1_STC							
R/W-0h							

Table 118. Register 57h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT1_STC	R/W	0h	Determines spare interrupt 1 start

8.6.2.68 Register 58h (address = 58h) [reset = 0h]

Figure 143. Register 58h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
PROG_INT1_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
PROG_INT1_ENDC							
R/W-0h							

Table 119. Register 58h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	PROG_INT1_ENDC	R/W	0h	Determines spare interrupt 1 end

8.6.2.69 Register 61h (address = 61h) [reset = 0h]

Figure 144. Register 61h

23	22	21	20	19	18	17	16
0	0	0	0	ENABLE_ECG_CHOP	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 120. Register 61h Field Descriptions

Bit	Field	Type	Reset	Description
23-20	0	W	0h	Must write 0
19	ENABLE_ECG_CHOP	R/W	0h	0 = Chopping of ECG signal chain is disabled 1 = Chopping of ECG signal chain enabled
18-0	0	W	0h	Must write 0

8.6.2.70 Register 62h (address = 62h) [reset = 0h]

Figure 145. Register 62h

23	22	21	20	19	18	17	16
ENABLE_RLD	EN_ILEAOFF	EN_LEADOFF_COMP	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h		W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 121. Register 62h Field Descriptions

Bit	Field	Type	Reset	Description
23	ENABLE_RLD	R/W	0h	0 = RLD Output is disabled 1 = RLD Output is enabled
22	EN_ILEADOFF	R/W	0h	Enables connection of lead-off current sources to the INP_ECG and INM_ECG pins in both dc and ac lead-off detect schemes.
21	EN_LEADOFF_COMP	R/W	0h	Enables connection of lead-off comparators (high voltage and low voltage) to the INP_ECG and INM_ECG pins in dc lead-off detect scheme.
20-0	0	W	0h	Must write 0

8.6.2.71 Register 63h (address = 63h) [reset = 0h]

Figure 146. Register 63h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	RCOMP_INP_HIGH	RCOMP_INP_LOW	RCOMP_INM_HIGH	RCOMP_INM_LOW
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 122. Register 63h Field Descriptions

Bit	Field	Type	Reset	Description
23-4	0	W	0h	Must write 0
3	RCOMP_INP_HIGH	R/W	0h	Output of high-side comparator on INP_ECG in dc lead-off detect mode
2	RCOMP_INP_LOW	R/W	0h	Output of low-side comparator on INP_ECG in dc lead-off detect mode
1	RCOMP_INM_HIGH	R/W	0h	Output of high-side comparator on INM_ECG in dc lead-off detect mode
0	RCOMP_INM_LOW	R/W	0h	Output of low-side comparator on INM_ECG in dc lead-off detect mode

8.6.2.72 Register 64h (address = 64h) [reset = 0h]

Figure 147. Register 64h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_TIA_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_TIA_STC							
R/W-0h							

Table 123. Register 64h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_TIA_STC	R/W	0h	Determines the start of the active phase of the TIA coinciding with the start of the device active phase.

8.6.2.73 Register 65h (address = 65h) [reset = 0h]

Figure 148. Register 65h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_TIA_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_TIA_ENDC							
R/W-0h							

Table 124. Register 65h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_TIA_ENDC	R/W	0h	Determines the end of the TIA active phase coinciding with the end of the device active phase.

8.6.2.74 Register 66h (address = 66h) [reset = 0h]

Figure 149. Register 66h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_ADC_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_ADC_STC							
R/W-0h							

Table 125. Register 66h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_ADC_STC	R/W	0h	Determines the start of the ADC active phase coinciding with the start of the device active phase.

8.6.2.75 Register 67h (address = 67h) [reset = 0h]

Figure 150. Register 67h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_ADC_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_ADC_ENDC							
R/W-0h							

Table 126. Register 67h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_ADC_ENDC	R/W	0h	Determines the end of the ADC active phase coinciding with the end of the device active phase.

8.6.2.76 Register 68h (address =68h) [reset = 0h]

Figure 151. Register 68h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_CLK_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_CLK_STC							
R/W-0h							

Table 127. Register 68h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_CLK_STC	R/W	0h	Determines the start of the active phase of the 4-MHz oscillator used for ADC conversion. Coincides with the start of the device active phase.

8.6.2.77 Register 69h (address = 69h) [reset = 0h]

Figure 152. Register 69h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DYN_CLK_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DYN_CLK_ENDC							
R/W-0h							

Table 128. Register 69h Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DYN_CLK_ENDC	R/W	0h	Determines the end of the active phase of the 4-MHz oscillator used for ADC conversion. Coincides with the end of the device active phase.

8.6.2.78 Register 6Ah (address = 6Ah) [reset = 0h]

Figure 153. Register 6Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DEEP_SLEEP_STC							
R/W-0h							
7	6	5	4	3	2	1	0
DEEP_SLEEP_STC							
R/W-0h							

Table 129. Register 6Ah Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DEEP_SLEEP_STC	R/W	0h	Determines the start of deep sleep phase.

8.6.2.79 Register 6Bh (address = 6Bh) [reset = 0h]

Figure 154. Register 6Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DEEP_SLEEP_ENDC							
R/W-0h							
7	6	5	4	3	2	1	0
DEEP_SLEEP_ENDC							
R/W-0h							

Table 130. Register 6Bh Field Descriptions

Bit	Field	Type	Reset	Description
23-16	0	W	0h	Must write 0
15-0	DEEP_SLEEP_ENDC	R/W	0h	Determines the end of deep sleep phase.

8.6.2.80 Register 6Ch (address = 6Ch) [reset = 0h]

Figure 155. Register 6Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	ENABLE_PD1_SHORT	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 131. Register 6Ch Field Descriptions

Bit	Field	Type	Reset	Description
23-12	0	W	0h	Must write 0
11	ENABLE_PD1_SHORT	R/W	0h	Short PD1 input pins to V_{CM} (internal common mode voltage) when PD1 is disconnected from the active TIA.
10-0	0	W	0h	Must write 0

8.6.2.81 Register 6Dh (address = 6Dh)

Figure 156. Register 6Dh

23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x
R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh
7	6	5	4	3	2	1	0
REG_POINTER_DIFF							
R-xh							

Table 132. Register 6Dh Field Descriptions

Bit	Field	Type	Reset	Description
23-8	x	R	n/a	Read-only (don't care)
7-0	REG_POINTER_DIFF	R	n/a	The instantaneous value of the (write pointer minus read pointer) minus 1 is stored in REG_POINTER_DIFF. When a FIFO_RDY interrupt is issued, the value stored in REG_POINTER_DIFF is expected to be equal to the value programmed in REG_WM_FIFO.

8.6.2.82 Register 72h (address = 72h) [reset = 0h]

Figure 157. Register 72h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
EN_DRV2_ LED4	EN_DRV2_ LED3	EN_DRV2_ LED2	EN_DRV2_ LED1	DIS_DRV1_ LED4	DIS_DRV1_ LED3	DIS_DRV1_ LED2	DIS_DRV1_ LED1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 133. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
23-8	0	W	0h	Must write 0
7	EN_DRV2_LED4	R/W	0h	Enables driver 2 controls for LED4.
6	EN_DRV2_LED3	R/W	0h	Enables driver 2 controls for LED3.
5	EN_DRV2_LED2	R/W	0h	Enables driver 2 controls for LED2.
4	EN_DRV2_LED1	R/W	0h	Enables driver 2 controls for LED1.
3	DIS_DRV1_LED4	R/W	0h	Disables driver 1 controls for LED4.
2	DIS_DRV1_LED3	R/W	0h	Disables driver 1 controls for LED3.
1	DIS_DRV1_LED2	R/W	0h	Disables driver 1 controls for LED2.
0	DIS_DRV1_LED1	R/W	0h	Disables driver 1 controls for LED1.

8.6.2.83 Register 73h (address = 73h) [reset = 0h]

Figure 158. Register 73h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHANGE_SEL_LOGIC	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 134. Register 73h Field Descriptions

Bit	Field	Type	Reset	Description
23-22	0	W	0h	Must write 0
1-0	CHANGE_SEL_LOGIC	R/W	0h	Determines whether the THR_DET_RDY interrupt is generated by the output code going in-range or out-of-range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following points are a collection of important considerations related to using the AFE4900 and are summarized as a handy reference:

1. Avoid extended operation of the AFE4900 where some supplies are on and others are off. Such operation can result in spurious currents; see the *Power Supply Recommendations* section for additional guidelines related to power supplies.
2. Always issue a reset (either through the pin or through software) after the three supplies have stabilized and before writing into the registers. If using a software reset, write register 00h first with the SW_RESET bit set to 1. Then, after a delay, again program the other bits in register 00h with the SW_RESET bit set to 0.
3. Always set the ENABLE_ULP register bit to 1 before configuring the other registers. A full set of recommended registers to be included in the initialization sequence is listed in .
4. Do not expose the device to high temperatures or to UV light (see the *Absolute Maximum Ratings* table).
5. If system-level ESD requirements exceed the device-level ESD specifications, additional external protection diodes may be required.
6. In compliance with the absolute maximum ratings, ensure that the LED_ON duty cycles do not exceed the rated specifications.
7. A reduction in the LED_ON time and the associated reduction in the SAMP width can help reduce the power consumption of both the transmitter and receiver. However, excessively short LED_ON and SAMP durations can cause an attenuation in the heart-rate signal; see the *Sampling Width Considerations for PPG Signal Acquisition* section for guidelines on choosing the SAMP duration.
8. To ensure that there is always a mechanism for the AFE to maintain proper bias on the PD, follow the guidelines mentioned in the *PD Bias Settling Time Considerations* section.
9. Ensure that the PD has characteristics that satisfy the guidelines outlined in the *Choosing a PD with the Right Characteristics* section.
10. There can be cases that require all four LED_ON signals to be defined if the corresponding SAMP phase is used as an ambient phase; see Table 29 for a list of such cases.

Application Information (continued)

11. See the *Operation With One, Two, or Three LEDs* section for the associated considerations when changing the order of the four phases without using one or more of the four phases.
12. When dealing with high modulation in ambient light, use the guidelines mentioned in the *Reducing Sensitivity to Ambient Light Modulation* section to reduce or eliminate the artefacts associated with ambient light.
13. Use the appropriate interface circuit when interfacing the ECG electrodes to the AFE. Additional considerations related to safety must be taken care of as part of the system design.

The AFE4900 is designed to operate with a minimal number of external components. A reset (hardware or software reset) is essential after power-up to ensure that all registers are reset to default values. The AFE4900 can be driven with an external clock. The photodiode outputs are prone to picking up noise. As such, especially when operating in coexistence and close proximity with RF communication circuitry [such as Bluetooth® low energy (BLE)], a common-mode choke can be used in the path of the device inputs to reject the RF interference. Contact the factory for further details.

Figure 159 and Figure 160 illustrate the typical connections of the AFE4900. The following points must be followed:

1. Use decoupling capacitors (1 µF or higher) placed close to the device to filter noise on RX_SUP, IO_SUP, and TX_SUP.
2. The voltage level used for IO_SUP must be the same as the I/O voltage level for the MCU. CONTROL1 and I2C_SPI_SEL can be directly driven from the MCU (with IO_SUP levels) if their V_{IH}, V_{IL} levels can be satisfied. In LDO enable mode, a level shifter may be required on the I2C_SPI_SEL input if RX_SUP is higher than IO_SUP by more than 0.3 V.
3. A series resistor (R_{series}, for example, 1 kΩ) is recommended to be connected on the CLK pin. At power-up and before a RESET pulse is applied, the CLK pin can be configured as an output pin in the uninitialized state. In such a scenario, R_{series} limits the current because the MCU also attempts to drive the CLK pin.
4. When in power-down mode (PWDN), the external CLK can be shut off to avoid any switching current.

Application Information (continued)

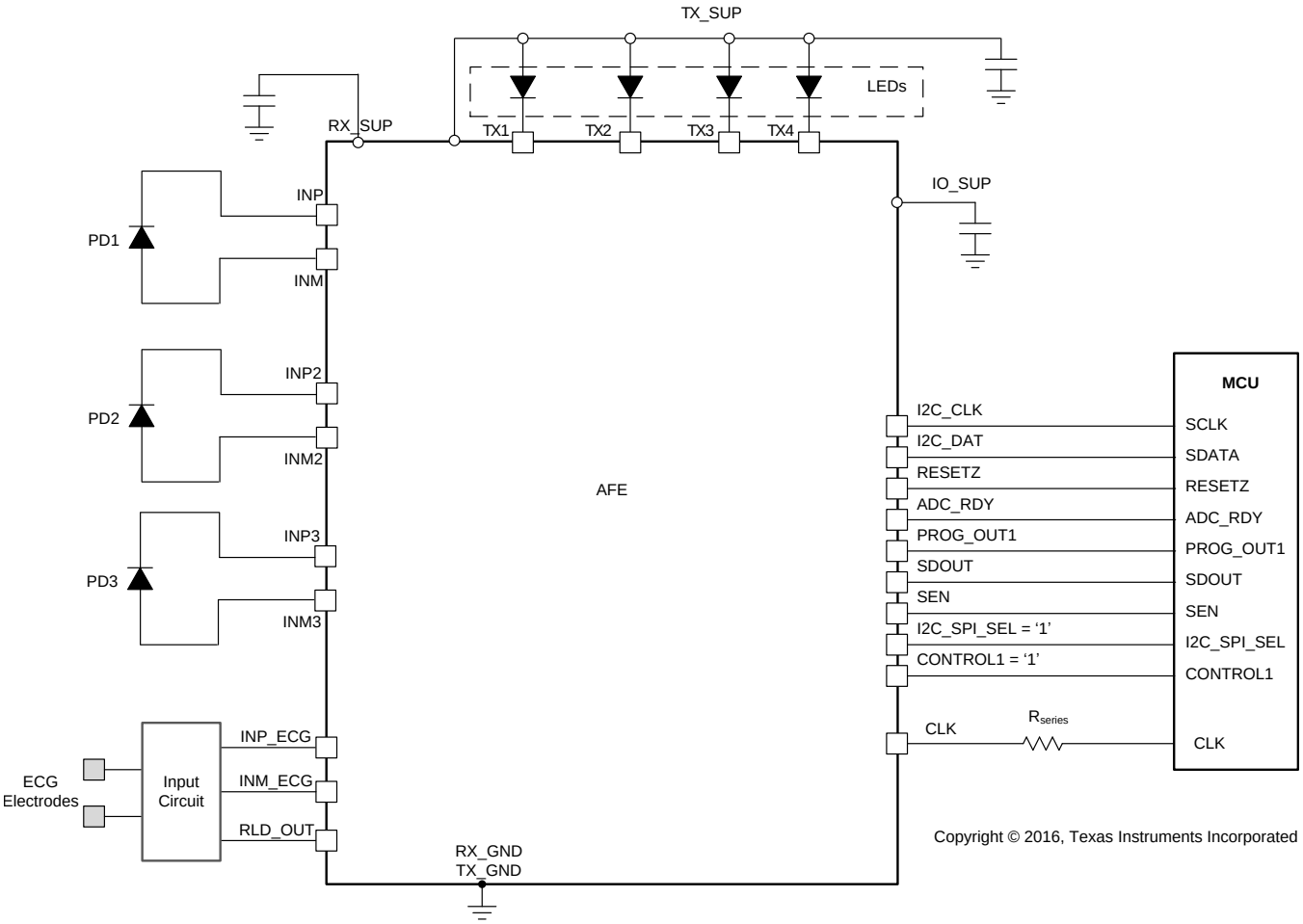


Figure 159. Typical Device Connections in SPI Interface Mode With an External Clock: LDO Bypass Mode

Application Information (continued)

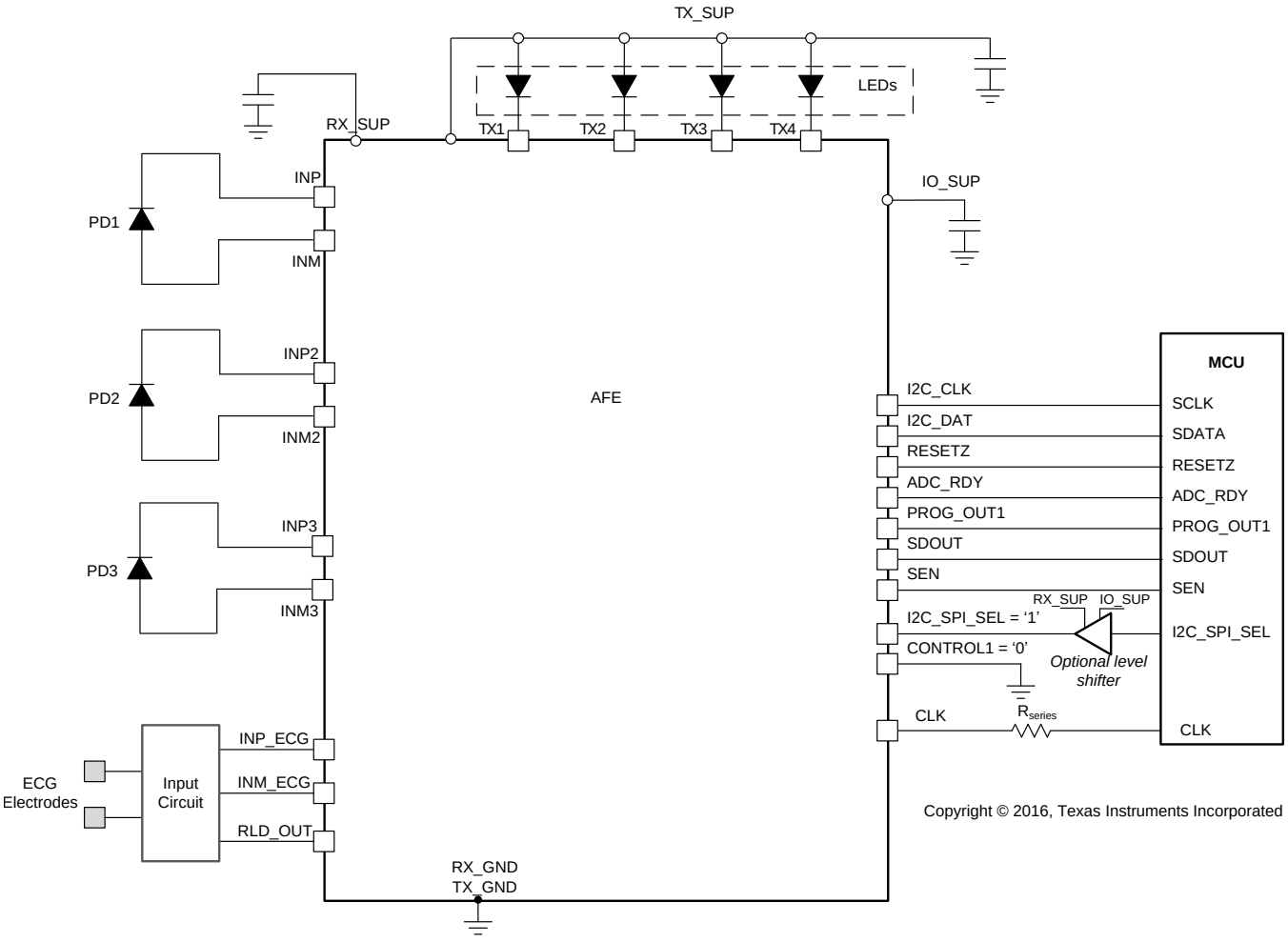


Figure 160. Typical Device Connections in SPI Interface Mode With an External Clock: LDO Enable Mode

9.1.1 Operation With One, Two, or Three LEDs

Up to three LEDs can be turned on sequentially within a pulse repetition period. Using all three LEDs leaves a common ambient phase that can be subtracted from each of the three LED signals. For the subtraction to be effective, the TIA settings must be the same between each of the LED phases and the ambient phase.

Figure 161 shows the LED_ON and sample signals for the case of three LEDs and one ambient phase.

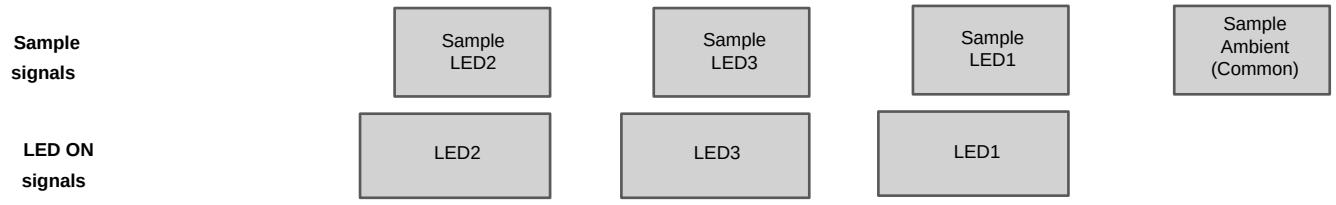


Figure 161. Use Case With Three LEDs and One Ambient Phase

Application Information (continued)

If two LED phases are used, then the remaining two phases can be used as ambient phases. The gain settings for the LED and the corresponding ambient must be set to the same value. However, the gain settings for LED1, Ambient1 can be set differently from LED2, Ambient2 by setting ENSEPGAIN = 1. Figure 162 details this case.

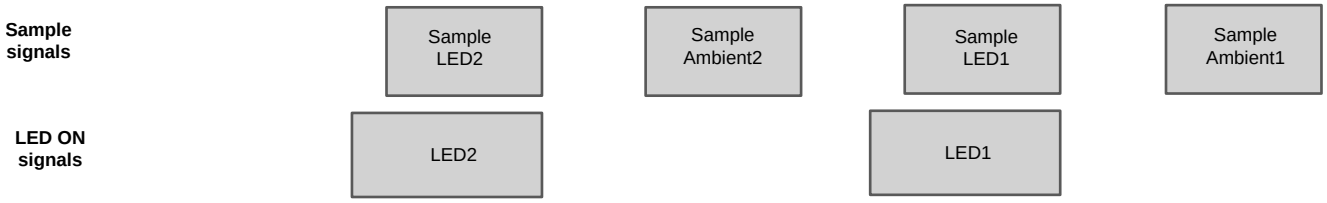


Figure 162. Use Case With Two LEDs and Two Ambient Phases

If only one LED phase is required, then one of the other phases can be used as an ambient phase and the other two phases can be blanked out. Use a common TIA setting (default, ENSEPGAIN = 0, ENSEPGAIN4 = 0). Figure 163 shows the case with one LED and one ambient phase.

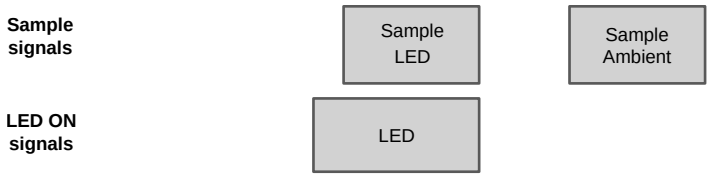


Figure 163. Use Case With One LED and One Ambient Phase

1. If a particular LED or ambient phase is not required, then the timing signals (LED_ON, sampling, ADC conversion) corresponding to the unused phase are recommended to be blanked out by setting the start and end counts to a value greater than PRPCT.
2. If the sequence of the LED phases is altered with respect to what is described in Figure 161, then the sequence of the SAMP phases must also be correspondingly changed. Table 135 describes the manner in which the contents of the output registers must be reinterpreted. If some of the conversion phases are blanked out, then the corresponding registers do not hold any relevant content.

Table 135. Generalized Content of the Output Registers

REGISTER	CONTENT
2Ah	ADC output corresponding to the 1st CONV phase
2Bh	ADC output corresponding to the 2nd CONV phase
2Ch	ADC output corresponding to the 3rd CONV phase
2Dh	ADC output corresponding to the 4th CONV phase
2Eh	ADC output corresponding to the difference of the 1st and 2nd CONV phases
2Fh	ADC output corresponding to the difference of the 3rd and 4th CONV phases
3Fh	Averaged output in decimation mode corresponding to the difference of the 1st and 2nd CONV phases
40h	Averaged output in decimation mode corresponding to the difference of the 3rd and 4th CONV phases

3. Table 136 shows the FIFO_PARTITION for a generalized timing scheme.

Table 136. FIFO Partitioning Based on Conversion Order

FIFO_PARTITION	PHASE 1	PHASE 2	PHASE 3	PHASE 4	PHASE 5	PHASE 6
0000	1st CONV	2nd CONV	3rd CONV	4th CONV	—	—
0001	(3rd-4th CONV)	—	—	—	—	—
0010	3rd CONV	4th CONV	—	—	—	—
0011	(1st-2nd CONV)	—	—	—	—	—
0100	1st CONV	2nd CONV	—	—	—	—
0101	(1st-2nd CONV)	(3rd-4th CONV)	—	—	—	—
0110	(3rd-4th CONV)	(1st-4th CONV)	(2nd-4th CONV)	—	—	—
0111	1st CONV	2nd CONV	(1st-2nd CONV)	3rd CONV	4th CONV	(3rd-4th CONV)
1000	Average (all 4 CONVs)	—	—	—	—	—
Other settings	Do not use					

9.1.2 Example LED Configurations

A few typical LED configurations are shown in this section.

9.1.2.1 Case I: Up to Three LEDs in Sequential Operation

Figure 164 shows the suggested configuration for this operation. LED2, LED3, and LED1 are fired in sequence one after the other with SAMP2, SAMP3, and SAMP1 being the corresponding sampling phases. SAMP4 is used as the ambient phase.

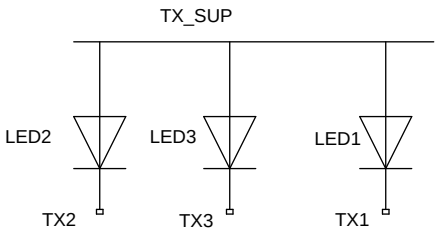


Figure 164. Configuration for Three LEDs in Sequential Operation

Table 137 lists the positioning of the SAMP, LED, and CONV phases. The position of the common ambient can also be adjusted to fall between when the LEDs are fired.

Table 137. Timing Control for Three LEDs in Sequential Operation

SAMP PHASE	LED2	LED3	LED1	LED4	CONV PHASE	COMMENTS
SAMP2	On	—	—	—	CONV2	First LED
SAMP3	—	On	—	—	CONV3	Second LED
SAMP1	—	—	On	—	CONV1	Third LED
SAMP4	—	—	—	—	CONV4	Common ambient

9.1.2.2 Case II: Two LEDs in Parallel Operation and Up to Two Such Sets in Sequence

Figure 165 shows the suggested configuration for this operation. LED2 and LED3 are fired in parallel (with SAMP2 as the common sampling phase). LED1 and LED4 are also fired in parallel with SAMP1 as the common sampling phase. SAMP3 and SAMP4 can be positioned outside the two LED firing windows and can be used to acquire the ambient signals.

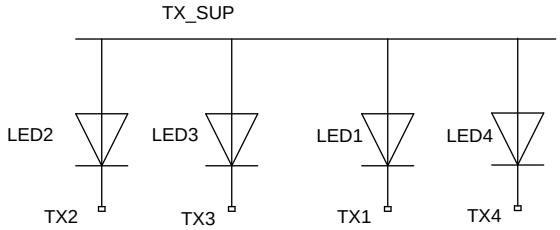


Figure 165. Configuration for Two LEDs in Parallel Operation and Up to Two Such Sets in Sequence

Table 138 lists the positioning of the SAMP, LED, and CONV phases.

Table 138. Timing Control for Two LEDs in Parallel Operation and Up to Two Such Sets in Sequence

SAMP PHASE	LED2	LED3	LED1	LED4	CONV PHASE	COMMENTS
SAMP2	On	On	—	—	CONV2	First set of LEDs
SAMP3	—	—	—	—	CONV3	First ambient
SAMP1	—	—	On	On	CONV1	Second set of LEDs
SAMP4	—	—	—	—	CONV4	Second ambient

9.1.2.3 Case III: Two LEDs in Parallel Operation and in Sequence With Two More LEDs

Figure 166 shows the suggested configuration for this operation. LED2 and LED3 are fired in parallel with SAMP2 as the common sampling phase. The parallel firing is followed by a common ambient phase defined by SAMP3. This phase can then be followed by the sequential firing of LED1 and LED4 with SAMP1 and SAMP4 as the respective sampling phases.

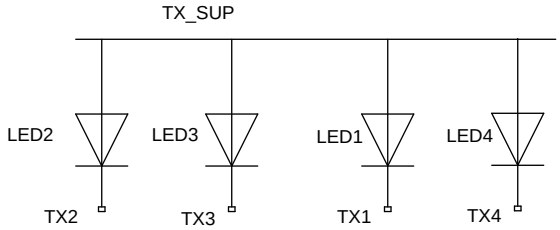


Figure 166. Configuration for Two LEDs in Parallel Operation and in Sequence With Two More LEDs

Table 139 lists the positioning of the SAMP, LED, and CONV phases.

Table 139. Timing Control for Two LEDs in Parallel Operation and in Sequence With Two More LEDs

SAMP PHASE	LED2	LED3	LED1	LED4	CONV PHASE	COMMENTS
SAMP2	On	On	—	—	CONV2	First set of LEDs
SAMP3	—	—	—	—	CONV3	Common ambient
SAMP1	—	—	On	—	CONV1	Second LED
SAMP4	—	—	—	On	CONV4	Third LED

9.1.3 Reducing Sensitivity to Ambient Light Modulation

Ambient light has an additive effect to the LED phase output of the AFE because ambient light is incident on the photodiode in a manner similar to the light originating from the LED. Therefore, any artifacts in the ambient light can interfere with the extraction of the heart rate from the signal in the LED phase. The purpose of subtracting the ambient phase signal from the LED phase signal is to remove this effect.

The effect of low-frequency ambient light is rejected by subtracting the ambient phase data from the LED phase data.

If the effect of ambient light on the LED and ambient phase outputs is unequal, then subtraction of the ambient phase data from the LED phase data gives only an incomplete cancellation of the ambient light modulation effect. In that case, a periodic pattern in the ambient light can cause spurious tones to appear in the LED minus ambient data. The start of LED_ON to the start of SAMP (t_{LED_SAMP}) plays a role in the sensitivity to ambient light modulation. Increasing this separation improves the rejection to interference from ambient light. Also, the TIA maintains the photodiode bias through a negative feedback. If the TIA output saturates, then the photodiode bias is disturbed. The associated transient for the photodiode bias to be restored can increase the sensitivity to ambient light modulation. For example, in the timing scheme described in Figure 161, a saturation of the TIA output during the LED3 phase can cause the TIA recovery response to span both the LED1 and Ambient1 phases. Such a transient recovery can cause the channel response to differ between these two phases, thereby rendering the ambient subtraction, LED1 minus Ambient1 signal, to be incomplete. Therefore, the output of every phase is recommended to be prevented from saturating (through periodic signal monitoring and gain adjustment) even if the data from that phase is not used by the heart-rate estimation algorithm. If the ambient light changes at a fast rate, the effective ambient signal during the LED and ambient phases can be different because of the difference between the sampling instants. This difference also can cause the ambient subtraction to be incomplete. Reducing the spacing between the sampling instants of the LED and ambient phases can reduce this effect.

Figure 167 shows the modulation in ambient light that is common to both the LED and ambient phases. Ideal ambient cancellation requires the LED minus ambient signal to completely reject the modulation in the ambient light. Figure 168 shows the LED minus ambient data for when the AFE4900 settings are not optimal. Figure 169 shows the LED minus ambient signal for optimal settings.

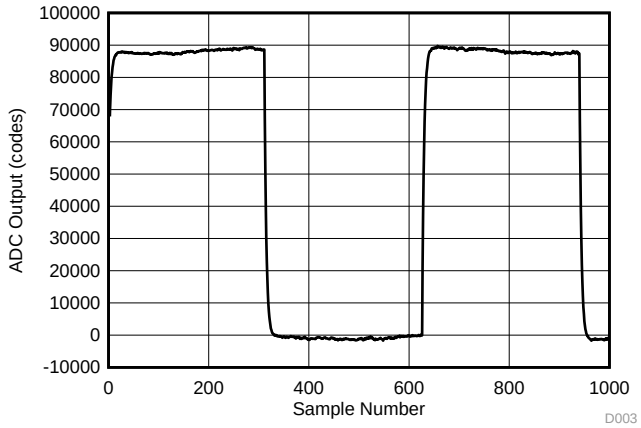


Figure 167. Ambient Data With Ambient Light Modulation

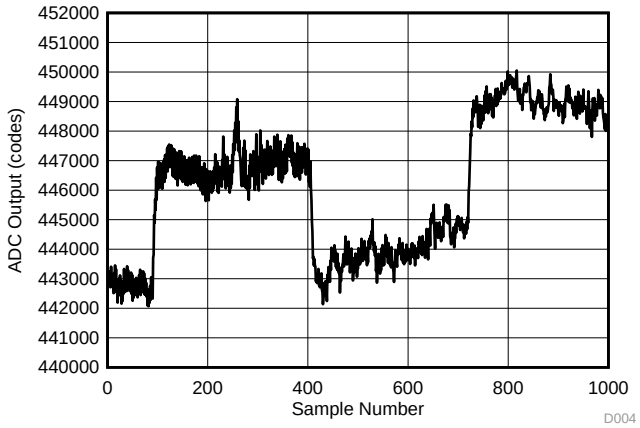


Figure 168. LED – Ambient Data with a Nonoptimal AFE4900 Setting

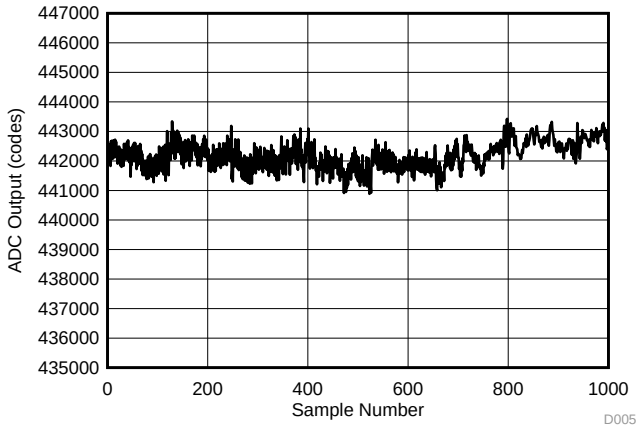


Figure 169. LED – Ambient Data With an Optimal AFE4900 Setting

9.1.4 Sampling Width Considerations for PPG Signal Acquisition

There are multiple factors that govern the choice of the sampling width (SAMP signal) and LED_ON time. Figure 170 shows the TIA settling behavior during the LED and SAMP phases. The TIA is shown to be the superposition of the following two components:

- $V(TIA_{LED})$: the settling of the TIA to the current signal from the PD resulting from the LED turning on
- $V(TIA_{OFFSET\_DAC})$: the settling of the TIA to the transition in the offset DAC

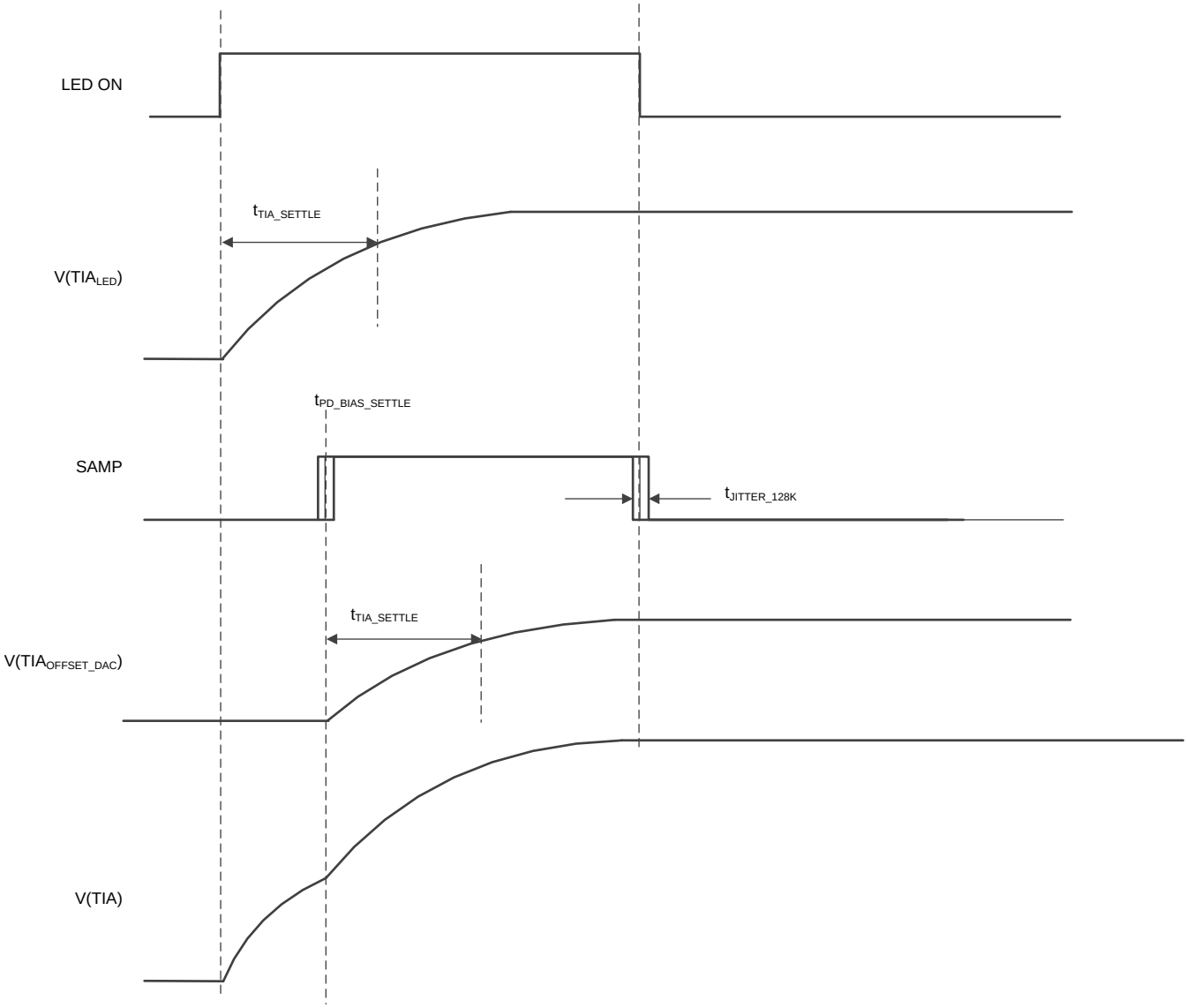


Figure 170. TIA Settling Transient

To speed up the TIA settling when there is a transition in the offset DAC setting across phases, set the EARLY_OFFSET_DAC register bit. Figure 171 shows that this bit causes the offset DAC transition to begin at the start of the LED_ON signal instead of at the start of the SAMP signal and results in a faster transient.

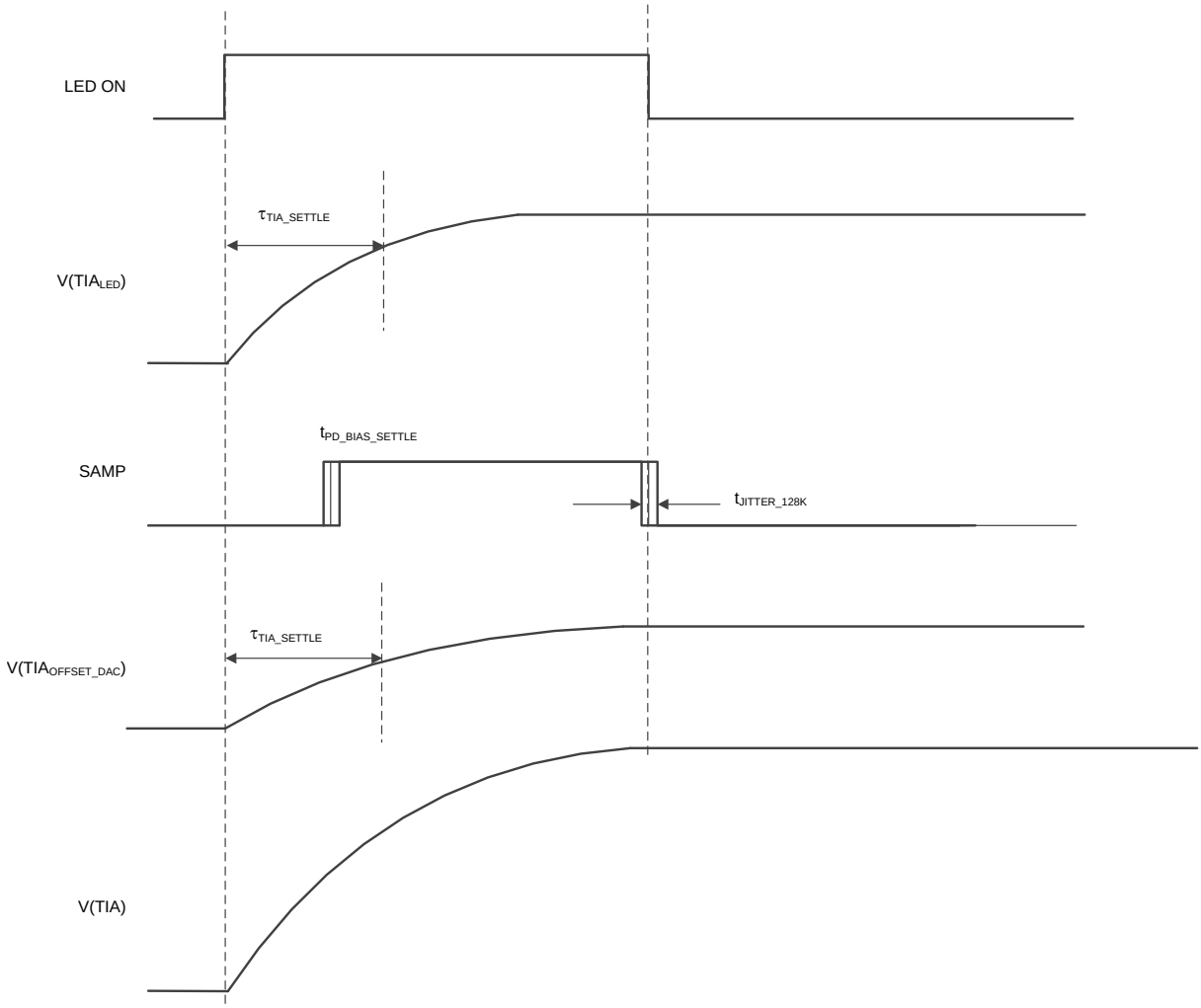


Figure 171. TIA Settling Transient With EARLY_OFFSET_DAC Set to 1

With the EARLY_OFFSET_DAC set to 1, the considerations for determining the LED and SAMP width are as follows:

- The TIA time constant (τ_{TIA_SETTLE}) is given by the product of R_F and C_F.
- The noise-reduction filter is connected to the TIA output in the SAMP phase. Ideally, connect the noise-reduction filter to the TIA output only after the output has settled close to the final value. Therefore, t_{LED_SAMP} (the separation between the LED_ON start and the SAMP start) is recommended to be at least 3 × τ_{TIA_SETTLE}. Additional considerations from achieving optimal ambient rejection may require a separation higher than this value.
- f_{SIG}, the effective signal bandwidth is determined as $f_{RC} \times t_{W\_SAMP} / t_{PRF}$, where f_{RC}, t_{W_SAMP}, and t_{PRF} correspond to the noise-reduction filter bandwidth, SAMP width, and PRF period (respectively). Choose the parameters such that the signal bandwidth is much higher than the bandwidth of interest (for example, 4 Hz). f_{RC} can have a device-to-device variation that can cause the value to be up to 35% lower than the nominal value. As an example, with an external clock of 32 kHz (t_{TE} = 31.25 µs): f_{RC} = 2.5 kHz, t_{W_SAMP} = 93.75 µs (3 × t_{TE}), and t_{PRF} = 20 ms (50-Hz PRF). For this case, a worst-case (lowest) f_{SIG} is: f_{SIG} = (2.5 kHz × 0.65) (93.75µs) / 20 ms = 7.6 Hz.
- An additional consideration when operating in internal oscillator mode (t_{TE} = 7.8125 µs) comes from the jitter of the 128-kHz oscillator that affects the sampling instant. To avoid any noise degradation from this jitter, the

TIA output must be well settled at the falling edge of the SAMP signal. The SAMP width is recommended to be at least 7 to 8 TIA time constants to keep the noise degradation from jitter small. As an example, for t_{W_SAMP} = 31.25 µs (equal to 4 × t_{TE}), R_F= 500 kΩ. The jitter considerations require t_{TIA_SETTLE} to be approximately 4 µs or lower. So for this case, C_F can be chosen to be the highest setting with a value lower than 8 pF. With the EARLY_OFFSET_DAC bit set to 1, the TIA settling is advanced and the effect of jitter reduces for the same SAMP duration.

9.1.5 Handling Signal-Chain Transient Behavior

Because of presence of the noise-reduction filter in the receiver signal chain, any disturbance to the steady-state signal from the photodiode in a given phase can result in an associated settling time that can span multiple PRF cycles. The time constant associated with the noise-reduction filter is equal to 1 / ($2\pi f_{RC}$). Thus, for an f_{RC} = 2.5 kHz, the time constant of the filter is 64 µs. Depending on the extent of the signal transient, 5 to 10 filter time constants may be required to return to steady state. The filter is switched to the TIA output only during the SAMP phase; therefore, the filter recovery can span over several PRF cycles.

For example, at 50-Hz PRF, 90.55-µs SAMP width, and f_{RC} = 2.5 kHz, the time required for recovery from a disturbance to the signal can be in the range of 100 ms, a parameter referred to as $t_{CHANNEL}$.

The quickest way to speed up this transient and reduce $t_{CHANNEL}$ is to change the timing temporarily to a higher PRF so that the filter has more frequent active time for enabling quicker settling. The other way to speed up the transient is to temporarily increase the filter bandwidth setting. However, a change in filter bandwidth setting slightly changes the dc value of the output code.

The other type of transient behavior is when the TIA saturates in one of the phases. The recovery of the TIA can affect the subsequent phase especially if the SAMP phases are close to each other. The recovery time also depends on the oversaturation factor, which is the factor by which the signal current in the saturating phase is higher than the input current required to cause a full-scale TIA output. Figure 172 shows the recovery in the ambient phase as a function of the oversaturation factor in the preceding LED phase.

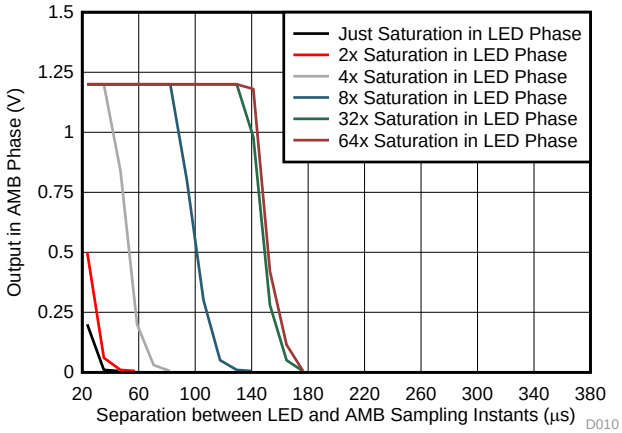


Figure 172. Recovery of the Ambient Phase as a Function of the Oversaturation Factor in the LED Phase

9.1.6 Reference Circuits for ECG Signal Acquisition

Figure 173 shows a few schemes for connecting the ECG electrodes to the AFE input pins. Scheme 1 shows the electrodes ac-coupled to the ECG input pins and require the ac lead-off detection. Schemes 2 and 3 show the electrodes dc-coupled to the ECG inputs and can work with dc lead-off detection. These circuits are only meant to be for reference. The choice of the exact scheme and the component values depends on factors related to the product design and may need to be modified from the below schemes based on other considerations like product safety, grounding strategy, noise optimization, signal acquisition time, and so forth.

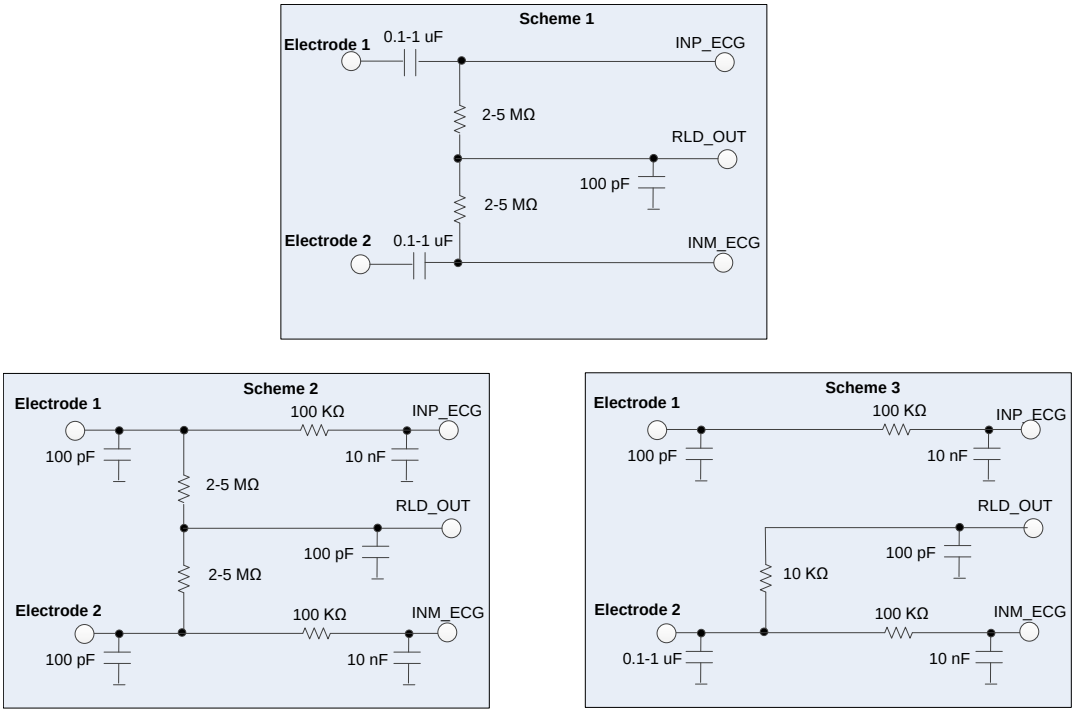


Figure 173. Reference Circuits for Connecting the ECG Electrodes to the ECG Input Pins

9.1.7 ECG Lead-Off Detection

The choice of ECG lead-off detect scheme (dc or ac) depends on whether the electrodes are dc-coupled to the input pins or ac-coupled. Figure 174 illustrates the dc lead-off scheme being used to detect the presence or absence of electrodes.

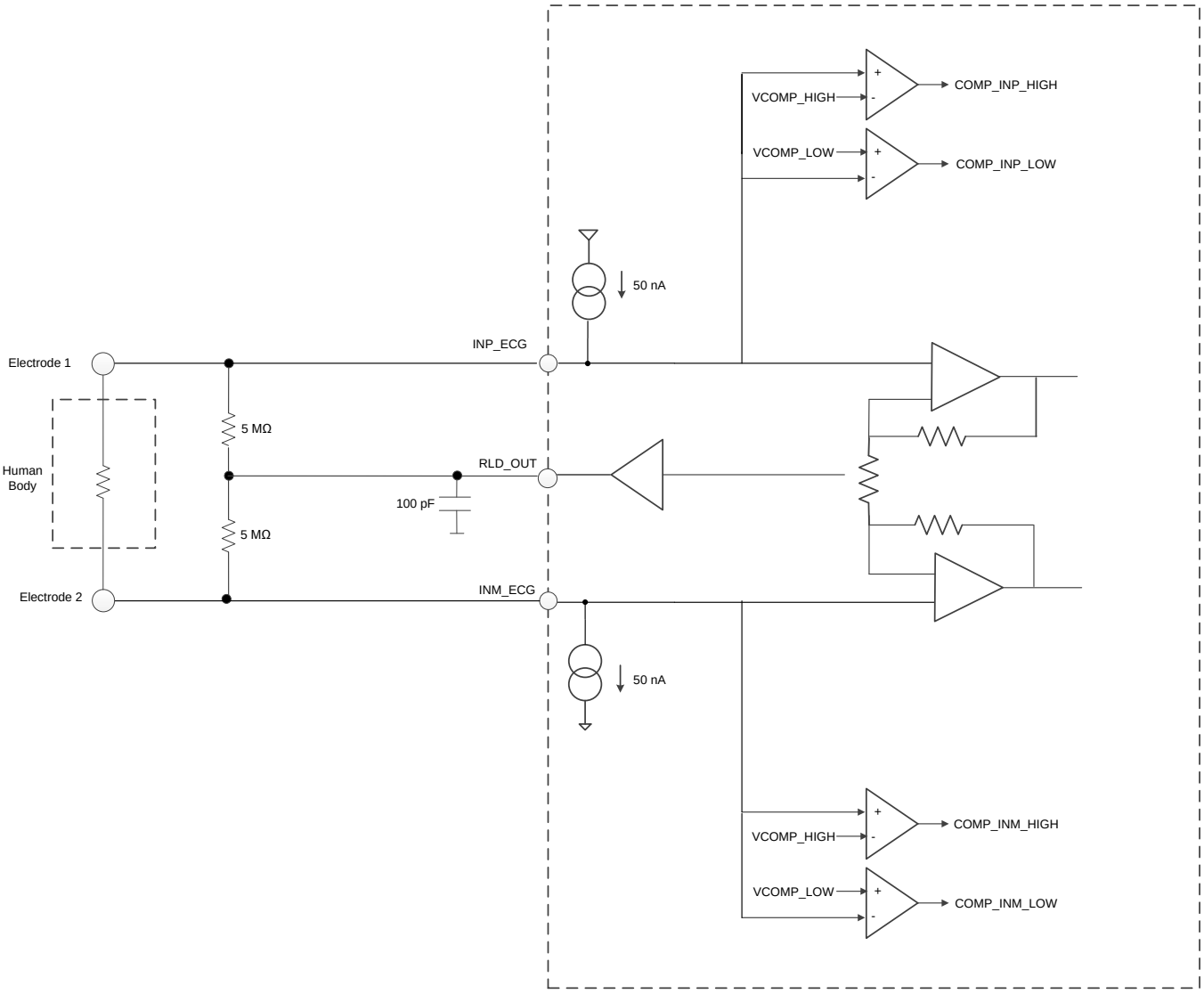


Figure 174. Illustration of DC Lead-Off Detect Scheme

The dc lead-off currents on INP_ECG and INM_ECG are shown as programmed to 50 nA with opposite polarities (source on INP_ECG and sink on INM_ECG). With the electrodes not contacted by the human body, the current sources flow in and out of an impedance of 10 MΩ, generating a differential drop of 500 mV. With the human body contacting the electrodes, a low impedance shunt path is presented to the current sources and the differential voltage across INP_ECG, INM_ECG goes low. The programmable thresholds of the dc lead-off detect comparators can be set appropriately to detect the presence or absence of the human contact to the electrodes.

When the ac lead-off detect is used, the component corresponding to the lead-off impedance appears at the ECG output. The frequency of this component can be either f_{ECG} / 2 or f_{ECG} / 4 based on the AC_LEADOFF_FREQ register setting. The strength of this component can be used to determine if there is a lead-off condition. To extract the strength of this component, either frequency domain processing could be used or time domain processing could turn out to be sufficient. For example, for the f_{ECG} / 2 setting, a difference between the moving average of the odd and even samples can be an indicator of the strength of this component.

9.1.8 Connecting Two AFE4900s in Parallel

As shown in Figure 175, if two AFE4900s running in parallel must share a common I^2C bus, then such parallel operation can be accomplished by keeping the slave address of the two AFE4900s different in the LSB by connecting the SEN pins of device 1 and device 2.

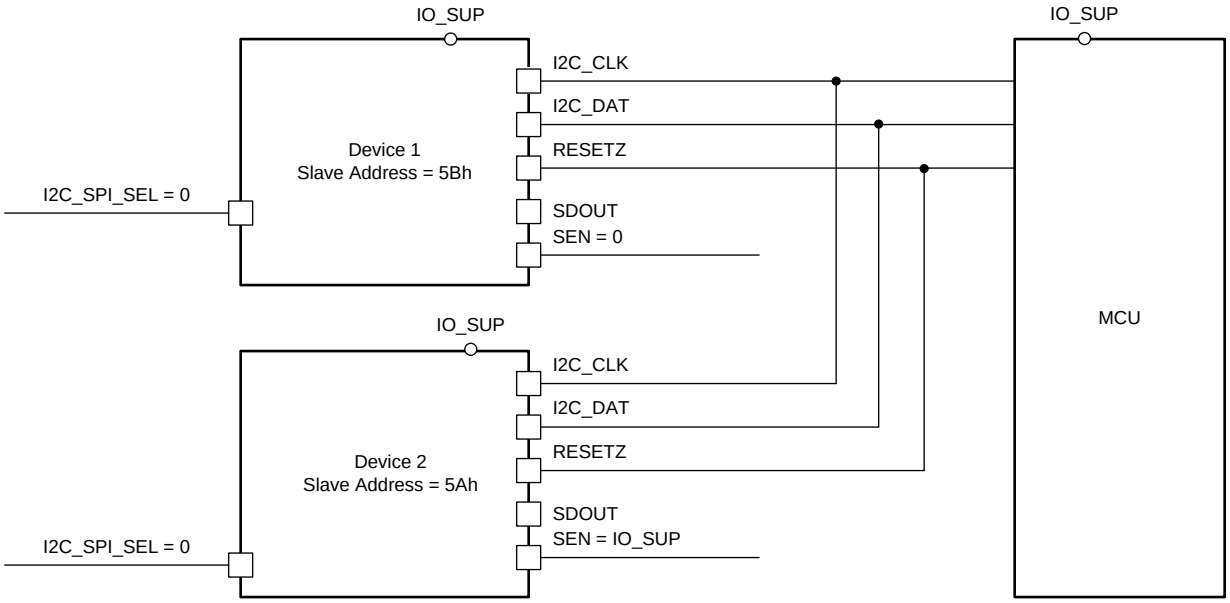


Figure 175. Connection of Two AFE4900s to the MCU When Operating in I^2C Mode

Figure 176 shows a case where the parallel devices are operated in SPI mode with two fully independent SPI interfaces from the MCU.

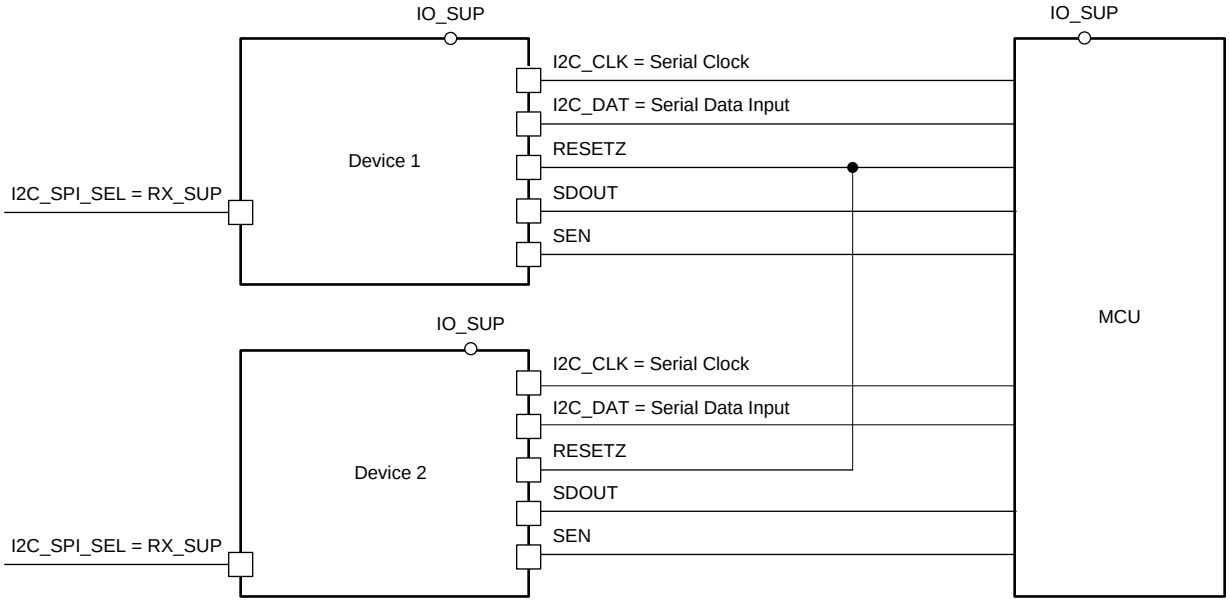


Figure 176. Connection of Two AFE4900s in SPI Mode With an Independent SPI Bus

Figure 177 shows a case where the parallel AFE4900s share some part of the SPI bus. The serial clock and serial data can be shared between the two AFE4900s but the SEN control to each device must be separate. Additionally, if the SDOUTs are shared between the two devices, then care must be taken to avoid a situation where there is a simultaneously active SEN on both devices.

When an AFE is powered down, its SDOUT line is internally pulled to ground. Thus, the SDOUT bus between two AFEs cannot be shared if the bus is required to operate one AFE in active mode and the other in power-down mode.

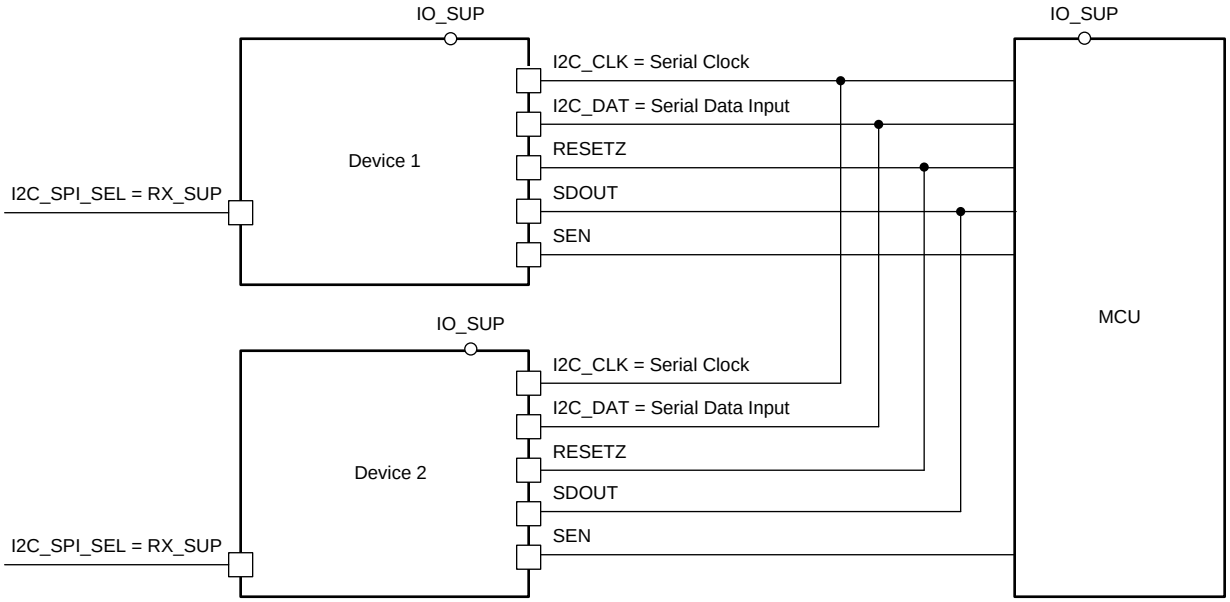


Figure 177. Connection of Two AFE4900s in SPI Mode That Share a Portion of the SPI Bus

9.1.9 Choosing a PD with the Right Characteristics

The TIA of the AFE sets the bias on the INP, INM pins through negative feedback. The differential voltage on the INP, INM pins (INP–INM) is nominally at 0 V, causing the PD to operate in zero bias. However, depending on offsets in the TIA, the differential voltage can be either slightly positive or slightly negative, resulting in the PD operating with either slight forward bias or slight reverse bias. Therefore, TI recommends choosing a PD that has a fairly constant sensitivity to light over ±150 mV of bias over the operating range of light intensity. Figure 178 illustrates the *sensitivity versus reverse bias* characteristics of two PDs—one that is fairly flat over a ±150-mV range of bias (recommended) and the other that falls sharply to approximately zero bias (not recommended).

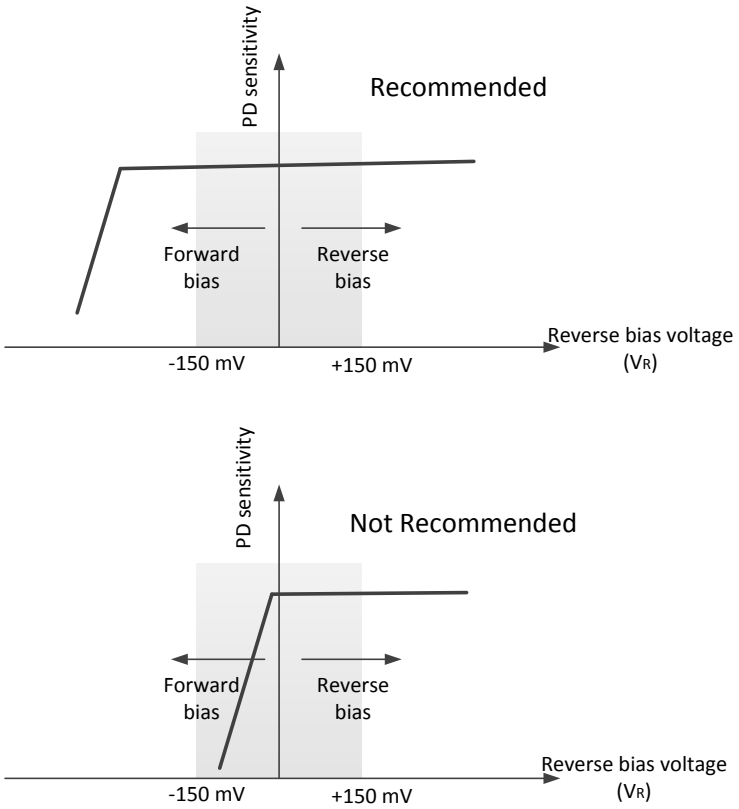


Figure 178. PD Sensitivity vs Reverse Bias Characteristics for Two Types of PDs (Recommended and Not Recommended)

9.2 Typical Application

A typical application of the device is synchronized ECG and PPG signal acquisition. Figure 179 shows an overview of such a system using the AFE4900.

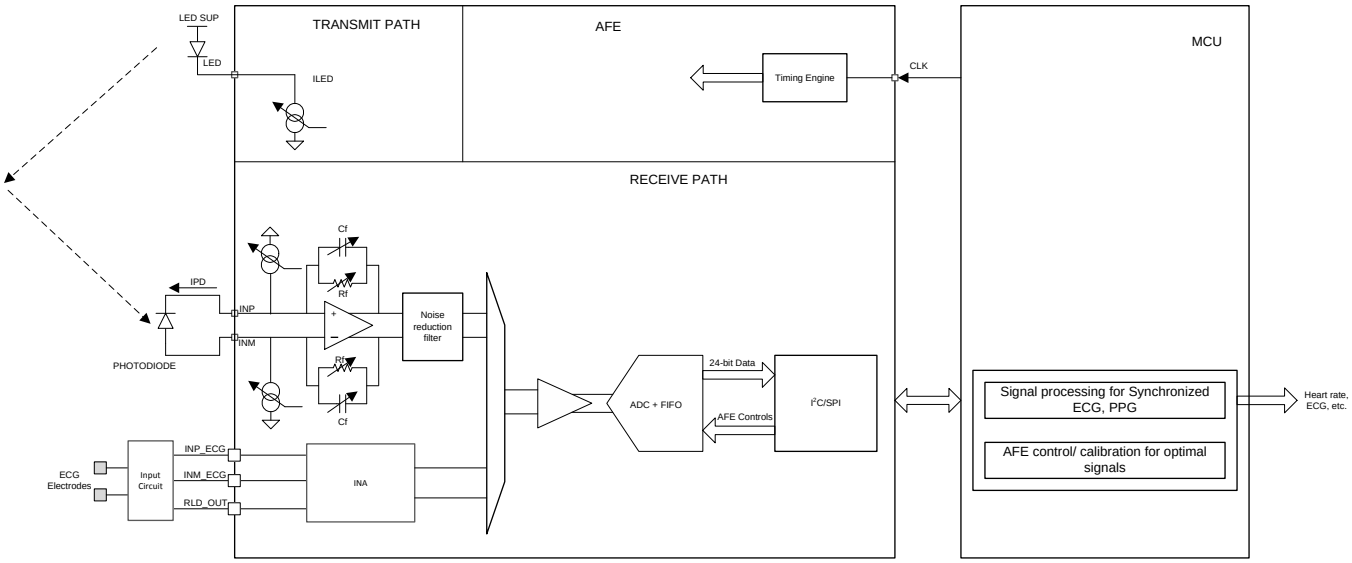


Figure 179. Overview of a Typical ECG + PPG Signal Acquisition System

Typical Application (continued)

The system uses the LED to make a light incident on the human skin. The pulsatile signal reflection is converted to a current using a photodiode (PD) and processed by the AFE4900 receive signal chain. The ECG signal received from electrodes are also input to the AFE through the appropriate interface circuit. The digital equivalent of the PPG and ECG signals is output from the AFE on an I^2C or SPI interface and processed by the MCU to extract parameters such as heart rate. The entire system is clocked using a clock signal from the MCU when the device operates in external clock mode. The signal processing block in the MCU can also calibrate and optimize the device signal chain settings to maximize the signal strength output from the AFE.

9.2.1 Design Requirements

Table 140 shows the typical design requirements of a synchronized ECG+PPG signal acquisition system using the AFE.

Table 140. Design Requirements of the OHRM System

PARAMETER	EXAMPLE VALUE	COMMENTS
RX_SUP	2.1 V in LDO enable mode	Have enough margin for dc inaccuracy and ripple in the supply driver. The most power-optimal way to drive RX_SUP in a battery-powered application is to use a buck converter to derive a voltage of approximately 2.1 V and operate the AFE4900 in LDO enable mode. The LDO internal to the device can be used to reject the tones generated by the buck converter. When operating in LDO bypass mode, an external LDO may be required to achieve the required PSRR and to eliminate output tones.
TX_SUP	Battery voltage	If directly driven from the battery, the LED driver is functional down to the lowest battery voltage where the headroom requirements are satisfied. If driven by the output of a boost converter, choose the boost converter output voltage based on the LED forward voltage and the voltage headroom requirements of the AFE4900 current driver at the maximum current setting.
IO_SUP	1.8 V	Compatible with the I/O level of the MCU. Can be either the same as RX_SUP or lower than RX_SUP.
PRF	500-Hz ECG 250-Hz PPG	Based on the data rate required by the algorithm as well as the degree of time synchronization required between the ECG and PPG signals.

9.2.2 Detailed Design Procedure

The following important factors are key to extracting the full performance benefit from the AFE for the PPG signal acquisition:

1. Good optics including bright LEDs and high-sensitivity photodiodes
2. Good mechanical design
3. An automatic calibration loop that sets the optimal device settings based on the signal conditions

The AFE4900 has an available dynamic range of >95 dBFS. This high dynamic range can be very useful in enabling accurate heart rate monitoring even when the pulsatile signal is weak or in the presence of highly interfering ambient and motion artifacts. The control knobs include TIA gain (R_F), TIA bandwidth, LED current (I_{LED}), offset cancellation DAC (I_OFFDAC), and the bandwidth setting of the noise-reduction filter (f_{RC}).

The photoplethysmogram (PPG) signal is one-sided and contains a high dc signal and a small ac signal (which is the signal of interest). If such a signal is directly input to the TIA, then severe underutilization of the device dynamic range results. However, by subtracting a programmable current at the input of the TIA using the offset cancellation DAC, the signal going into the TIA can be centered around zero and a high gain can be applied so that the signal fills up a large fraction of the dynamic range. Operating at higher TIA gains results in a lower input-referred noise. The TIA gain and the LED current can be constantly adjusted so that the signal at the output of the AFE remains within a safe guard band away from the full-scale range of the signal chain.

The control mechanism for various device parameters can be contained in the automatic calibration loop that operates on the AFE output data and runs in the MCU. Such a calibration can be done at the start of operation. Additionally, whenever the output signal goes outside a pre-defined threshold range (for example, ±50% of the device full-scale range), reconvergence of the calibration loop can be initiated by the MCU. The threshold detect mode and interrupt from the device can be configured if required to detect such a condition where the output goes beyond a programmed range.

The calibration loop must be designed in a manner that does not rely on the accuracy of the LED current, TIA gain, and offset cancellation DAC, thus allowing for device-to-device variations. Specifically, the offset cancellation DAC is not trimmed at production and can have a significant device-to-device variation (±20%). If the calibration routine requires an accurate estimate of the offset cancellation DAC, then PD_DISCONNECT mode can be used to estimate the offset cancellation DAC range on a given device. PD_DISCONNECT mode disconnects the photodiode from the TIA inputs. In this mode IPD = 0 and, thus, the effective input current to the TIA comes solely from the offset cancellation DAC (I_{eff} = I_OFFDAC). As a result, the offset cancellation DAC value can be directly estimated from the device output code.

When the calibration loop is in the process of converging to steady state, the device settings can continually be refreshed to new values. Ideally, a time equal to $t_{CHANNEL}$ is provided for the AFE to settle to any change in signal-chain settings. However, this time can lead to unacceptably large delays in the convergence of the calibration routine. Therefore, during the transient (when the calibration routine is in the transient phase), the wait times can be reduced to as low as $t_{CHANNEL}$ / 10. After the calibration routine converges to the final settings, a wait time of $t_{CHANNEL}$ can then be applied before high-accuracy data are read out from the AFE4410. Methods to speed up the settling of the channel are:

1. Temporarily set the sampling pulse durations to a higher value and open up the effective bandwidth of the switched RC filter to a higher value
2. Temporarily increase the PRF setting and open up the effective bandwidth of the switched RC filter
3. Temporarily increase the physical bandwidth of the switched RC filter

There may be cases where data from only one or two out of the four phases are required. Even in such cases, the calibration loop is recommended to monitor the device output even for the unused phases and adjust the TIA gain and LED current so that the output does not saturate. The reason for such is that whenever the TIA output saturates, the TIA amplifier no longer effectively sets the bias of the PD. Thus, if the TIA output saturates in one of the phases, then there can be additional unwanted settling times for the PD bias to recover when the saturation is removed.

Table 141 lists the selection of various parameters of the device signal chain.

Table 141. Parameter Selection: Device Signal Chain

DEVICE PARAMETER	METHOD OF SELECTION	SUGGESTED CONTROL
LED_ON width	60 µs or higher (set count based on the clock used for the timing engine)	Usually a fixed setting, can be changed based on the frequency range of the heart rate signal (or) to speed up convergence.
SAMP width	At least 25 µs non-overlap (at the start) with respect to the LED_ON signal	
R_F	Highest gain setting that allows operation without saturating the AFE4900 output even in the presence of sudden changes in the dc signal level	Controlled by the calibration loop in the MCU based on the signal dynamics. Use a lower gain setting when the signal current keeps changing more in time.
LED current	Lowest current that obtains the desired ac signal level	Controlled by the calibration loop in the MCU to obtain the required signal-to-noise ratio
Offset DAC current	Adjust dynamically to cancel the dc signal component	Controlled by the calibration loop in the MCU to center the effective signal to the TIA around zero
C_F	Choose the highest value (for the chosen R_F) so that the TIA time constant is less than or equal to 1/7th of the SAMP width	Usually a fixed setting but may have to change based on changes in the R_F setting
NUMAV	The number of ADC averages plays a larger role in device SNR at lower TIA gain settings. At higher TIA gain settings, the number of averages can be set to a constant number (such as 2 or 4) and SNR can be traded off with a total active time	Usually a fixed setting
CONV width	Choose based on the NUMAV setting using Table 27	—
Filter bandwidth setting	Operate with an effective bandwidth (physical bandwidth of the filter multiplied by the SAMP duty cycle) that is at least double the largest frequency content in the signal	Usually a fixed setting, can be changed based on the frequency range of the heart rate signal (or) to speed up convergence

The following factors are important concerns for the ECG signal acquisition:

1. Electrodes with good contact to skin (low contact impedance)
2. Appropriate interface circuit between the electrodes and the ECG input pins
3. Signal processing in the MCU (for example, low-pass filter, notch filter at 50 Hz or 60 Hz, and so forth)

Small form-factor electrodes can result in high contact impedance that can be modeled as a source impedance in series with the ECG signal. When ac-coupling the electrodes to the ECG input pins, the ac impedance of the coupling capacitor also adds in series to this source impedance. The combination of the source impedance and the effective differential impedance in shunt between the INP_ECG, INM_ECG pins forms a voltage divider that can lead to attenuation of the ECG signal. Therefore, the resistors biasing the input pins to the RLD bias must be of high value (in the MΩ range). However, the use of large resistors and large ac-coupling capacitors can lead to high time constants that can cause a delay in the stable acquisition of the ECG signals after contact is made with the electrodes. The interface circuit therefore must be optimized to trade-off between signal quality and signal acquisition time for the specific electrodes being used in the system.

Additional digital signal processing in the MCU may be essential to remove high-frequency noise in the ECG waveforms and to filter out the 50-Hz to 60-Hz noise pickup from the mains.

9.2.3 Application Curve

Figure 180 shows one application curve relevant to the OHRM application. The SNR in dBFS corresponds to the noise referred to the full-scale value of the AFE4900, equal to 2 V_{PP}. The dc component of the signal usually fills up a fraction of the full-scale, and the ac signal is a fraction of the dc signal. As an example, assume the TIA gain is set to 500 kΩ and the number of ADC averages is set to 8. In Figure 180, the SNR is approximately 96 dBFS. With an ac signal amplitude of 1 mV_{PP} at the output of the device, the ac signal amplitude can be expressed as –66 dBFS. Thus, the SNR with respect to the ac signal is approximately 30 dB. SNR can be improved by using the offset cancellation DAC to subtract a portion of the dc signal, enabling operation at a higher TIA gain, and resulting in reduced input-referred current noise for the receiver. These SNR estimations do not include the effect of additional noise contributions from the sensor.

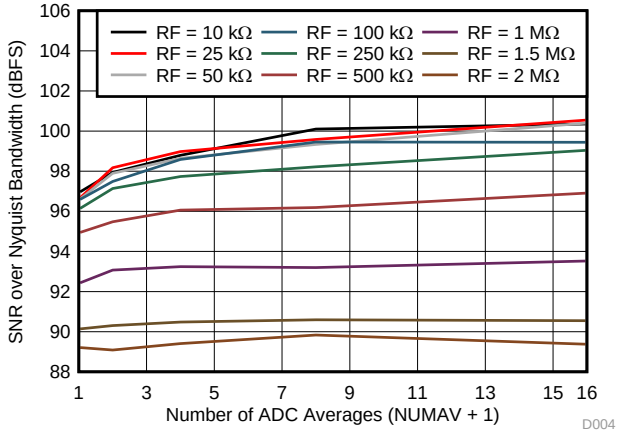


Figure 180. Signal-to-Noise Ratio vs ADC Averaging Across TIA Gains

10 Power Supply Recommendations

Figure 181, Figure 182, and Table 142 show the guidelines for power-supply sequencing and device initialization.

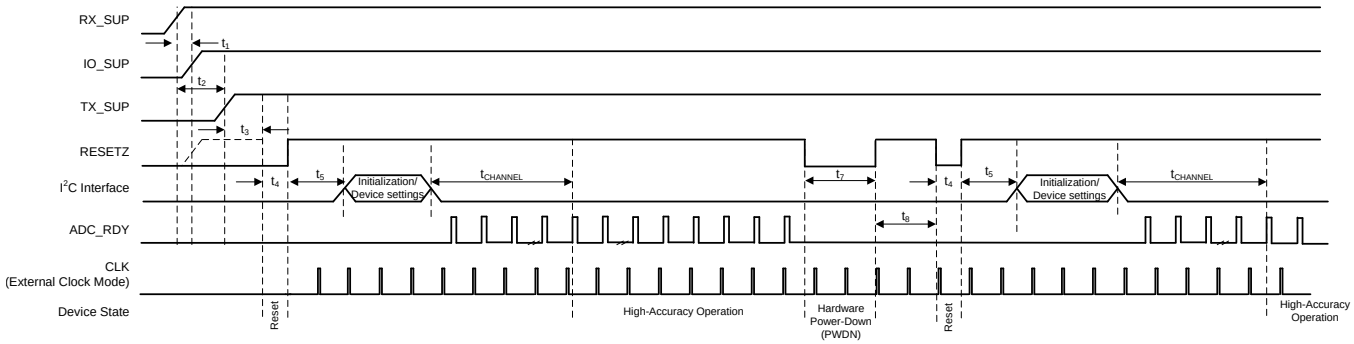


Figure 181. Power-Supply Sequencing, Device Initialization, and Hardware Power-Down Timing

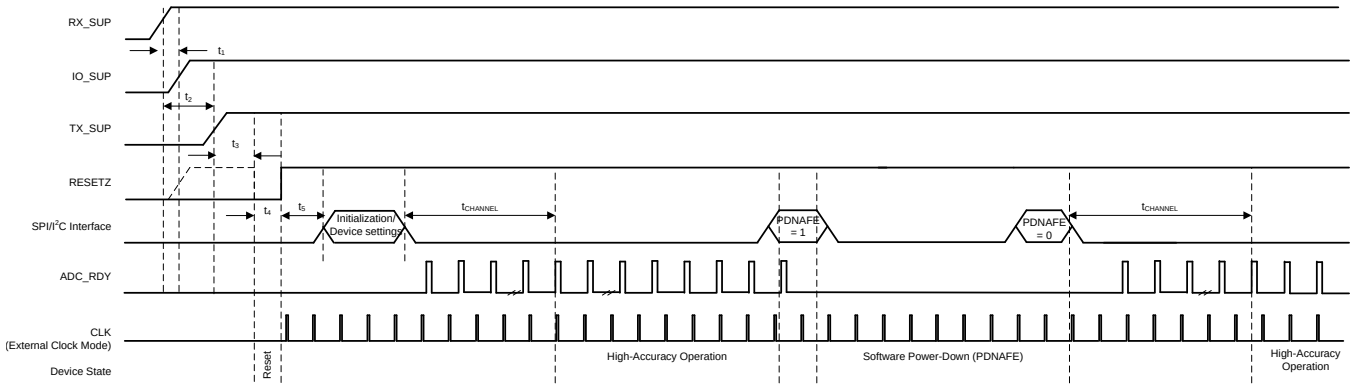


Figure 182. Power-Supply Sequencing, Device Initialization, and Software Power-Down Timing

Table 142. Timing Parameters for Power-Supply Sequencing, Device Initialization, and Power-Down Timing

		VALUE
t_1	Time between RX_SUP and IO_SUP ramping up	Keep t_1 as small as possible (for example, ±10 ms)
t_2	Time between RX_SUP and TX_SUP ramping up	Keep t_2 as small as possible (for example,10 ms)
t_3	Time between all supplies stabilizing and start of the RESETZ low-going pulse	> 10 ms
t_4	RESETZ pulse duration for the device to be reset	Between 25 µs and 50 µs
t_5	Time between resetting the device and issuing of I^2C commands	> 1 ms
$t_{CHANNEL}$	Time for the channel to start operating at full accuracy (channel recovery time)	$t_{CHANNEL}$ (1)
t_7	RESETZ pulse duration for the device to enter PWDN (power-down) mode	> 200 µs
t_8	Time from exiting power-down mode and subsequently resetting the device	> 10 ms

(1) The $t_{CHANNEL}$ parameter is defined in the *Handling Signal-Chain Transient Behavior* section.

Follow these important guidelines:

1. Never operate the device for extended periods of time with one supply on (or off) and the other two supplies off (or on). Such operations can result in spurious leakage currents.
2. The device must be reset before configuring any of the registers. Only perform a reset operation after all three supplies have turned on and are stabilized.

Table 143 lists the configuration register settings that are recommended to be programmed as part of the initialization sequence after power-up when operating in LDO bypass mode.

Table 143. Recommended Register Settings for Device Initialization

REGISTER CONTROL	REGISTER BIT ADDRESS IN HEX [Bits]	SETTING	COMMENTS
ENABLE_ULP	0[5]	1	Enable ULP mode. Set this bit first before setting other bits.
CONTROL_DYN_TIA	23[4]	1	TIA is power cycled
CONTROL_DYN_ADC	23[3]	1	ADC is power cycled
CONTROL_DYN_BIAS	23[14]	1	Bias is power cycled
CONTROL_DYN_TX(1)	50[3]	1	TX amplifier is power cycled
CONTROL_DYN_TX(0)	23[20]	1	
CONTROL_DYN_BG(1)	4B[0]	1	Band gap is power cycled
CONTROL_DYN_VCM(1)	4B[3]	1	VCM buffer is power cycled
ENABLE_INPUT_SHORT	31[5]	1	During power-down phase of the TIA, the analog inputs are differentially shorted to maintain the PD bias
ENABLE_PD2_SHORT	50[4]	1	PD2 is shorted to VCM (internal common-mode) when PD1 is connected to the TIA input during the TG_PD1 phase in dual PD mode
EARLY_OFFSET_DAC	3A[20]	1	Offset DAC transitions at the rising edge of LED_ON instead of at the rising edge of SAMP
ENABLE_PTT(2)	4E[2]	1	Enable PTT mode
ENABLE_ECG_CHOP(2)	61[19]	1	Enable ECG chop mode
ENABLE_RLD(2)	62[23]	1	Enable RLD output
CONTROL_DYN_ALDO(3)	4B[1]	1	ALDO is power cycled
CONTROL_DYN_DLDO(3)	4B[2]	1	DLDO is power cycled
SHORT_ALDO_TO_DLDO_IN_DEEP_SLEEP(3)	50[5]	1	ALDO output is shorted to DLDO output in deep sleep phase

(1) Do not set these bits if operating in PTT mode.
(2) Set these bits if operating in PTT mode.
(3) Set these bits to 0 if operating in PTT mode.

11 Layout

11.1 Layout Guidelines

Two key layout guidelines are:

1. TX1, TX2, TX3, and TX4 are fast-switching lines and must be routed away from sensitive lines (such as the INP, INM inputs).
2. The device can draw high-switching currents from the TX_SUP pin. A decoupling capacitor must be electrically close to the pin.
3. Route the PD input lines as well as the ECG input lines differentially and shield them from neighbouring switching lines, if any. If needed, use a common mode choke to reject RF interference, if any.

11.2 Layout Example

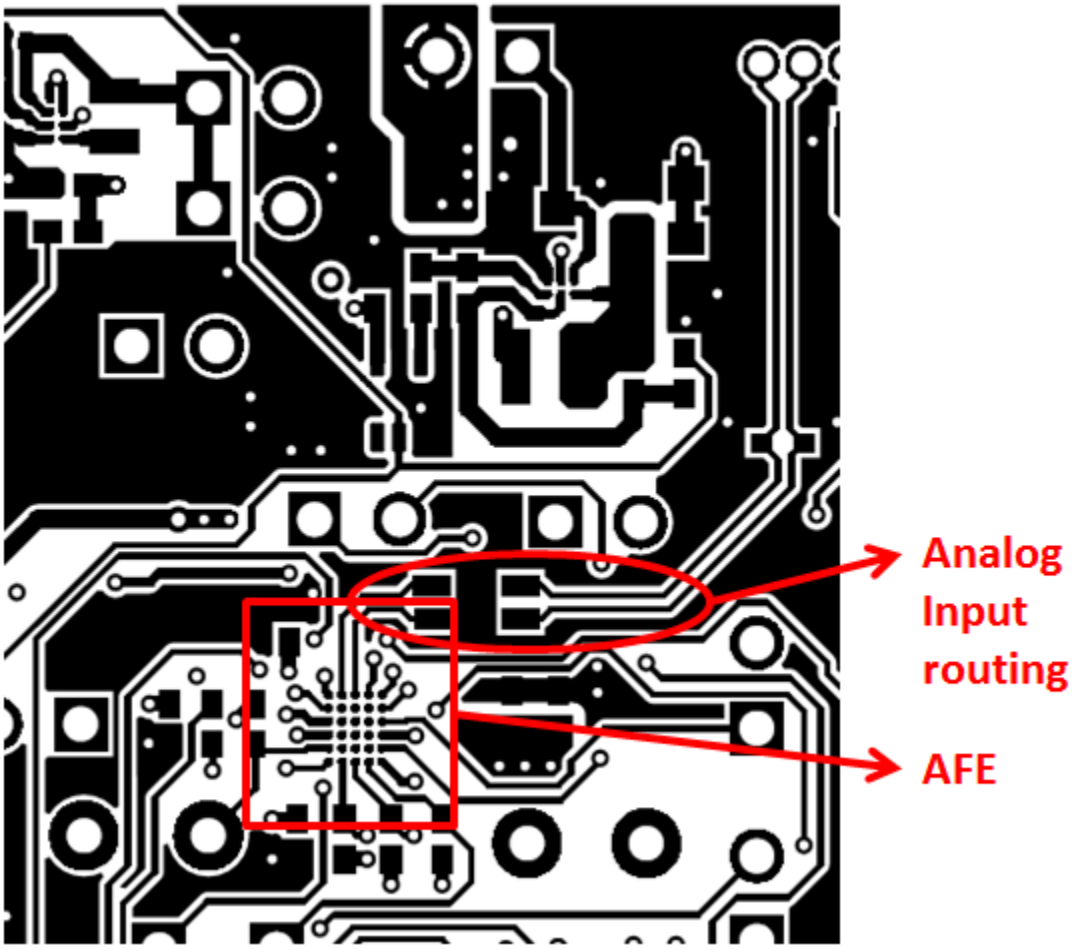


Figure 183. Example Layout

12 Device and Documentation Support

12.1 Trademarks

Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(3)	MSL Peak Temp(4)	Op Temp (°C)	Device Marking(5)(6)
AFE4900YZR	PREVIEW	DSBGA	YZ	30	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4900
AFE4900YZT	PREVIEW	DSBGA	YZ	30	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-20 to 70	AFE4900

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

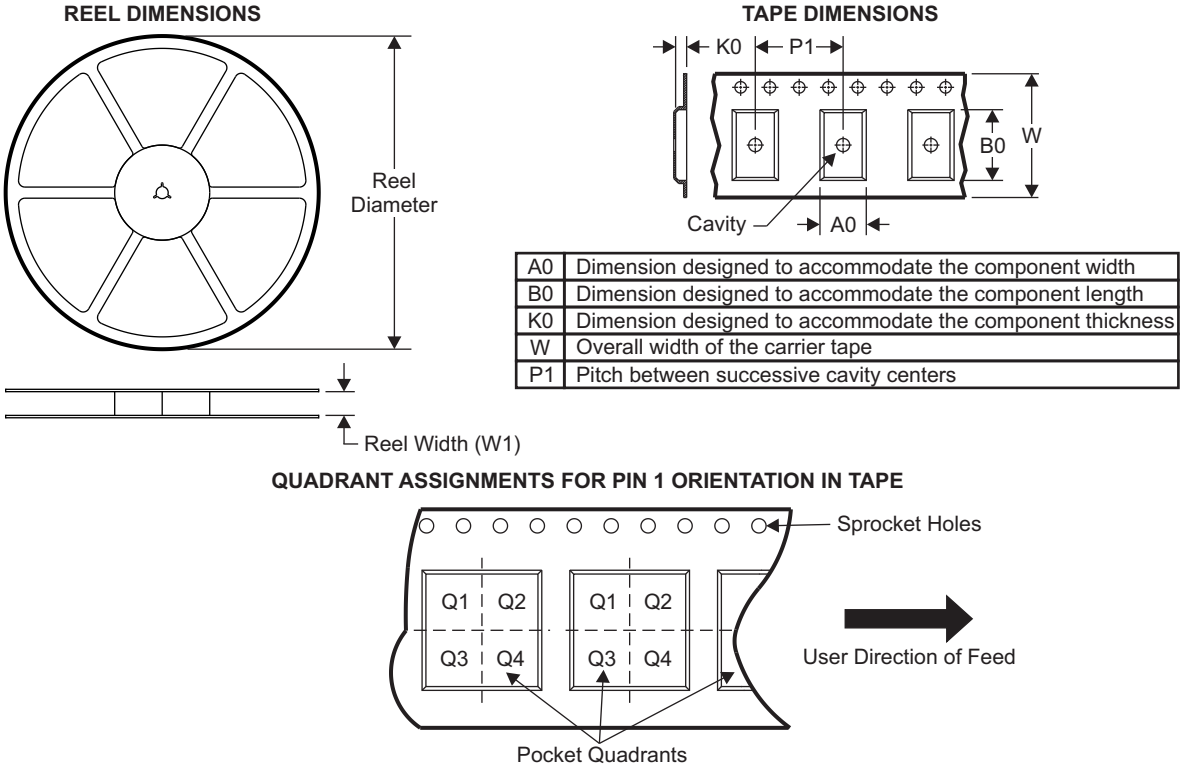
(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

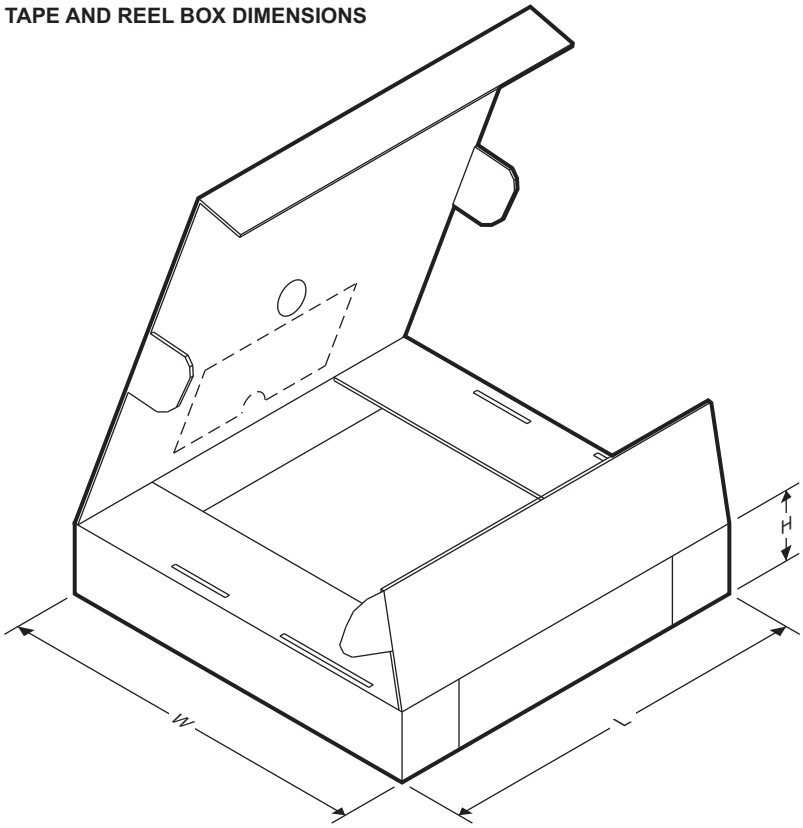
13.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

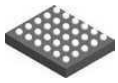
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4900YZR	DSBGA	YZ	30	3000	180.0	8.4	2.16	2.66	0.6	4.0	8.0	Q1
AFE4900YZT	DSBGA	YZ	30	250	180.0	8.4	2.16	2.66	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4900YZR	DSBGA	YZ	30	3000	210.0	185.0	35.0
AFE4900YZT	DSBGA	YZ	30	250	210.0	185.0	35.0

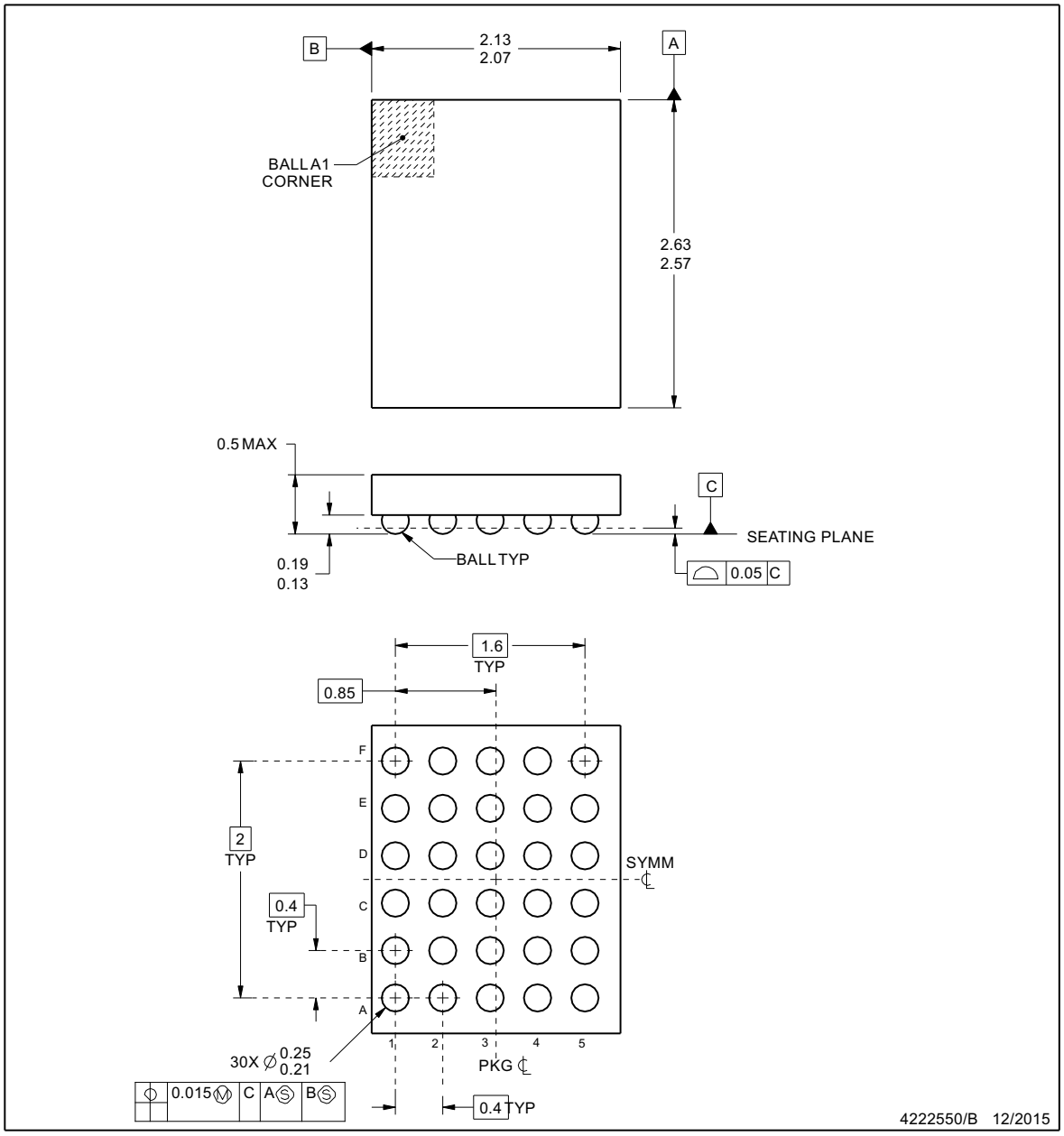
YZ0030-C01



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

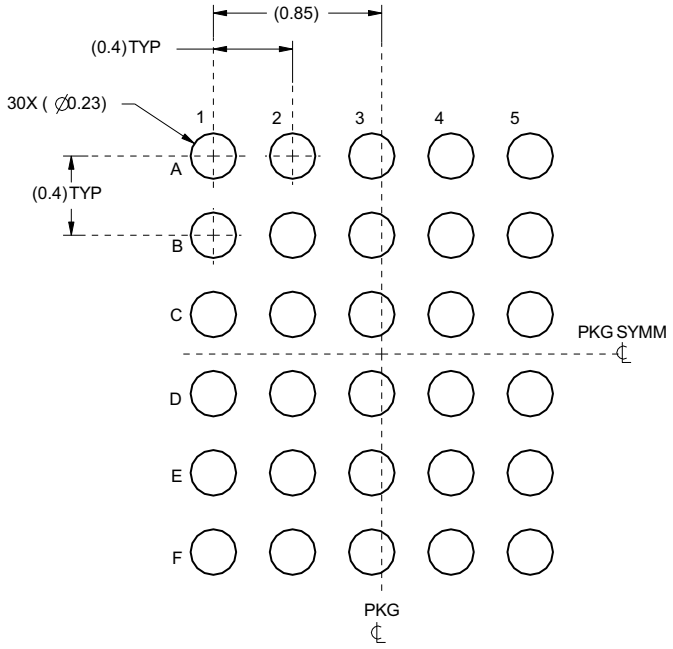
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

YZ0030-C01

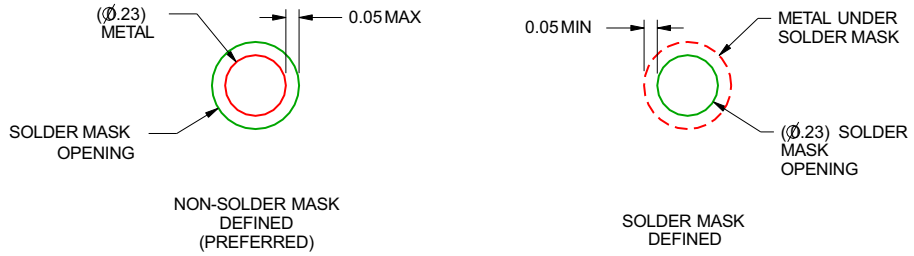
EXAMPLE BOARD LAYOUT

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4222550/B 12/2015

NOTES: (continued)

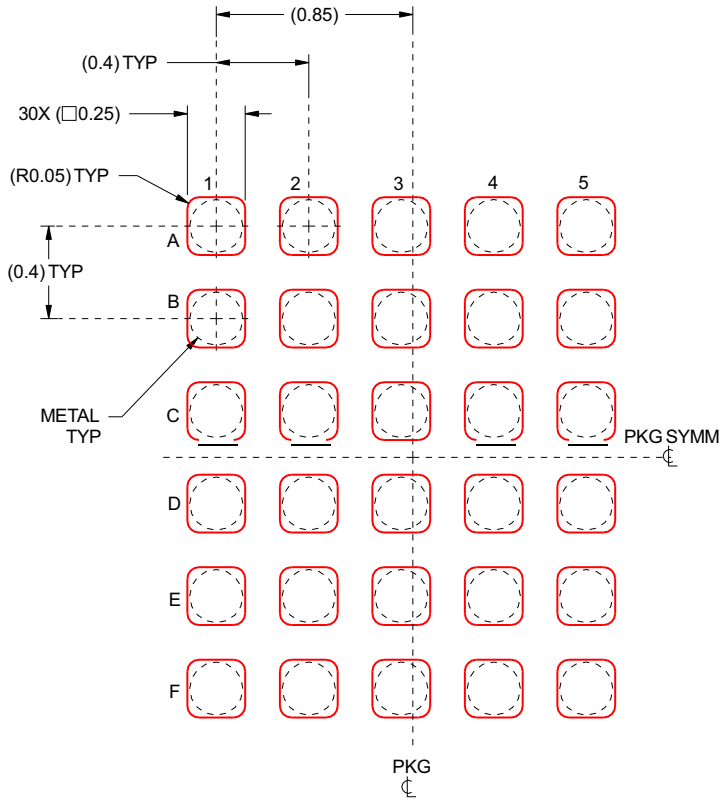
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

YZ0030-C01

EXAMPLE STENCIL DESIGN

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

4222550/B 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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